



# SANYO Semiconductors

## DATA SHEET

# LA72710V

Monolithic Linear IC  
For JPN TV  
Multi Channel Television  
Sound Decoder

### Overview

The LA72710V is a JPN MTS (Multi Channel Television Sound) Decoder.

### Features

- With SIF circuit, alignment-free STEREO channel separation.
- Separation is fine-tuned by input level adjustment.
- Included filters are adjustment free.

### Functions

- Stereo & Bilingual demodulate.
- Stereo & Bilingual detection.
- JUST CLOCK OUT.
- Built-in ALC.

### Specifications

**Maximum Ratings** at Ta = 25°C

| Parameter                   | Symbol              | Conditions  | Ratings     | unit |
|-----------------------------|---------------------|-------------|-------------|------|
| Maximum supply voltage      | V <sub>CC</sub> max |             | 9.6         | V    |
| Allowable power dissipation | Pd max              | Ta ≤ 70°C * | 610         | mW   |
| Operating temperature       | Topr                |             | -10 to +70  | °C   |
| Storage temperature         | Tstg                |             | -55 to +150 | °C   |

\* When mounted on a 114.3×76.1×1.6mm<sup>3</sup> glass epoxy board.

**Operating Conditions** at Ta = 25°C

| Parameter                         | Symbol             | Conditions | Ratings    | unit |
|-----------------------------------|--------------------|------------|------------|------|
| Recommended operating voltage     | V <sub>CC</sub>    |            | 9.0        | V    |
| Allowable operating voltage range | V <sub>CC</sub> op |            | 8.5 to 9.5 | V    |

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# LA72710V

## Electrical Characteristics at Ta = 25°C, VCC = 9.0V

| Parameter                      | Symbol            | Conditions                                                                | Ratings |      |      | unit |
|--------------------------------|-------------------|---------------------------------------------------------------------------|---------|------|------|------|
|                                |                   |                                                                           | min     | typ  | max  |      |
| Current dissipation            | I <sub>CC</sub>   | No signal, Inflow current at Pin 19                                       | 40      | 50   | 60   | mA   |
| Input level                    | V <sub>SIN</sub>  | fc = 4.5MHz                                                               | 80      | 90   | 100  | dBμV |
| MONO output level              | V <sub>OMN</sub>  | fm = 1kHz, 100% Mod, Pre-Emphasis OFF                                     | -7.5    | -6   | -4.5 | dBV  |
| MONO L/R level difference      | ΔV <sub>OMN</sub> | fm = 1kHz, 100% Mod, Pre-Emphasis OFF                                     | -1.5    | 0    | 1.5  | dB   |
| MONO distortion                | THDM              | fm = 1kHz, 100% Mod, Pre-Emphasis OFF                                     |         | 0.2  | 0.5  | %    |
| MONO frequency characteristics | fcM1              | fm = 10kHz/1kHz, 100% Mod, 15kHz LPF<br>Pre-Emphasis OFF                  | -18     | -14  |      | dB   |
| MONO S/N                       | SNM               | Non Mod, 15kHz LPF                                                        | 50      |      |      | dB   |
| STEREO output level            | V <sub>OST</sub>  | fm = 1kHz, 100% Mod, Cue (Stereo),<br>15kHz LPF                           | -7.5    | -6   | -4.5 | dBV  |
| STEREO distortion              | THDS              | fm = 1kHz, 100% Mod, Cue (Stereo),<br>15kHz LPF                           |         | 0.7  | 1.5  | %    |
| STEREO S/N                     | SNS               | Sub Carrier (Non Mod), Cue (Stereo),<br>15kHz LPF                         | 45      |      |      | dB   |
| Main output level              | V <sub>OMA</sub>  | fm = 1kHz, 100% Mod, Cue (Bilingual),<br>15kHz LPF                        | -7.5    | -6   | -4.5 | dBV  |
| Main distortion                | THDMA             | fm = 1kHz, 100% Mod, Cue (Bilingual),<br>15kHz LPF                        |         | 0.3  | 1    | %    |
| Main S/N                       | SNMA              | Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF                         | 50      |      |      | dB   |
| SUB output level               | V <sub>OSU</sub>  | fm = 1kHz, 100% Mod, Cue (Bilingual),<br>15kHz LPF                        | -7.5    | -6   | -4.5 | dBV  |
| SUB distortion                 | THDSU             | fm = 1kHz, 100% Mod, Cue (Bilingual),<br>15kHz LPF                        |         | 1    | 2    | %    |
| SUB frequency characteristics  | fcSU              | fm = 10kHz/1kHz, 60% Mod, Cue (Bilingual),<br>15kHz LPF, Pre-Emphasis OFF | -18     | -14  |      | dB   |
| SUB Main S/N                   | SNSU              | Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF                         | 45      |      |      | dB   |
| STEREO separation L → R        | SEPR              | fm = 1kHz (L-only), 60% Mod, Cue (Stereo),<br>15kHz LPF                   | 30      | 35   |      | dB   |
| STEREO separation R → L        | SEPL              | fm = 1kHz (R-only), 60% Mod, Cue (Stereo),<br>15kHz LPF                   | 30      | 35   |      | dB   |
| Stay behind carrier level      | CLSU              | Main = 0%, Sub = 0% (Carrier)<br>Cue (Bilingual)                          |         | -50  | -40  | dBV  |
| Stay behind carrier level      | CLMA              | Main = 0%, Sub = 0% (Carrier)<br>Cue (Bilingual)                          |         | -55  | -45  | dBV  |
| Cross-talk MAIN → SUB          | CTSUB             | Main: fm = 1kHz, 100% modulation,<br>Cue (Bilingual), 15kHz LPF           | 35      | 45   |      | dB   |
| Cross-talk SUB → MAIN          | CTMA              | Sub: fm = 1kHz, 100% modulation,<br>Cue (Bilingual), 15kHz LPF            | 45      | 55   |      | dB   |
| MODE output MONO               | MODMO             | Input = Mono Signal                                                       | 0.7     | 1    | 1.3  | V    |
| MODE output STEREO             | MODST             | Input = Stereo Signal                                                     | 1.7     | 2    | 2.3  | V    |
| MODE output BILINGUAL          | MODBI             | Input = Bilingual Signal                                                  | 2.7     | 3    | 3.3  | V    |
| Just Clock output High volt    | JCH               | f = 400Hz (mono), 40%Mod                                                  | 4       |      |      | V    |
| Just Clock output Low volt     | JCL               | f = 400Hz (mono), 10%Mod                                                  |         |      | 1    | V    |
| ALC level                      | V <sub>ALC</sub>  | MONO 1kHz Mod 100%                                                        | -11     | -9.5 | -8   | dBV  |
| ALC Distortion                 | THDALC            | MONO 1kHz Mod 100%                                                        |         | 0.2  | 0.5  | %    |

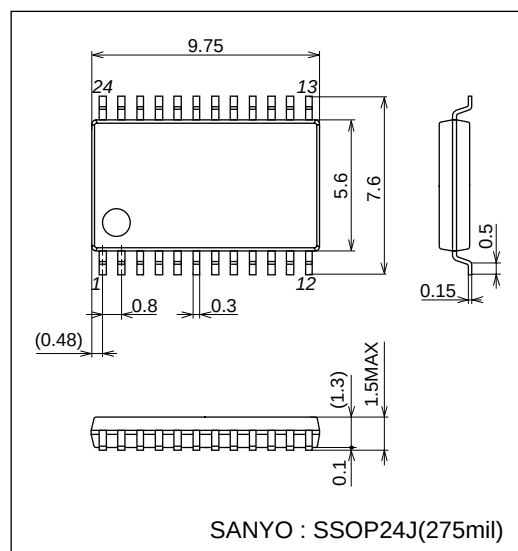
[Condition of input signal at pin 5] Deviation of SIF input MONO: (fm = 400Hz) 100% → 4.5MHz ± 25kHz Pre-Emphasis ON.

[Output] L-ch : pin 14, R-ch : pin 13.

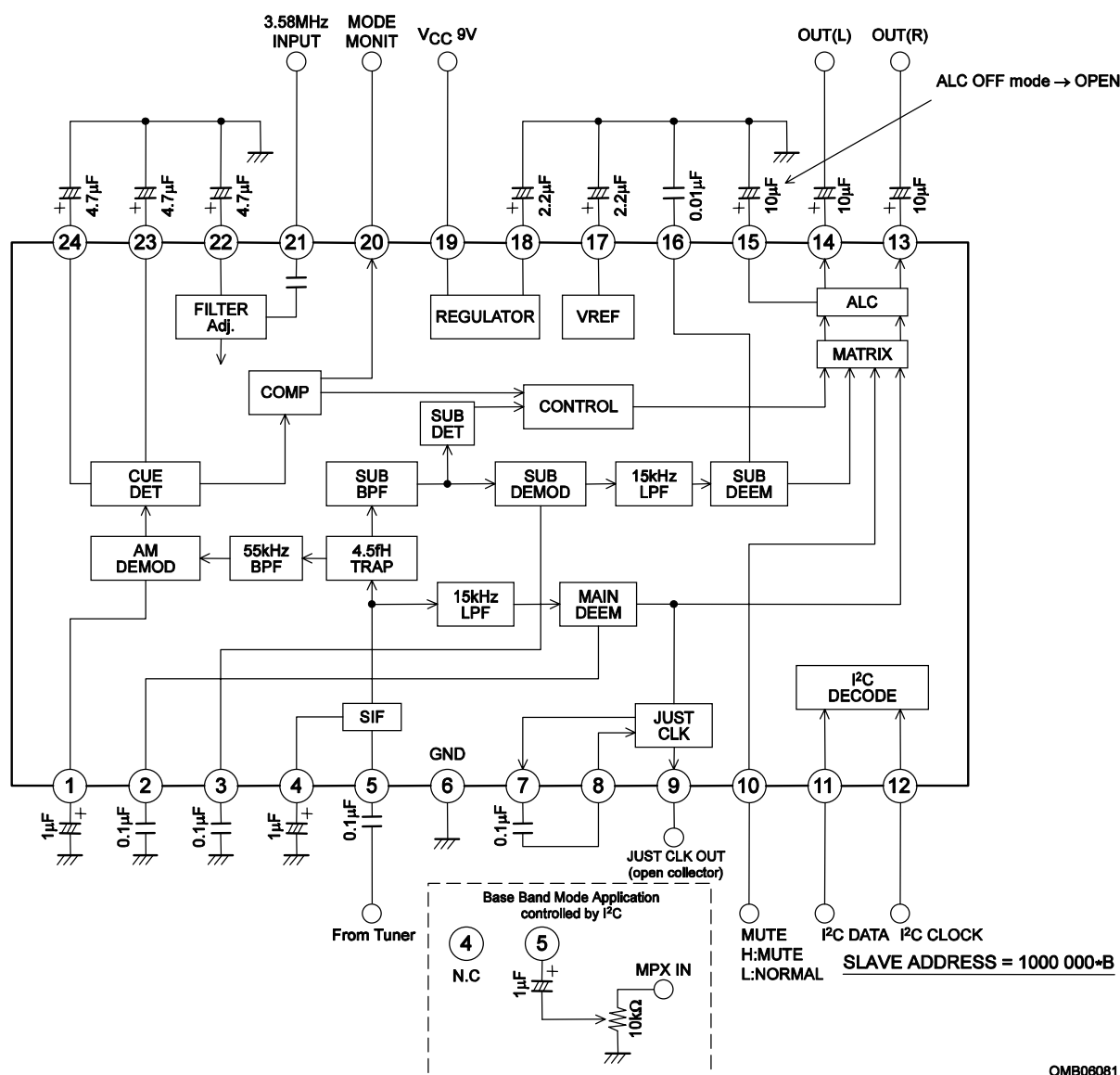
## Package Dimensions

unit : mm

3315



## Block Diagram and Sample Application Circuit



OMB06081

## Pin Functions

| Pin No.      | Pin Name                   | Function                                                                                                                                                                                                                                                                                                                                     | DC voltage<br>AC level | Equivalent Circuit |
|--------------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|--------------------|
| 1            | AMDET                      | Reference terminal of AM detection.                                                                                                                                                                                                                                                                                                          |                        |                    |
| 2<br>3<br>16 | DCFIL1<br>DCFIL1<br>DCFIL1 | Absorbing the DC offset of signal line by external capacity.                                                                                                                                                                                                                                                                                 | DC: 2.4V               |                    |
| 4            | FMFIL                      | Filter terminal for making stable DC voltage of FM detection output in SIF part.<br>Normally, use a condenser of 1μF. Increase the capacity value with concerning frequency characteristics of low level.                                                                                                                                    |                        |                    |
| 5            | SIFIN                      | Input terminal for SIF.<br>The input impedance is about 5kΩ. Be care for about pattern layout of the input circuit, because of causing buzz-beat and buzz by leaking noise signal into the input terminal. (The noise signal depending on sound is particularly video signal and chroma signal and so on. VIF carrier becomes noise signal.) |                        |                    |
| 6            | GND                        |                                                                                                                                                                                                                                                                                                                                              |                        |                    |
| 7            | JCKO                       | 20dB amplifier output for JUST CLOCK.                                                                                                                                                                                                                                                                                                        | DC: 3.8V               |                    |
| 8            | CMPIN                      | Comparator input for JUST CLOCK.                                                                                                                                                                                                                                                                                                             | DC: 3.8V               |                    |

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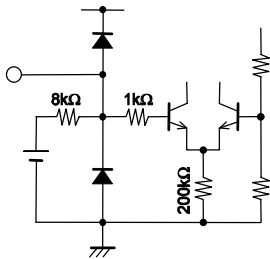
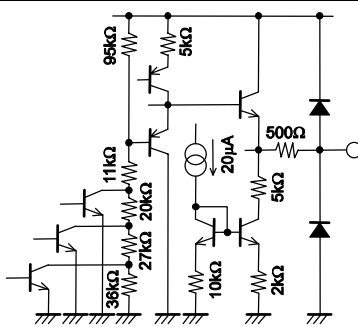
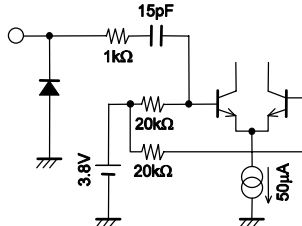
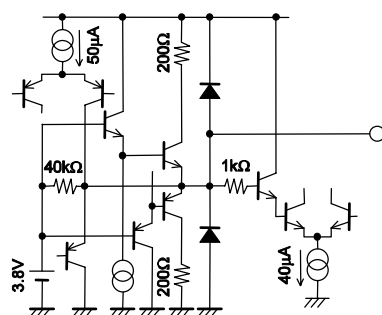
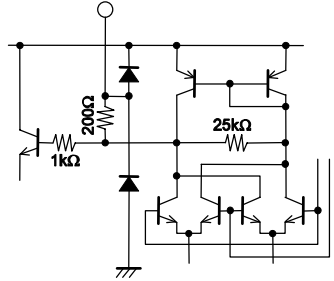
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| Pin No. | Pin Name | Function                                                                    | DC voltage<br>AC level | Equivalent Circuit |
|---------|----------|-----------------------------------------------------------------------------|------------------------|--------------------|
| 9       | JCKRWO   | Rectangle wave output for JUST CLOCK.<br>(OPEN Collector)                   | 5V<br>0V               |                    |
| 10      | MUTE     | MUTE control terminal.<br>MUTE: 2.8V to                                     |                        |                    |
| 11      | SDA      | Serial data input / output terminal.<br>High: 3.5V to 5V<br>Low: 0V to 1.5V | 5V<br>0V               |                    |
| 12      | SCL      | Serial clock input terminal<br>High: 3.5V to 5V<br>Low: 0V to 1.5V          | 5V<br>0V               |                    |
| 13      | RCH      | Line Out (R) terminal.                                                      | DC: 3.8V<br>AC: -6dBV  |                    |
| 14      | LCH      | Line Out (L) terminal.                                                      |                        |                    |
| 15      | ALCDET   | ALC detection terminal.                                                     |                        |                    |
| 17      | REGFIL   | Filter terminal of reference voltage source.                                | DC: 4.5V               |                    |

Continued on next page

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Continued from preceding page.

| Pin No. | Pin Name        | Function                                                                                                       | DC voltage<br>AC level | Equivalent Circuit                                                                    |
|---------|-----------------|----------------------------------------------------------------------------------------------------------------|------------------------|---------------------------------------------------------------------------------------|
| 18      | PCREG           | Band gap source terminal block.                                                                                | DC: 1.2V               |    |
| 19      | V <sub>CC</sub> | Power supply terminal.                                                                                         | DC: 9V                 |                                                                                       |
| 20      | MODE            | Detection output for M.T.S. signal.<br>BILINGUAL: 3.0V<br>STEREO: 2.0V<br>MONO: 1.0V                           |                        |    |
| 21      | FSCIN           | Input terminal for FSC (3.58MHz).                                                                              | AC: 200mVp-p           |   |
| 22      | PLLFIL          | Loop filter terminal.<br>Automatic adjusting for PLL.                                                          |                        |  |
| 23      | ST              | PHASE COMPARATOR input (STEREO).<br>This detection pin becomes High (6.6V or more) when ST signal is input.    |                        |  |
| 24      | BIL             | PHASE COMPARATOR input (BILINGAL).<br>This detection pin becomes High (6.6V or more) when BIL signal is input. |                        |                                                                                       |

## I<sup>2</sup>C BUS serial interface specification

### (1) Data Transfer Manual

This IC adopts control method (I<sup>2</sup>C-BUS) with serial data, and controlled by two terminals which called SCL (serial clock) and SDA (serial data). At first, set up<sup>\*1</sup> the condition of starting data transfer, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit), and save the order. The 9th bit takes ACK (Acknowledge) period, during SCL terminal takes 'H' this IC pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of<sup>\*2</sup> data transfer stop condition, thus the transfer comes to close.

\*1 Defined by SCL rise down SDA during 'H' period.

\*2 Defined by SCL rise up SDA during 'H' period.

### (2) Transfer Data Format

After transfer start condition, transfers slave address (1000 000\*B) to SDA terminal, control data, then, stop condition (See figure 1).

Slave address is made up of 7bits, 8th bit<sup>\*3</sup> shows the direction of transferring data, if it is 'L' takes write mode (As this IC side, this is input operation mode), and in case of 'H' reading mode (As this IC side, this is output operation mode). Data works with all of bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled the transfer dates.

\*3 It is called R/W bit.

Fig.1 DATA STRUCTURE "WRITE" mode

|                 |               |                  |     |              |     |                |
|-----------------|---------------|------------------|-----|--------------|-----|----------------|
| START Condition | Slave Address | R/W <sub>L</sub> | ACK | Control data | ACK | STOP condition |
|-----------------|---------------|------------------|-----|--------------|-----|----------------|

Fig.2 DATA STRUCTURE "READ" mode

|                 |               |                  |     |                 |     |                |
|-----------------|---------------|------------------|-----|-----------------|-----|----------------|
| START condition | Slave Address | R/W <sub>H</sub> | ACK | Internal Data * | ACK | STOP condition |
|-----------------|---------------|------------------|-----|-----------------|-----|----------------|

\* Output 8bits data as follows;

bit8 is result of STERO DET (H : STEREO)

bit7 is result of BILINGUAL DET (H : BILINGUAL)

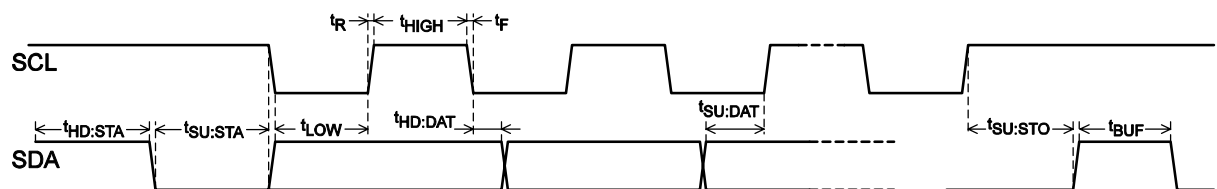
bit6 to bit1 are fixed to 'L'

### (3) Initialize

This IC is initialized for circuit protection. Initial condition is "0 (All bits)."

I<sup>2</sup>C Timing Specifications

| Parameter                                                                        | Symbol              | min  | max | unit |
|----------------------------------------------------------------------------------|---------------------|------|-----|------|
| LOW level input voltage                                                          | V <sub>IL</sub>     | -0.5 | 1.5 | V    |
| HIGH level input voltage                                                         | V <sub>IH</sub>     | 3.0  | 5.5 | V    |
| LOW level output current                                                         | I <sub>OL</sub>     |      | 3.0 | mA   |
| SCL clock frequency                                                              | f <sub>SCL</sub>    | 0    | 100 | kHz  |
| Set-up time for a repeated START condition                                       | t <sub>SU:STA</sub> | 4.7  |     | μs   |
| Hold time START condition. After this period, the first clock pulse is generated | t <sub>HD:STA</sub> | 4.0  |     | μs   |
| LOW period of the SCL clock                                                      | t <sub>LOW</sub>    | 4.7  |     | μs   |
| Rise time of both SDA and SDL signals                                            | t <sub>R</sub>      | 0    | 1.0 | μs   |
| HIGH period of the SCL clock                                                     | t <sub>HIGH</sub>   | 4.0  |     | μs   |
| Fall time of both SDA and SDL signals                                            | t <sub>F</sub>      | 0    | 1.0 | μs   |
| Data hold time                                                                   | t <sub>HD:DAT</sub> | 0    |     | μs   |
| Data set-up time                                                                 | t <sub>SU:DAT</sub> | 250  |     | ns   |
| Set-up time for STOP condition                                                   | t <sub>SU:STO</sub> | 4.0  |     | μs   |
| BUS free time between a STOP and START condition                                 | t <sub>BUF</sub>    | 4.7  |     | μs   |



OMT00010

I<sup>2</sup>C Control Conditions

Grp-1

(SLAVE ADDRESS 80H)

|   | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | Condition            |
|---|----|----|----|----|----|----|----|----|----------------------|
| * |    |    |    |    |    |    | 0  | 0  | Bilingual            |
|   |    |    |    |    |    |    | 0  | 1  | Main                 |
|   |    |    |    |    |    |    | 1  | 0  | Sub                  |
|   |    |    |    |    |    |    | 1  | 1  | (Prohibit)           |
| * |    |    |    |    |    | 0  |    |    | Normal               |
|   |    |    |    |    |    | 1  |    |    | Forced MONO          |
| * |    |    |    |    | 0  |    |    |    | Normal (MUTE Off)    |
|   |    |    |    |    | 1  |    |    |    | MUTE                 |
| * |    |    |    | 0  |    |    |    |    | ALC Off (Through)    |
|   |    |    |    | 1  |    |    |    |    | ALC On               |
| * |    |    | 0  |    |    |    |    |    | JUST CLOCK Off       |
|   |    |    | 1  |    |    |    |    |    | JUST CLOCK On        |
| * |    | 0  |    |    |    |    |    |    | SIF Mode             |
|   |    | 1  |    |    |    |    |    |    | BASE BAND Mode       |
| * | 0  |    |    |    |    |    |    |    | Fix                  |
|   | 1  |    |    |    |    |    |    |    | Prohibit (TEST Mode) |

\*:Initial condition

## Read out data

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | Condition     |
|----|----|----|----|----|----|----|----|---------------|
|    |    | 0  | 0  | 0  | 0  | 0  | 0  | Fixed         |
|    | 0  |    |    |    |    |    |    | Normal        |
|    | 1  |    |    |    |    |    |    | Bilingual det |
| 0  |    |    |    |    |    |    |    | Normal        |
| 1  |    |    |    |    |    |    |    | Stereo det    |



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## Mode Select (pin & I<sup>2</sup>C setting)

| Broadcast signal | MUTE  | I <sup>2</sup> C setting |    |    |    | MATRIX OUT  |             |        | READ MODE OUT |    | MODE OUT |
|------------------|-------|--------------------------|----|----|----|-------------|-------------|--------|---------------|----|----------|
|                  | pin10 | D4                       | D3 | D2 | D1 | LCH (pin14) | RCH (pin13) | MODE   | D8            | D7 | Pin20    |
| Bilingual        | L     | 0                        | 0  | 0  | 0  | MAIN        | SUB         | BOTH   | L             | H  | 3V       |
|                  | L     | 0                        | 0  | 0  | 1  | MAIN        | MAIN        | MAIN   | L             | H  |          |
|                  | L     | 0                        | 0  | 1  | 0  | SUB         | SUB         | SUB    | L             | H  |          |
|                  | L     | 0                        | 1  | *  | *  | MAIN        | MAIN        | MONO   | L             | H  |          |
|                  | *     | 1                        | *  | *  | *  | MUTE        | MUTE        | MUTE   | L             | H  |          |
|                  | H     | *                        | *  | *  | *  | MUTE        | MUTE        | MUTE   | L             | H  |          |
| STEREO           | L     | 0                        | 0  | *  | *  | L           | R           | STEREO | H             | L  | 2V       |
|                  | L     | 0                        | 1  | *  | *  | L+R         | L+R         | MONO   | H             | L  |          |
|                  | *     | 1                        | *  | *  | *  | MUTE        | MUTE        | MUTE   | H             | L  |          |
|                  | H     | *                        | *  | *  | *  | MUTE        | MUTE        | MUTE   | H             | L  |          |
| MONO             | L     | 0                        | *  | *  | *  | L+R         | L+R         | MONO   | L             | L  | 1V       |
|                  | *     | 1                        | *  | *  | *  | MUTE        | MUTE        | MUTE   | L             | L  |          |
|                  | H     | *                        | *  | *  | *  | MUTE        | MUTE        | MUTE   | L             | L  |          |

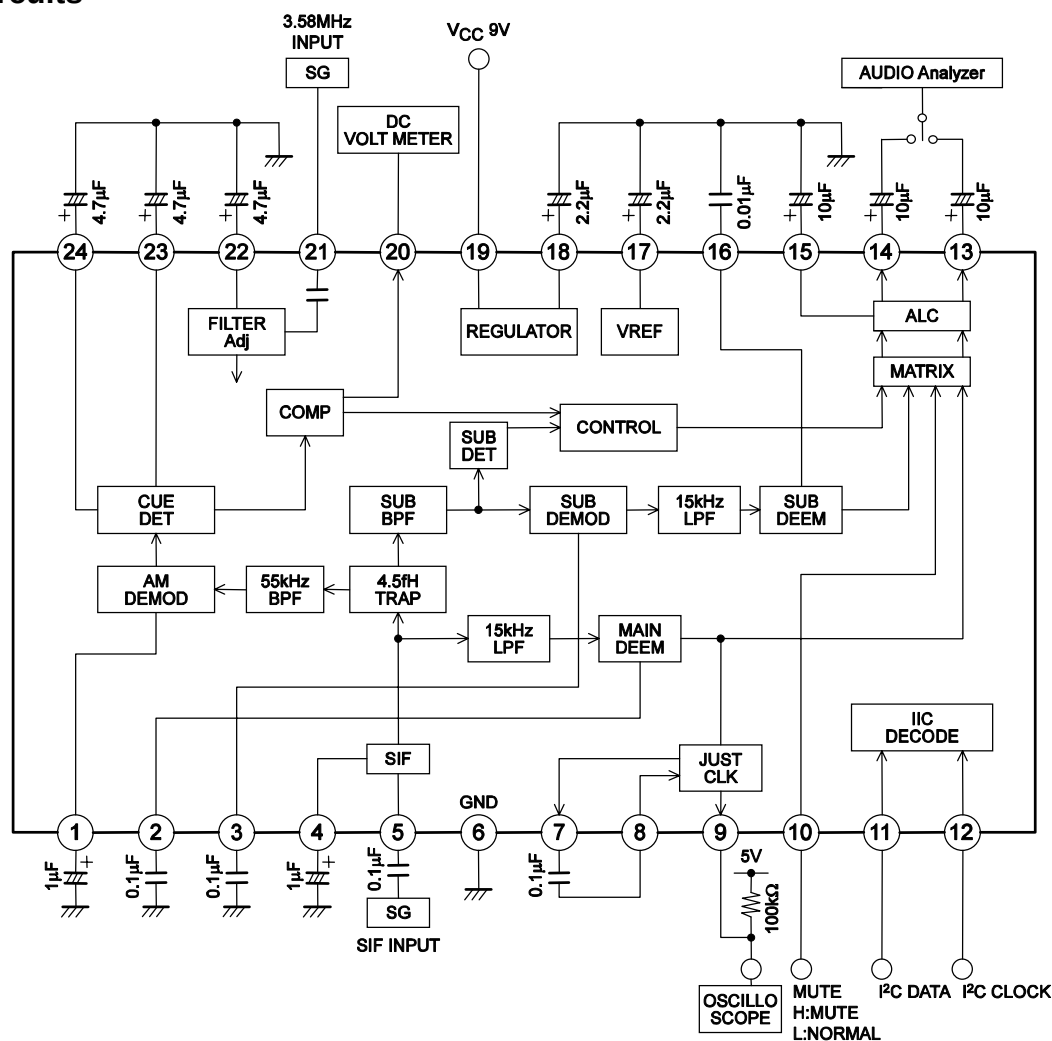
\*: Don't care.

## Serial Data Specification (I<sup>2</sup>C bus communication)

| MSB<br>D8            | D7                             | D6            | D5                   | D4                   | D3                   | D2                                                      | LSB<br>D1 |
|----------------------|--------------------------------|---------------|----------------------|----------------------|----------------------|---------------------------------------------------------|-----------|
| TEST                 | SIF or<br>BASE BAND            | JUST<br>CLK   | ALC                  | NORMAL OUT<br>MUTE   | Forced<br>MONO       | MULTIPLEX mode select                                   |           |
| <u>0:OFF</u><br>1:ON | <u>0:SIF</u><br>1:BASE<br>BAND | 0:OFF<br>1:ON | <u>0:OFF</u><br>1:ON | <u>0:OFF</u><br>1:ON | <u>0:OFF</u><br>1:ON | 00:BILINGUAL<br><u>01:MAIN</u><br>10:SUB<br>11:Unusable |           |

Note: Underline shows default setting.

## Test Circuits



OMB06080

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