

### Description

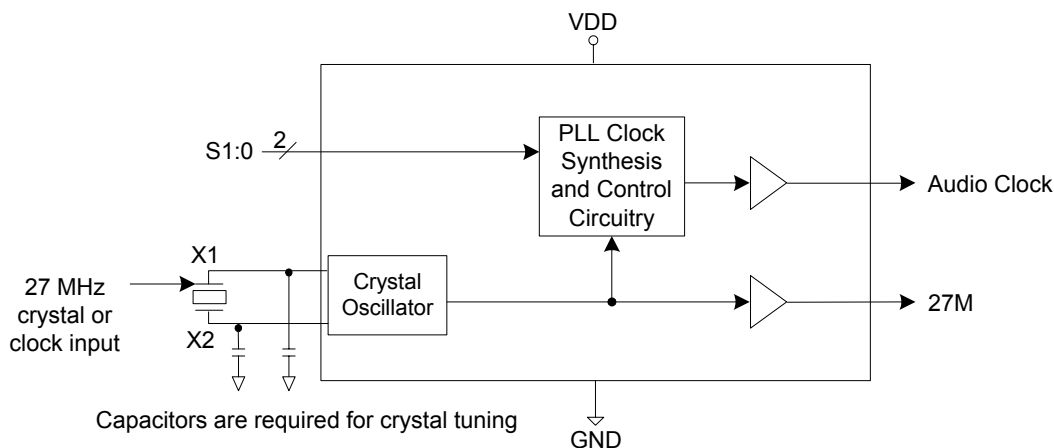
The MK2703 is a low-cost, low-jitter, high-performance PLL clock synthesizer designed to replace oscillators and PLL circuits in set-top box and multimedia systems. Using IDT's patented analog Phase Locked Loop (PLL) techniques, the device uses a 27 MHz crystal or clock input to produce a buffered reference clock and a selectable audio clock.

IDT manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult IDT to eliminate VCXOs, crystals and oscillators from your board.

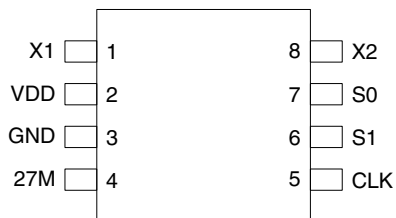
### Features

- Packaged in 8-pin SOIC
- Pb (lead) free package
- Uses an inexpensive, fundamental mode crystal or clock
- Supports MPEG sampling rates of 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Patented zero ppm synthesis error in all clocks
- All frequencies are frequency locked
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V or 5 V
- Industrial temperature version available
- ***The MK2703B is recommended for new designs***

### Block Diagram



## Pin Assignment



8-pin (150 mil) SOIC

## AUDIO CLOCK OUTPUT SELECT TABLE

| S1 | S0 | CLK (MHz) |
|----|----|-----------|
| 0  | 0  | 8.192     |
| 0  | 1  | 11.2896   |
| 1  | 0  | 12.288    |
| 1  | 1  | 24.576    |

Key: 0 = Connect pin directly to ground

1 = Connect pin directly to VDD

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description                                                                                          |
|------------|----------|----------|----------------------------------------------------------------------------------------------------------|
| 1          | X1       | XI       | Crystal Connection. Connect to a 27 MHz fundamental crystal or clock.                                    |
| 2          | VDD      | Power    | Connect to +3.3 V or +5 V.                                                                               |
| 3          | GND      | Power    | Connect to ground.                                                                                       |
| 4          | 27M      | Output   | 27 MHz buffered reference clock output.                                                                  |
| 5          | CLK      | Output   | Audio clock output per table above.                                                                      |
| 6          | S1       | Input    | Audio clock frequency select input #1. Determines CLK output per table above. Internal pull-up resistor. |
| 7          | S0       | Input    | Audio clock frequency select input #0. Determines CLK output per table above. Internal pull-up resistor. |
| 8          | X2       | XO       | Crystal connection to a 27 MHz crystal, or leave unconnected for clock output.                           |

## External Components

### Decoupling Capacitor

As with any high-performance mixed-signal IC, the MK2703 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01  $\mu$ F must be connected between VDD and GND on pins 2 and 3. It must be connected close to the MK2703 to minimize lead inductance. No external power supply filtering is required for the MK2703.

### Series Termination Resistor

A 33  $\Omega$  terminating resistor can be used next to the clock outputs for trace lengths over one inch.

### Crystal Load Capacitors

The total on-chip capacitance is approximately 16 pF. A parallel resonant, fundamental mode, AT cut 27 MHz crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the

stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be

connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal  $(C_L - 16 \text{ pF}) \times 2$ . In this equation,  $C_L$  = crystal load capacitance in pF. Example: For a crystal with an 18 pF load capacitance, each crystal capacitor would be 4 pF  $[(18 - 16) \times 2] = 4$ .

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2703. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                                 | Rating              |
|------------------------------------------------------|---------------------|
| Supply Voltage, VDD                                  | -0.5 V to 7 V       |
| All Inputs and Outputs                               | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature, MK2703S (commercial)  | 0 to +70° C         |
| Ambient Operating Temperature, MK2703SI (industrial) | -40 to +85° C       |
| Storage Temperature                                  | -65 to +150° C      |
| Soldering Temperature                                | 260° C              |

## Recommended Operation Conditions

| Parameter                                         | Min.  | Typ. | Max.  | Units |
|---------------------------------------------------|-------|------|-------|-------|
| Ambient Operating Temperature                     | -40   |      | +85   | ° C   |
| Power Supply Voltage (measured in respect to GND) | +3.13 |      | +5.50 | V     |

## DC Electrical Characteristics

VDD=3.3 V  $\pm 5\%$ , Ambient temperature -40 to +85° C, unless stated otherwise

| Parameter           | Symbol          | Conditions               | Min.      | Typ.  | Max.      | Units |
|---------------------|-----------------|--------------------------|-----------|-------|-----------|-------|
| Operating Voltage   | VDD             |                          | 3.13      |       | 5.50      | V     |
| Input High Voltage  | V <sub>IH</sub> | X1 pin only<br>Note 1    | (VDD/2)+1 | VDD/2 |           | V     |
| Input Low Voltage   | V <sub>IL</sub> | X1 pin only<br>Note 1    |           | VDD/2 | (VDD/2)-1 | V     |
| Input High Voltage  | V <sub>IH</sub> | S0, S1 pins              | 2.0       |       |           | V     |
| Input Low Voltage   | V <sub>IL</sub> | S0, S1 pins              |           |       | 0.8       | V     |
| Output High Voltage | V <sub>OH</sub> | I <sub>OH</sub> = -12 mA | 2.4       |       |           | V     |

| Parameter                       | Symbol    | Conditions               | Min.    | Typ.     | Max. | Units      |
|---------------------------------|-----------|--------------------------|---------|----------|------|------------|
| Output Low Voltage              | $V_{OL}$  | $I_{OL} = 12 \text{ mA}$ |         |          | 0.4  | V          |
| Output High Voltage, CMOS level | $V_{OH}$  | $I_{OH} = -4 \text{ mA}$ | VDD-0.4 |          |      | V          |
| Operating Supply Current        | IDD       | No load<br>VDD = 3.3 V   |         | 25       |      | mA         |
| Short Circuit Current           |           | CLK output               |         | $\pm 50$ |      | mA         |
| Input Capacitance               | $C_{IN}$  | S0, S1 pins              |         | 5        |      | pF         |
| Nominal Output Impedance        |           |                          |         | 20       |      | $\Omega$   |
| Frequency Synthesis Error       |           | All Clocks               |         |          | 0    | ppm        |
| Internal Pull-up Resistor       | $R_{PUP}$ | S1, S0 pins              |         | 500      |      | k $\Omega$ |

Note 1: CMOS level input. Nominal trigger point is VDD/2 for 3.3 V or 5 V operation.

## AC Electrical Characteristics

VDD = 3.3 V  $\pm 5\%$ , Ambient Temperature -40 to +85° C, unless stated otherwise

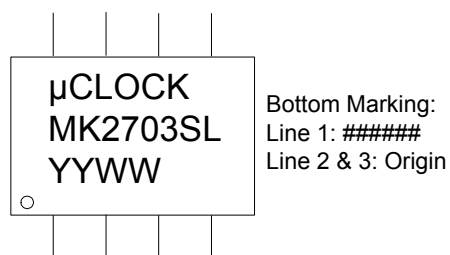
| Parameter                               | Symbol   | Conditions           | Min. | Typ.      | Max. | Units |
|-----------------------------------------|----------|----------------------|------|-----------|------|-------|
| Input Crystal or Clock Frequency        | $F_{IN}$ |                      |      | 27        |      | MHz   |
| Output Clock Rise Time                  | $t_{OR}$ | 0.8 to 2.0 V, Note 1 |      |           | 1.5  | ns    |
| Output Clock Fall Time                  | $t_{OF}$ | 2.0 to 8.0 V, Note 1 |      |           | 1.5  | ns    |
| Clock Stabilization Time after Power-up |          |                      |      |           | 10   | ms    |
| Changing Frequency Setting              |          |                      |      |           | 10   | ms    |
| Output Clock Duty Cycle                 |          | at VDD/2, Note 1     | 40   |           | 60   | %     |
| Maximum Absolute Jitter, short term     | $t_{ja}$ | Deviation from mean  |      | $\pm 190$ |      | ps    |

Note 1: Measured with 15 pF load.

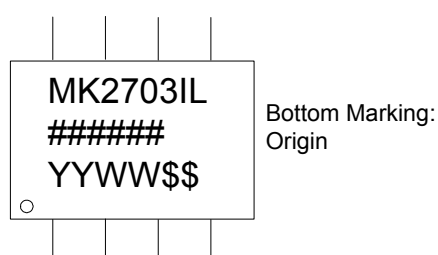
## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units |
|----------------------------------------|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 150  |      | °C/W  |
|                                        | $\theta_{JA}$ | 1 m/s air flow |      | 140  |      | °C/W  |
|                                        | $\theta_{JA}$ | 3 m/s air flow |      | 120  |      | °C/W  |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 40   |      | °C/W  |

## Marking Diagram - MK2703SLF



## Marking Diagram - MK2703SILF

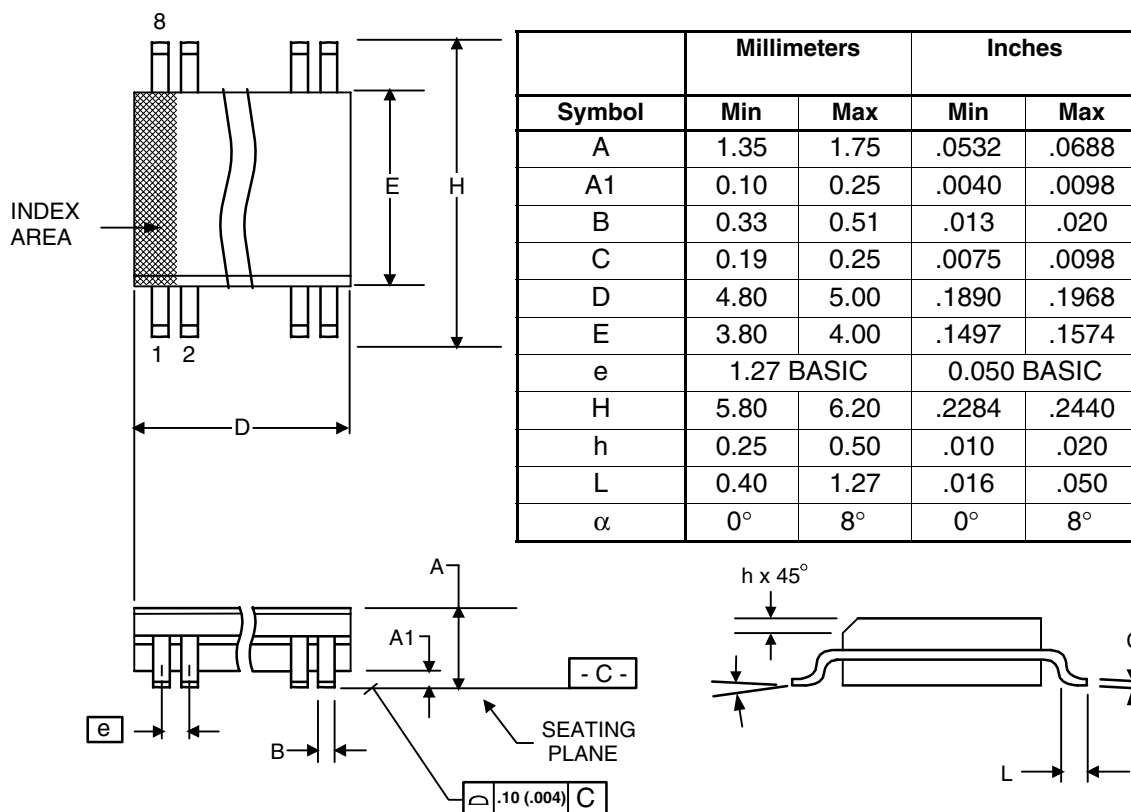


### Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and the week number that the part was assembled.
3. Bottom mark denotes country of origin.

## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



## Ordering Information

| Part / Order Number | Marking    | Shipping Packaging | Package    | Temperature   |
|---------------------|------------|--------------------|------------|---------------|
| MK2703SLF           | see page 5 | Tubes              | 8-pin SOIC | 0 to +70° C   |
| MK2703SLFTR         |            | Tape and Reel      | 8-pin SOIC | 0 to +70° C   |
| MK2703SILF          | see page 5 | Tubes              | 8-pin SOIC | -40 to +85° C |
| MK2703SILFTR        |            | Tape and Reel      | 8-pin SOIC | -40 to +85° C |

“LF” denotes Pb (lead) free package.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

**MK2703**

**PLL AUDIO CLOCK SYNTHESIZER**

**CLOCK SYNTHESIZER**

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.