



Low voltage CMOS 16-bit bus buffer (3-state non inverter) with 3.6 V tolerant inputs and outputs



FLAT-48 The upper metallic lid is internally connected to ground

Product status link

54VCXH162244

Features

- 1.8 to 3.6 V operating voltage
- 5 ns propagation delay
- 100 mV typical input hysteresis
- Power down protection on inputs and outputs
- Symmetrical output impedance
- 26 Ω series resistance in outputs
- · Bus hold on data inputs
- · Cold spare function
- Latch-up performance exceeds 300 mA (JESD 17)
- 300 krad(Si) total ionizing dose (TID)
- No SEL, no SEU and no SET at 110 MeV.cm2/mg LET
- QML-V qualified
- SMD 5962F05210

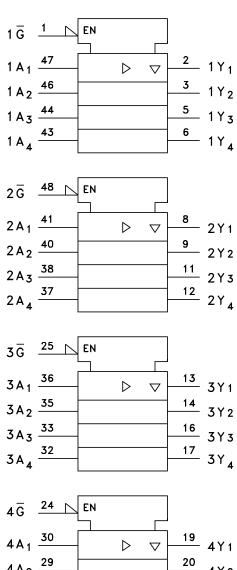
Description

The 54VCXH162244 is a low voltage CMOS 16-bit bus buffer (non inverted) fabricated with submicron silicon gate and five-layer metal wiring C²MOS technology. It is ideal for low power and very high speed 1.8 V to 3.6 V applications; it can be interfaced to 3.6 V signal environment for both inputs and outputs. Any nG output control governs four BUS buffers. Output enable input (nG) tied together gives full 16-bit operation. When nG is low, the outputs are on. When nG is high, the output are in high impedance state. This device is designed to be used with 3-state memory address drivers, etc. Bus hold on data inputs is provided in order to eliminate the need for external pull-up or pull-down resistor. The device circuits is including 26 Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2 kV ESD immunity and transient excess voltage.



Logic symbols and I/O equivalent circuit

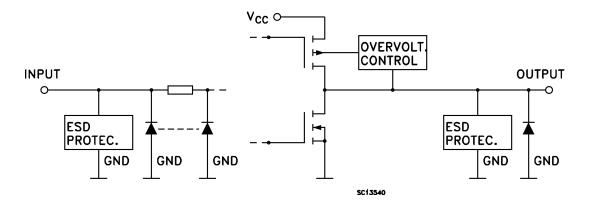
Figure 1. IEC logic symbols



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Figure 2. Input and output equivalent circuit



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2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view) <u>1G</u> □ 48 2G 1 Y ₁ 2 🖂 □ 47 1A₁ 1 Y 2 3 🗔 □ 46 1A₂ GND 4 □ 45 GND □ 44 1A₃ 1Y₃ 5 1Y₄ 6 □ 43 1A₄ 42 V_{CC} V_{CC} 7 <u></u> 2Y₁ 8 🗆 □ 41 2A₁ 2Y₂ 9 🗔 □ 40 2A₂ GND 10 □ 39 GND 2Y₃ 11 □ 38 2A₃ 2Y₄ 12 □ 37 2A₄ 3Y₁ 13 □ 36 3A₁ 3Y₂ 14 □ 35 3A₂ GND 15 ☐ 34 GND 3Y₃ 16 33 3A₃ 3Y₄ 17 □ 32 3A₄ V_{CC} 18 □ 31 V_{CC} 4Y₁ 19 □ 30 4A₁ 4Y₂ 20 □ 29 4A₂ GND 21 □ 28 GND 4Y₃ 22 □ 27 4A₃ 4Y₄ 23 🗆 □ 26 4A₄ 4G 24 □ □ 25 <u>3G</u>

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Pin description 2.2

Table 1. Pin description

Pin	Symbol	Name and function
1	1G	Output enable input
2, 3, 5, 6	1Y1 to 1Y4	Data outputs
8, 9, 11, 12	2Y1 to 2Y4	Data outputs
13, 14, 16, 17	3Y1 to 3Y4	Data outputs
19, 20, 22, 23	4Y1 to 4Y4	Data outputs
24	4 G	Output enable input
25	3 G	Output enable input
30, 29, 27, 26	4A1 to 4A4	Data outputs
36, 35, 33, 32	3A1 to 3A4	Data outputs
41, 40, 38, 37	2A1 to 2A4	Data outputs
47, 46, 44, 43	1A1 to 1A4	Data outputs
48	2 G	Output enable input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	VCC	Positive supply voltage

2.3 **Truth table**

Table 2. Truth table

Inputs		Outputs	
G	An	Yn	
L	L	L	
L	Н	Н	
Н	X	Z	

X = do not care; Z = high impedance

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3 Maximum ratings

Stressing the device above the rating listed in the "absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	-0.5 to +4.6	V
VI	DC input voltage	-0.5 to +4.6	V
Vo	DC output voltage (OFF-state) ⁽¹⁾	-0.5 to +4.6	V
Vo	DC output voltage (high or low-state)	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC input diode current	-50	mA
I _{OK}	DC output diode current ⁽²⁾	-50	mA
Io	DC output current	±50	mA
I _{CC} or I _{GND}	DC V _{CC} or ground current per supply pin	±100	mA
P _D	Power dissipation	400	mW
T _{stg}	Storage temperature	-65 to +150	°C
TL	Lead temperature (10 s)	260	°C
R _{thjc}	Thermal resistance junction-to-case ⁽³⁾	22	°C/W
ESD	HBM: human body model ⁽⁴⁾	2	kV

^{1.} I_{O} absolute maximum rating must be observed.

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^{2.} $V_{O} < GND, V_{O} > V_{CC}$.

^{3.} Short-circuits can cause excessive heating and destructive dissipation. Values are typical.

^{4.} Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.



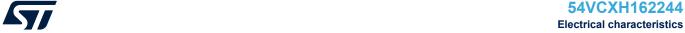
3.1 Recommended conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	1.8 to 3.6	V
VI	Input voltage	-0.3 to 3.6	V
Vo	Output voltage (OFF-state)	0 to 3.6	V
Vo	Output voltage (high or low-state)	0 to VCC	V
I _{OH} , I _{OL}	High or low level output current (V _{CC} = 3.0 to 3.6 V)	± 12	mA
I _{OH} , I _{OL}	High or low level output current (V _{CC} = 2.3 to 2.7 V)	± 8	mA
T _{op}	Operating temperature	-55 to 125	°C
dt/dv	Input rise and fall time ⁽¹⁾	0 to 10	ns/V

^{1.} V_{IN} from 0.8 V to 2 V at V_{CC} = 3.0 V.

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Electrical characteristics

Table 5. DC specifications

			Value				
Symbol	Parameter	V 00		-55 to 1	25 °C	Unit	
		V _{CC} (V)		Min.	Max.		
V _{IH}	High level input voltage	0.74.00		2.0		.,	
V _{IL}	Low level input voltage	2.7 to 3.6			0.8	V	
		2.7 to 3.6	Ι _Ο = -100 μΑ	V _{CC} -0.2			
V		2.7	I _O = -6 mA	2.2			
V _{OH}	High level output voltage	0.0	I _O = -8 mA	2.4		V	
		3.0	I _O = -12 mA	2.2			
		2.7 to 3.6	Ι _Ο = 100 μΑ		0.2		
.,		2.7	I _O = 6 mA		0.4	V	
V _{OL}	Low level output voltage		I _O = 8 mA		0.5		
		3	I _O = 12 mA		0.8		
II	Input leakage current	2.7 to 3.6	V _I = V _{CC} or GND		±5	μA	
			V _I = 0.8 V	75			
I _{I(HOLD)}	Input hold current	3	V _I = 2 V	-75		μA	
		3.6	VI = 0 to 3.6 V		±500		
I _{off}	Power off leakage current	0	V_I or V_O = 0 to 3.6 V		10	μA	
l _{OZ}	High impedance output leakage current	2.7 to 3.6	$V_I = V_{IH}$ or $V_{IL}V_O = 0$ to 3.6 V		±10	μA	
1	Outroped supply supply	274222	$V_I = V_{CC}$ or GND		20	μA	
I _{CC} Quiescent supply c	Quiescent supply current	2.7 to 3.6	V_{I} or $V_{O} = V_{CC}$ to 3.6 V		±20	μA	
Δl _{CC}	I _{CC} incr. per input	2.7 to 3.6	V _{IH} = V _{CC} - 0.6 V		750	μA	

Table 6. DC specifications

		Test conditions		Value		
Symbol	Parameter	V _{CC} (V)		-55 to 125 °C		Unit
		VCC (V)		Min.	Max.	
Viii	V _{IH} High level input voltage	2.3		1.6		
VIII		1.8		1.2		V
Vu	V _{IL} Low level input voltage	2.3			0.7	V
VIL.		1.8			0.4	
	High level output voltage	2.3	$I_O = -6 \text{ mA}$	1.8		
V _{OH}			I _O = -8 mA	1.7		V
		1.8	I _O = -4 mA	1.4		
	Low level output voltage	2.3	I _O = 6 mA		0.4	V
V _{OL}			I _O = 8 mA		0.6	
		1.8	I _O = 4 mA		0.3	

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Table 7.	Dynamic	switching	charact	eristics

Cumbal	Symbol Parameter Vo		Test conditions			Unit
Symbol				Min.	Max.	Unit
V _{OLP}	Low level V _{CC} bounce noise (1)(2)	2.2	., ., .,		500	m\/
V _{OLV}	Low level VCC bounce noise	3.3	$V_{IL} = 0 \text{ V}, V_{IH} = V_{CC}$		-350	mV
V _{OHP}	High level V _{CC} bounce noise (2)(3)	2.2	$C_L = 30 \text{ pF, } R_L = 500 \text{ ohm}$		850	m\/
V _{OHV}	Lifti level ACC portice tioise (=v=)	3.3	25 0		-1050	mV

- 1. Number of outputs defined as "n". Measured with "n-1" output switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.
- 2. Parameters guaranteed by design.
- 3. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.

Table 8. AC electrical characteristics

			Value			
Symbol Parame	Parameter	V 00		-55 to	125 °C	Unit
		V _{CC} (V)		Min.	Max.	
		3.6		0.8	5	
t _{PLH} , t _{PHL}	t _{PLH} , t _{PHL} Propagation delay time	2.3		1	5.2	ns
		1.8		1	8.2	
		3.6	C. = 20 pE B. = 500 ohm	0.8	4.2	ns
t _{PZL} , t _{PZH}	Output enable time	2.3	$C_L = 30 \text{ pF, } R_L = 500 \text{ ohm}$ tr = tf = 2 ns	1	5.8	
		1.8		1	8.7	
		3.6		0.8	4	
t _{PLZ} , t _{PHZ}	Output disable time	2.3		1	4.5	
		1.8		1	5.8	

Table 9. Capacitive characteristics

Sumbol Barranton		Test		Value	Unit	
Symbol	Parameter	V _{CC} (V)		Min.	Max.	Unit
C _{IN}	Input capacitance	GND	25°C		10	pF
C _{OUT}	Output capacitance	3.3	25°C		12	pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	3.3	25 °C, F=1 MHz		80	pF

CPD is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current
consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation.

I_{CC(opr)} = C_{PD} x V_{CC} x f_{IN} + I_{CC}/16 (per circuit).

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5 Test circuit

Figure 4. Application circuit

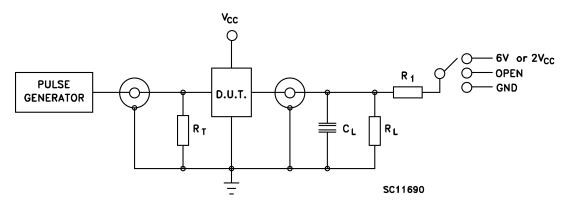


Table 10. Test circuit

Symbol	V _{CC}				
- Cymbei	1.8 V and 2.3 V to 2.7 V	3.0 v to 3.6 V			
V _{IH}	V _{CC}	2.7 V			
V_{M}	V _{CC/2}	1.5 V			
V _X	V _{OL} + 0.15 V	V _{OL} + 0.3 V			
V _Y	V _{OH} - 0.15 V	V _{OH} - 0.3 V			

 C_L = 30 pF or equivalent (includes jig and probe capacitance)

 R_L = R_1 = 500 Ω or equivalent

 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

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6 Waveforms

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)

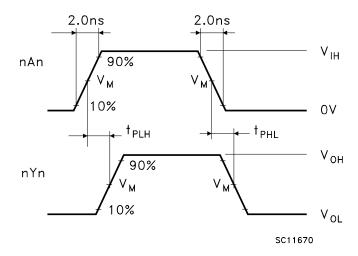
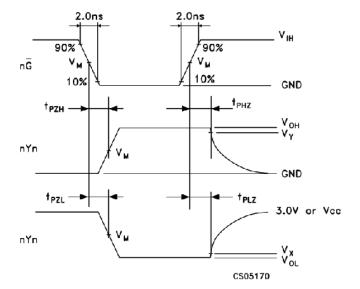


Figure 6. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)



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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 FLAT-48 package information

N Places

N-2 Places

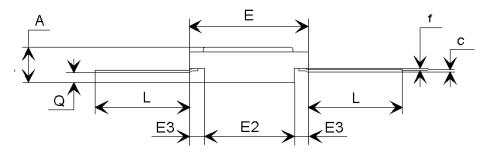
D

S1

Figure 7. FLAT-48 package outline

25

4 Places



24

Note: The upper metallic lid is internally connected to ground

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Table 11. FLAT-48 package mechanical data

Cumbal		mm		Inches ⁽¹⁾		
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	2.18	2.47	2.72	.086	.097	.107
b	0.20	0.254	0.30	.008	.010	.012
С	0.12	0.15	0.18	.005	.006	.007
D	15.57	15.75	15.92	.613	.620	.627
E	9.52	9.65	9.78	.375	.380	.385
E2	6.22	6.35	6.48	.245	.250	.255
E3	1.52	1.65	1.78	.060	.065	.070
е		0.635			.025	
f		0.20			.008	
L	6.85	8.38	9.40	.270	.330	.370
Q	0.66	0.79	0.92	.026	.031	.036
S1	0.25	0.43	0.61	.010	.017	.024

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

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8 Ordering information

Order code	SMD ⁽¹⁾	Qualification level	Mass	Package	Lead finish	Marking ⁽²⁾	Packing
RHFXH162244K1	-	Engineering model	1.5 g	Flat-48		RHFXH162244K1	
RHFXH162244K03V	5962F05210	QML-V Flight			Gold	5962F0521002VXC	Conductive strip pack
RHFXH162244K05V	5962F05210	QML-V Flight		Flat-48 with grounded lid		5962F0521002VYC	

- 1. Standard microcircuit drawing
- 2. Specific marking only. Complete marking includes the following:
 - ST logo
 - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)

Other information

Date code:

The date code is structured as engineering model: EM xyywwz Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 12. Product documentation

Quality level	Item			
Engineering model	Certificate of conformance including :			
	Customer name			
	Customer purchase order number			
	ST sales order number and item			
	ST part number			
	Quantity delivered			
	Date code			
	Reference to ST datasheet			
	Reference to TN1181 on engineering models			
	ST Rennes assembly lot ID			
	Certificate of Conformance including:			
	Customer name			
	Customer purchase order number			
OMI VIII-bi	ST sales order number and item			
QML-V Flight	ST part number			
	Quantity delivered			
	Date code			
	Serial numbers			

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Quality level	Item			
QML-V Flight	Group C reference			
	Group D reference			
	Reference to the applicable SMD			
	ST Rennes assembly lot ID			
	Quality control inspection (groups A, B, C, D, E)			
	Screening electrical data in/out summary			
	Precap report			
	PIND (particle impact noise detection) test			
	SEM (scanning electronic microscope) inspection report			
	X-ray plates			

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Revision history

Table 13. Document revision history

Date	Version	Changes
09-Jul-2004	1	Initial release.
17-May-2005	2	SMD qualified
19-Jun-2006	3	300 krad bullet updated, new template, mechanical data updated
11-Apr-2007	4	Updated cover page features
30-Jul-2007	5	Typo in Table 12 on page 14
17-Sep-2008	6	Updated cover page
09-Jan-2009	7	Updated cover page
23-Sep-2009	8	Updated Table 13 on page 16
29-Jul-2011	9	Added Note: on page 15 and in the "Pin connections" diagram on the cover page.
11-Jun-2019	10	Updated cover image, Section 7.1: FLAT-48 package information and Section 8: Ordering information.
		Updated figure and features on the cover page.
22-Jan-2024	11	Updated Table 6. DC specifications, Table 7. Dynamic switching characteristics, Table 8. AC electrical characteristics, Table 10, Section 8: Ordering information.

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