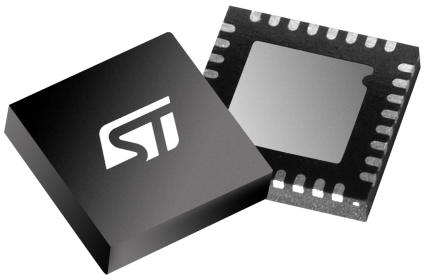
L9961

Data brief

Battery management system solution



VFQFPN32
(5x5x1.00 mm)

Features

- 2 µA SHIPMENT - DEEP SLEEP mode current and 5 µA Standby consumption (with VREG LDO active)
- Integrated 3.3 V VREG LDO for supplying MCU and LEDs
- Measures Cell Voltage (3 to 5 cells), with Over/Under voltage detection and Balance Under voltage protection
- 12-bit voltage measurement with maximum error of ± 15 mV in the [1.5 – 4.5] V range, for -40 °C < TJ < 105 °C
- Measures Stack Voltage, with Over/Under voltage detection and Plausibility Check vs. Sum Of Cells
- Measures Pack Temperature via NTC, with Over/Under Temperature detection
- Ratiometric temperature measurement with ± 0.8% max. gain error in the [0.2 – VREG] V range, for -40 °C < TJ < 105 °C
- Measures Battery Current, with Coulomb Counting, Over current (both directions) and Short-circuit in discharge protection.
- 16-bit signed current measurement with maximum error of 0.25%, for -40 °C < TJ < 120 °C after customer end of line calibration with a single point
- I^2C peripheral for device programming and data transfers over I^2C bus
- Cell balancing supporting up to 70 mA per cell
- Dual configurable HS/LS pre-driver for pack relay management
- Pack fuse management
- Embedded NVM for configuration parameters storage
- High hot plug robustness

Application

- Cordless Power Tools
- Backup energy storage systems and UPS
- Light Electric Vehicles (E-bikes, Scooters, etc.)
- Portable and semi-portable equipment
- Medical Equipment

Product status link
L9961

Product label

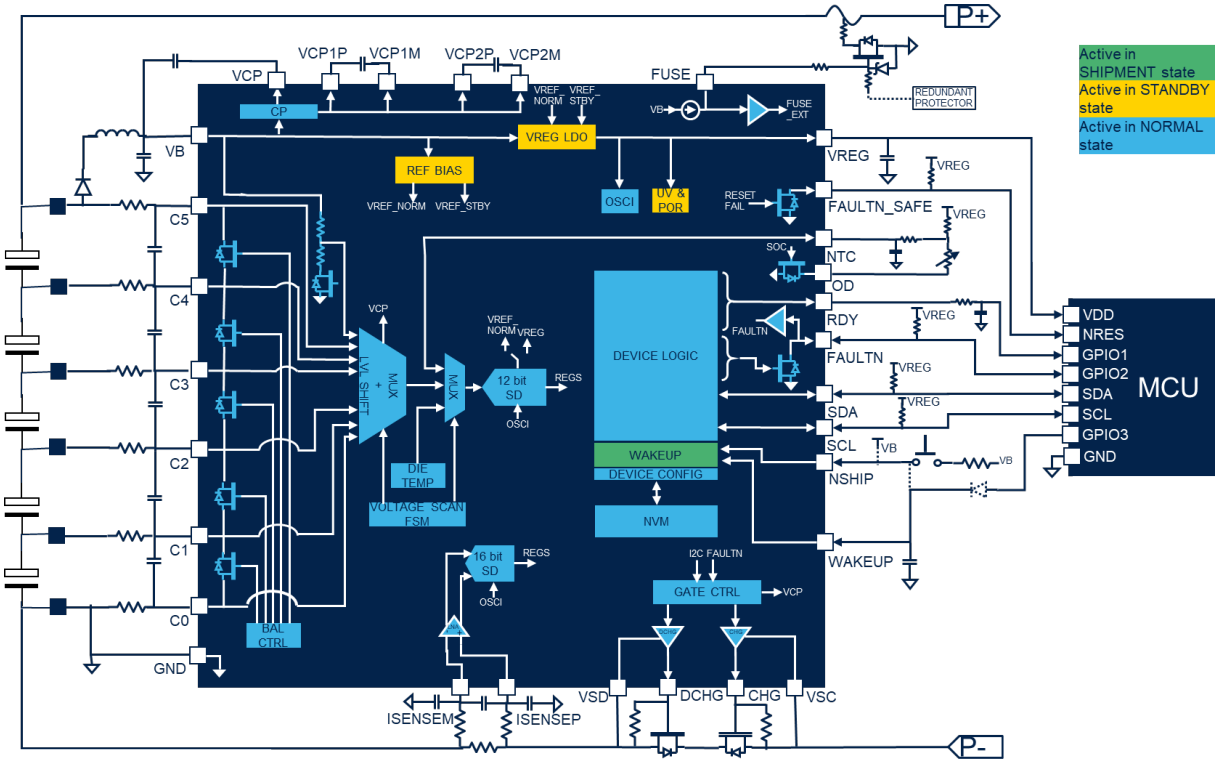

Product summary		
Order code	Package	Packing
L9961	VFQFPN32	Tray
L9961-TR		Tape and Reel

Description

The L9961 is part of a complete battery pack monitoring, balancing, and protection system for Li-Ion and Li-Polymer cells in 3, 4 or 5 series configurations. The L9961 uses a high precision ADC to provide cell voltage, stack voltage and temperature conversion via external NTC. Voltage monitoring functions are cyclically performed with a programmable loop time. Stack current is also monitored via a high accuracy CSA, continuously running and performing also Coulomb Counting. Cell balancing is available and can be simultaneously activated on all cells. IC configuration and information exchange for SOC/SOH estimation are performed via I^2C peripheral. The IC also integrates a dual pre-driver programmable in both HS/LS configurations for driving pack relays. L9961 also implements battery pack fuse protection to prevent fire and explosion hazards. A 3.3 V regulator with a high current capability is available for supplying pack controller and other external circuitry in both standby and normal operation modes. The IC protects the battery pack against over/under voltage conditions and monitors for over/under temperature. It also features protection against over current (both directions) and short-circuit in discharge events. Safety-relevant configurations can be stored in the internal NVM to avoid re-programming the device at each wakeup.

1 Block and typical application diagrams

Figure 1. **Block and typical application diagrams**



2 Pin description

Table 1. **Pin description**

Pin #	Name	Function	Type
1	C0	Cell 1 negative terminal	Analog Input
2	ISENSEP	Current Sense ADC positive input terminal	Analog Input
3	ISENSEM	Current Sense ADC negative input terminal	Analog Input
4	GND	Device Ground	Power Input
5	SCL	I^2C Clock line	Digital Input
6	SDA	I^2C Data line	Digital Input/Open Drain
7	RDY	Ready interrupt output	Push/Pull
8	VREG	3.3 V LDO output	Power Output
9	NTC	NTC sensing input	Analog Input
10	OD	Open-Drain switch for NTC connection to GND	Open Drain
11	FAULTN_SAFE	Critical Fault output	Open Drain
12	FAULTN	Fault output/external CHG/DCHG shutdown trigger	Digital Input/Open Drain
13	TM_ENTER	Reserved for Debug, connect to GND.	-
14	WAKEUP	Wakeup from STANDBY input	Digital Input/Output
15	NSHIP	Wakeup from SHIPMENT - DEEP SLEEP input	Analog Input
16	FUSE	Fuse pre-driver output/external Fuse activation trigger	Analog Output/Digital Input
17	DCHG	Discharge switch Gate	Analog Output
18	VSD	Discharge switch Source	Analog Output
19	VSC	Charge switch Source	Analog Output
20	CHG	Charge switch Gate	Analog Output
21	VCP1M	Charge Pump flying capacitor input	Analog
22	VCP1P	Charge Pump flying capacitor input	Analog
23	VCP2M	Charge Pump flying capacitor input	Analog
24	VCP2P	Charge Pump flying capacitor input	Analog
25	VCP	Charge Pump output	Power Output
26	VB	Device battery input	Power Input
27	TM1	Reserved for debug, connect to GND.	-
28	C5	Cell 5 positive terminal	Analog Input
29	C4	Cell 4 positive terminal	Analog Input
30	C3	Cell 3 positive terminal	Analog Input
31	C2	Cell 2 positive terminal	Analog Input
32	C1	Cell 1 positive terminal	Analog Input

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 VFQFPN (5x5x1.00 mm) package information

Figure 2. VFQFPN (5x5x1.00 mm) package outline

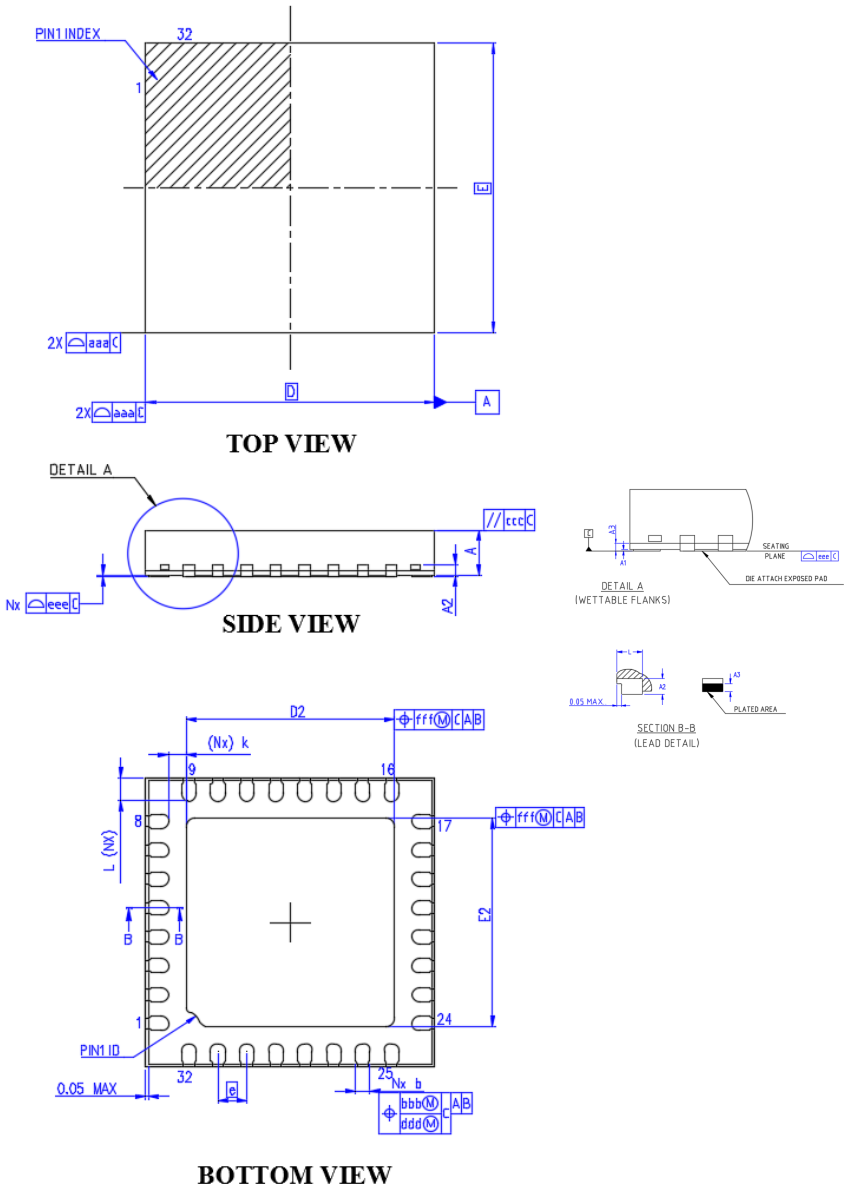


Table 2. **VFQFPN (5x5x1.00 mm) package mechanical data**

Symbol	Dimensions in mm			Note
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	12
A1	0.00	-	0.05	9,12
A2		0.2 REF.		-
A3	0.10	-	-	12
b	0.20	0.25	0.30	5, 6, 7, 12, 13
D		5.00 BSC		4, 1
D2	3.50	3.60	3.70	10,12
e		0.50 BSC		12
E		5.00 BSC		4, 12
E2	3.50	3.60	3.70	10, 12
L	0.30	0.40	0.50	12, 13
k	0.20	-	-	-
N		32		8
Tolerance of form and position				
aaa		0.15		-
bbb		0.10		-
ccc		0.10		-
ddd		0.05		-
eee		0.08		-
fff		0.10		-
NOTE		1.12		-
REF		-		-

NOTES

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *All Dimensions are in millimeters.*
3. *Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked or metallized feature.*
4. *Outlines with “D” and “E” increments less than 0.5 mm should be registered as “stand alone” outlines. These outlines should use as many of the algorithms and dimensions states in the design standard as possible to insure predictability in manufacturing.*
5. *Dimension ‘b’ / ‘b1’ / ‘b2’ applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension ‘b’ / ‘b1’ / ‘b2’ should not be measured in that radius area.*
6. *Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap “k”. This feature should not affect the terminal width “b” / ‘b1’ / ‘b2’, which is measured L/2 from the edge of the package body.*
7. *Exact shape of the leads at the edge of the package is optional.*

8. *"N" is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions:*
   - *Depopulation scheme must be consistent in each quadrant of the package.*
   - *Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.*
9. *A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).*
10. *Dimension D2 and E2 refer to exposed pad. For exposed pad dimensions see Variations Table.*
11. *For Tolerance of Form and Position see Table.*
12. *Critical dimensions:*
    - *12.1 A*
    - *12.2 A1*
    - *12.3 A3*
    - *12.4 D & E*
    - *12.5 B & L*
    - *12.6 e*
    - *12.7 D2 & E2*
13. *Dimensions "b" / 'b1' / 'b2' and "L" are measured at terminal plating surface.*
14. *For Symbols, Recommended Values and Tolerances see Table below: (ACCORDING TO PACKAGE OR JEDEC SPEC IF REGISTERED)*

Table 3. Symbols, recommended values and tolerances

SYMBOL	DEFINITION	NOTES
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones aredefined by the basic dimensions D and E.	-
bbb	The tolerance that controls the position of the entire terminal pattern with respect to Datum's A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to Datum's A and B.	-
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	-
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
// // //	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be the datum's defined by the centerlines of the package body.	-

Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

Revision history

Table 4. **Document revision history**

Date	Version	Changes
10-Nov-2021	1	Initial release.

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