

NPN Silicon Power Darlington Transistors

MJB5742T4G

The Darlington transistors are designed for high-voltage power switching in inductive circuits.

Features

- These Devices are Pb-Free and are RoHS Compliant

Applications

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{CEO(sus)}$	Collector-Emitter Voltage	400	Vdc
V_{CEV}	Collector-Emitter Voltage	800	Vdc
V_{EB}	Emitter-Base Voltage	8	Vdc
I_C I_{CM}	Collector Current – Continuous – Peak (Note 1)	8 16	Adc
I_B I_{BM}	Base Current – Continuous – Peak (Note 1)	2.5 5	Adc
P_D	Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	2 0.016	W W/ $^\circ\text{C}$
P_D	Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	100 0.8	W W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-65 to +150	$^\circ\text{C}$

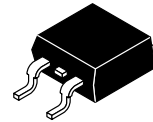
THERMAL CHARACTERISTICS

Symbol	Characteristics	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$
T_L	Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	275	$^\circ\text{C}$

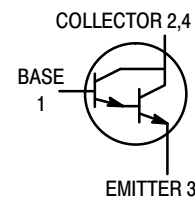
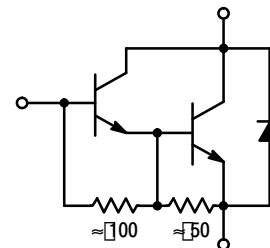
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

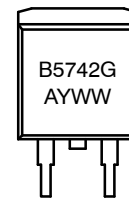
POWER DARLINGTON TRANSISTORS 8 AMPERES, 400 VOLTS 100 WATTS



D²PAK
CASE 418B
STYLE 1



MARKING DIAGRAM



B5742 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
MJB5742T4G	D ² PAK (Pb-Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

MJB5742T4G

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (Note 2)

$V_{CEO(sus)}$	Collector–Emitter Sustaining Voltage ($I_C = 50\text{ mA}$, $I_B = 0$)	400	–	–	Vdc
I_{CEV}	Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	– –	– –	1 5	mAdc
I_{EBO}	Emitter Cutoff Current ($V_{EB} = 8\text{ Vdc}$, $I_C = 0$)	–	–	75	mAdc

SECOND BREAKDOWN

$I_{S/b}$	Second Breakdown Collector Current with Base Forward Biased	See Figure 6			
RBSOA	Clamped Inductive SOA with Base Reverse Biased	See Figure 7			

ON CHARACTERISTICS (Note 2)

h_{FE}	DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 4\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	50 200	100 400	– –	–
$V_{CE(sat)}$	Collector–Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 0.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	– – –	– – –	2 3 2.2	Vdc
$V_{BE(sat)}$	Base–Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 8\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 0.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	– – –	– – –	2.5 3.5 2.4	Vdc
V_f	Diode Forward Voltage (Note 3) ($I_F = 5\text{ Adc}$)	–	–	2.5	Vdc

SWITCHING CHARACTERISTICS

Typical Resistive Load (Table 1)						
t _d	Delay Time	(V _{CC} = 250 Vdc, I _{C(pk)} = 6 A I _{B1} = I _{B2} = 0.25 A, t _p = 25 μs, Duty Cycle ≤ 1%)	–	0.04	–	μs
t _r	Rise Time		–	0.5	–	μs
t _s	Storage Time		–	8	–	μs
t _f	Fall Time		–	2	–	μs
Inductive Load, Clamped (Table 1)						
t _{sv}	Voltage Storage Time	(I _{C(pk)} = 6 A, V _{CE(pk)} = 250 Vdc I _{B1} = 0.06 A, V _{BE(off)} = 5 Vdc)	–	4	–	μs
t _c	Crossover Time		–	2	–	μs

2. Pulse Test: Pulse Width 300 μs , Duty Cycle = 2%.

3. The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.



TYPICAL CHARACTERISTICS

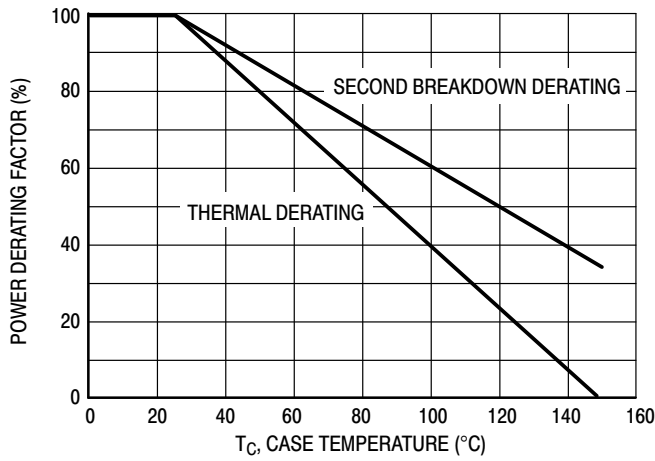


Figure 1. Power Derating

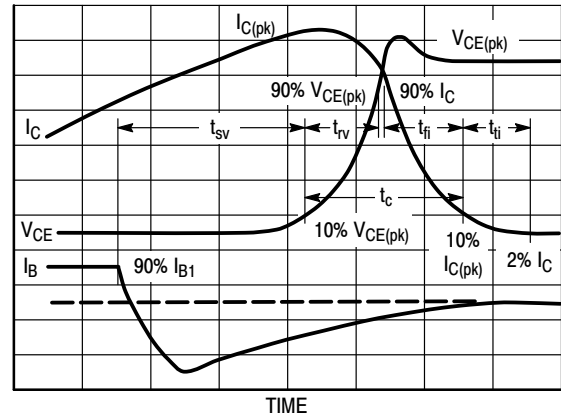


Figure 2. Inductive Switching Measurements

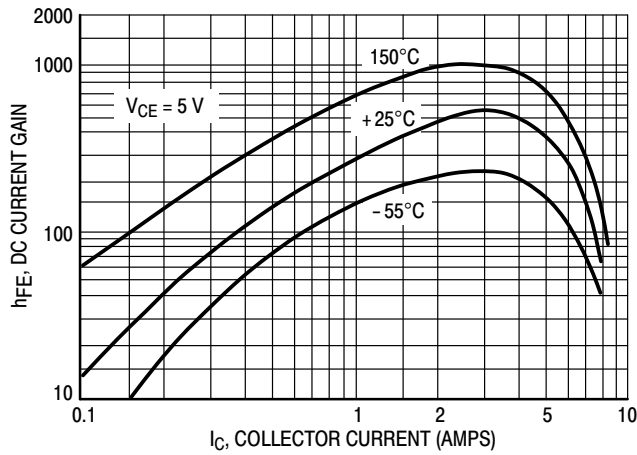


Figure 3. DC Current Gain

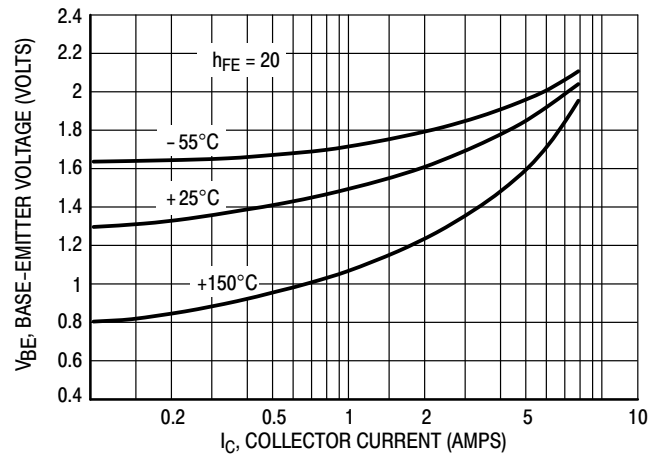


Figure 4. Base-Emitter Voltage

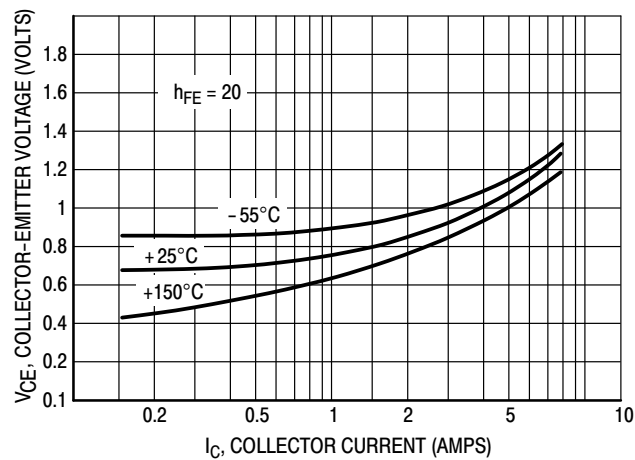


Figure 5. Collector-Emitter Saturation Voltage

MJB5742T4G

Table 1. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING			RESISTIVE SWITCHING
TEST CIRCUITS	DUTY CYCLE $\leq 10\%$ $t_r, t_f \leq 10 \text{ ns}$ NOTE: PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}		
CIRCUIT VALUES	COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~16 TURNS) #16 GAP FOR 200 $\mu\text{H}/20 \text{ A}$ $L_{\text{coil}} = 200 \mu\text{H}$ $V_{CC} = 30 \text{ V}$ $V_{CE(pk)} = 250 \text{ Vdc}$ $I_{C(pk)} = 6 \text{ A}$		$V_{CC} = 250 \text{ V}$ $D1 = 1\text{N}5820 \text{ OR EQUIV.}$
TEST WAVEFORMS	OUTPUT WAVEFORMS t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{\text{coil}} (I_{C(pk)})}{V_{CC}}$ $t_2 \approx \frac{L_{\text{coil}} (I_{C(pk)})}{V_{\text{clamp}}}$ TEST EQUIPMENT SCOPE-TEKTRONICS 475 OR EQUIVALENT		$t_r, t_f < 10 \text{ ns}$ DUTY CYCLE = 1% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

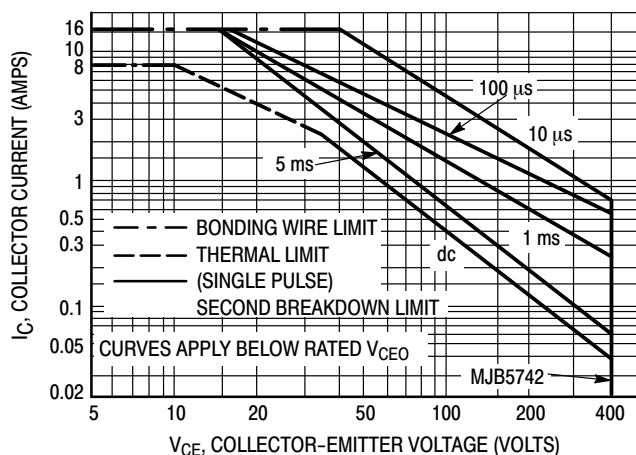


Figure 6. Forward Bias Safe Operating Area

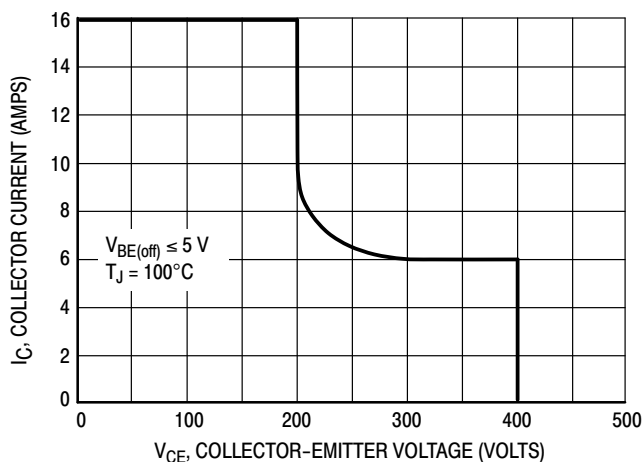


Figure 7. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

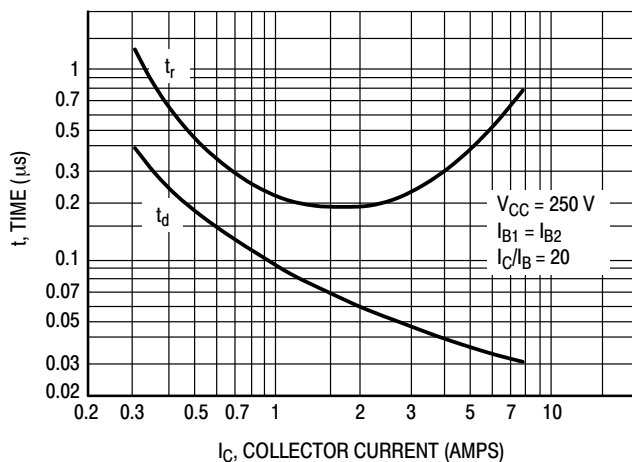


Figure 8. Turn-On Time

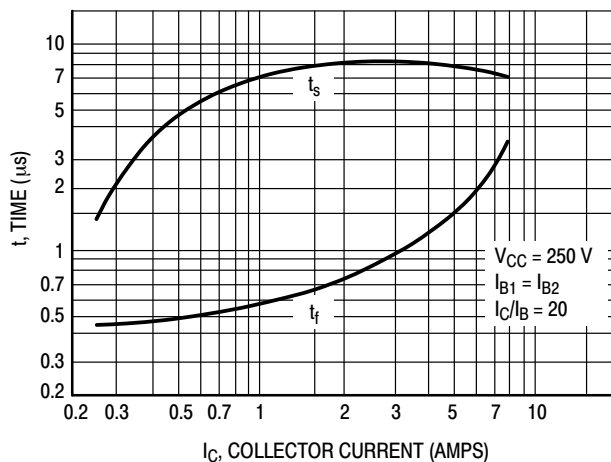
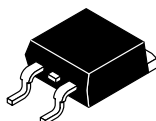


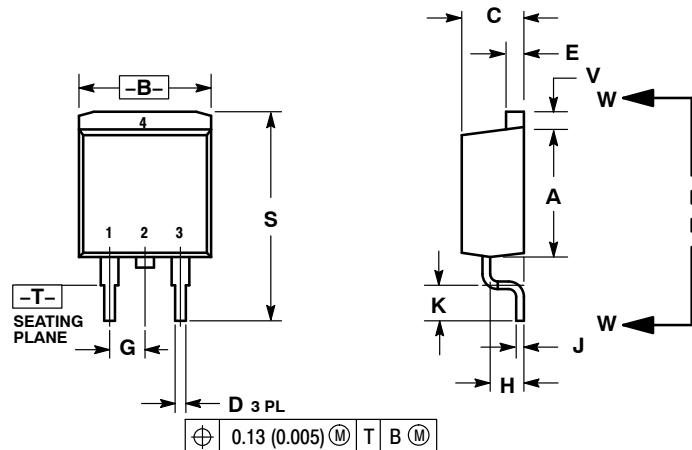
Figure 9. Turn-Off Time



D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

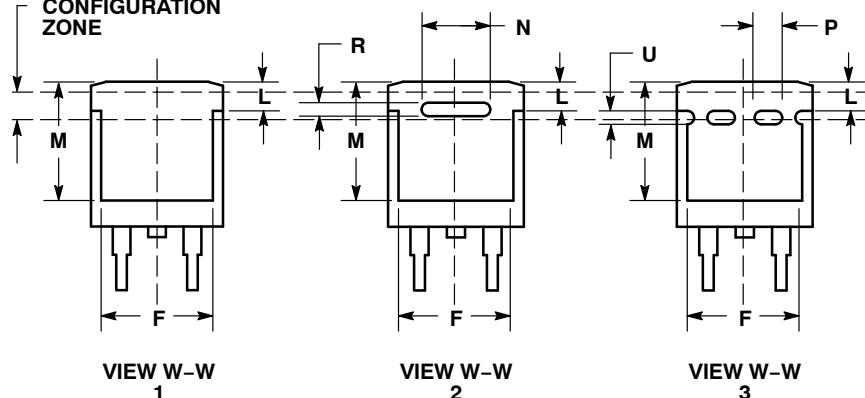


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE
CONFIGURATION
ZONE



STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:

- PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:

- PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:

- PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

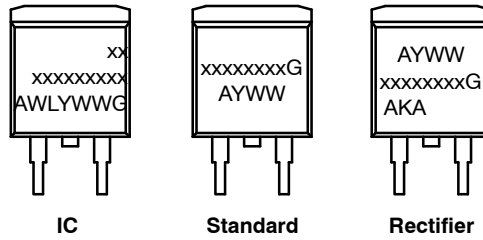
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D²PAK 3
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ISSUE L

DATE 17 FEB 2015

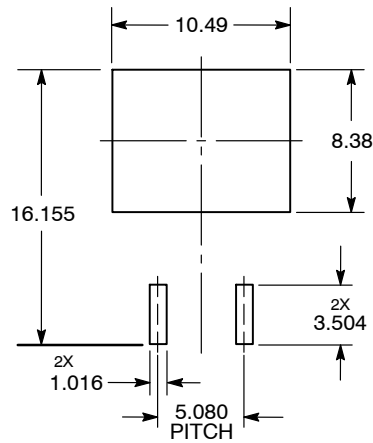
**GENERIC
MARKING DIAGRAM***



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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