S-89230/89240 Series

MINI ANALOG SERIES
CMOS COMPARATOR

www.ablic.com

© ABLIC Inc., 2009-2010

Rev.3.0_02

The mini-analog series is a group of ICs that incorporate a general purpose analog circuit in a small package.
The S-89230/89240 Series is a CMOS type comparator works on a lower voltage and lower current consumption. These features make this product the ideal solution for small battery-powered portable equipment.
This product is a dual comparator (with 2 circuits).

■ Features

- Lower operating voltage than the conventional general-purpose: V_{DD} = 1.8 V to 5.5 V
- Low current consumption (per circuit): I_{DD} = 23 μA Typ. (S-89230 Series)
  I_{DD} = 5 μA Typ. (S-89240 Series)
- Low input offset voltage: 4.0 mV Max.
- Output full swing
- A dual comparator (with 2 circuits)
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

- Mobile phones
- Notebook PCs
- Digital cameras
- Digital video cameras

■ Packages

- SNT-8A
- TMSOP-8

Downloaded from Arrow.com.

■ Block Diagram

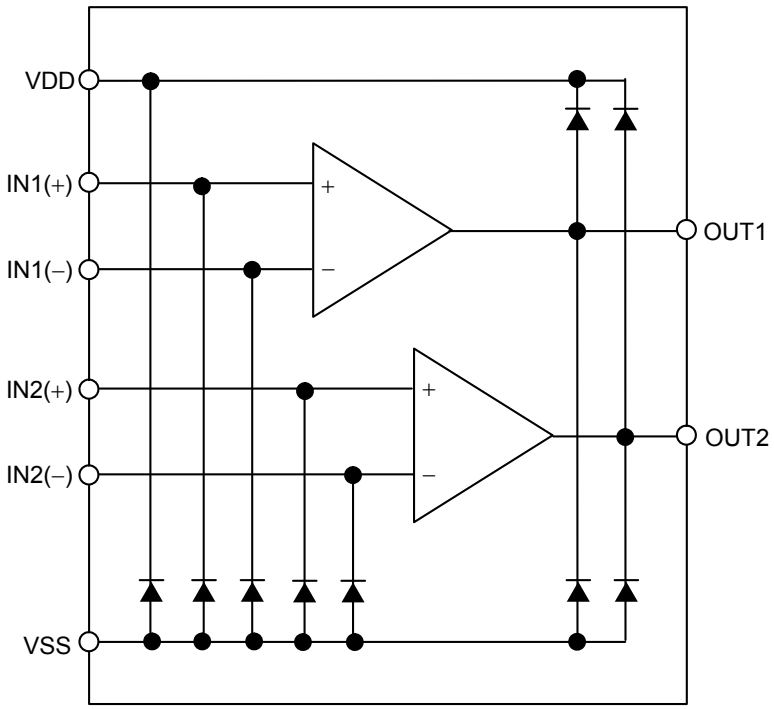


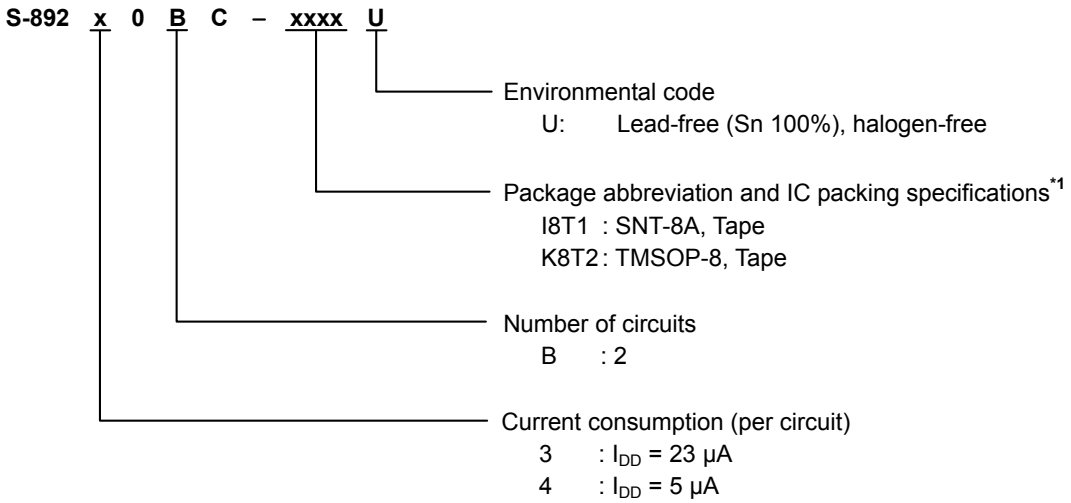
Figure 1

Downloaded from Arrow.com.

■ Product Name Structure

Users can select the product type and package for the S-89230/89240 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Package**" regarding the package drawings and "**3. Product name list**" regarding the product type.

1. Product name



***1.** Refer to the tape specifications.

2. Package

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–

3. Product name list

Table 1

Product name	Current consumption (per circuit)	Rise propagation delay time*1	Fall propagation delay time*1	Number of circuits	Package
S-89230BC-I8T1U	23 µA	26 µs	4 µs	2 circuits	SNT-8A
S-89230BC-K8T2U	23 µA	26 µs	4 µs	2 circuits	TMSOP-8
S-89240BC-I8T1U	5 µA	100 µs	18 µs	2 circuits	SNT-8A
S-89240BC-K8T2U	5 µA	100 µs	18 µs	2 circuits	TMSOP-8

***1.** The value when V_{DD} = 3.0 V

Remark Please select products of environmental code = U for Sn 100%, halogen-free products.

Downloaded from Arrow.com.

■ Pin Configurations

SNT-8A
Top view

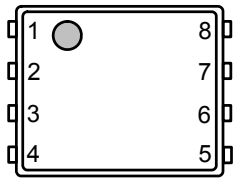


Figure 2

Table 2

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

TMSOP-8
Top view

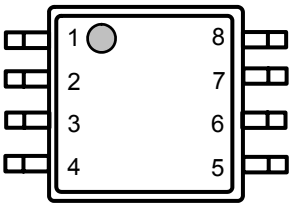


Figure 3

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

Downloaded from Arrow.com.

■ Absolute Maximum Ratings

Table 4

(Ta =+25°C unless otherwise specified)

Parameter		Symbol	Absolute maximum ratings	Unit
Power supply voltage		V_{DD}	V_{SS}−0.3 to V_{SS}+7.0	V
Input voltage		V_{IN}	V_{SS}−0.3 to V_{SS}+7.0	V
Output voltage		V_{OUT}	V_{SS}−0.3 to V_{DD}+0.3	V
Differential input voltage		V_{IND}	±7.0	V
Output pin current		I_{SINK}	20	mA
Power dissipation	SNT-8A	P_D	450*1	mW
	TMSOP-8		650*1	mW
Operating ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

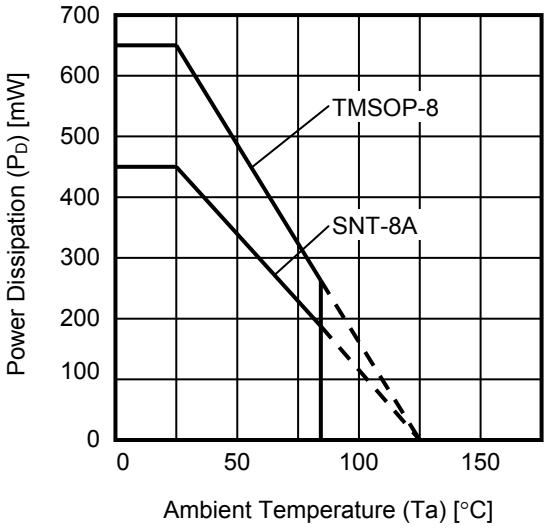


Figure 4 Power Dissipation of Package (When Mounted on Board)

Downloaded from Arrow.com.

■ Electrical Characteristics

Table 5

(Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Range of operating power supply voltage	V_{DD}	–	1.8	–	5.5	V	–

1. V_{DD} = 5.0 V

Table 6

DC Electrical Characteristics (V_{DD} = 5.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	S-89230 Series		–	23	40	μA	5
		S-89240 Series		–	5	9	μA	5
Input offset voltage drift	V_{IO}	–		–4	±3	+4	mV	1
Input offset voltage	$\frac{\Delta V_{IO}}{\Delta Ta}$	Ta = –40°C to +85°C		–	±10	–	μV/°C	1
Input offset current	I_{IO}	–		–	1	–	pA	–
Input bias current	I_{BIAS}	–		–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–		0	–	4.3	V	2
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ		4.9	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ		–	–	0.01	V	4
Common-mode input signal rejection ratio	CMRR	–		60	70	–	dB	2
Power supply voltage rejection ratio	PSRR	–		60	70	–	dB	1
Source current	I_{SOURCE}	V_{OUT} = 0 V	S-89230 Series	120	–	–	μA	6
			S-89240 Series	25	–	–	μA	6
Sink current	I_{SINK}	V_{OUT} = 0.5 V	S-89230 Series	5	–	–	mA	7
			S-89240 Series	3.5	–	–	mA	7

Table 7

AC Electrical Characteristics (V_{DD} = 5.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Rise propagation delay time	t_{PLH}	Overdrive = 100 mV C_L = 15 pF (Refer to **Figure 12**)	S-89230 Series	–	26	–	μs
			S-89240 Series	–	100	–	μs
Fall propagation delay time	t_{PHL}		S-89230 Series	–	5	–	μs
			S-89240 Series	–	22	–	μs
Rise response time	t_{TLH}		S-89230 Series	–	3	–	μs
			S-89240 Series	–	15	–	μs
Fall response time	t_{THL}		S-89230 Series	–	3	–	μs
			S-89240 Series	–	15	–	μs

Downloaded from Arrow.com.

2. V_{DD} = 3.0 V

Table 8

DC Electrical Characteristics (V_{DD} = 3.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	S-89230 Series		–	23	40	μA	5
		S-89240 Series		–	5	9	μA	5
Input offset voltage drift	V_{IO}	–		−4	±3	+4	mV	1
Input offset voltage	$\frac{\Delta V_{IO}}{\Delta Ta}$	Ta = −40°C to +85°C		–	±10	–	μV/°C	1
Input offset current	I_{IO}	–		–	1	–	pA	–
Input bias current	I_{BIAS}	–		–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–		0	–	2.3	V	2
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ		2.9	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ		–	–	0.01	V	4
Common-mode input signal rejection ratio	CMRR	–		60	70	–	dB	2
Power supply voltage rejection ratio	PSRR	–		60	70	–	dB	1
Source current	I_{SOURCE}	V_{OUT} = 0 V	S-89230 Series	120	–	–	μA	6
			S-89240 Series	25	–	–	μA	6
Sink current	I_{SINK}	V_{OUT} = 0.5 V	S-89230 Series	5	–	–	mA	7
			S-89240 Series	3.5	–	–	mA	7

Table 9

AC Electrical Characteristics (V_{DD} = 3.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Rise propagation delay time	t_{PLH}	Overdrive = 100 mV C_L = 15 pF (Refer to **Figure 12**)	S-89230 Series	–	26	–	μs
			S-89240 Series	–	100	–	μs
Fall propagation delay time	t_{PHL}		S-89230 Series	–	4	–	μs
			S-89240 Series	–	18	–	μs
Rise response time	t_{TLH}		S-89230 Series	–	2	–	μs
			S-89240 Series	–	10	–	μs
Fall response time	t_{THL}		S-89230 Series	–	2	–	μs
			S-89240 Series	–	10	–	μs

Downloaded from Arrow.com.

3. V_{DD} = 1.8 V

Table 10

DC Electrical Characteristics (V_{DD} = 1.8 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	S-89230 Series		–	23	40	μA	5
		S-89240 Series		–	5	9	μA	5
Input offset voltage drift	V_{IO}	–		−4	±3	+4	mV	1
Input offset voltage	$\frac{\Delta V_{IO}}{\Delta Ta}$	Ta = −40°C to +85°C		–	±10	–	μV/°C	1
Input offset current	I_{IO}	–		–	1	–	pA	–
Input bias current	I_{BIAS}	–		–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–		0	–	1.1	V	2
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ		1.7	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ		–	–	0.01	V	4
Common-mode input signal rejection ratio	CMRR	–		60	70	–	dB	2
Power supply voltage rejection ratio	PSRR	–		60	70	–	dB	1
Source current	I_{SOURCE}	V_{OUT} = 0 V	S-89230 Series	100	–	–	μA	6
			S-89240 Series	20	–	–	μA	6
Sink current	I_{SINK}	V_{OUT} = 0.5 V	S-89230 Series	5	–	–	mA	7
			S-89240 Series	3.5	–	–	mA	7

Table 11

AC Electrical Characteristics (V_{DD} = 1.8 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Rise propagation delay time	t_{PLH}	Overdrive = 100 mV C_L = 15 pF (Refer to **Figure 12**)	S-89230 Series	–	18	–	μs
			S-89240 Series	–	87	–	μs
Fall propagation delay time	t_{PHL}		S-89230 Series	–	3.5	–	μs
			S-89240 Series	–	15	–	μs
Rise response time	t_{TLH}		S-89230 Series	–	1.2	–	μs
			S-89240 Series	–	6	–	μs
Fall response time	t_{THL}		S-89230 Series	–	1.2	–	μs
			S-89240 Series	–	6	–	μs

Downloaded from Arrow.com.

■ Test Circuit (Per Circuit)

1. Power supply voltage rejection ratio, input offset voltage

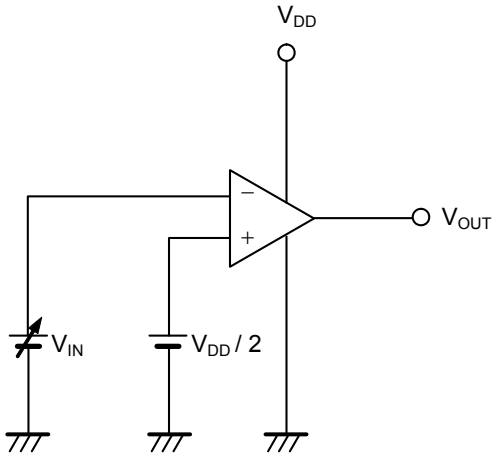


Figure 5

- **Power supply voltage rejection ratio (PSRR)**
  Input offset voltage (V_{IO})

  The input offset voltage (V_{IO}) is defined as V_{IN} − V_{DD} / 2 when V_{OUT} is changed by changing V_{IN} to V_{DD} / 2 level. The power supply voltage rejection ratio (PSRR) can be calculated by following expression, with the value of V_{IO} measured at each V_{DD}.

  Measurement conditions:
  When V_{DD} = 1.8 V: $V_{DD} = V_{DD1}$, $V_{IO} = V_{IO1}$
  When V_{DD} = 5.0 V: $V_{DD} = V_{DD2}$, $V_{IO} = V_{IO2}$

$$PSRR = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{V_{IO1} - V_{IO2}} \right| \right)$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

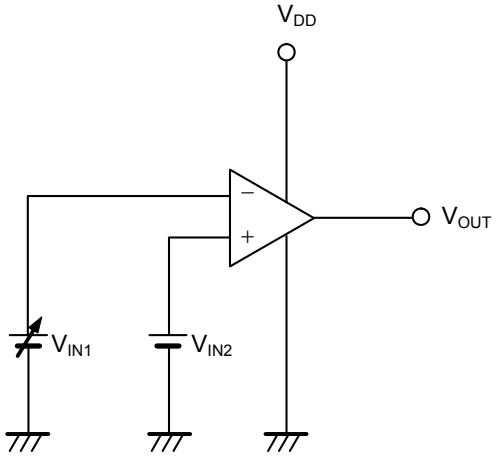


Figure 6

- **Common-mode input signal rejection ratio (CMRR)**
  The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with the offset voltage (V_{IO}) set as V_{IN1} − V_{IN2} after V_{OUT} is changed by changing V_{IN1}.

  Measurement conditions:
  When $V_{IN2} = V_{CMR\ Max.}$: $V_{IN2} = V_{INH}$, $V_{IO} = V_{IO1}$
  When $V_{IN2} = V_{DD}/2$: $V_{IN2} = V_{INL}$, $V_{IO} = V_{IO2}$

$$CMRR = 20 \log \left(\left| \frac{V_{INH} - V_{INL}}{V_{IO1} - V_{IO2}} \right| \right)$$

- **Common-mode input voltage range (V_{CMR})**
  Varying V_{IN2}, the range of V_{IN2} that satisfies the common-mode input signal rejection ratio (CMRR) is the common-mode input voltage range (V_{CMR}).

Downloaded from Arrow.com.

3. Maximum output swing voltage (V_{OH})

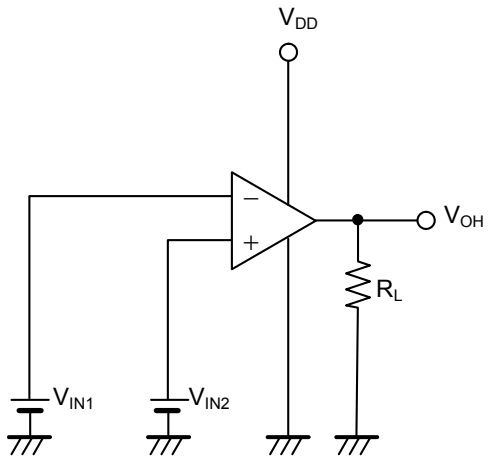


Figure 7

- **Maximum output swing voltage (V_{OH})**

Test conditions:

$V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

R_L = 1 MΩ

4. Maximum output swing voltage (V_{OL})

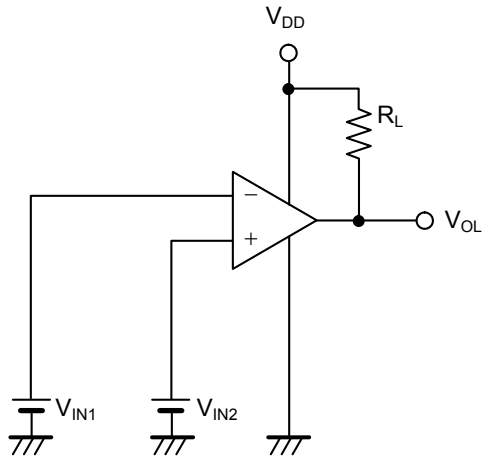


Figure 8

- **Maximum output swing voltage (V_{OL})**

Test conditions:

$V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

R_L = 1 MΩ

Downloaded from Arrow.com.

5. Current consumption

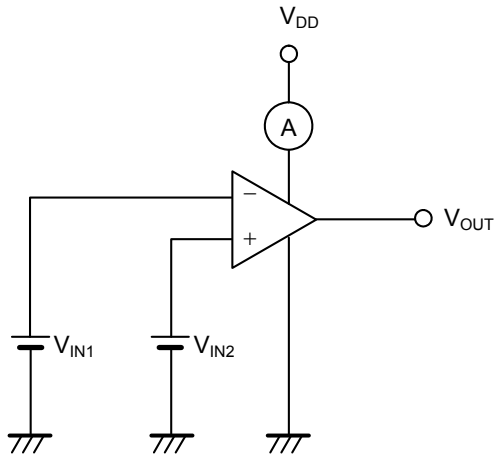


Figure 9

- **Current consumption (I_{DD})**

Test conditions:
$V_{IN} = V_{SS}$
$V_{IN} = V_{CMR\ Max.}$

6. Source current

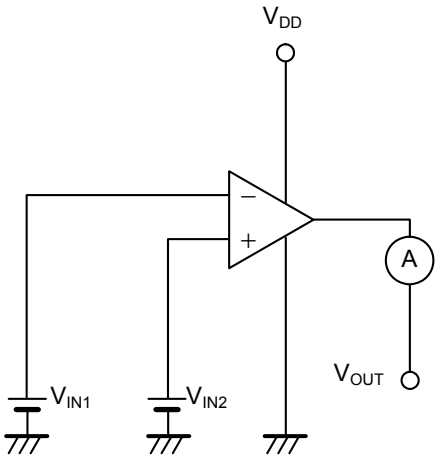


Figure 10

- **Source current (I_{SOURCE})**

Test conditions:
V_{OUT} = 0 V
$V_{IN1} = \frac{V_{DD}}{2} - 0.5\ V$
$V_{IN2} = \frac{V_{DD}}{2} + 0.5\ V$

7. Sink current

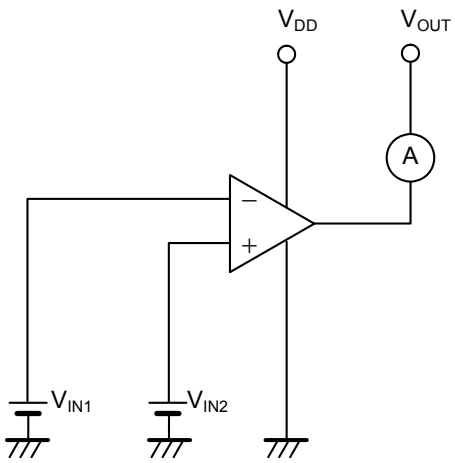


Figure 11

- **Sink current (I_{SINK})**

Test conditions:
V_{OUT} = 0.5 V
$V_{IN1} = \frac{V_{DD}}{2} + 0.5\ V$
$V_{IN2} = \frac{V_{DD}}{2} - 0.5\ V$

Downloaded from Arrow.com.

8. Propagation time, response time

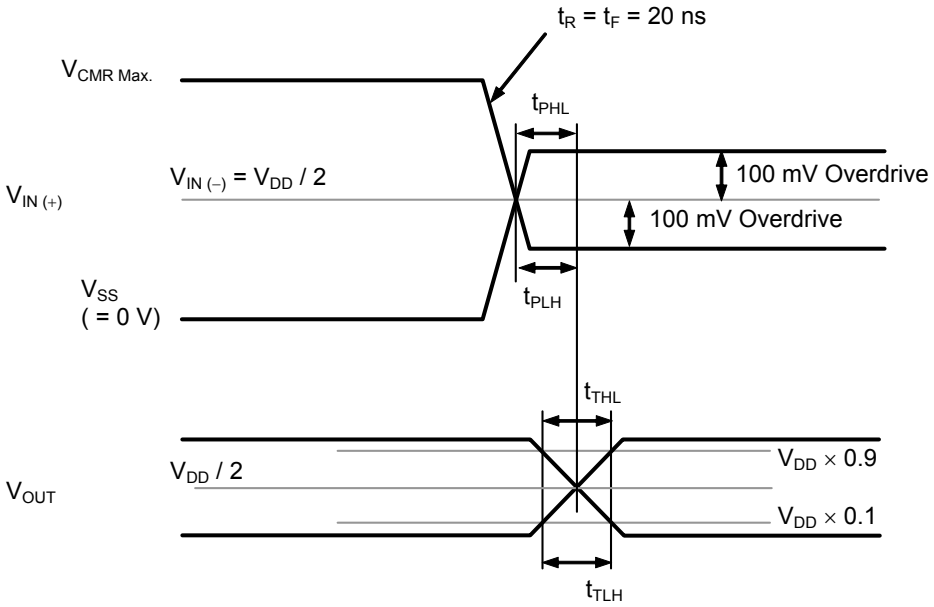


Figure 12

Downloaded from Arrow.com.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.

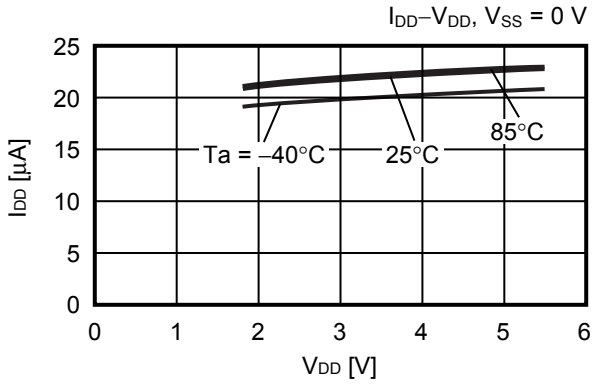
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

Downloaded from Arrow.com.

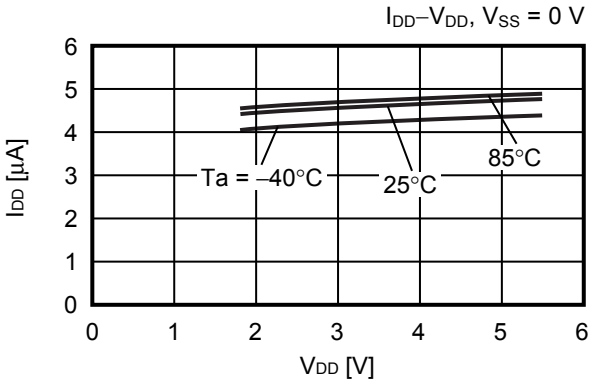
■ Characteristics (Typical Data)

1. Current consumption (per circuit, I_{DD}) vs. Power supply voltage (V_{DD})

(1) S-89230 Series



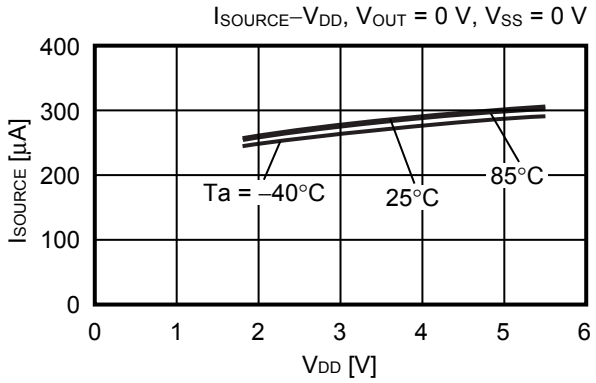
(2) S-89240 Series



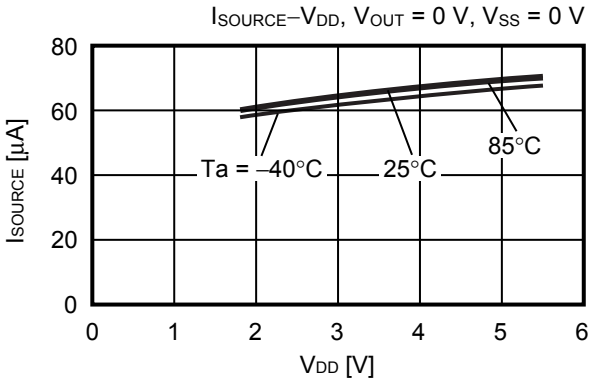
2. Output current characteristics

2. 1 Source current (I_{SOURCE}) vs. Power supply voltage (V_{DD})

(1) S-89230 Series

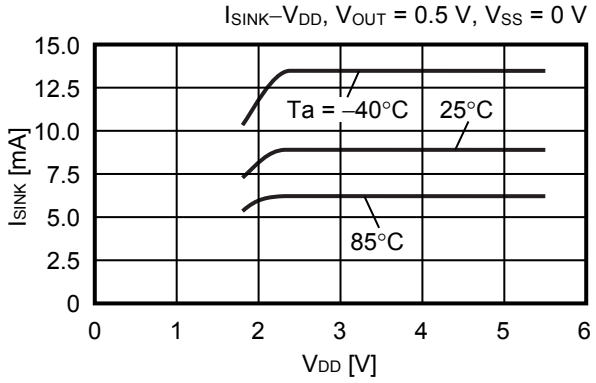


(2) S-89240 Series

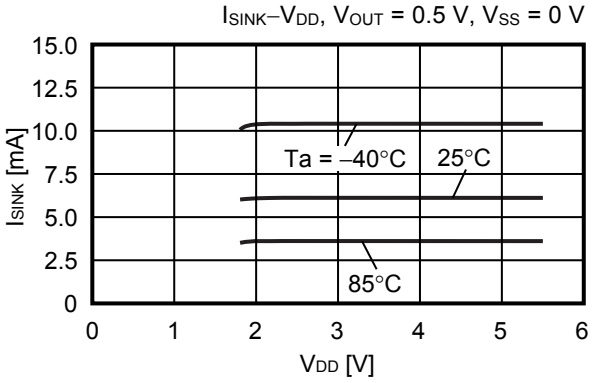


2. 2 Sink current (I_{SINK}) vs. Power supply voltage (V_{DD})

(1) S-89230 Series



(2) S-89240 Series

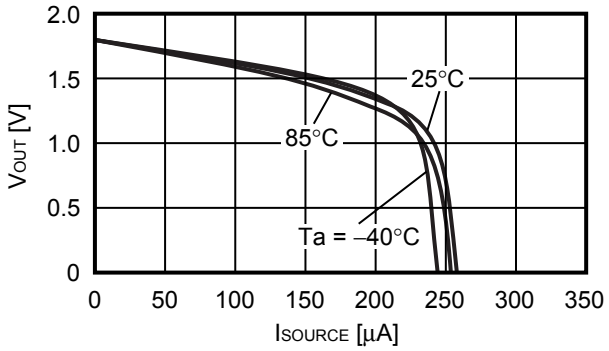


Downloaded from Arrow.com.

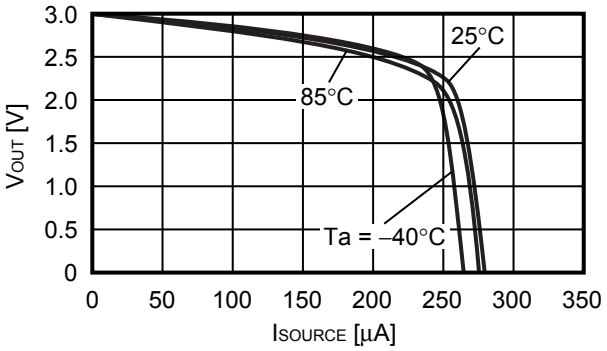
2. 3 Output voltage (V_{OUT}) vs. Source current (I_{SOURCE})

(1) S-89230 Series

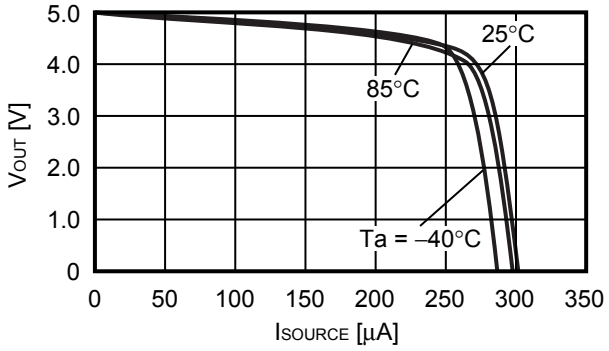
V_{OUT}–I_{SOURCE}, V_{DD} = 1.8 V, V_{SS} = 0 V



V_{OUT}–I_{SOURCE}, V_{DD} = 3.0 V, V_{SS} = 0 V

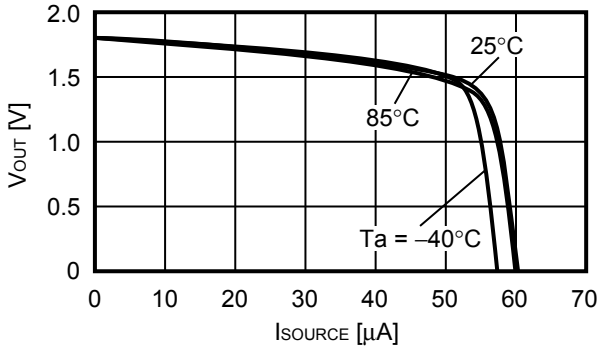


V_{OUT}–I_{SOURCE}, V_{DD} = 5.0 V, V_{SS} = 0 V

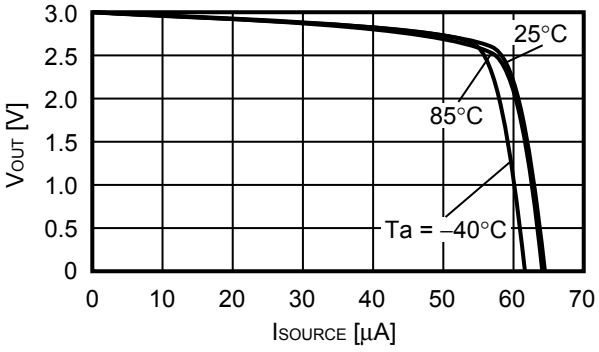


(2) S-89240 Series

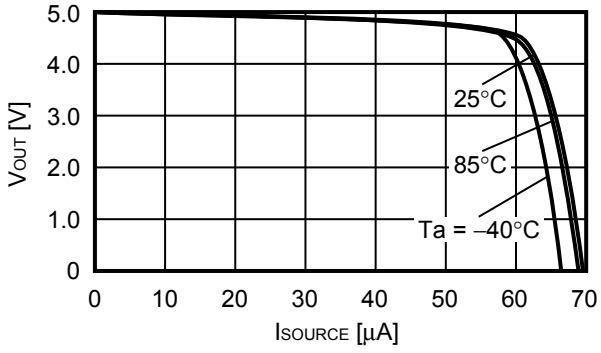
V_{OUT}–I_{SOURCE}, V_{DD} = 1.8 V, V_{SS} = 0 V



V_{OUT}–I_{SOURCE}, V_{DD} = 3.0 V, V_{SS} = 0 V



V_{OUT}–I_{SOURCE}, V_{DD} = 5.0 V, V_{SS} = 0 V

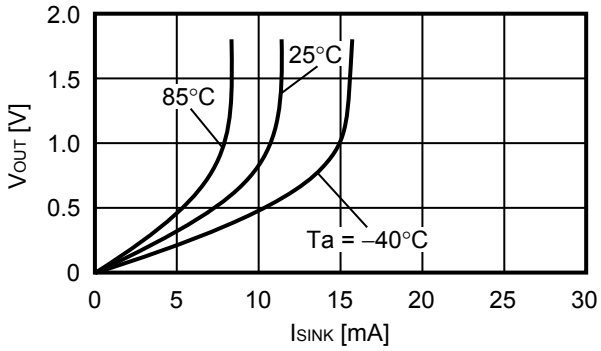


Downloaded from Arrow.com.

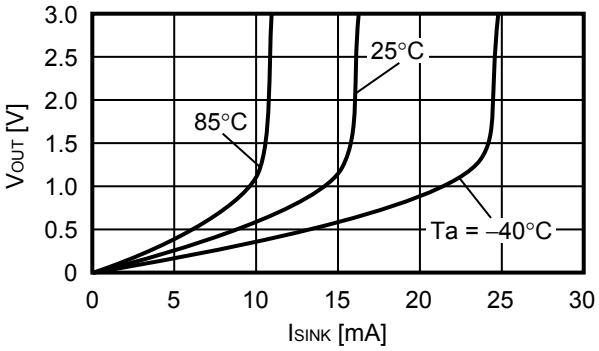
2. 4 Output voltage (V_{OUT}) vs. Sink current (I_{SINK})

(1) S-89230 Series

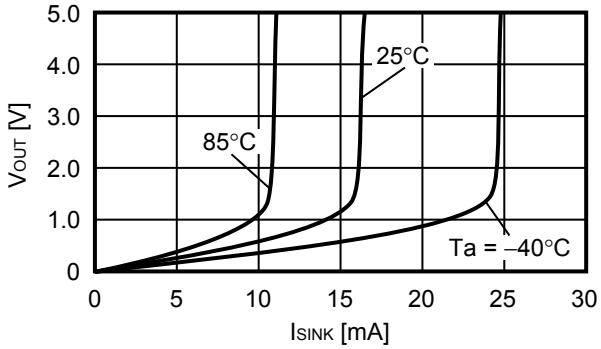
V_{OUT}–I_{SINK}, V_{DD} = 1.8 V, V_{SS} = 0 V



V_{OUT}–I_{SINK}, V_{DD} = 3.0 V, V_{SS} = 0 V

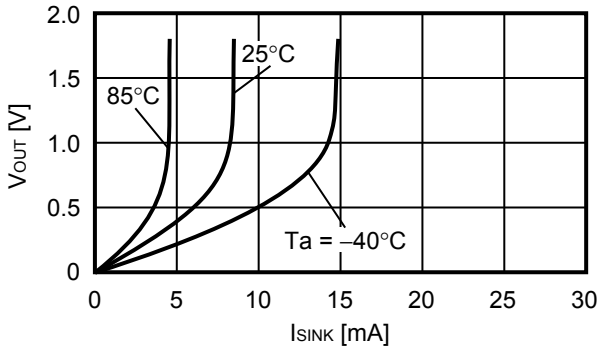


V_{OUT}–I_{SINK}, V_{DD} = 5.0 V, V_{SS} = 0 V

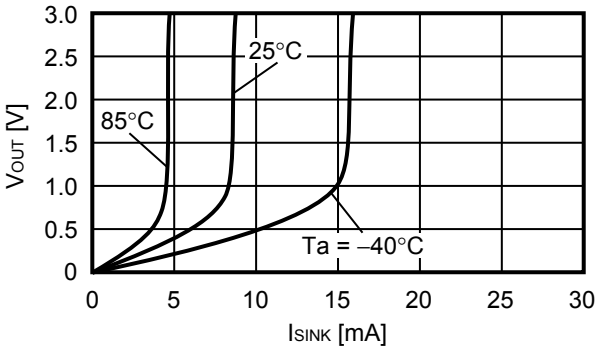


(2) S-89240 Series

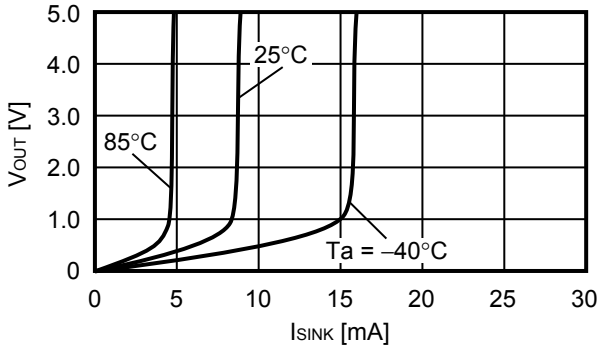
V_{OUT}–I_{SINK}, V_{DD} = 1.8 V, V_{SS} = 0 V



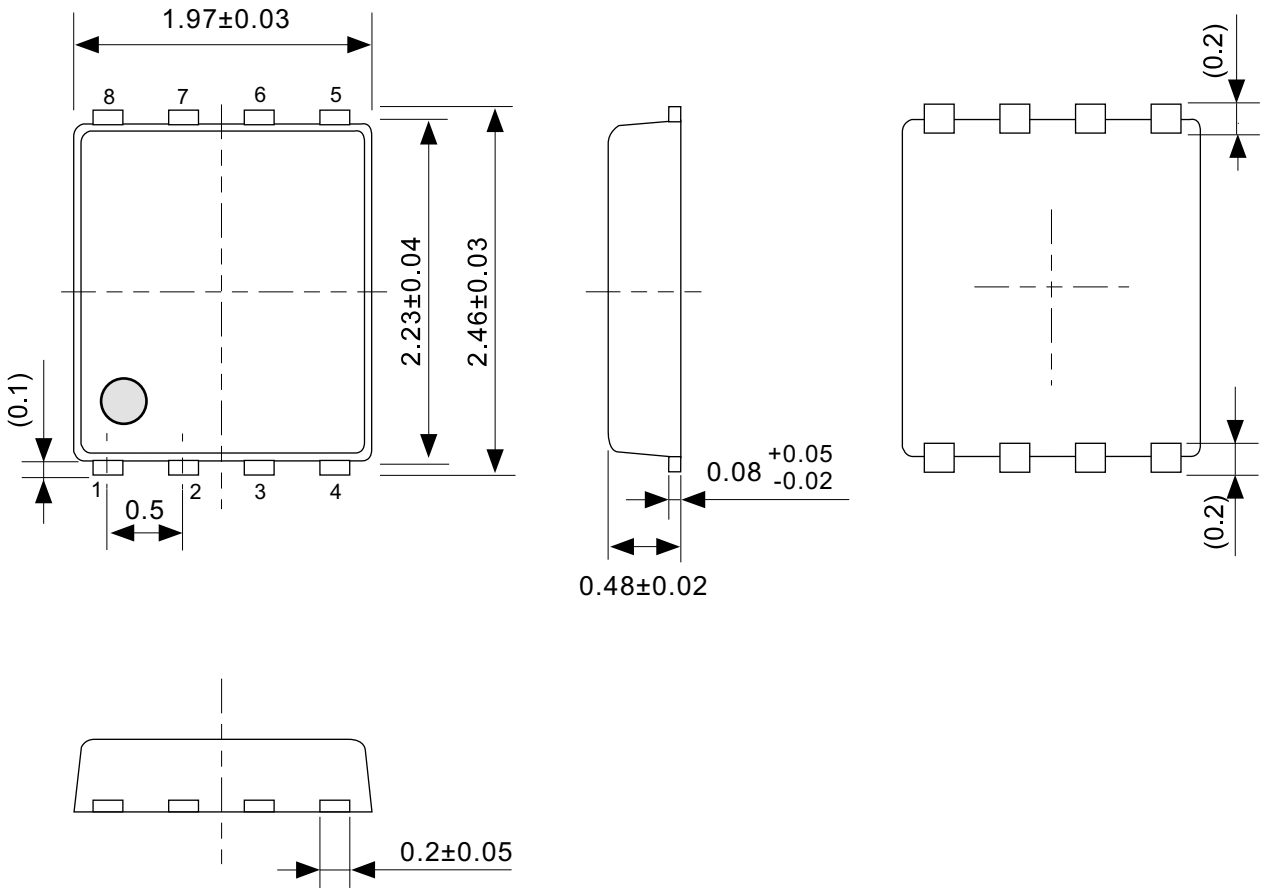
V_{OUT}–I_{SINK}, V_{DD} = 3.0 V, V_{SS} = 0 V



V_{OUT}–I_{SINK}, V_{DD} = 5.0 V, V_{SS} = 0 V



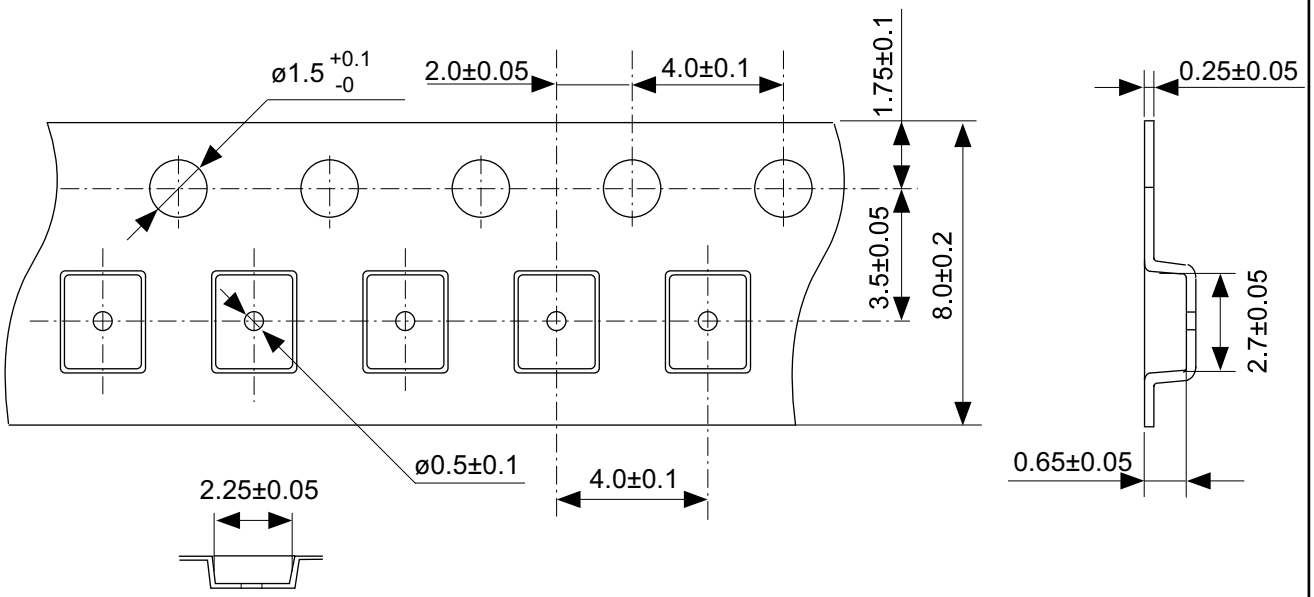
Downloaded from Arrow.com.

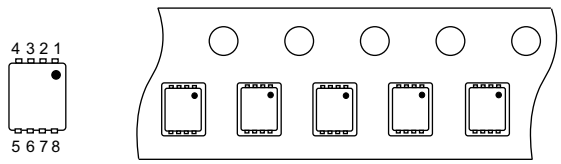


No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.



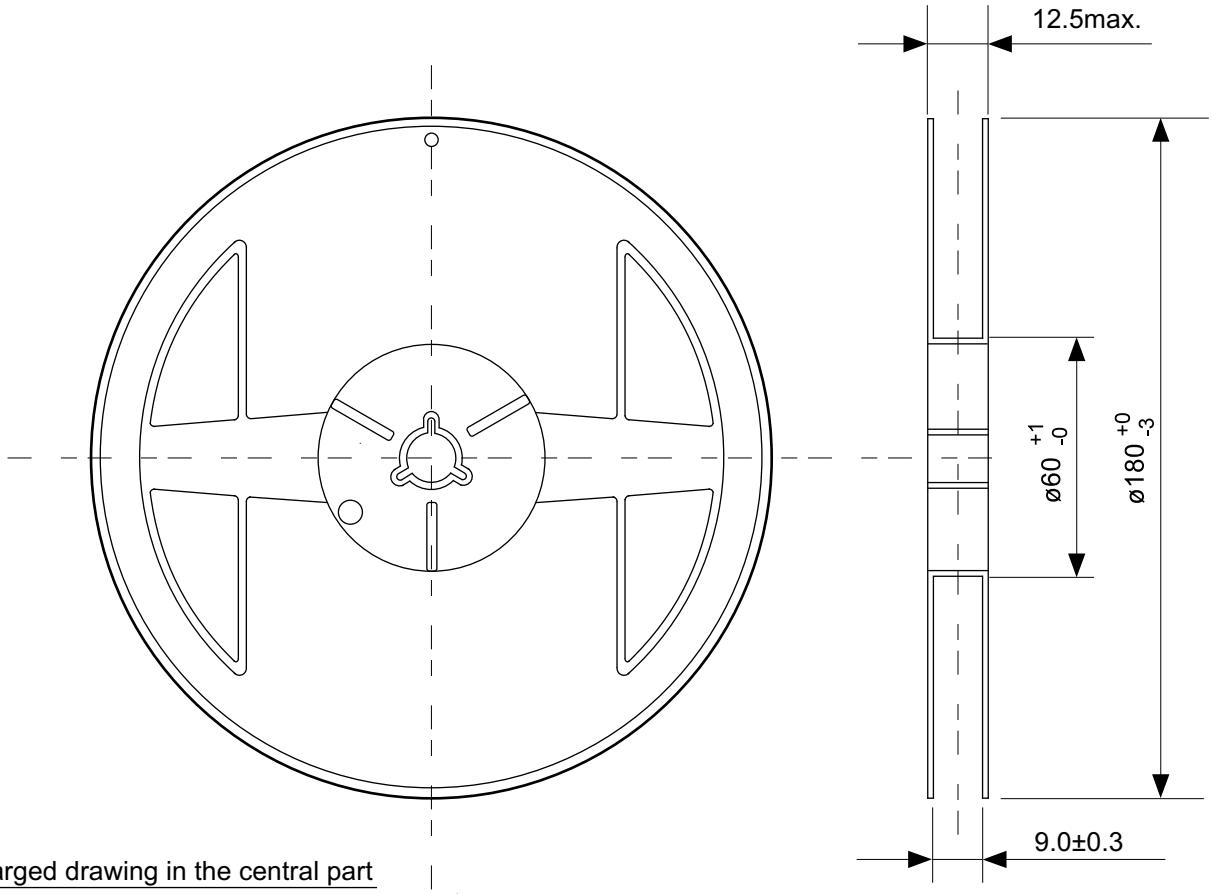


Feed direction

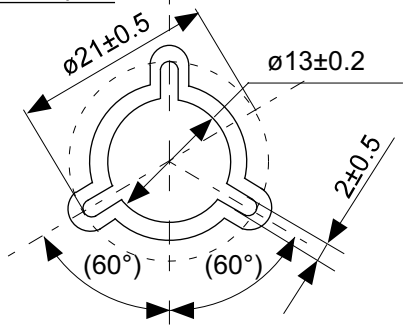
No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.



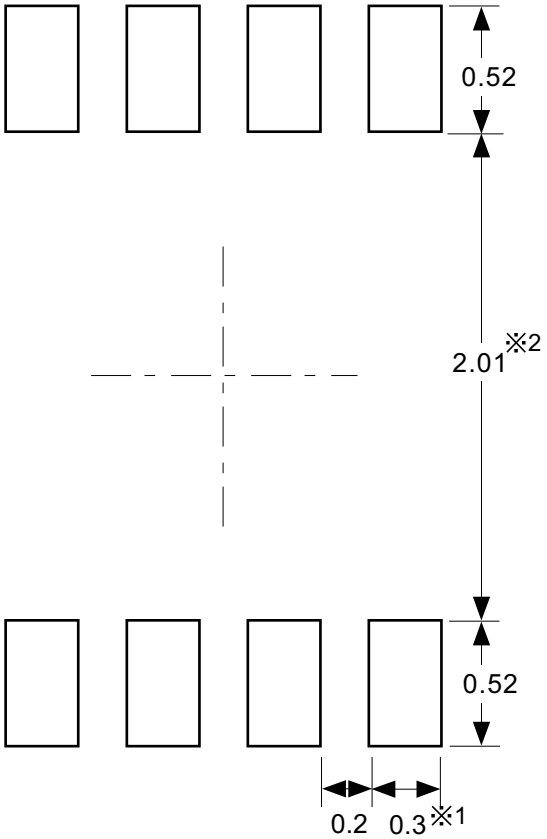
Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

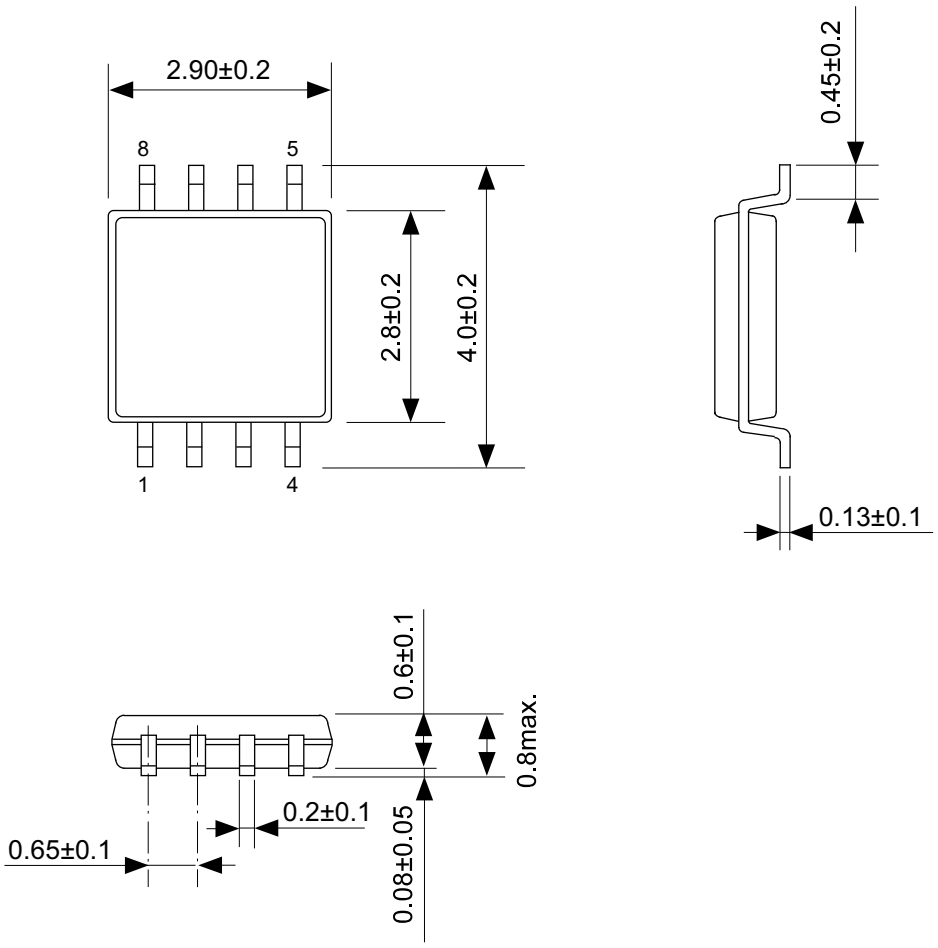
※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

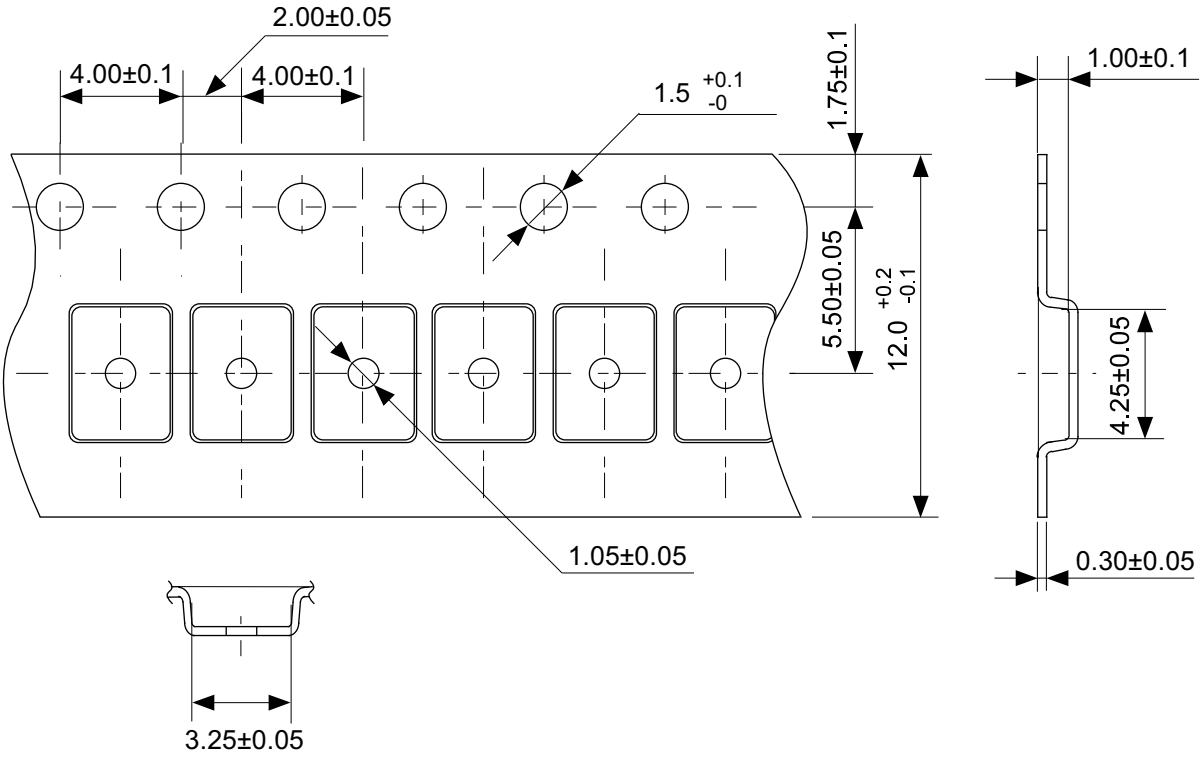
Downloaded from Arrow.com.

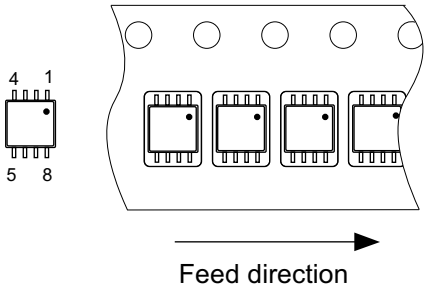


No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.

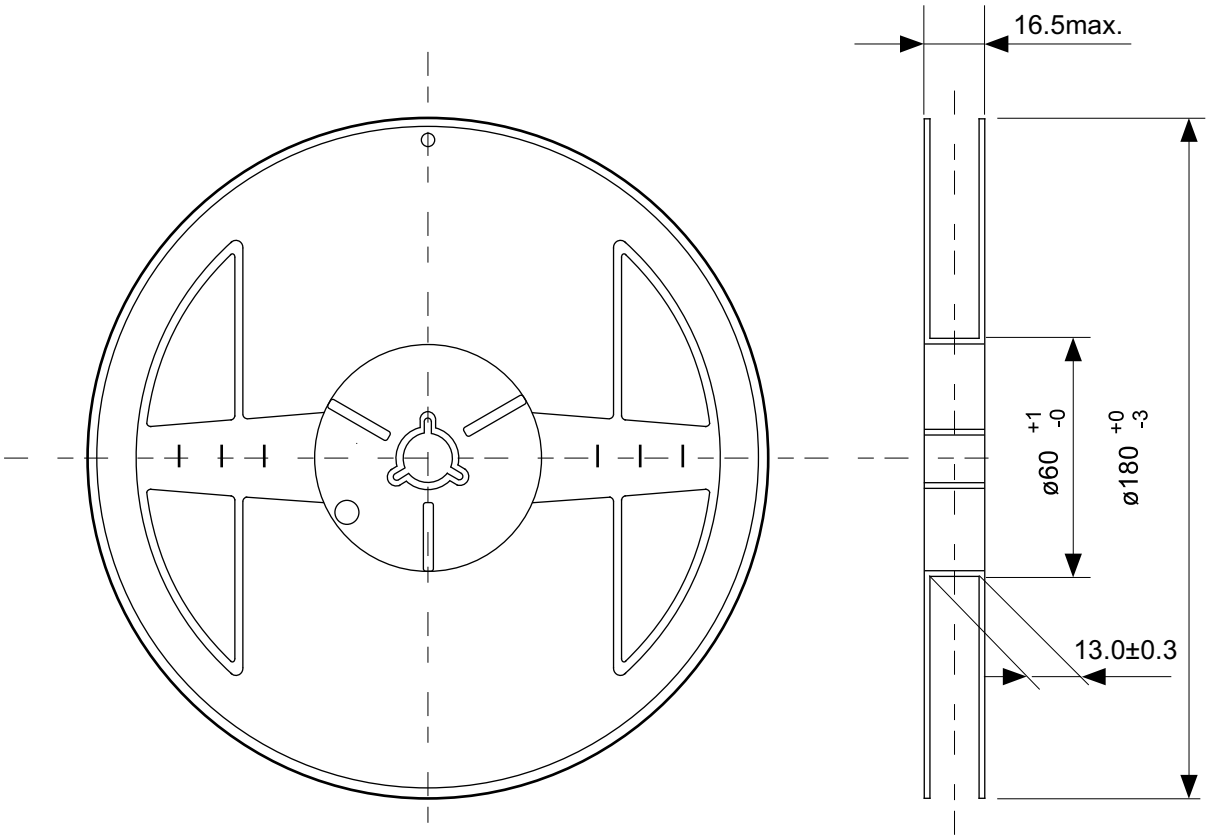




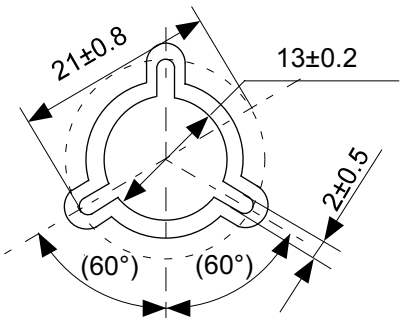
No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

Downloaded from Arrow.com.