RL78/F13, F14

RENESAS MCU

R01DS0460EJ0230
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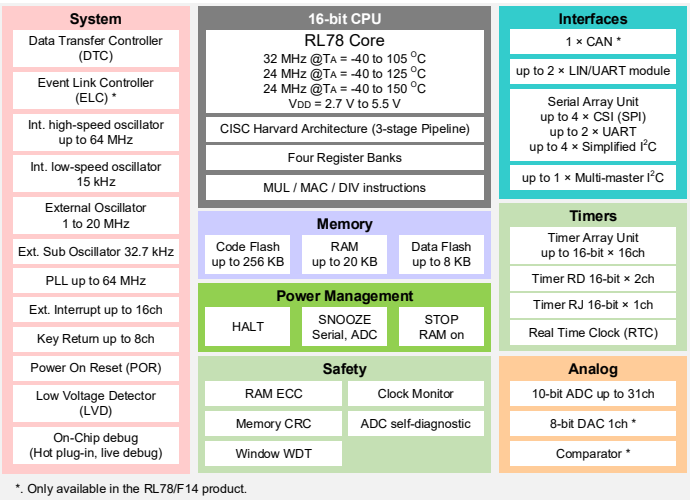
RL78/F13, F14 microcontrollers are successors to the 78K0R and R8C, are available in a 20- to 100-pin, 16 KB to 256 KB flash memory lineup and realize the industry's lowest level of consumption current. They have a built-in CAN module and LIN module for automotive interfaces and also support BLDC motor control using timer RD, comparator and D/A converter. And in addition to the functional safety features of RL78/F12 product, a RAM ECC function, PLL lock function, port output state monitoring, stack overflow detection, dedicated WDT oscillator and more have also been added. Since a more highly reliable system can be built, these microcontrollers can be used for industrial applications and of course automotive applications.

1. OVERVIEW

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.03125 µs: @ 32 MHz operation with high-speed on-chip oscillator clock or PLL clock) to ultra low-speed (66.6 µs: @ 15 kHz operation with low-speed on-chip oscillator clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM: 16 to 256 KB
- RAM: 1 to 20 KB
- Data flash memory: 4 KB/8 KB
- High-speed on-chip oscillator clock
  Selectable from 32 MHz (Typ.), 24 MHz (Typ.), 16 MHz (Typ.), 12 MHz (Typ.), 8 MHz (Typ.), 4 MHz (Typ.), and 1 MHz (Typ.)
  (Selectable from 64 MHz (Typ.) and 48 MHz (Typ.) when using Timer RD)
- Low-speed on-chip oscillator clock: 15 kHz × 2 channels (one for WWDT and one for CPU and peripherals other than WWDT)
- On-chip PLL (×3, ×4, ×6, ×8)
- On-chip single-power-supply flash memory (with prohibition of block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated low-speed on-chip oscillator clock)
- Multiply/divide/multiply & accumulate instructions are supported
  16 bits × 16 bits = 32 bits (Unsigned or signed)
  32 bits ÷ 32 bits = 32 bits (Unsigned)
  16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 16 to 92 (including one input-only pin)
- Timer
  - 16-bit timer array unit: 8 to 16 channels
  - 16-bit timer RD:2 channels (six triangle-wave outputs; sawtooth wave/triangle-wave modulation)
  - 16-bit timer RJ: 1 channel
  - Watchdog timer: 1 channel
  - Real-time clock: 1 channel
- Serial interface
  - CSI
  - UART/UART (LIN-bus supported)
  - LIN module (master/slave supported)
  - I^2C/simplified I^2C
  - CAN interface (RS-CAN lite)
- 8/10-bit resolution A/D converter (V_{DD} = 2.7 to 5.5 V): 4 to 31 channels
- DTC (Max. 44 sources)
- ELC (Max. 26 channels for event link source, Max. 9 channels for event link destination) **Note**
- Safety functions (CRC calculation, Clock monitor, AD test, SFR guard, etc.)
- 8-bit D/A converter **Note**
- On-chip comparator: 1 channel (input pin: 4 channels) **Note**
- Power supply voltage: V_{DD} = 2.7 to 5.5 V
- Operating ambient temperature:
  T_A = -40 to +105°C (grade L)
  T_A = -40 to +125°C (grade K)
  T_A = -40 to +150°C (grade Y)

Note Only available in the RL78/F14.



RL78/F13, F14 Block Diagram (Outline)

Applications

General automotive electrical applications (motor control, door control, headlight control, etc.), motorcycle engine control

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1.2 Product Lineup

Table 1-1. RL78/F14 Lineup

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Code Flash	Data Flash	RAM	Pin Count						
			100 pins (LFQFP)	80 pins (LFQFP)	64 pins (LFQFP)	48 pins (HVQFN)	48 pins (LFQFP)	32 pins (HVQFN/HWQFN)	30 pins (LSSOP)
48 KB	4 KB	4 KB	—	—	—	R5F10PGD	R5F10PGDC	R5F10PBD R5F10PBDC	R5F10PAD R5F10PADC
64 KB		6 KB	R5F10PPEC	R5F10PMEC	R5F10PLEC	R5F10PGE	R5F10PGEC	R5F10PBE R5F10PBEC	R5F10PAE R5F10PAEC
96 KB		8 KB	R5F10PPFC	R5F10PMFC	R5F10PLFC	R5F10PGF	R5F10PGFC	—	—
128 KB	8 KB	10 KB	R5F10PPGC	R5F10PMGC	R5F10PLGC	R5F10PGG	R5F10PGGC	—	—
192 KB		16 KB	R5F10PPHC	R5F10PMHC	R5F10PLHC	R5F10PGH	R5F10PGHC	—	—
256 KB		20 KB	R5F10PPJC	R5F10PMJC	R5F10PLJC	R5F10PGJ	R5F10PGJC	—	—

Table 1-2. RL78/F13 (CAN and LIN incorporated) Lineup

<R>

Code Flash	Data Flash	RAM	Pin Count					
			80 pins (LFQFP)	64 pins (LFQFP)	48 pins (HVQFN)	48 pins (LFQFP)	32 pins (HVQFN/HWQFN)	30 pins (LSSOP)
32 KB	4 KB	2 KB	—	R5F10BLCC	R5F10BGC	R5F10BGCC	R5F10BBC R5D10BBCC	R5F10BAC R5D10BACC
48 KB		3 KB	—	R5F10BLDC	R5F10BGD	R5F10BGDC	R5F10BBD R5F10BBDC	R5F10BAD R5F10BADC
64 KB		4 KB	R5F10BMEC	R5F10BLEC	R5F10BGE	R5F10BGEC	R5F10BBE R5F10BBEC	R5F10BAE R5F10BAEC
96 KB		6 KB	R5F10BMFC	R5F10BLFC	R5F10BGF	R5F10BGFC	R5F10BBF R5F10BBFC	R5F10BAF R5F10BAFC
128 KB		8 KB	R5F10BMGC	R5F10BLGC	R5F10BGG	R5F10BGGC	R5F10BBG R5F10BBGC	R5F10BAG R5F10BAGC

Table 1-3. RL78/F13 (LIN incorporated) Lineup

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Code Flash	Data Flash	RAM	Pin Count						
			80 pins (LFQFP)	64 pins (LFQFP)	48 pins (HVQFN)	48 pins (LFQFP)	32 pins (HVQFN/HWQFN)	30 pins (LSSOP)	20 pins (LSSOP)
16 KB	4 KB	1 KB	—	—	R5F10AGA	R5F10AGAC	R5F10ABA R5F10ABAC	R5F10AAA R5F10AAAC	R5F10A6A R5F10A6AC
32 KB		2 KB	—	R5F10ALCC	R5F10AGC	R5F10AGCC	R5F10ABC R5F10ABCC	R5F10AAC R5F10AACC	R5F10A6C R5F10A6CC
48 KB		3 KB	—	R5F10ALDC	R5F10AGD	R5F10AGDC	R5F10ABD R5F10ABDC	R5F10AAD R5F10AADC	R5F10A6D R5F10A6DC
64 KB		4 KB	R5F10AMEC	R5F10ALEC	R5F10AGE	R5F10AGEC	R5F10ABE R5F10ABEC	R5F10AAE R5F10AAEC	R5F10A6E R5F10A6EC
96 KB		6 KB	R5F10AMFC	R5F10ALFC	R5F10AGF	R5F10AGFC	—	—	—
128 KB		8 KB	R5F10AMGC	R5F10ALGC	R5F10AGG	R5F10AGGC	—	—	—

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1.3 Function Overview

1.3.1 RL78/F14 Functions List

Table 1-4. RL78/F14 Functions List (1/2)

Series Name			R5F10PP	R5F10PM	R5F10PL	R5F10PG	R5F10PB	R5F10PA
		Pin Count	100 pins	80 pins	64 pins	48 pins	32 pins	30 pins
Code flash			64 to 256KB			48 to 256KB	48KB, 64KB	
Data flash			8KB/4KB				4KB	
RAM			6 to 20KB			4 to 20KB	48KB, 64KB	
Supply voltage range			2.7 V to 5.5 V					
Maximum operation frequency			32 MHz (grade L), 24 MHz (grade K, grade Y)					
System clock	Main system clock oscillator	Crystal/ceramic/ square wave	1 to 20 MHz (operating at 2.7 V to 5.5 V)					
	High-speed on-chip oscillator	Normal high accuracy	32 MHz (typ.)					
	Low-speed on-chip oscillator	For low-speed operation	15 kHz (typ.)					
	Subsystem clock oscillator		32.768 kHz[Note 7]				None	
	PLL		PLL multiplication factor: ×3/×4/×6/×8					
Clock for peripherals	Low-speed on-chip oscillator	For peripherals other than WDT	15 kHz (typ.)					
		For WDT	15 kHz (typ.)					
POR		When power supply is rising	1.56 V (typ.)					
		When power supply is falling	1.55 V (typ.)					
LVD	V_{DD} voltage detection	When power supply is rising	2.81 V (typ.) to 4.74 V (typ.) (in 6 steps)					
		When power supply is falling	2.75 V (typ.) to 4.64 V (typ.) (in 6 steps)					
Safety functions	WWDT (window watchdog timer)		Yes					
	Illegal instruction execution detection function		Yes					
	Flash memory CRC operation function		Yes					
	RAM1 bit error correction function		Yes					
	RAM2 bit error detection function		Yes					
	Invalid memory access detection function		Yes					
	Frequency detection function		Yes					
	Clock monitor function		Yes					
	Stack pointer monitor function		Yes					
	I/O port output signal level detection function		Yes					
	A/D test function		Yes					
I/O ports	Input/Output	CMOS	86ch	68ch	52ch	38ch	25ch	23ch
	Output	CMOS	1ch				None	
	Input	Shared with oscillator pins	4ch[Note 7]				2ch	
		Input only	1ch					
Power supply pins	For internal circuits		V_{DD}, V_{SS}, REGC					
	For I/O ports		EV_{DD0}, EV_{SS0} EV_{DD1}, EV_{SS1}	EV_{DD0}, EV_{SS0}		None		
	For analog circuits (AD, DA, COMP)		V_{DD}, V_{SS} (AV_{REFP}, AV_{REFM}: For AD)					
Multiply/divide and multiply-accumulate functions	Multiply		16 bits × 16 bits (signed)					
			16 bits × 16 bits (unsigned)					
	Divide		32 bits ÷ 32 bits (unsigned)					
	Multiply-accumulate		16 bits × 16 bits + 32 bits (signed)					
			16 bits × 16 bits + 32 bits (unsigned)					
	Arithmetic instructions (extended instruction set)		Yes					
Vectored interrupt sources	External	Products with at least 128 Kbytes of code flash memory	16ch [Notes 4, 6]	16ch [Notes 4, 6]	15ch [Notes 3, 6]	14ch [Note 2]	9ch [Note 1]	
		Products with up to 96 Kbytes of code flash memory		14ch [Notes 3, 5]	14ch [Notes 3, 5]	13ch [Note 2]		
	Internal	Products with at least 128 Kbytes of code flash memory	48ch [Note 4]	48ch [Note 4]	48ch [Note 3]	48ch [Note 2]	41ch [Note 1]	40ch [Note 1]
		Products with up to 96 Kbytes of code flash memory		41ch [Note 3]	41ch [Note 3]	41ch [Note 2]		
Key return detection			8ch				6ch	8ch
DTC			44 sources	44 sources/38 sources			37 sources	
Timer	TAU		16 bits (8ch × 2)	16 bits (8ch × 2/8ch + 4ch)			16 bits (8ch + 4ch)	
	RTC		1ch					
	Timer RJ		16 bits × 1					
	Timer RD		16 bits × 2					
Serial I/F	CSI/simplified I^2C /UART		4ch/4ch/2ch				3ch/3ch/2ch	
		SPI	Yes					
	Multimaster I^2C		1ch					None
	LIN/UART module (RLIN3)		2ch	2ch/1ch			1ch	
	CAN interface (RS-CAN lite)		1ch					

(**Notes** and **Caution** are listed on the next page.)

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Table 1-4. RL78/F14 Functions List (2/2)

Series Name		R5F10PP	R5F10PM	R5F10PL	R5F10PG	R5F10PB	R5F10PA
	Pin Count	100 pins	80 pins	64 pins	48 pins	32 pins	30 pins
A/D converter 10-bit SAR	V_{DD}	24ch	18ch/16ch	17ch/16ch	13ch	8ch	10ch
	EV_{DD}	7ch	7ch/4ch	3ch	5ch/2ch	2ch	
	Internal	2ch					
D/A converter	8-bit	1ch					
Comparator		1ch					
ELC		Link source: 26ch Link destination: 9ch	Link source: 26ch/20ch Link destination: 9ch/7ch			Link source: 20ch Link destination: 7ch	
PCLBUZ		1ch				None	
Self-programming		Yes					
On-chip debug	Trace	Yes					
	Hot plug-in	Yes					
Option byte		Yes					

Notes 1. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP5 and INTCMP0.

2. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP5 and INTCMP0, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H.

3. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP5 and INTCMP0, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H, INTP10 and INTTM03H.

4. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP5 and INTCMP0, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H, INTP10 and INTTM03H, INTP13 and INTCLM.

5. INTP11 and INTLIN0WUP are counted as a single source because using them at the same time is not possible.

6. Both sources in the following pairs are counted as a single source in this number: INTP11 and INTLIN0WUP, INTP12 and INTLIN1WUP.

7. Do not use the XT1 and XT2 pin functions in grade-Y products.

Caution For details, see 1.5 Pin Configurations.

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1.3.2 RL78/F13 (CAN and LIN incorporated) Functions List

Table 1-5. RL78/F13 (CAN and LIN incorporated) Functions List

Series Name			R5F10BM	R5F10BL	R5F10BG	R5F10BB	R5F10BA
		Pin Count	80 pins	64 pins	48 pins	32 pins	30 pins
Code flash			64 to 128KB	32 to 128KB			
Data flash			4KB				
RAM			4 to 8KB	2 to 8KB			
Supply voltage range			2.7 V to 5.5 V				
Maximum operation frequency			32 MHz (grade L), 24 MHz (grade K, grade Y)				
System clock	Main system clock oscillator	Crystal/ceramic/ square wave	1 to 20 MHz (operating at 2.7 V to 5.5 V)				
	High-speed on-chip oscillator	Normal high accuracy	32 MHz (typ.)				
	Low-speed on-chip oscillator	For low-speed operation	15 kHz (typ.)				
	Subsystem clock oscillator		32.768 kHz Note 5			None	
	PLL		PLL multiplication factor: ×3/×4/×6/×8				
Clock for peripherals	Low-speed on-chip oscillator	For peripherals other than WDT	15 kHz (typ.)				
		For WDT	15 kHz (typ.)				
POR		When power supply is rising	1.56 V (typ.)				
		When power supply is falling	1.55 V (typ.)				
LVD	V_{DD} voltage detection	When power supply is rising	2.81 V (typ.) to 4.74 V (typ.) (in 6 steps)				
		When power supply is falling	2.75 V (typ.) to 4.64 V (typ.) (in 6 steps)				
Safety functions	WWDT (window watchdog timer)		Yes				
	Illegal instruction execution detection function		Yes				
	Flash memory CRC operation function		Yes				
	RAM1 bit error correction function		Yes				
	RAM2 bit error detection function		Yes				
	Invalid memory access detection function		Yes				
	Frequency detection function		Yes				
	Clock monitor function		Yes				
	Stack pointer monitor function		Yes				
	I/O port output signal level detection function		Yes				
	A/D test function		Yes				
I/O ports	Input/Output	CMOS	68ch	52ch	38ch	25ch	23ch
	Output	CMOS	1ch			None	
	Input	Shared with oscillator pins	4ch Note 5			2ch	
		Input only	1ch				
Power supply pins	For internal circuits		V_{DD}, V_{SS}, REGC				
	For I/O ports		EV_{DD0}, EV_{SS0}		None		
	For analog circuits (AD, DA, COMP)		V_{DD}, V_{SS} (AV_{REFP}, AV_{REFM}: For AD)				
Multiply/divide and multiply-accumulate functions	Multiply		16 bits × 16 bits (signed)				
			16 bits × 16 bits (unsigned)				
	Divide		32 bits ÷ 32 bits (unsigned)				
	Multiply-accumulate		16 bits × 16 bits + 32 bits (signed)				
			16 bits × 16 bits + 32 bits (unsigned)				
	Arithmetic instructions (extended instruction set)		Yes				
Vectored interrupt sources	External		14ch Notes 3, 4		13ch Note 2	9ch Note 1	
	Internal		40ch Note 3		40ch Note 2	40ch Note 1	39ch Note 1
Key return detection			8ch			6ch	8ch
DTC			37 sources			36 sources	
Timer	TAU		16 bits (8ch + 4ch)				
	RTC		1ch				
	Timer RJ		16 bits × 1				
	Timer RD		16 bits × 2				
Serial I/F	CSI/simplified I^2C /UART		4ch/4ch/2ch			3ch/3ch/2ch	
		SPI	Yes				
	Multimaster I^2C		1ch				None
	LIN/UART module (RLIN3)		1ch				
	CAN interface (RS-CAN lite)		1ch				
A/D converter 10-bit SAR	V_{DD}		16ch	16ch	13ch	8ch	10ch
	EV_{DD}		4ch	3ch	2ch		
	Internal		2ch				
D/A converter	8-bit		None				
Comparator			None				
ELC			None				
PCLBUZ			1ch			None	
Self-programming			Yes				
On-chip debug	Trace		Yes				
	Hot plug-in		Yes				
Option byte			Yes				

(**Notes** and **Caution** are listed on the next page.)

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Notes 1. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM.

2. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H.

3. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H, INTP10 and INTTM03H.

4. INTP11 and INTLIN0WUP are counted as a single source because using them at the same time is not possible.

5. Do not use the XT1 and XT2 pin functions in grade-Y products.

Caution For details, see 1.5 Pin Configurations.

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1.3.3 RL78/F13 (LIN incorporated) Functions List

Table 1-6. RL78/F13 (LIN incorporated) Functions List (1/2)

Series Name			R5F10AM	R5F10AL	R5F10AG	R5F10AB	R5F10AA	R5F10A6
		Pin Count	80 pins	64 pins	48 pins	32 pins	30 pins	20 pins
Code flash			64 to 128KB	32 to 128KB	16 to 128KB	16 to 64KB		
Data flash			4KB					
RAM			4 to 8KB	2 to 8KB	1 to 8KB	1 to 4KB		
Supply voltage range			2.7 V to 5.5 V					
Maximum operation frequency			32 MHz (grade L), 24 MHz (grade K, grade Y)					
System clock	Main system clock oscillator	Crystal/ceramic/ square wave	1 to 20 MHz (operating at 2.7 V to 5.5 V)					
	High-speed on-chip oscillator	Normal high accuracy	32 MHz (typ.)					
	Low-speed on-chip oscillator	For low-speed operation	15 kHz (typ.)					
	Subsystem clock oscillator		32.768 kHz Note 6			None		
	PLL		PLL multiplication factor: ×3/×4/×6/×8					
Clock for peripherals	Low-speed on-chip oscillator	For peripherals other than WDT	15 kHz (typ.)					
		For WDT	15 kHz (typ.)					
POR		When power supply is rising	1.56 V (typ.)					
		When power supply is falling	1.55 V (typ.)					
LVD	V_{DD} voltage detection	When power supply is rising	2.81 V (typ.) to 4.74 V (typ.) (in 6 steps)					
		When power supply is falling	2.75 V (typ.) to 4.64 V (typ.) (in 6 steps)					
Safety functions	WWDT (window watchdog timer)		Yes					
	Illegal instruction execution detection function		Yes					
	Flash memory CRC operation function		Yes					
	RAM1 bit error correction function		Yes					
	RAM2 bit error detection function		Yes					
	Invalid memory access detection function		Yes					
	Frequency detection function		Yes					
	Clock monitor function		Yes					
	Stack pointer monitor function		Yes					
	I/O port output signal level detection function		Yes					
	A/D test function		Yes					
I/O ports	Input/Output	CMOS	68ch	52ch	38ch	25ch	23ch	13ch
	Output	CMOS	1ch			None		
	Input	Shared with oscillator pins	4ch Note 6			2ch		
		Input only	1ch					
Power supply pins	For internal circuits		V_{DD}, V_{SS}, REGC					
	For I/O ports		EV_{DD0}, EV_{SS0}		None			
	For analog circuits (AD, DA, COMP)		V_{DD}, V_{SS} (AV_{REFP}, AV_{REFM}: For AD)					
Multiply/divide and multiply-accumulate functions	Multiply		16 bits × 16 bits (signed)					
			16 bits × 16 bits (unsigned)					
	Divide		32 bits ÷ 32 bits (unsigned)					
	Multiply-accumulate		16 bits × 16 bits + 32 bits (signed)					
			16 bits × 16 bits + 32 bits (unsigned)					
	Arithmetic instructions (extended instruction set)		Yes					
Vectored interrupt sources	External	Products with at least 96 Kbytes of code flash memory	13ch Note 4, 5		12ch Note 3	—		
		Products with up to 64 Kbytes of code flash memory	13ch Note 4, 5	10ch Note 2		8ch Note 2		7ch Note 2
	Internal	Products with at least 96 Kbytes of code flash memory	35ch Note 4		35ch Note 3	—		
		Products with up to 64 Kbytes of code flash memory	35ch Note 4	26ch Note 2				
Key return detection			8ch			6ch	8ch	2ch
DTC	Products with at least 96 Kbytes of code flash memory		36 sources			—		
	Products with up to 64 Kbytes of code flash memory		36 sources	30 sources		29 sources		28 sources

(**Notes** and **Caution** are listed on the next page.)

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Table 1-6. RL78/F13 (LIN incorporated) Functions List (2/2)

Series Name			R5F10AM	R5F10AL	R5F10AG	R5F10AB	R5F10AA	R5F10A6
		Pin Count	80 pins	64 pins	48 pins	32 pins	30 pins	20 pins
TAU	Products with at least 96 Kbytes of code flash memory		16 bits (8ch + 4ch)			—		
	Products with up to 64 Kbytes of code flash memory		16 bits (8ch + 4ch)	16 bits (8ch)				
Timer	RTC		1ch					
	Timer RJ		16 bits × 1 Note 1					
	Timer RD		16 bits × 2					
Serial I/F	CSI/simplified I²C /UART	Products with at least 96 Kbytes of code flash memory	4ch/4ch/2ch			—		
		Products with up to 64 Kbytes of code flash memory	4ch/4ch/2ch	2ch/2ch/1ch				
	SPI		Yes					
	Multimaster I²C	Products with at least 96 Kbytes of code flash memory	1ch			—		
		Products with up to 64 Kbytes of code flash memory	1ch	None				
	LIN/UART module (RLIN3)		1ch					
	CAN interface (RS-CAN lite)		None					
A/D converter 10-bit SAR	V_{DD}	Products with at least 96 Kbytes of code flash memory	16ch	16ch	13ch	—		
		Products with up to 64 Kbytes of code flash memory	16ch	12ch	12ch	8ch	10ch	4ch
	EV_{DD}	Products with at least 96 Kbytes of code flash memory	4ch	3ch	2ch	—		
		Products with up to 64 Kbytes of code flash memory	4ch	None				
	Internal		2ch					
D/A converter	8-bit		None					
Comparator			None					
ELC			None					
PCLBUZ			1ch			None		
Self-programming			Yes					
On-chip debug	Trace		Yes					
	Hot plug-in		Yes					
Option byte			Yes					

Notes 1. The 20-pin products do not have TRJIO0 and TRJO0 pins.

2. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM.

3. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H.

4. The following pairs of internal and external sources are each counted as a single source in this number: INTP4 and INTSPM, INTP6 and INTTM11H, INTP7 and INTTM13H, INTP8 and INTRTC, INTP9 and INTTM01H, INTP10 and INTTM03H.

5. INTP11 and INTLIN0WUP are counted as a single source because using them at the same time is not possible.

6. Do not use the XT1 and XT2 pin functions in grade-Y products.

Caution For details, see 1.5 Pin Configurations.

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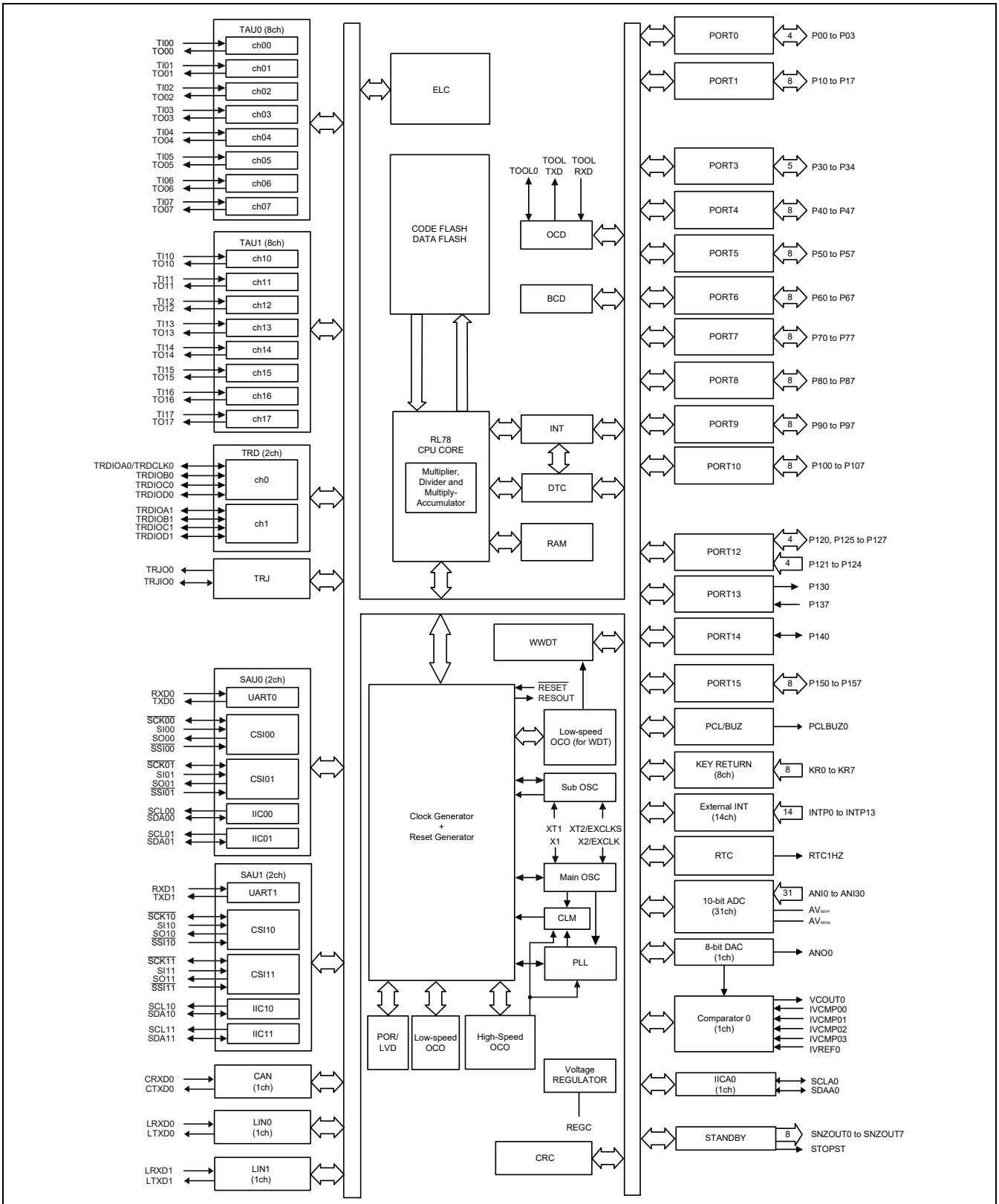
1.4 Block Diagram

1.4.1 RL78/F14: Block Diagram of R5F10PPn (n = E, F, G, H, J) 100-pin Products

Figure 1-1. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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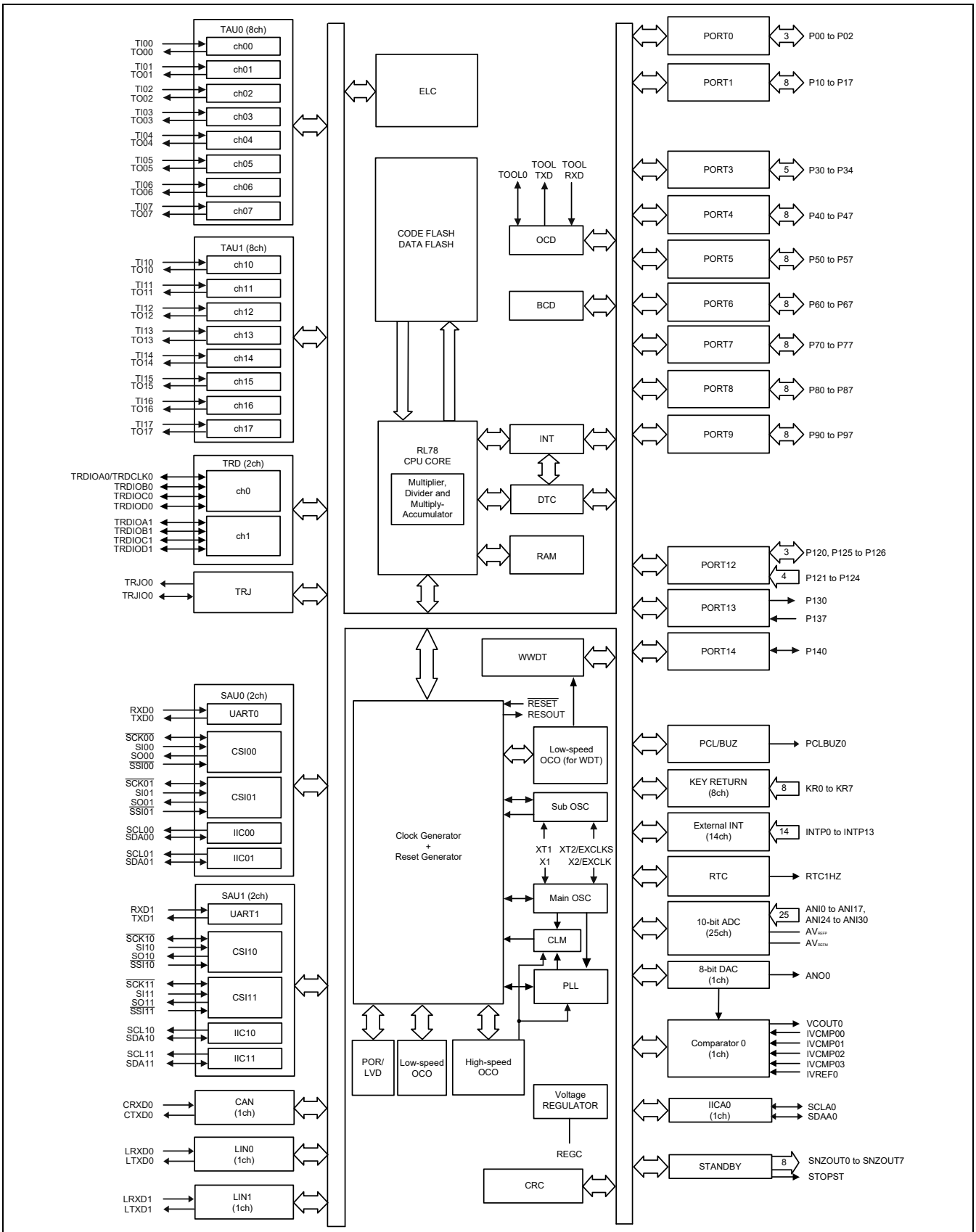
1.4.2 RL78/F14: Block Diagram of R5F10PMn (n = G, H, J) 80-pin Products

Figure 1-2. Block Diagram

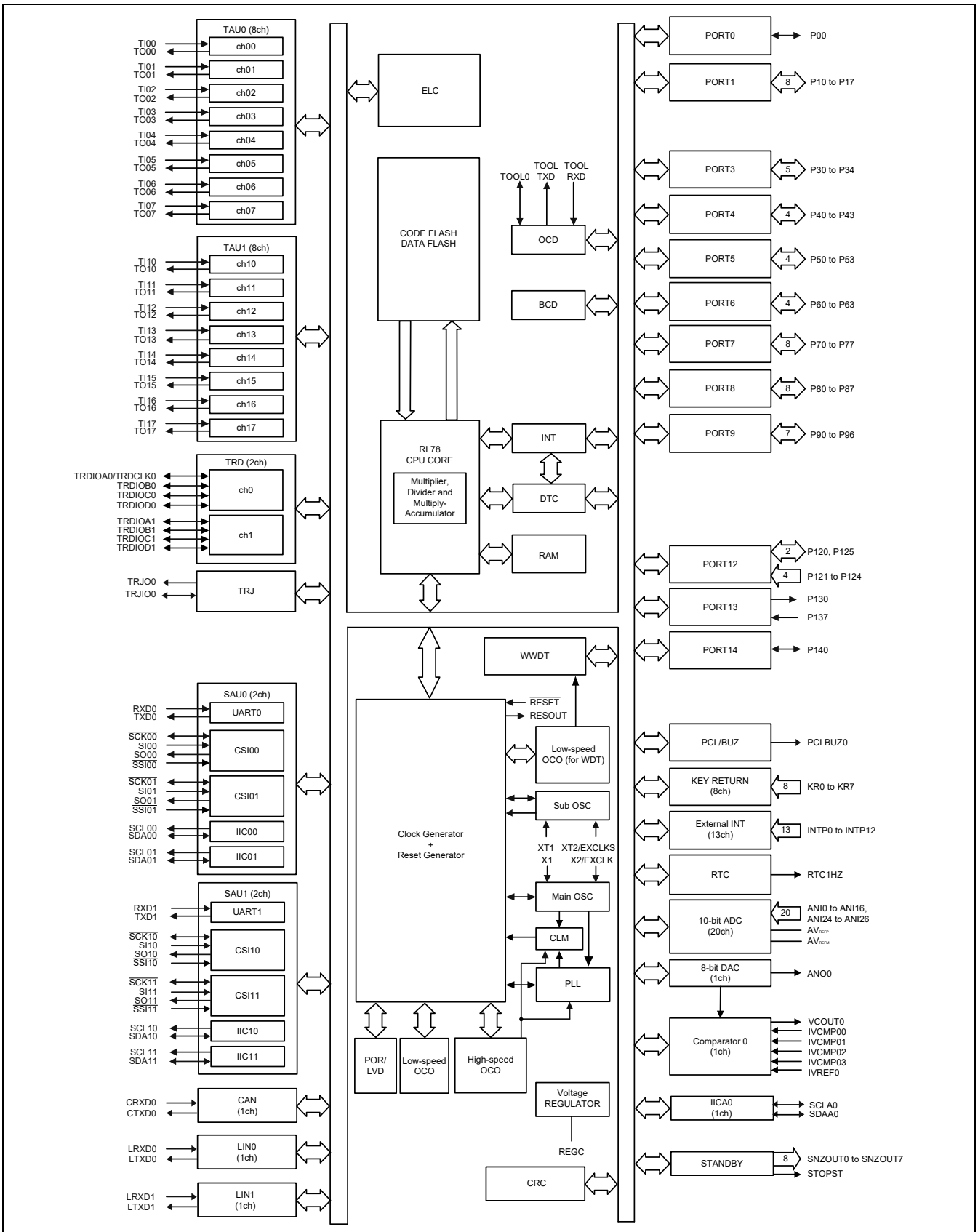


Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

Downloaded from Arrow.com.

1.4.3 RL78/F14: Block Diagram of R5F10PLn (n = G, H, J) 64-pin Products

Figure 1-3. Block Diagram



Cautions 1. Do not use the XT1 and XT2 pin functions in grade-Y products.

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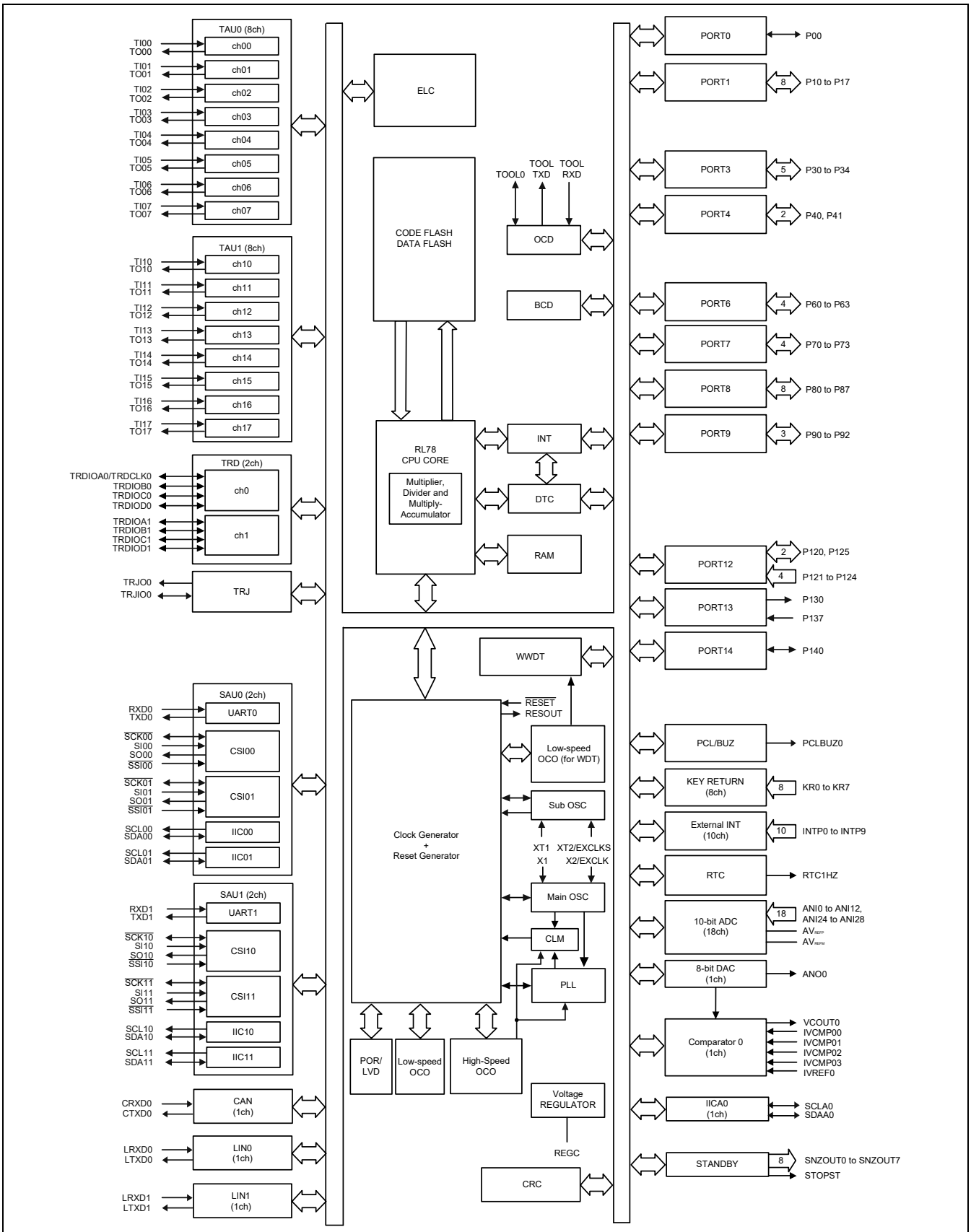
1.4.4 RL78/F14: Block Diagram of R5F10PGn (n = G, H, J) 48-pin Products

Figure 1-4. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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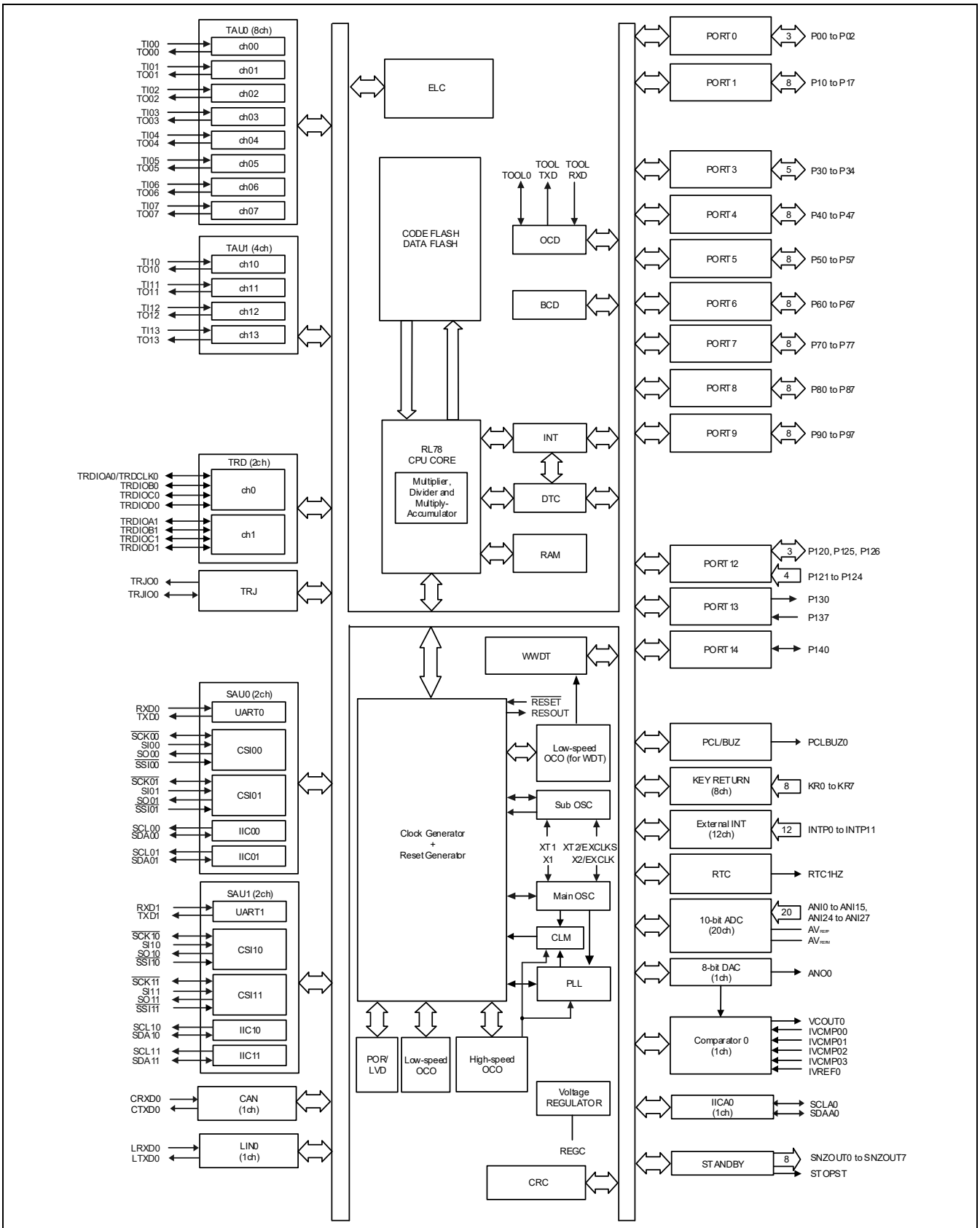
1.4.5 RL78/F14: Block Diagram of R5F10PMn (n = E, F) 80-pin Products

Figure 1-5. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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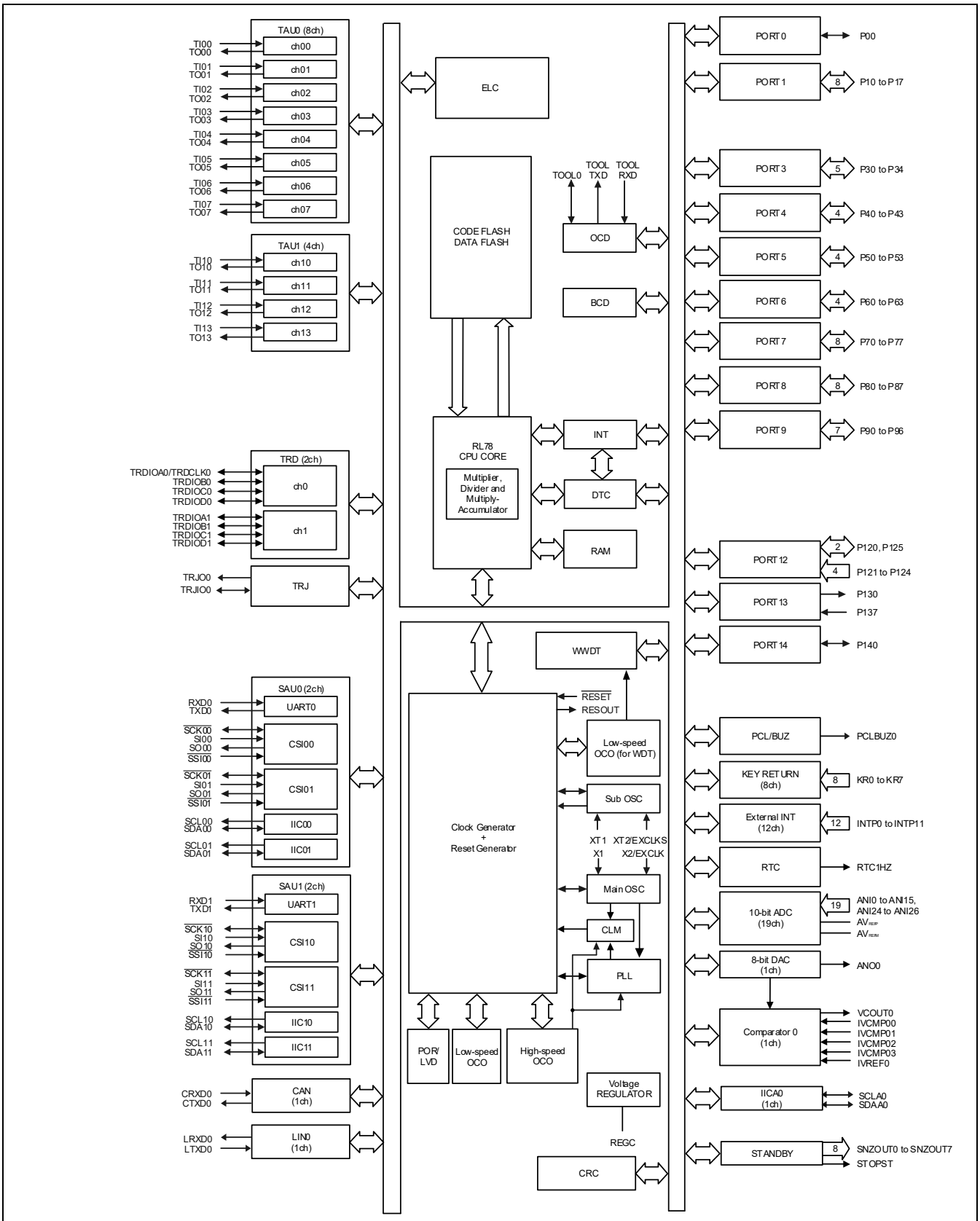
1.4.6 RL78/F14: Block Diagram of R5F10PLn (n = E, F) 64-pin Products

Figure 1-6. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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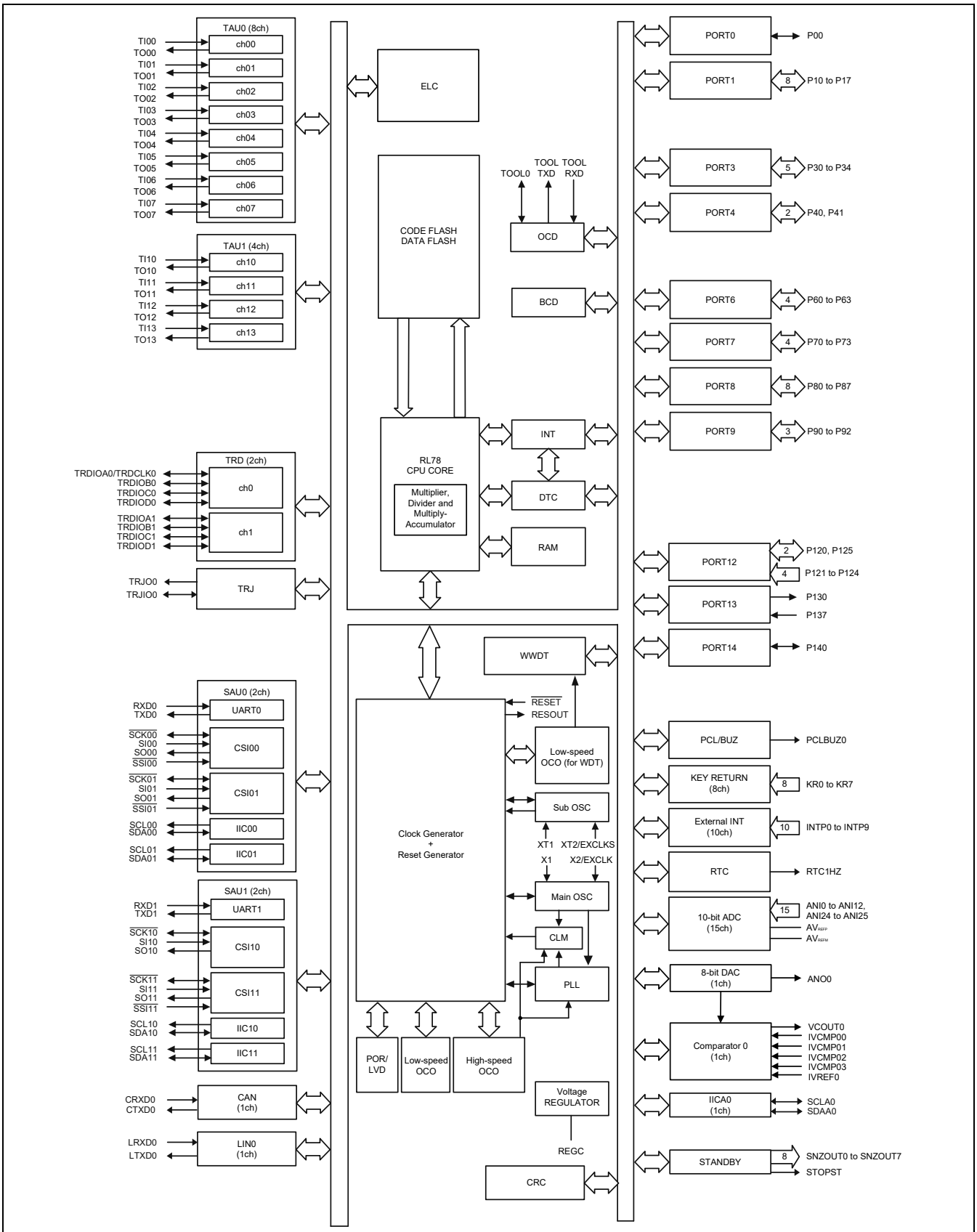
1.4.7 RL78/F14: Block Diagram of R5F10PGn (n = D, E, F) 48-pin Products

Figure 1-7. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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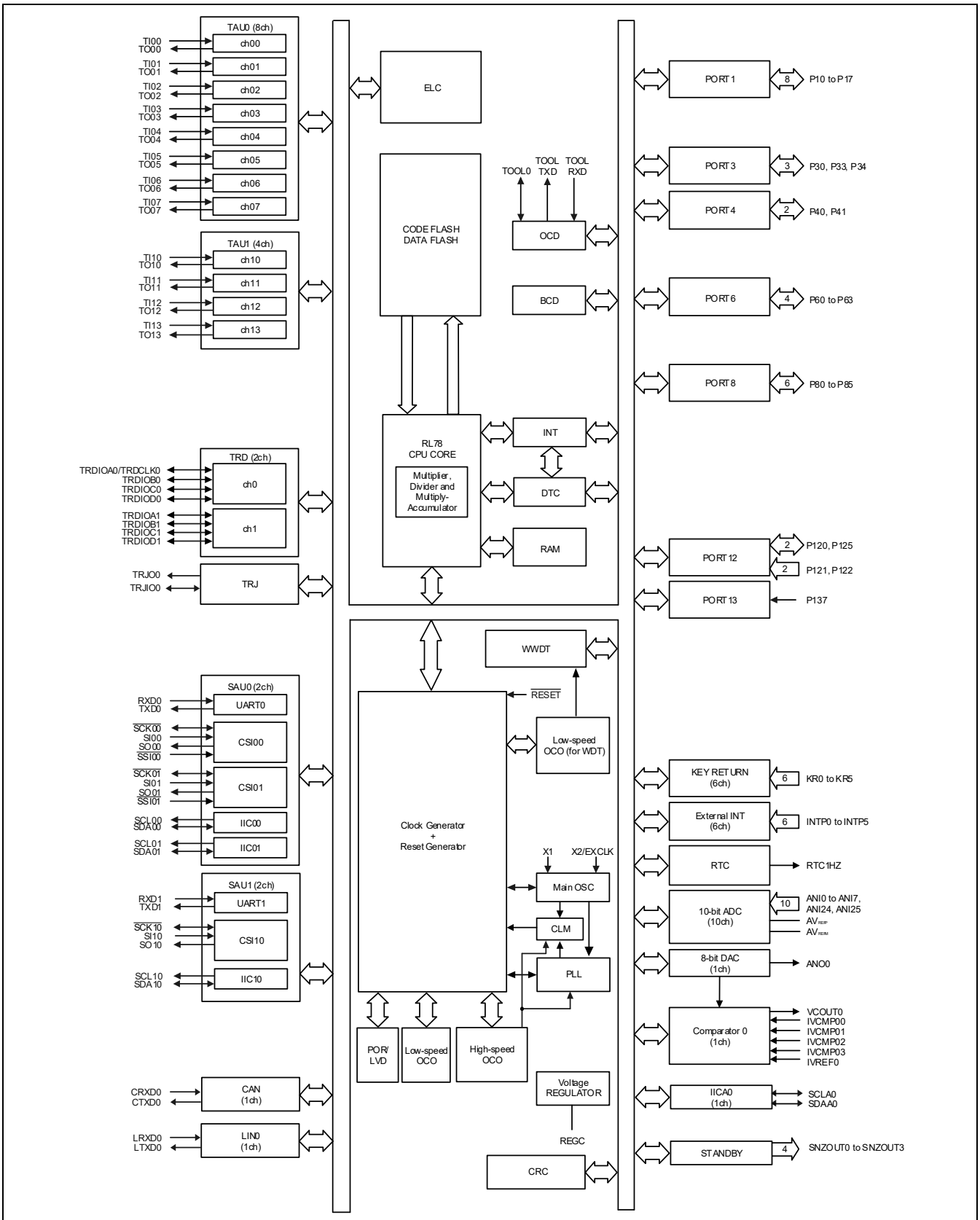
1.4.8 RL78/F14: Block Diagram of R5F10PBn (n = D, E) 32-pin Products

Figure 1-8. Block Diagram

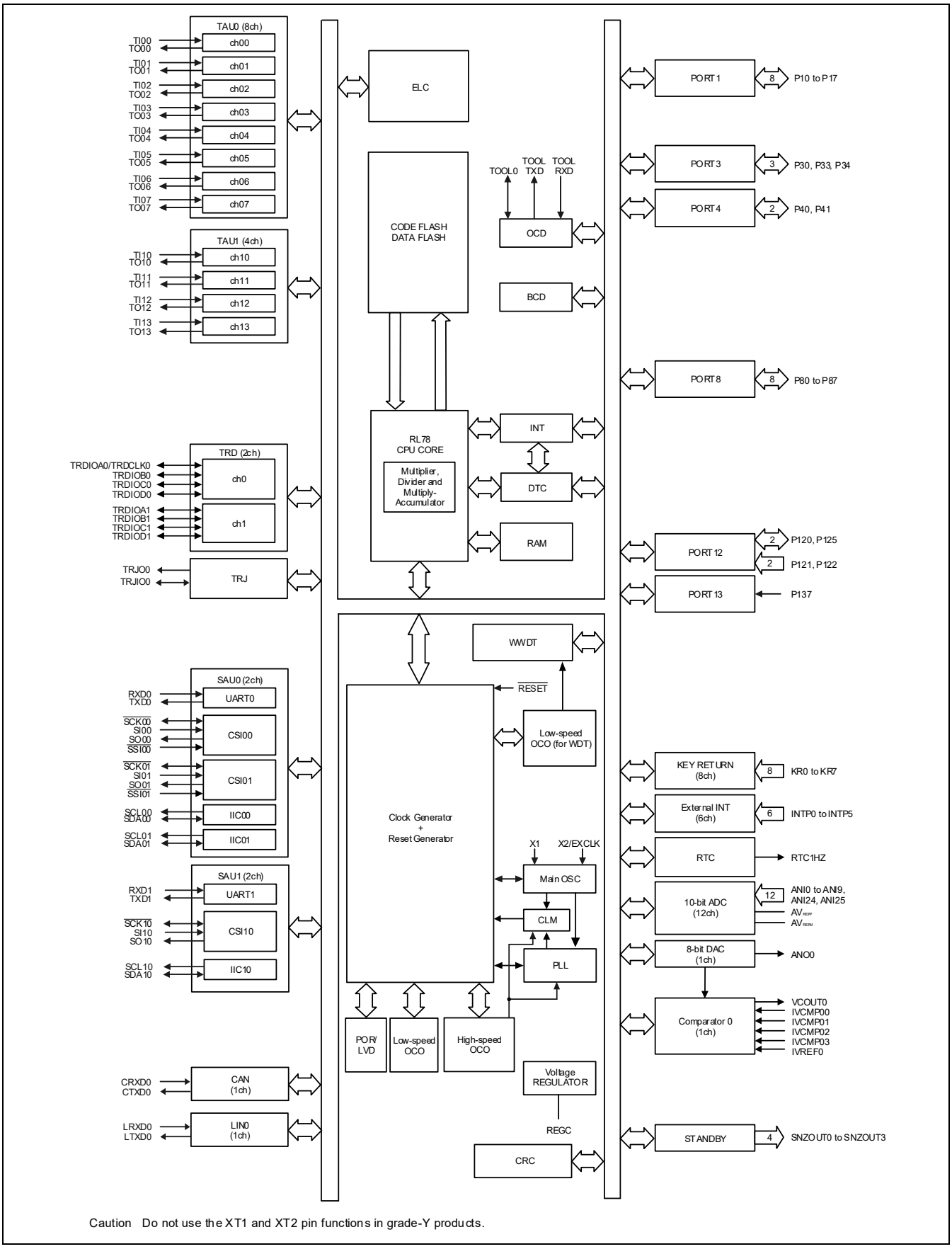


Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

Downloaded from Arrow.com.

1.4.9 RL78/F14: Block Diagram of R5F10PAn (n = D, E) 30-pin Products

Figure 1-9. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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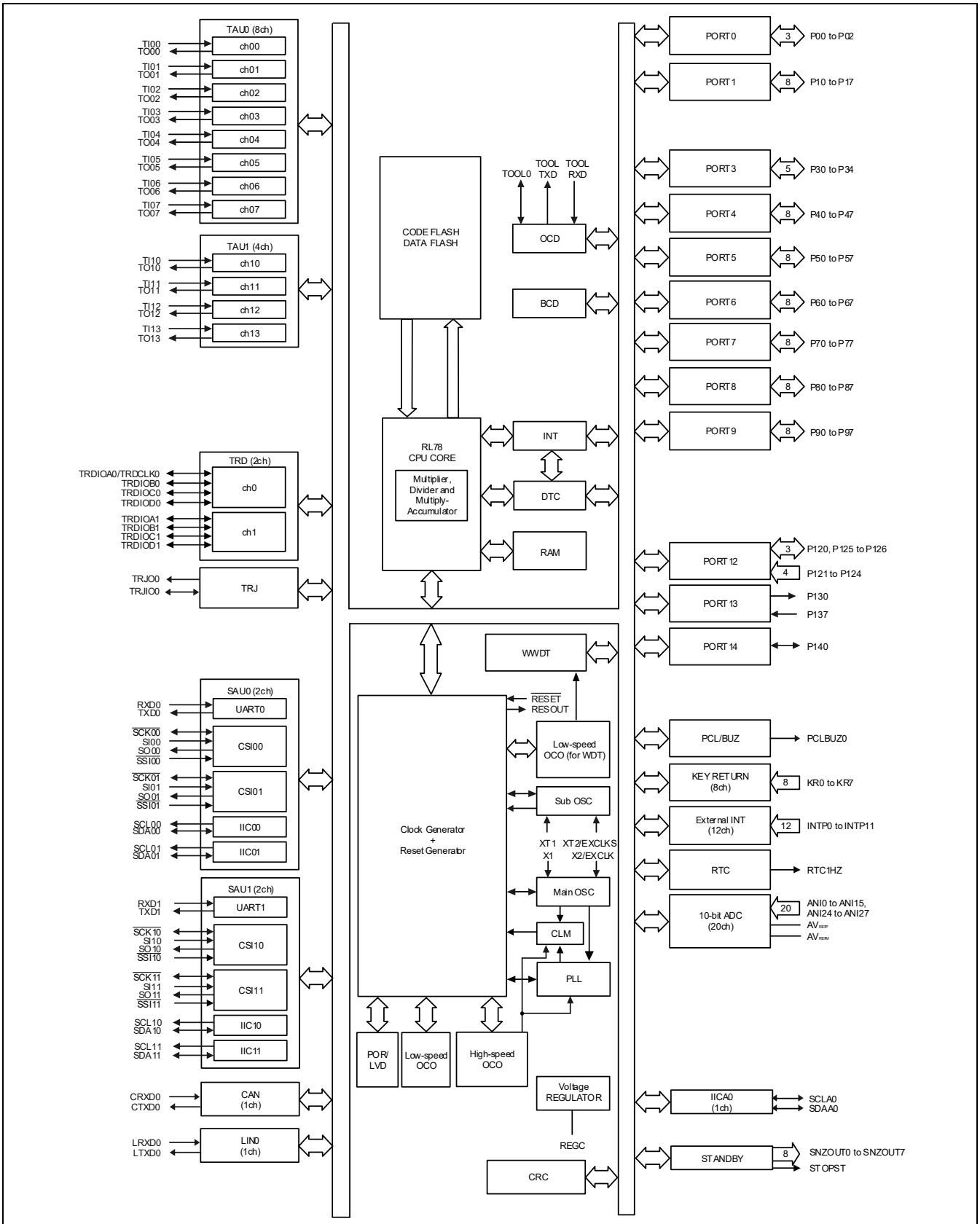
1.4.10 RL78/F13: Block Diagram of R5F10BMn (n = E, F, G) (CAN and LIN incorporated) 80-pin Products

Figure 1-10. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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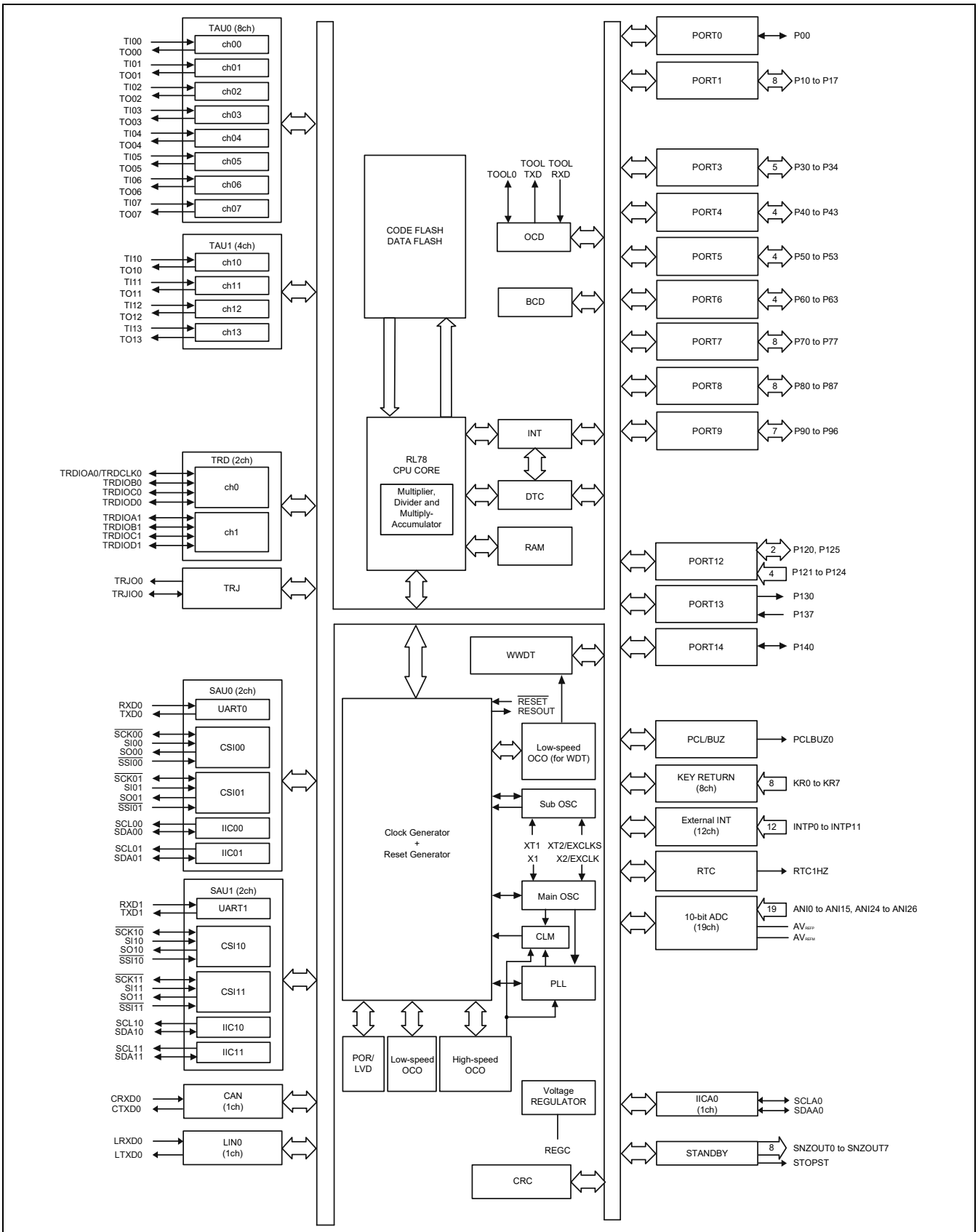
1.4.11 RL78/F13: Block Diagram of R5F10BLn (n = C, D, E, F, G) (CAN and LIN incorporated) 64-pin Products

Figure 1-11. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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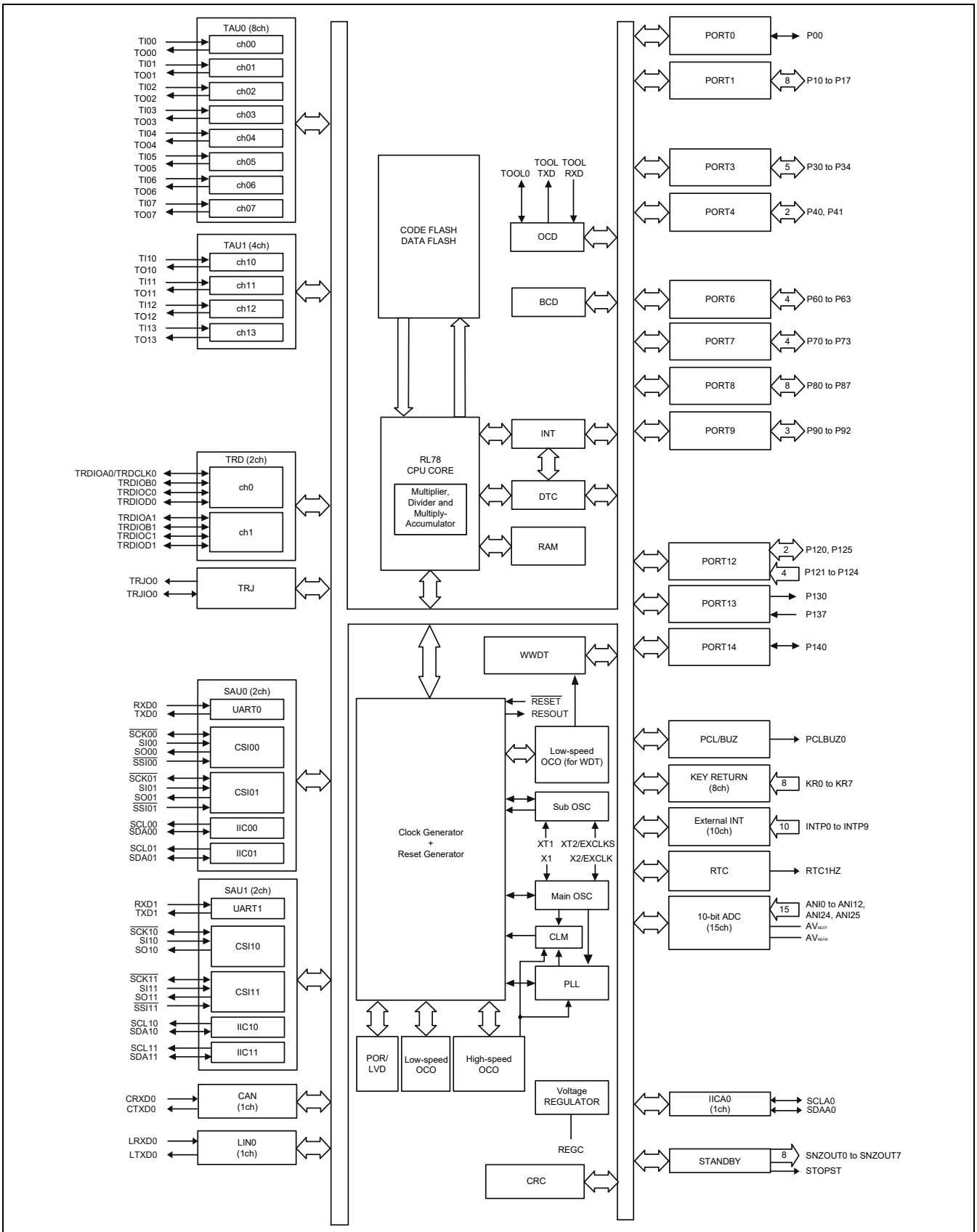
1.4.12 RL78/F13: Block Diagram of R5F10BGn (n = C, D, E, F, G) (CAN and LIN incorporated) 48-pin Products

Figure 1-12. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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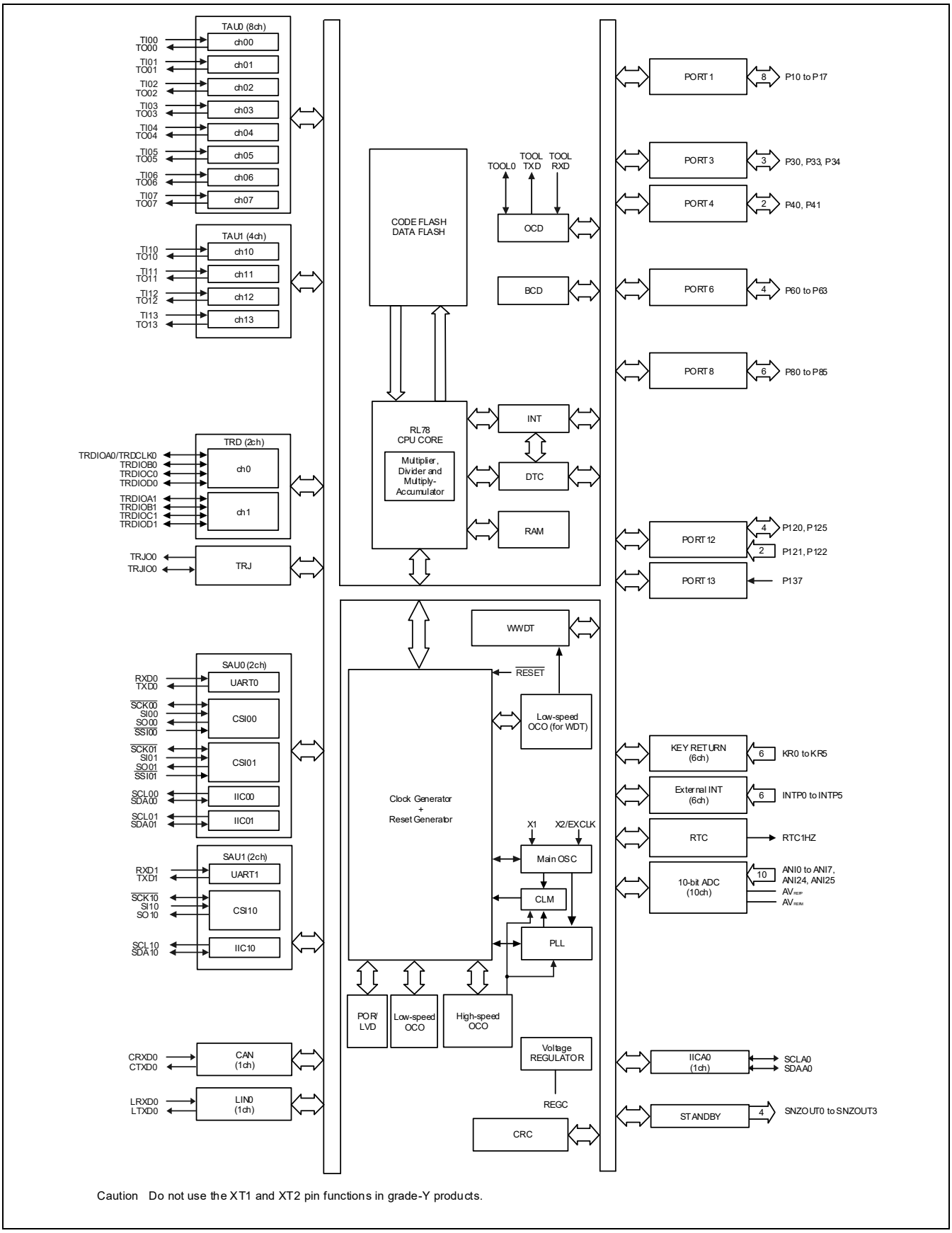
1.4.13 RL78/F13: Block Diagram of R5F10BBn (n = C, D, E, F, G) (CAN and LIN incorporated) 32-pin Products

Figure 1-13. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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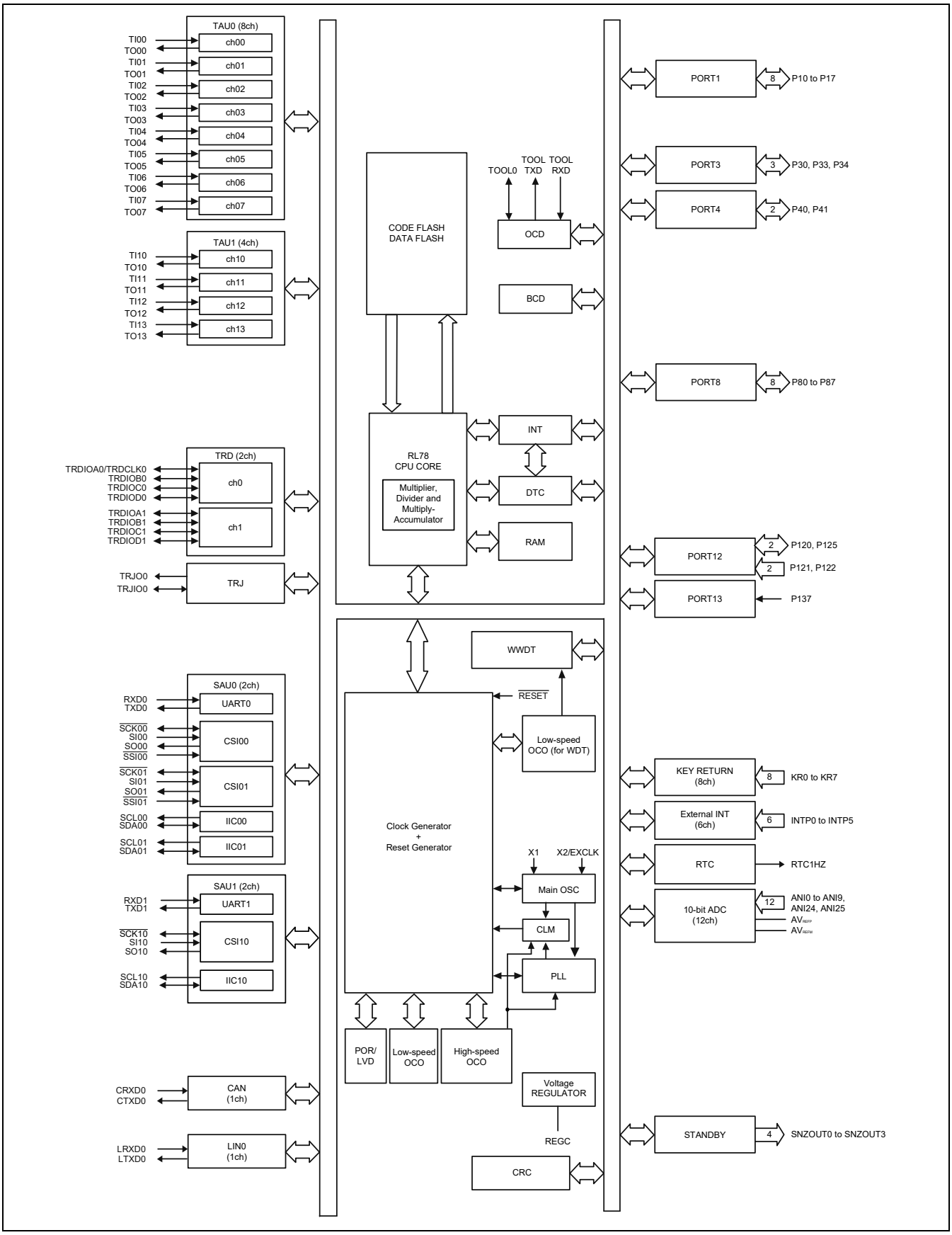
1.4.14 RL78/F13: Block Diagram of R5F10BAn (n = C, D, E, F, G) (CAN and LIN incorporated) 30-pin Products

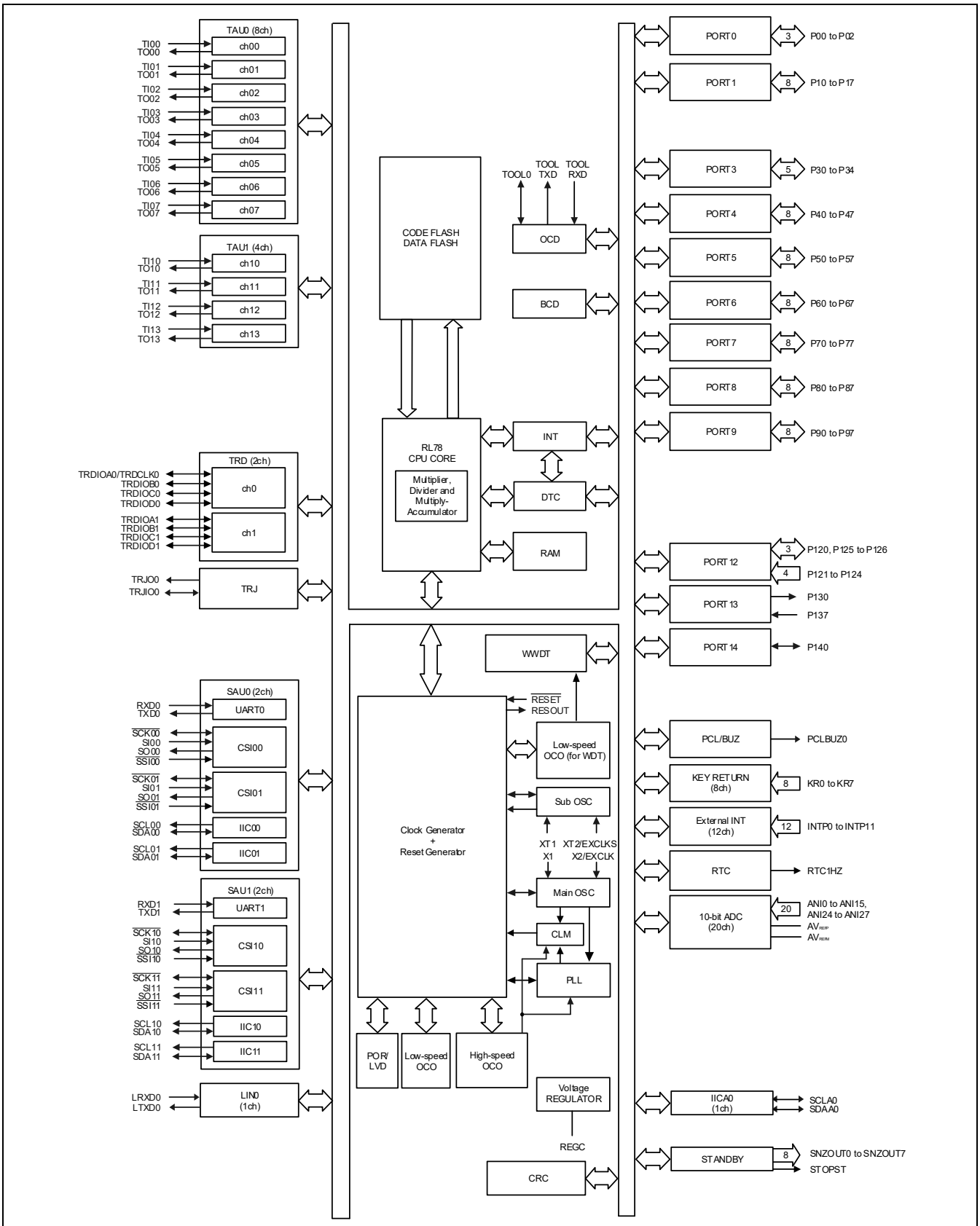
Figure 1-14. Block Diagram



Downloaded from Arrow.com.

1.4.15 RL78/F13: Block Diagram of R5F10AMn (n = E, F, G) (LIN incorporated) 80-pin Products

Figure 1-15. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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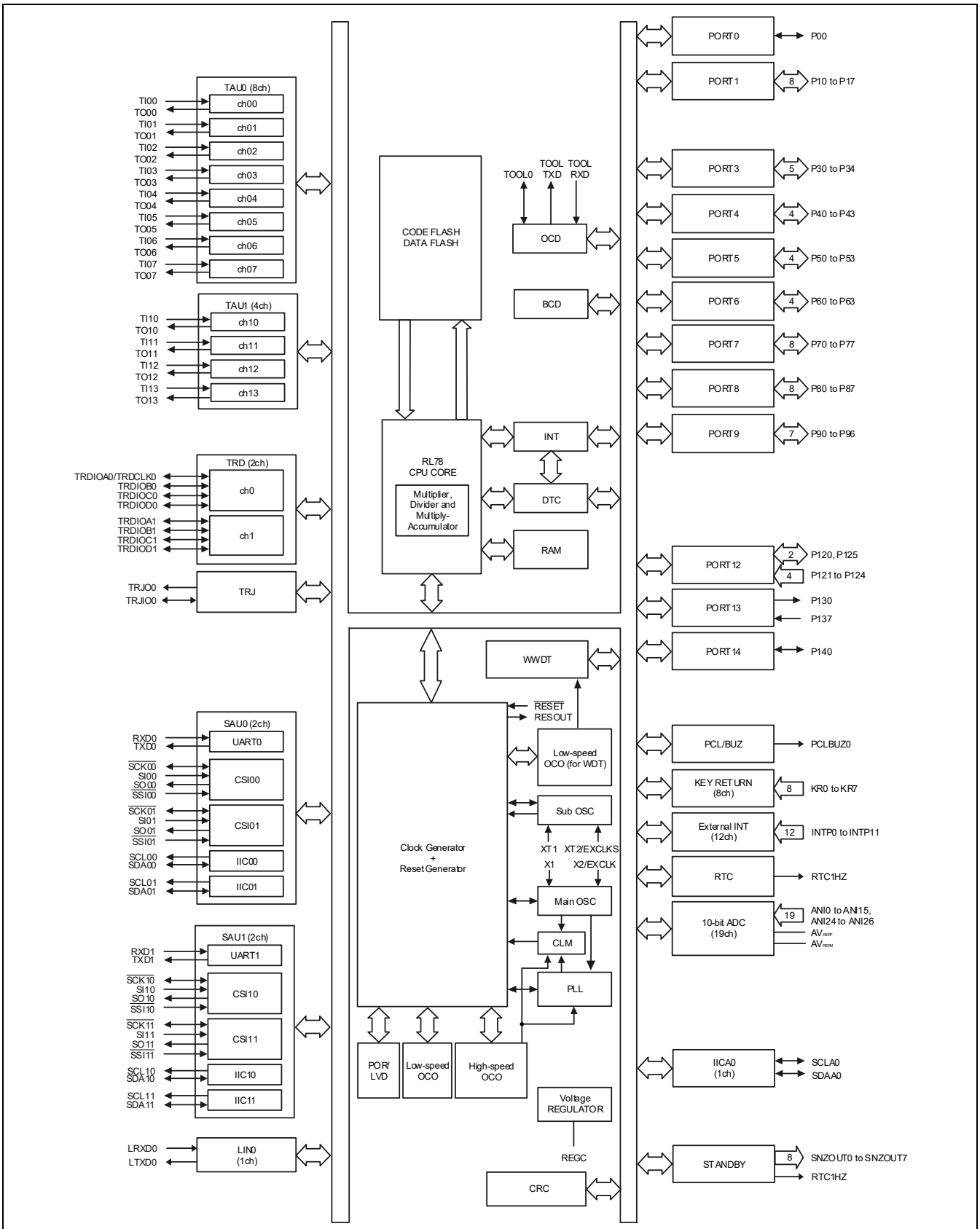
1.4.16 RL78/F13: Block Diagram of R5F10ALn (n = F, G) (LIN incorporated) 64-pin Products

Figure 1-16. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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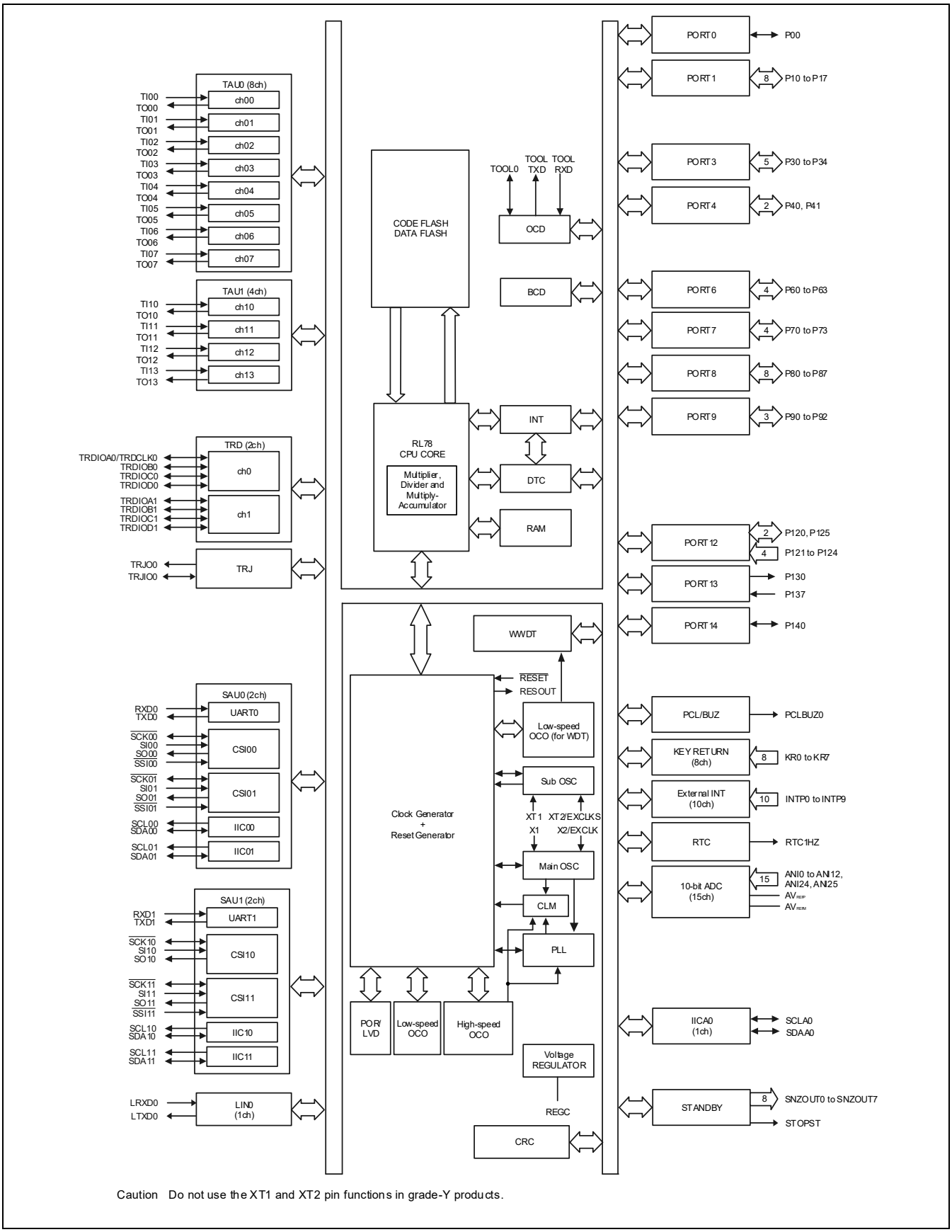
1.4.17 RL78/F13: Block Diagram of R5F10AGn (n = F, G) (LIN incorporated) 48-pin Products

Figure 1-17. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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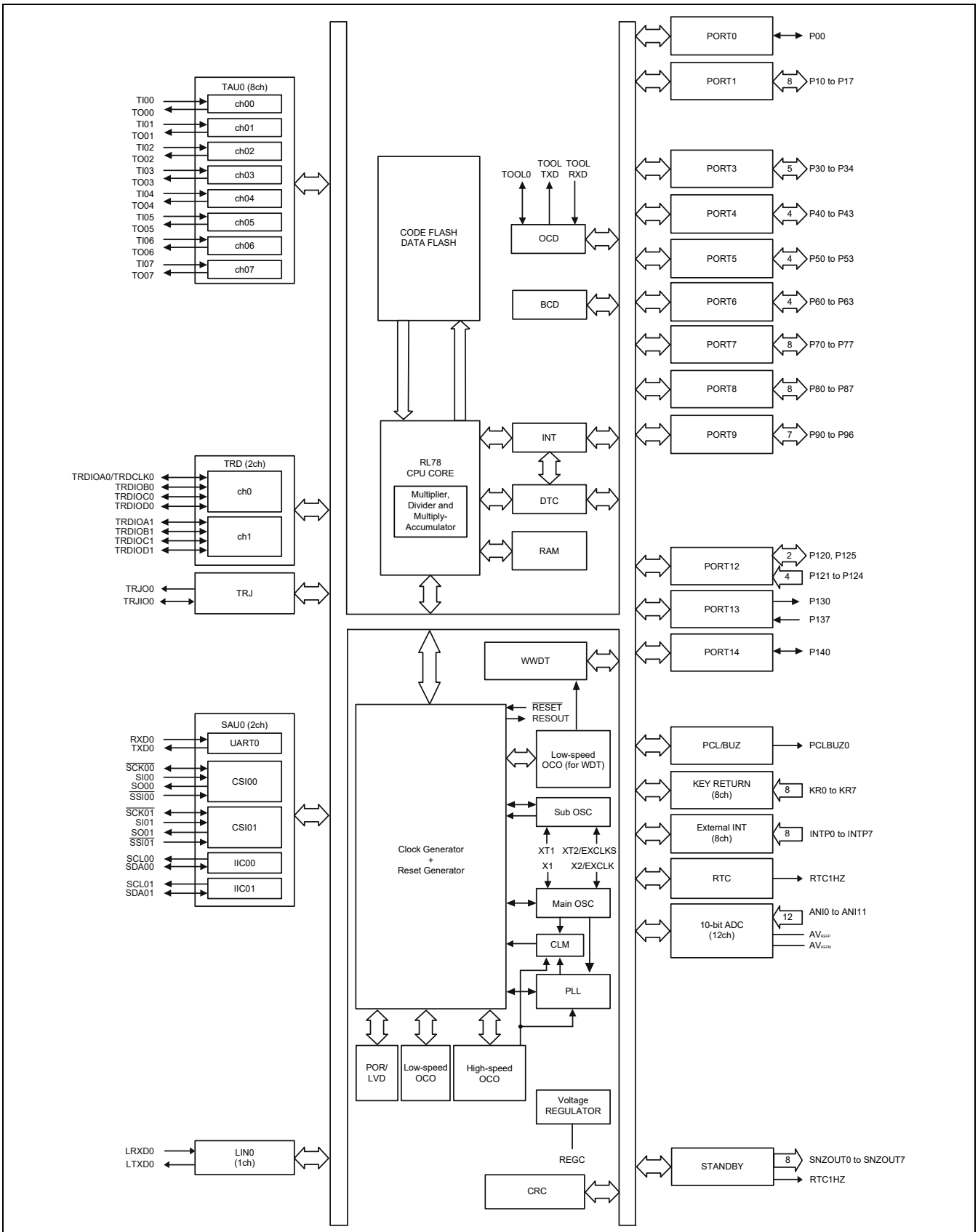
1.4.18 RL78/F13: Block Diagram of R5F10ALn (n = C, D, E) (LIN incorporated) 64-pin Products

Figure 1-18. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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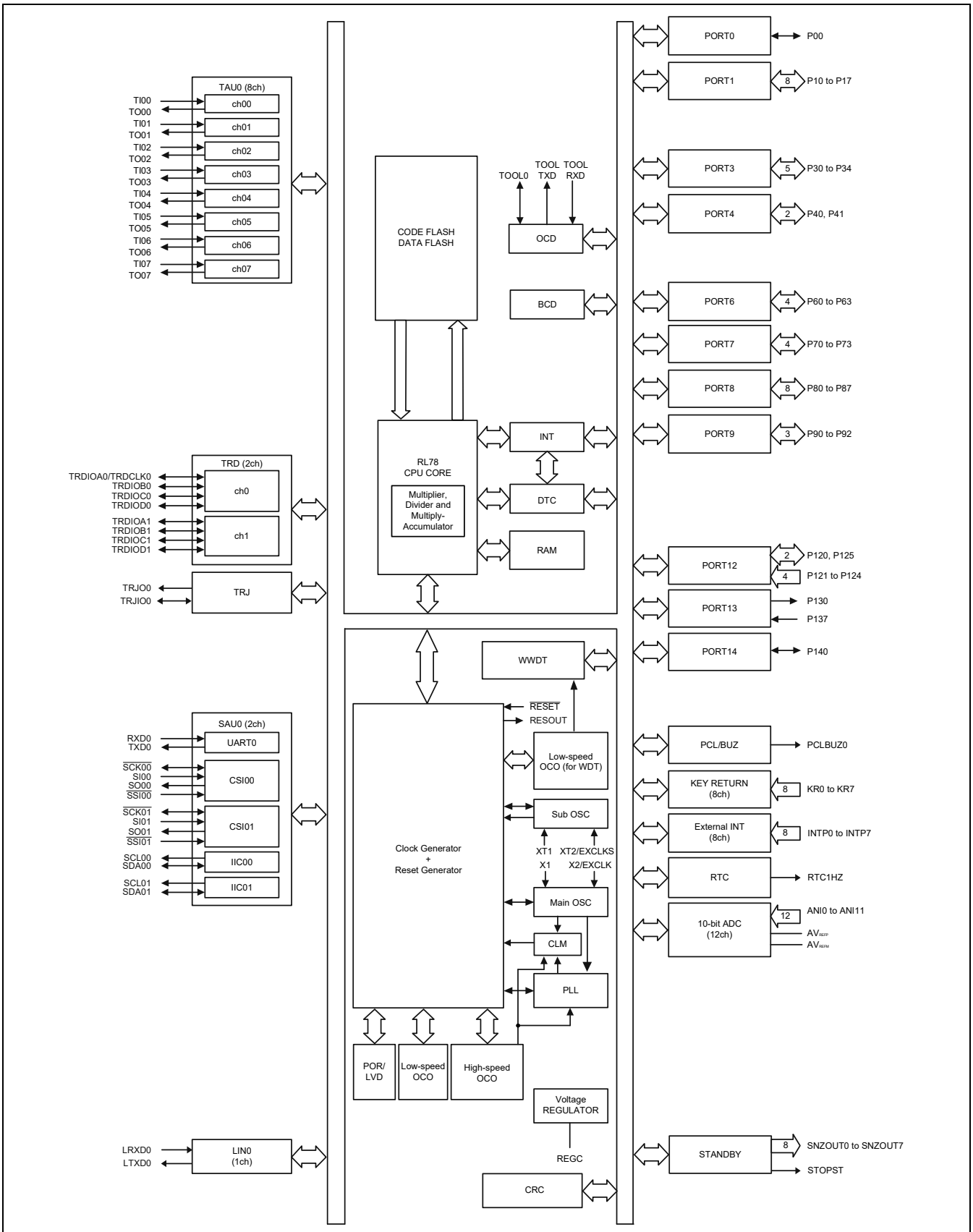
1.4.19 RL78/F13: Block Diagram of R5F10AGn (n = A, C, D, E) (LIN incorporated) 48-pin Products

Figure 1-19. Block Diagram



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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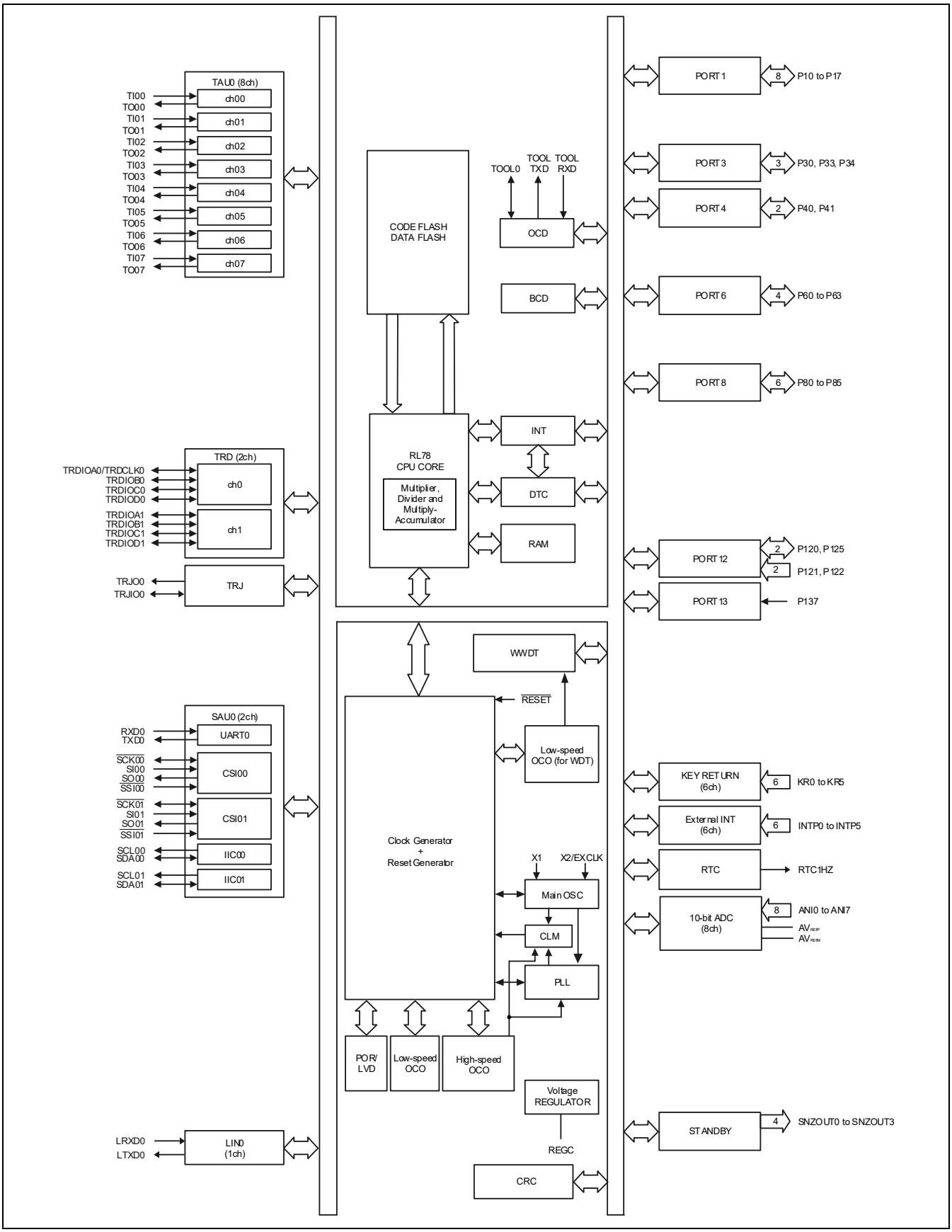
1.4.20 RL78/F13: Block Diagram of R5F10ABn (n = A, C, D, E) (LIN incorporated) 32-pin Products

Figure 1-20. Block Diagram



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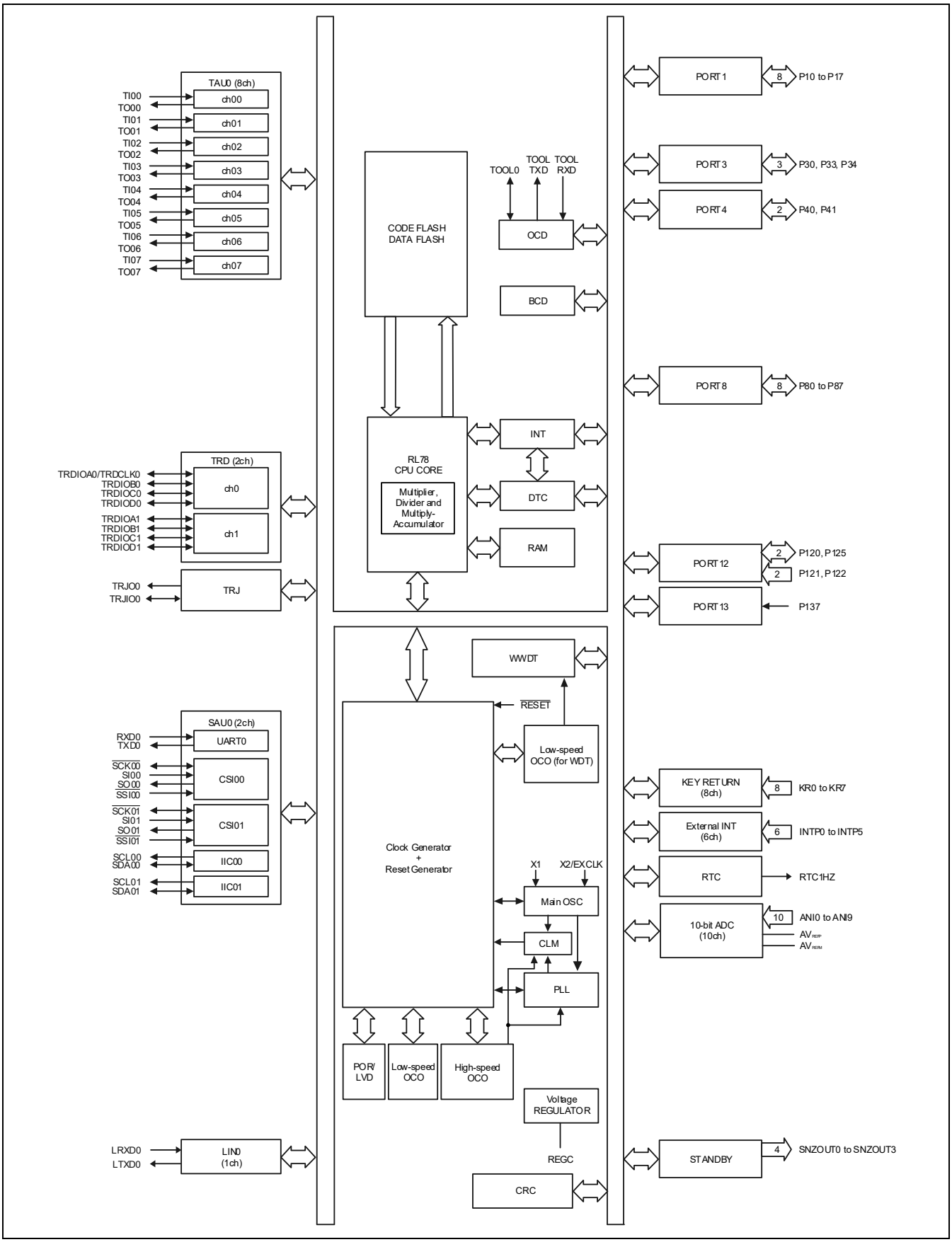
1.4.21 RL78/F13: Block Diagram of R5F10AAn (n = A, C, D, E) (LIN incorporated) 30-pin Products

Figure 1-21. Block Diagram



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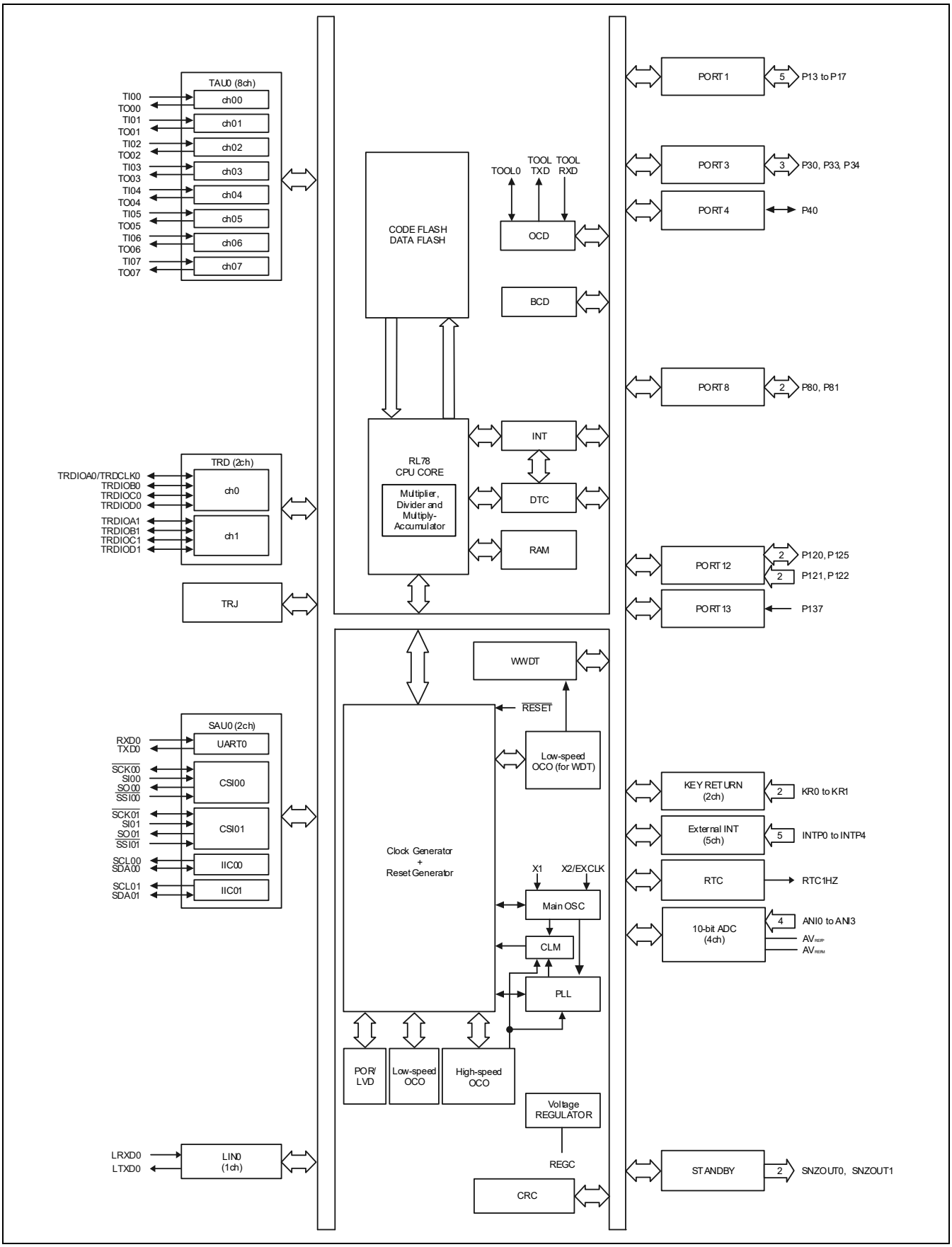
1.4.22 RL78/F13: Block Diagram of R5F10A6n (n = A, C, D, E) (LIN incorporated) 20-pin Products

Figure 1-22. Block Diagram



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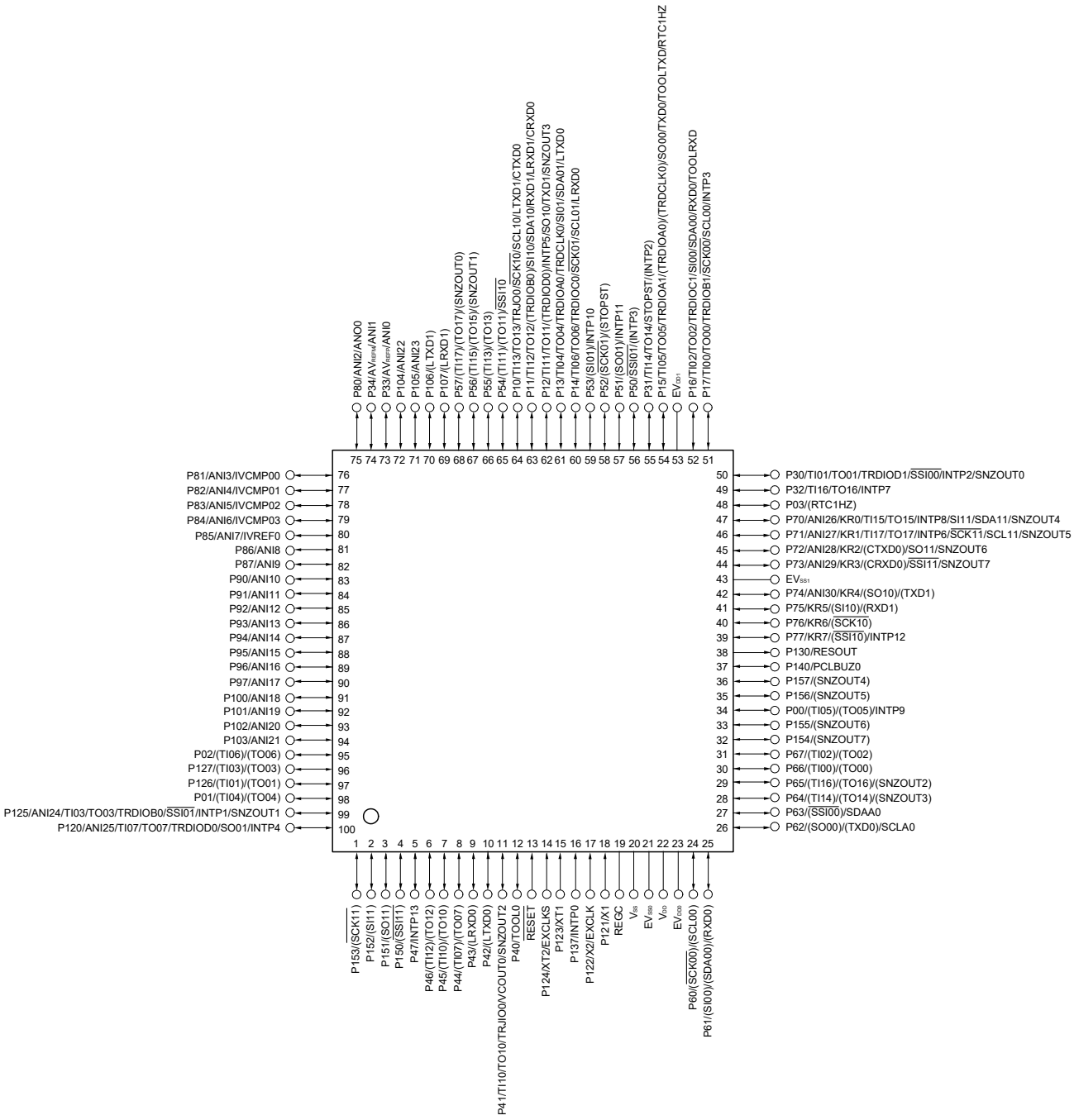
1.5 Pin Configurations

1.5.1 RL78/F14 Pin Configuration for 100-pin Products

<R>

- RL78/F14: 100-pin Plastic LFQFP (Fine Pitch) (14 x 14)

Figure 1-23. RL78/F14 Pin Configuration for 100-pin Products



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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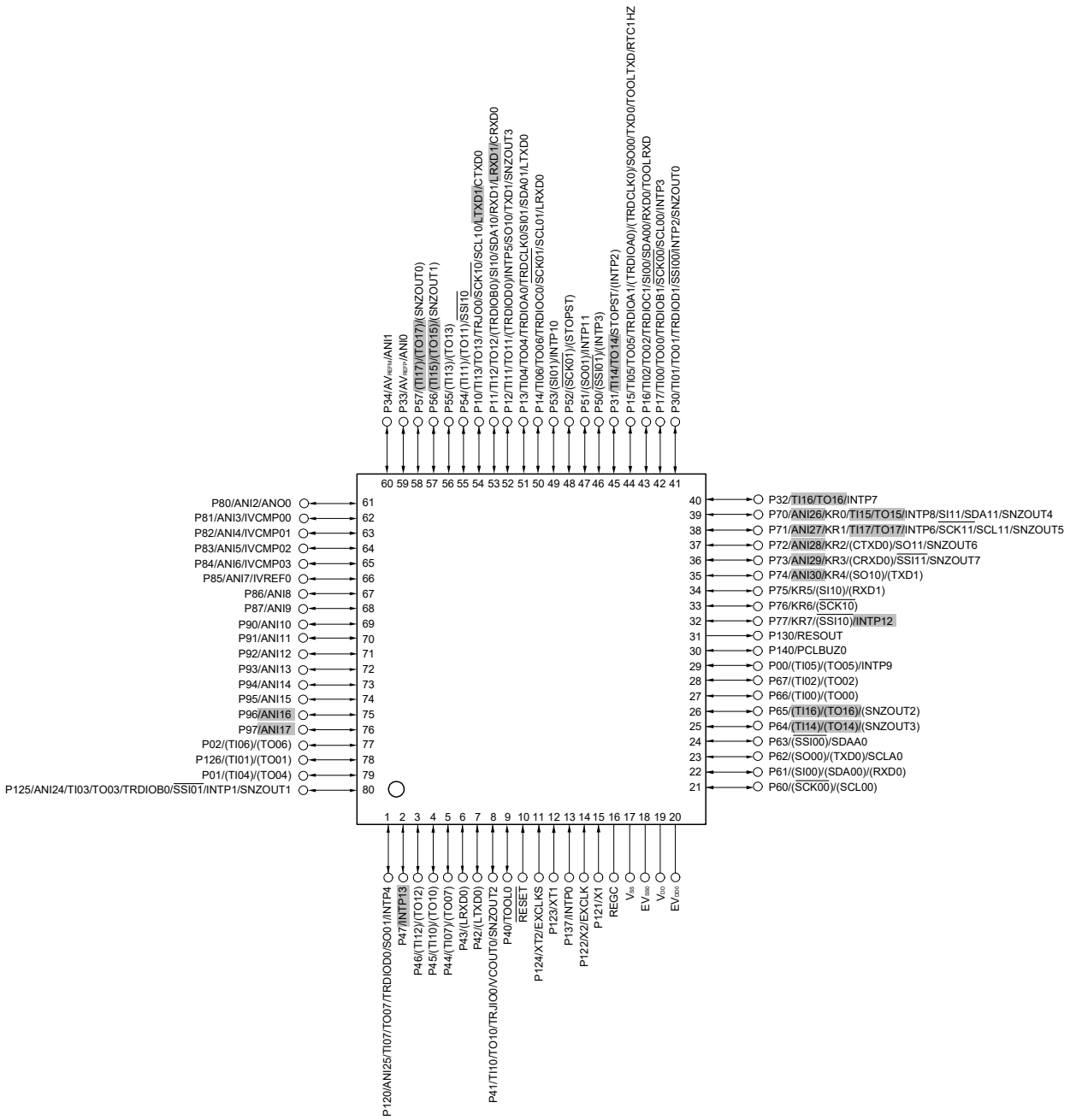
1.5.2 RL78/F14 Pin Configuration for 80-pin Products

<R> • RL78/F14: 80-pin Plastic LFQFP (Fine Pitch) (12 x 12)

Figure 1-24. RL78/F14 Pin Configuration for 80-pin Products



Cautions 1. ▒: Shaded pins are not available in the R5F10PME or R5F10PMF.
Note, however, that the functions of pins 75 and 76, to which ANI16 and ANI17 are assigned, differ depending on the product, as follows:
- R5F10PMG, R5F10PMH, R5F10PMJ: P96/ANI16 (pin 75)
  P97/ANI17 (pin 76)
- R5F10PME, R5F10PMF: P96/ANI26 (pin 75)
  P97/ANI27 (pin 76)

2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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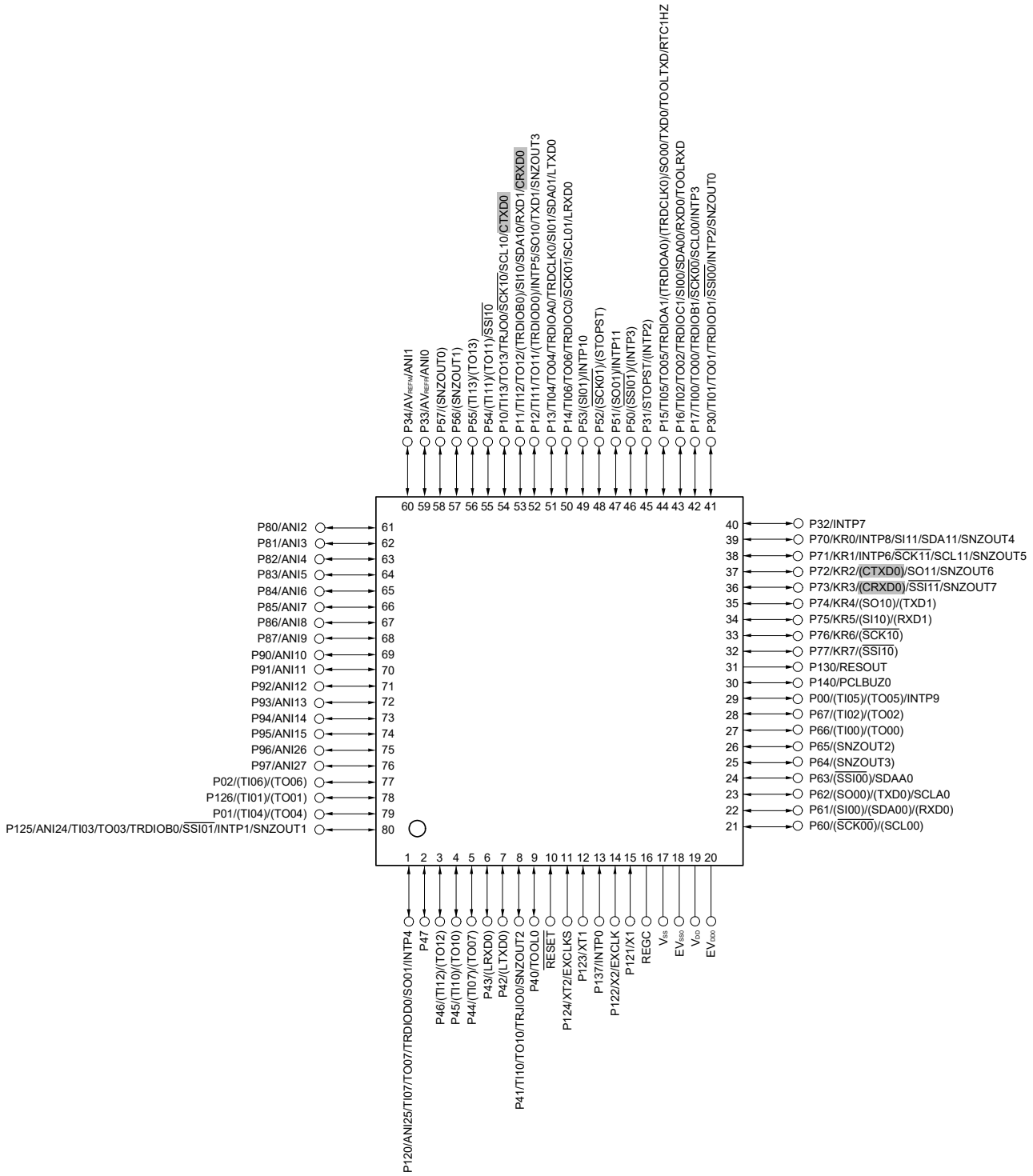
1.5.3 RL78/F13 Pin Configuration for 80-pin Products

<R> • RL78/F13: 80-pin Plastic LFQFP (Fine Pitch) (12 x 12)

Figure 1-25. RL78/F13 Pin Configuration for 80-pin Products



Cautions 1. ▒: Shaded pins are not available in the RL78/F13 (LIN incorporated) products (R5F10AME, R5F10AMF, R5F10AMG).
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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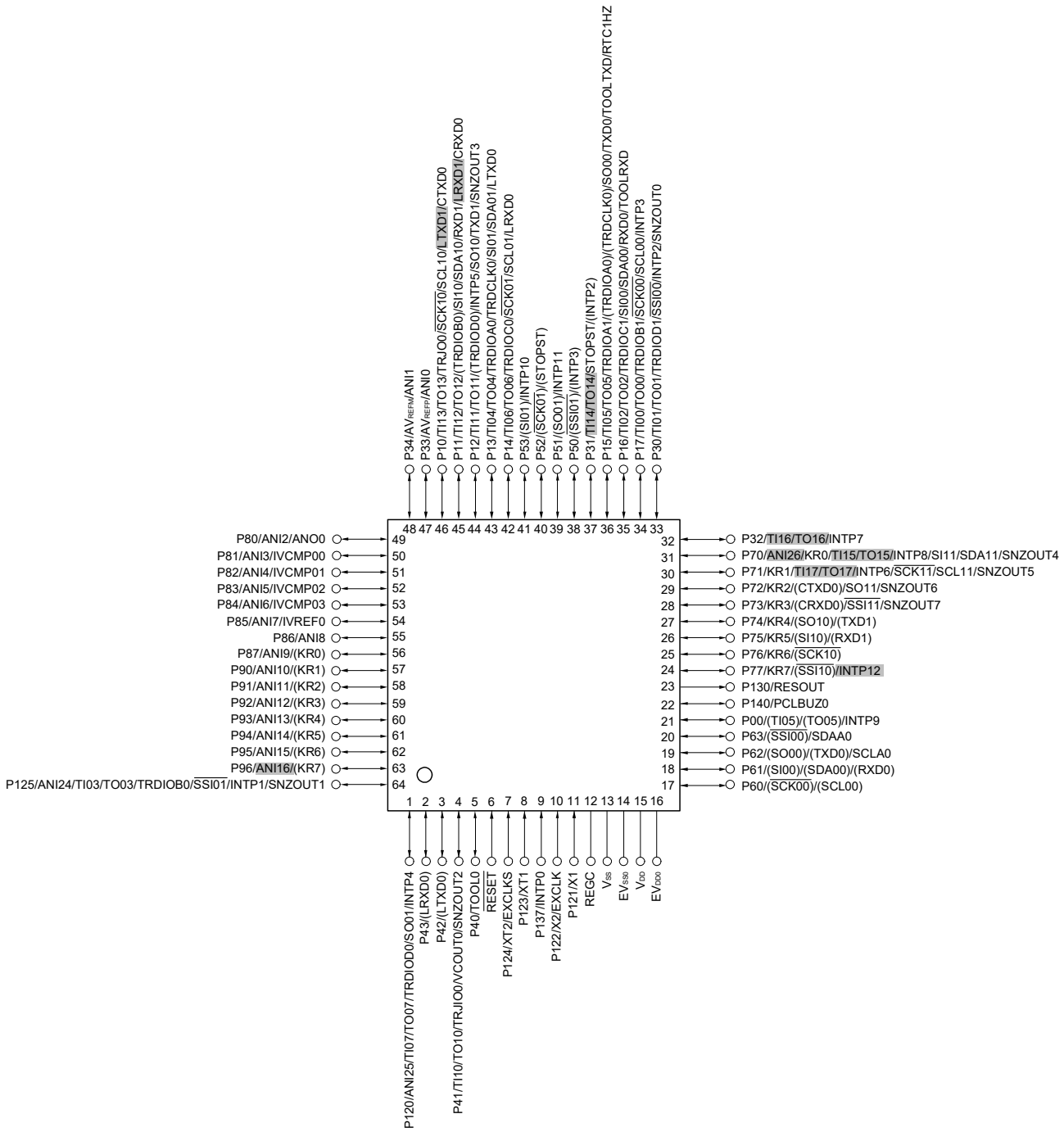
1.5.4 RL78/F14 Pin Configuration for 64-pin Products

<R> • RL78/F14: 64-pin Plastic LFQFP (Fine Pitch) (10 x 10)

Figure 1-26. RL78/F14 Pin Configuration for 64-pin Products



Cautions 1. ▒: Shaded pins are not available in the R5F10PLE or R5F10PLF.
Note, however, that the functions of pin 63 to which ANI16 is assigned, differ depending on the product, as follows:
• R5F10PLG, R5F10PLH, R5F10PLJ: P96/ANI16/(KR7)
• R5F10PLE, R5F10PLF: P96/ANI26/(KR7)
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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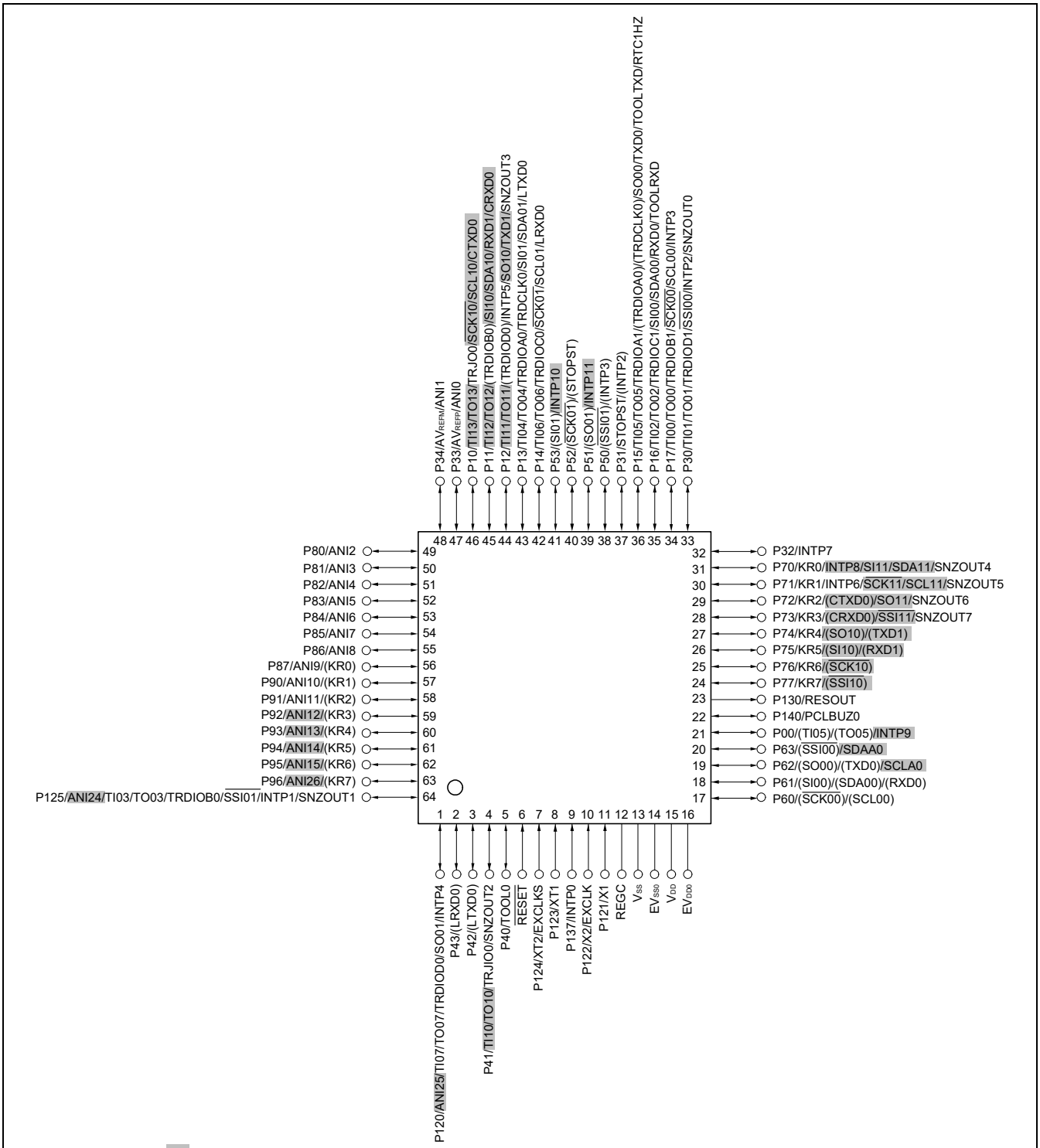
1.5.5 RL78/F13 Pin Configuration for 64-pin Product

<R> • RL78/F13: 64-pin Plastic LFQFP (Fine Pitch) (10 x 10)

Figure 1-27. RL78/F13 Pin Configuration for 64-pin Products



Cautions 1. ▒: Shaded pins are not available in the RL78/F13 (LIN incorporated) products (R5F10ALC, R5F10ALD, R5F10ALE).
CTXD0, CRXD0, (CTXD0), and (CRXD0) pins are not available in the RL78/F13 (LIN incorporated) products (R5F10ALF, R5F10ALG).
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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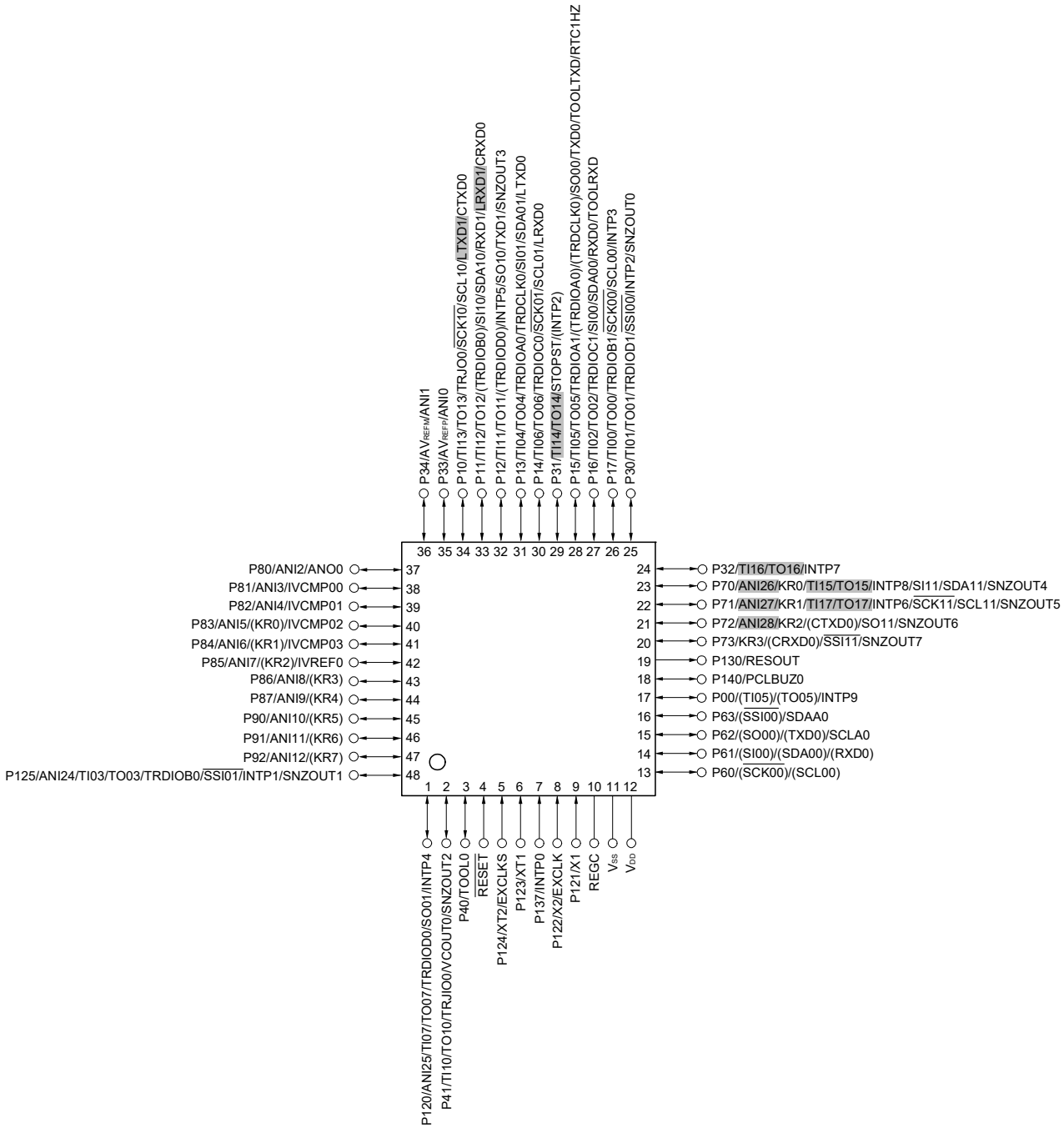
1.5.6 RL78/F14 Pin Configuration for 48-pin Products

<R>

- RL78/F14: 48-pin Plastic LFQFP and HVQFN

Figure 1-28. RL78/F14 Pin Configuration for 48-pin Products



Cautions 1. ▒: Shaded pins are not available in the R5F10PGD, R5F10PGE, or R5F10PGF.
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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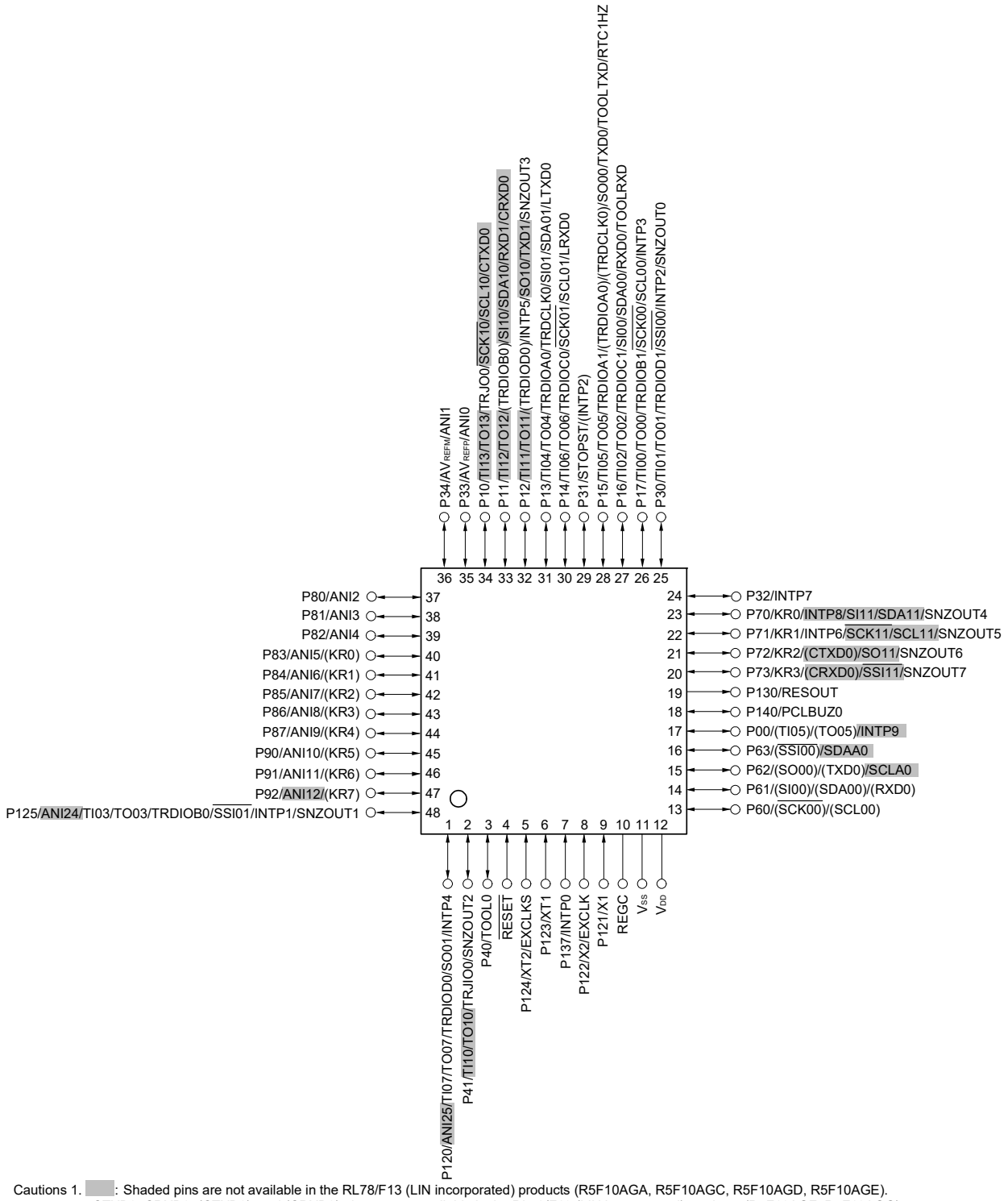
1.5.7 RL78/F13 Pin Configuration for 48-pin Products

<R>

- RL78/F13: 48-pin Plastic LFQFP and HVQFN

Figure 1-29. RL78/F13 Pin Configuration for 48-pin Products



Cautions 1. ▒: Shaded pins are not available in the RL78/F13 (LIN incorporated) products (R5F10AGA, R5F10AGC, R5F10AGD, R5F10AGE).
CTXD0, CRXD0, (CTXD0), and (CRXD0) pins are not available in the RL78/F13 (LIN incorporated) products (R5F10AGF, R5F10AGG).
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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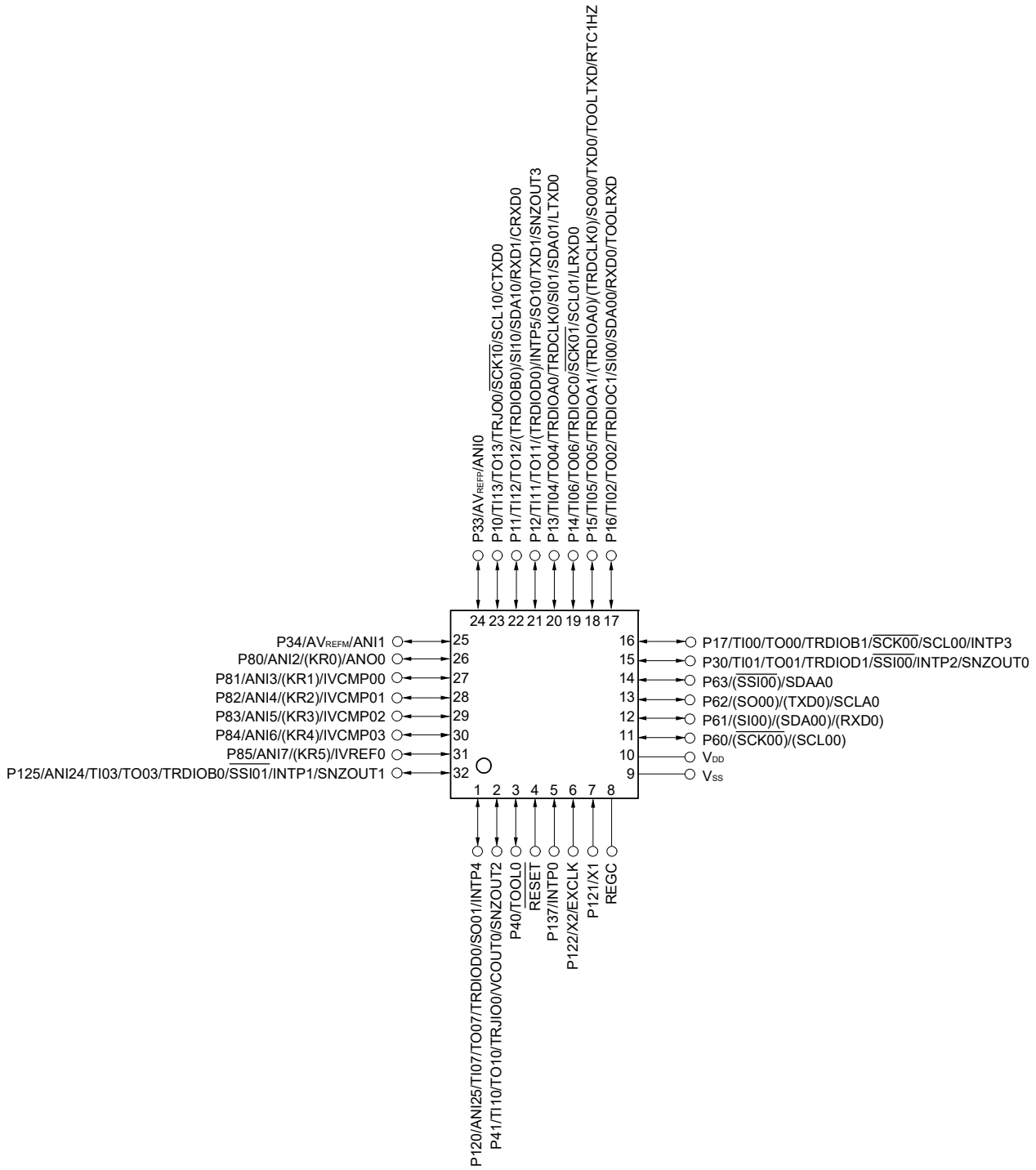
1.5.8 RL78/F14 Pin Configuration for 32-pin Products

<R> • RL78/F14: 32-pin Plastic HVQFN and HWQFN

Figure 1-30. RL78/F14 Pin Configuration for 32-pin Product



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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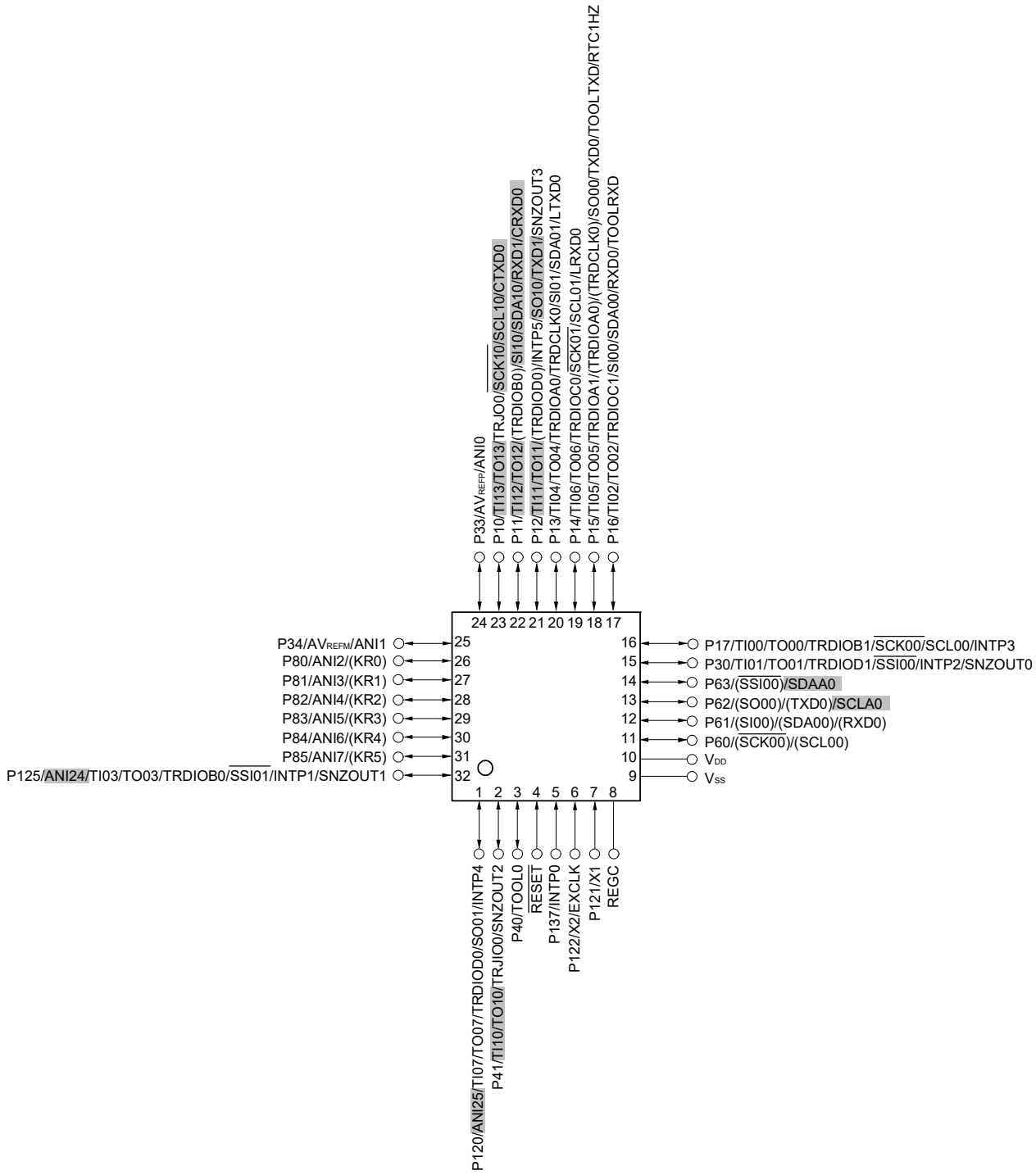
1.5.9 RL78/F13 Pin Configuration for 32-pin Products

<R> • RL78/F13: 32-pin Plastic HVQFN and HWQFN

Figure 1-31. RL78/F13 Pin Configuration for 32-pin Products



Cautions 1. ▒: Shaded pins are not available in the RL78/F13 (LIN incorporated) products (R5F10ABA, R5F10ABC, R5F10ABD, R5F10ABE).
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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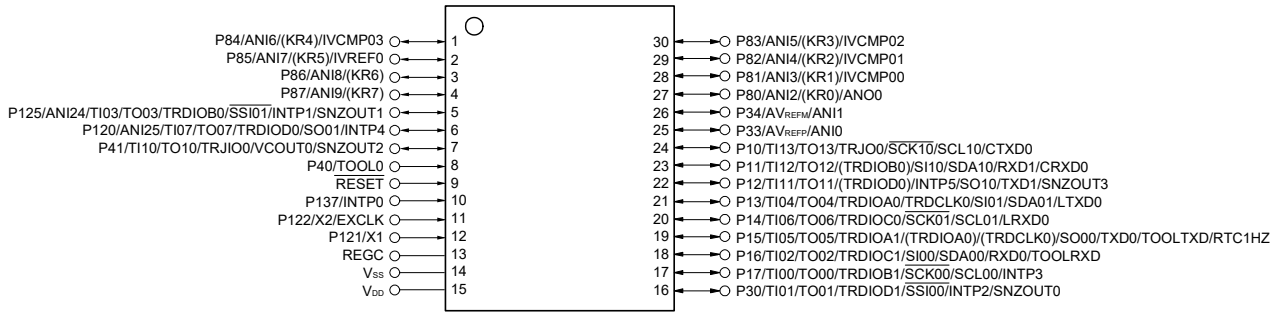
1.5.10 RL78/F14 Pin Configuration for 30-pin Products

<R> • RL78/F14: 30-pin Plastic LSSOP

Figure 1-32. RL78/F14 Pin Configuration for 30-pin Products



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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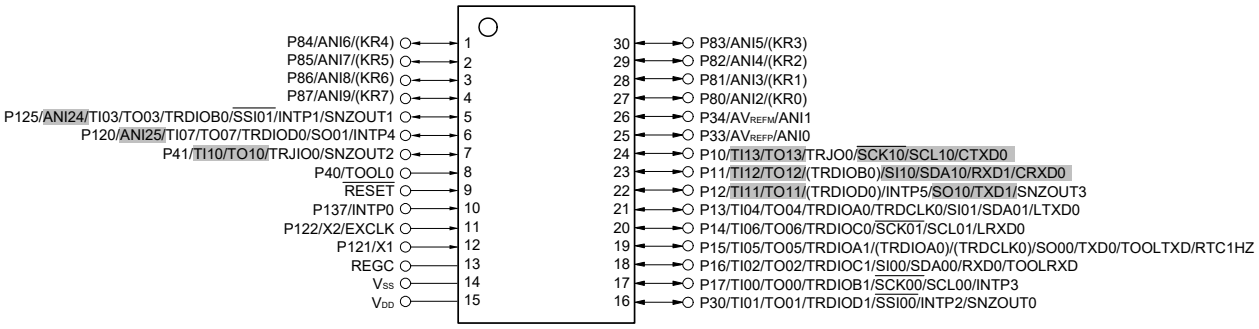
1.5.11 RL78/F13 Pin Configuration for 30-pin Products

<R>

- RL78/F13: 30-pin Plastic LSSOP

Figure 1-33. RL78/F13 Pin Configuration for 30-pin Products



Cautions 1. : Shaded pins are not available in the RL78/F13 (LIN incorporated) products (R5F10AAA, R5F10AAC, R5F10AAD, R5F10AAE).
2. The available pins and functions differ depending on the product. Refer to **CHAPTER 2 PIN FUNCTIONS** for details.
3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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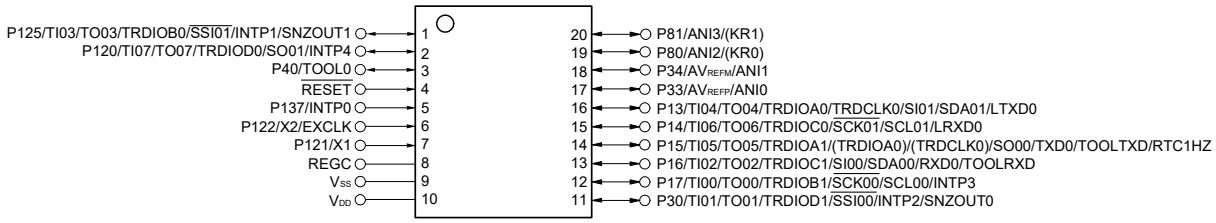
1.5.12 RL78/F13 Pin Configuration for 20-pin Products

<R> • RL78/F13: 20-pin Plastic LSSOP

Figure 1-34. RL78/F13 Pin Configuration for 20-pin Products



Caution Do not use the XT1 and XT2 pin functions in grade-Y products.

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1.6 Order Information

Tables 1-7 to 1-9 show the order information for RL78/F14, RL78/F13 (CAN and LIN incorporated), and RL78/F13 (LIN incorporated).

Table 1-7. Order Information for RL78/F14

<R>

Package	Device	Order Name
30-pin plastic LSSOP	Grade L	R5F10PADLSP, R5F10PADCLSP, R5F10PAELSP, R5F10PAECLSP
	Grade K	R5F10PADKSP, R5F10PADCKSP, R5F10PAEKSP, R5F10PAECKSP
	Grade Y	R5F10PADYSP, R5F10PADCYSP, R5F10PAEYSP, R5F10PAECYSP
32-pin plastic HVQFN, HWQFN	Grade L	R5F10PBDLNA, R5F10PBDCLNA, R5F10PBELNA, R5F10PBECLNA
	Grade K	R5F10PBDKNA, R5F10PBDCKNA, R5F10PBEKNA, R5F10PBECKNA
	Grade Y	R5F10PBDYNA, R5F10PBDCYNA, R5F10PBEYNA, R5F10PBECYNA
48-pin plastic LFQFP	Grade L	R5F10PGDCLFB, R5F10PGECLFB, R5F10PGFCLFB, R5F10PGGCLFB, R5F10PGHCLFB, R5F10PGJCLFB
	Grade K	R5F10PGDCKFB, R5F10PGECKFB, R5F10PGFCKFB, R5F10PGGCKFB, R5F10PGHCKFB, R5F10PGJCKFB
	Grade Y	R5F10PGDCYFB, R5F10PGECYFB, R5F10PGFCYFB, R5F10PGGCYFB, R5F10PGHCYFB, R5F10PGJCYFB
48-pin plastic HVQFN	Grade L	R5F10PGDLNA, R5F10PGELNA, R5F10PGFLNA, R5F10PGGLNA, R5F10PGHLNA, R5F10PGJLNA
	Grade K	R5F10PGDKNA, R5F10PGEKNA, R5F10PGFKNA, R5F10PGGKNA, R5F10PGHKNA, R5F10PGJKNA
	Grade Y	R5F10PGDYNA, R5F10PGEYNA, R5F10PGFYNA, R5F10PGGYNA, R5F10PGHYNA, R5F10PGJYNA
64-pin plastic LFQFP	Grade L	R5F10PLECLFB, R5F10PLFCLFB, R5F10PLGCLFB, R5F10PLHCLFB, R5F10PLJCLFB
	Grade K	R5F10PLECKFB, R5F10PLFCKFB, R5F10PLGCKFB, R5F10PLHCKFB, R5F10PLJCKFB
	Grade Y	R5F10PLECYFB, R5F10PLFCYFB, R5F10PLGCYFB, R5F10PLHCYFB, R5F10PLJCYFB
80-pin plastic LFQFP	Grade L	R5F10PMECLFB, R5F10PMFCLFB, R5F10PMGCLFB, R5F10PMHCLFB, R5F10PMJCLFB
	Grade K	R5F10PMECKFB, R5F10PMFCKFB, R5F10PMGCKFB, R5F10PMHCKFB, R5F10PMJCKFB
	Grade Y	R5F10PMECYFB, R5F10PMFCYFB, R5F10PMGCYFB, R5F10PMHCYFB, R5F10PMJCYFB
100-pin plastic LFQFP	Grade L	R5F10PPECLFB, R5F10PPFCLFB, R5F10PPGCLFB, R5F10PPHCLFB, R5F10PPJCLFB
	Grade K	R5F10PPECKFB, R5F10PPFCKFB, R5F10PPGCKFB, R5F10PPHCKFB, R5F10PPJCKFB
	Grade Y	R5F10PPECYFB, R5F10PPFCYFB, R5F10PPGCYFB, R5F10PPHCYFB, R5F10PPJCYFB

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Table 1-8. Order Information for RL78/F13 (CAN and LIN incorporated)

<R>

Package	Device	Order Name
30-pin plastic LSSOP	Grade L	R5F10BACLSP, R5F10BACCLSP, R5F10BADLSP, R5F10BADCLSP, R5F10BAELSP, R5F10BAECLSP, R5F10BAFLSP, R5F10BAFCLSP, R5F10BAGLSP, R5F10BAGCLSP
	Grade K	R5F10BACKSP, R5F10BACCKSP, R5F10BADKSP, R5F10BADCKSP, R5F10BAEKSP, R5F10BAECKSP, R5F10BAFKSP, R5F10BAFCKSP, R5F10BAGKSP, R5F10BAGCKSP
	Grade Y	R5F10BACYSP, R5F10BACCYSP, R5F10BADYSP, R5F10BADCYSP, R5F10BAEYSP, R5F10BAECYSP, R5F10BAFYSP, R5F10BAFCYSP, R5F10BAGYSP, R5F10BAGCYSP
32-pin plastic HVQFN, HWQFN	Grade L	R5F10BBCLNA, R5F10BBCCLNA, R5F10BBDLNA, R5F10BBDCLNA, R5F10BBELNA, R5F10BBECLNA, R5F10BBFLNA, R5F10BBFCLNA, R5F10BBGLNA, R5F10BBGCLNA
	Grade K	R5F10BBCKNA, R5F10BBCCKNA, R5F10BBDKNA, R5F10BBDCKNA, R5F10BBEKNA, R5F10BBECKNA, R5F10BBFKNA, R5F10BBFCKNA, R5F10BBGKNA, R5F10BBGCKNA
	Grade Y	R5F10BBCYNA, R5F10BBCCYNA, R5F10BBDYNA, R5F10BBDCYNA, R5F10BBEYNA, R5F10BBECYNA, R5F10BBFYNA, R5F10BBFCYNA, R5F10BBGYNA, R5F10BBGCYNA
48-pin plastic LFQFP	Grade L	R5F10BGCCLFB, R5F10BGDCLFB, R5F10BGECLFB, R5F10BGFCLFB, R5F10BGGCLFB
	Grade K	R5F10BGCCKFB, R5F10BGDCKFB, R5F10BGECKFB, R5F10BGFCKFB, R5F10BGGCKFB
	Grade Y	R5F10BGCCYFB, R5F10BGDCYFB, R5F10BGECYFB, R5F10BGFCYFB, R5F10BGGCYFB
48-pin plastic HVQFN	Grade L	R5F10BGCLNA, R5F10BGDLNA, R5F10BGELNA, R5F10BGFLNA, R5F10BGGLNA
	Grade K	R5F10BGCKNA, R5F10BGDKNA, R5F10BGEKNA, R5F10BGFKNA, R5F10BGGKNA
	Grade Y	R5F10BGCYNA, R5F10BGDYNA, R5F10BGEYNA, R5F10BGFYNA, R5F10BGGYNA
64-pin plastic LFQFP	Grade L	R5F10BLCCLFB, R5F10BLDCLFB, R5F10BLECLFB, R5F10BLFCLFB, R5F10BLGCLFB
	Grade K	R5F10BLCCKFB, R5F10BLDCKFB, R5F10BLECKFB, R5F10BLFCKFB, R5F10BLGCKFB
	Grade Y	R5F10BLCCYFB, R5F10BLDCYFB, R5F10BLECYFB, R5F10BLFCYFB, R5F10BLGCYFB
80-pin plastic LFQFP	Grade L	R5F10BMECLFB, R5F10BMFCLFB, R5F10BMGCLFB
	Grade K	R5F10BMECKFB, R5F10BMFCKFB, R5F10BMGCKFB
	Grade Y	R5F10BMECYFB, R5F10BMFCYFB, R5F10BMGCYFB

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Table 1-9. Order Information for RL78/F13 (LIN incorporated)

<R>

Package	Device	Order Name
20-pin plastic LSSOP	Grade L	R5F10A6ALSP, R5F10A6ACLSP, R5F10A6CLSP, R5F10A6CCLSP, R5F10A6DLSP, R5F10A6DCLSP, R5F10A6ELSP, R5F10A6ECLSP
	Grade K	R5F10A6AKSP, R5F10A6ACKSP, R5F10A6CKSP, R5F10A6CCKSP, R5F10A6DKSP, R5F10A6DCKSP, R5F10A6EKSP, R5F10A6ECKSP
	Grade Y	R5F10A6AYSP, R5F10A6ACYSP, R5F10A6CYSP, R5F10A6CCYSP, R5F10A6DYSP, R5F10A6DCYSP, R5F10A6EYSP, R5F10A6ECYSP
30-pin plastic LSSOP	Grade L	R5F10AAALSP, R5F10AAACLSP, R5F10AACLSP, R5F10AACCLSP, R5F10AADLSP, R5F10AADCLSP, R5F10AAELSP, R5F10AAECLSP
	Grade K	R5F10AAAKSP, R5F10AAACKSP, R5F10AACKSP, R5F10AACCKSP, R5F10AADKSP, R5F10AADCKSP, R5F10AAEKSP, R5F10AAECKSP
	Grade Y	R5F10AAAYSP, R5F10AAACYSP, R5F10AACYSP, R5F10AACCYSP, R5F10AADYSP, R5F10AADCYSP, R5F10AAEYSP, R5F10AAECYSP
32-pin plastic HVQFN, HWQFN	Grade L	R5F10ABALNA, R5F10ABACLNA, R5F10ABCLNA, R5F10ABCCLNA, R5F10ABDLNA, R5F10ABDCLNA, R5F10ABELNA, R5F10ABECLNA
	Grade K	R5F10ABAKNA, R5F10ABACKNA, R5F10ABCKNA, R5F10ABCCKNA, R5F10ABDKNA, R5F10ABDCKNA, R5F10ABEKNA, R5F10ABECKNA
	Grade Y	R5F10ABAYNA, R5F10ABACYNA, R5F10ABCYNA, R5F10ABCCYNA, R5F10ABDYNA, R5F10ABDCYNA, R5F10ABEYNA, R5F10ABECYNA
48-pin plastic LFQFP	Grade L	R5F10AGACLFB, R5F10AGCCLFB, R5F10AGDCLFB, R5F10AGECLFB, R5F10AGFCLFB, R5F10AGGCLFB
	Grade K	R5F10AGACKFB, R5F10AGCCKFB, R5F10AGDCKFB, R5F10AGECKFB, R5F10AGFCKFB, R5F10AGGCKFB
	Grade Y	R5F10AGACYFB, R5F10AGCCYFB, R5F10AGDCYFB, R5F10AGECYFB, R5F10AGFCYFB, R5F10AGGCYFB
48-pin plastic HVQFN	Grade L	R5F10AGALNA, R5F10AGCLNA, R5F10AGDLNA, R5F10AGELNA, R5F10AGFLNA, R5F10AGGLNA
	Grade K	R5F10AGAKNA, R5F10AGCKNA, R5F10AGDKNA, R5F10AGEKNA, R5F10AGFKNA, R5F10AGGKNA
	Grade Y	R5F10AGAYNA, R5F10AGCYNA, R5F10AGDYNA, R5F10AGEYNA, R5F10AGFYNA, R5F10AGGYNA
64-pin plastic LFQFP	Grade L	R5F10ALCCLFB, R5F10ALDCLFB, R5F10ALECLFB, R5F10ALFCLFB, R5F10ALGCLFB
	Grade K	R5F10ALCCKFB, R5F10ALDCKFB, R5F10ALECKFB, R5F10ALFCKFB, R5F10ALGCKFB
	Grade Y	R5F10ALCCYFB, R5F10ALDCYFB, R5F10ALECYFB, R5F10ALFCYFB, R5F10ALGCYFB
80-pin plastic LFQFP	Grade L	R5F10AMECLFB, R5F10AMFCLFB, R5F10AMGCLFB
	Grade K	R5F10AMECKFB, R5F10AMFCKFB, R5F10AMGCKFB
	Grade Y	R5F10AMECYFB, R5F10AMFCYFB, R5F10AMGCYFB

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2. PIN FUNCTIONS

2.1 Pin Function List

Pin I/O buffer power supplies depend on the product. Table 2-1 shows the relationship between these power supplies and the pins. EV_{DD} indicates EV_{DD0} and EV_{DD1}.

Table 2-1. Pin I/O Buffer Power Supplies

(1) 20-pin, 30-pin, 32-pin, and 48-pin products

Power Supply	Corresponding Pins
V_{DD}	All pins

(2) 64-pin products

Power Supply	Corresponding Pins
EV_{DD0}	• Port pins other than P33, P34, P80 to P87, P90 to P96 **Note**, P121 to P124, and P137
V_{DD}	• P33, P34, P80 to P87, P90 to P96 **Note**, P121 to P124, and P137 • Pins other than port pins

Note In R5F10PLE, R5F10PLF, R5F10BLC, R5F10BLD, R5F10BLE, R5F10BLF, R5F10BLG, R5F10ALF, and R5F10ALG, the power supply for P96 is EV_{DD0}. In R5F10ALC, R5F10ALD, and R5F10ALE, the power supply for P92 to P97 is EV_{DD0}.

(3) 80-pin products

Power Supply	Corresponding Pins
EV_{DD0}	• Port pins other than P33, P34, P80 to P87, P90 to P97 **Note**, P121 to P124, and P137
V_{DD}	• P33, P34, P80 to P87, P90 to P97 **Note**, P121 to P124, and P137 • Pins other than port pins

Note In R5F10PME, R5F10PMF, R5F10BME, R5F10BMF, R5F10BMG, R5F10AME, R5F10AMF, and R5F10AMG, the power supply for P96 and P97 is EV_{DD0}.

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(4) 100-pin products

Power Supply	Corresponding Pins
EV_{DD0}, EV_{DD1}	• Port pins other than P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, and P137
V_{DD}	• P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, and P137 • Pins other than port pins

The products are classified into the following five groups according to the product type, pin count, and code flash memory size.

Group A: RL78/F13 (LIN incorporated) products with 20, 30, 32, 48, or 64 pins and 16 Kbytes to 64 Kbytes of code flash memory

Group B: RL78/F13 (LIN incorporated) products with 48 or 64 pins and 96 Kbytes to 128 Kbytes of code flash memory or with 80 pins and 64 Kbytes to 128 Kbytes of code flash memory

Group C: RL78/F13 (CAN and LIN incorporated) products with 30, 32, 48, 64, or 80 pins and 32 Kbytes to 128 Kbytes of code flash memory

Group D: RL78/F14 products with 30, 32, 48, 64, or 80 pins and 48 Kbytes to 96 Kbytes of code flash memory

Group E: RL78/F14 products with 48, 64, or 80 pins and 128 Kbytes to 256 Kbytes of code flash memory or with 100 pins and 64 Kbytes to 256 Kbytes of code flash memory

This subchapter describes the 100-pin products of RL78/F14 and the 80-pin products of RL78/F13 (CAN and LIN incorporated) as examples.

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2.1.1 RL78/F14 100-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P01				(TI04)/(TO04)
P02				(TI06)/(TO06)
P03				(RTC1HZ)
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJO0/$\overline{\text{SCK10}}$/SCL10/LTXD1/CTXD0
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1/LRXD1/CRXD0
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				TI06/TO06/TRDIOC0/$\overline{\text{SCK01}}$/SCL01/LRXD0
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				TI00/TO00/TRDIOB1/$\overline{\text{SCK00}}$/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30, the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/$\overline{\text{SSI00}}$/INTP2/SNZOUT0
P31				TI14/TO14/STOPST/(INTP2)
P32				TI16/TO16/INTP7
P33			Analog input port	AV_{REFP}/ANI0
P34				AV_{REFM}/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/VCOUT0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P44				(TI07)/(TO07)
P45				(TI10)/(TO10)
P46				(TI12)/(TO12)
P47				INTP13
P50	I/O	Port 5 Input of P54 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50 and P52 to P54, the threshold level can be specified.	Input port	($\overline{\text{SSI01}}$)/(INTP3)
P51				(SO01)/INTP11
P52				($\overline{\text{SCK01}}$)/(STOPST)
P53				(SI01)/INTP10
P54				(TI11)/(TO11)/$\overline{\text{SSI10}}$
P55				(TI13)/(TO13)
P56				(TI15)/(TO15)/(SNZOUT1)
P57				(TI17)/(TO17)/(SNZOUT0)
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	($\overline{\text{SCK00}}$)/(SCL00)
P61				(SI00)/(SDA00)/(RXD0)
P62				(SO00)/(TXD0)/SCLA0
P63				($\overline{\text{SSI00}}$)/SDAA0
P64				(TI14)/(TO14)/(SNZOUT3)
P65				(TI16)/(TO16)/(SNZOUT2)
P66				(TI00)/(TO00)
P67				(TI02)/(TO02)

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

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(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. P70 to P74 can be set to analog input. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Analog input port	ANI26/KR0/TI15/TO15/INTP8/SI11/SDA11/SNZOUT4
P71				ANI27/KR1/TI17/TO17/INTP6/SCK11/SCL11/SNZOUT5
P72				ANI28/KR2/(CTXD0)/SO11/SNZOUT6
P73				ANI29/KR3/(CRXD0)/$\overline{\text{SSI11}}$/SNZOUT7
P74				ANI30/KR4/(SO10)/(TXD1)
P75			Input port	KR5/(SI10)/(RXD1)
P76				KR6/($\overline{\text{SCK10}}$)
P77				KR7/($\overline{\text{SSI10}}$)/INTP12
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2/ANO0
P81				ANI3/IVCMP00
P82				ANI4/IVCMP01
P83				ANI5/IVCMP02
P84				ANI6/IVCMP03
P85				ANI7/IVREF0
P86				ANI8
P87				ANI9
P90	I/O	Port 9 P90 to P97 can be set to analog input.	Analog input port	ANI10
P91				ANI11
P92				ANI12
P93				ANI13
P94				ANI14
P95				ANI15
P96				ANI16
P97				ANI17
P100	I/O	Port 10 P100 to P105 can be set to analog input. For P106 and P107, use of an on-chip pull-up resistor can be specified by a software setting. For input to P107, the threshold level can be specified.	Analog input port	ANI18
P101				ANI19
P102				ANI20
P103				ANI21
P104				ANI22
P105				ANI23
P106			Input port	(LTXD1)
P107				(LRXD1)
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120 and P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O		Analog input port	ANI24/TI03/TO03/TRDIOB0/$\overline{\text{SSI01}}$/INTP1/SNZOUT1
P126			Input port	(TI01)/(TO01)
P127				(TI03)/(TO03)
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0
P150	I/O	Port 15 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P150, P152, and P153, the threshold level can be specified.	Input port	($\overline{\text{SSI11}}$)
P151				(SO11)
P152				(SI11)
P153				($\overline{\text{SCK11}}$)
P154				(SNZOUT7)
P155				(SNZOUT6)
P156				(SNZOUT5)
P157				(SNZOUT4)

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

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2.1.2 RL78/F13 (CAN and LIN incorporated) 80-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P01				(TI04)/(TO04)
P02				(TI06)/(TO06)
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJO0/$\overline{\text{SCK10}}$/SCL10/CTXD0
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1/CRXD0
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				TI06/TO06/TRDIOC0/$\overline{\text{SCK01}}$/SCL01/LRXD0
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				TI00/TO00/TRDIOB1/$\overline{\text{SCK00}}$/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30, the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/$\overline{\text{SSI00}}$/INTP2/SNZOUT0
P31				STOPST/(INTP2)
P32				INTP7
P33			Analog input port	AV_{REFP}/ANI0
P34				AV_{REFM}/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P44				(TI07)/(TO07)
P45				(TI10)/(TO10)
P46				(TI12)/(TO12)
P47				—
P50	I/O	Port 5 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50 and P52 to P54, the threshold level can be specified. Input of P54 can be set to TTL input buffer.	Input port	($\overline{\text{SSI01}}$)/(INTP3)
P51				(SO01)/INTP11
P52				($\overline{\text{SCK01}}$)/(STOPST)
P53				(SI01)/INTP10
P54				(TI11)/(TO11)/$\overline{\text{SSI10}}$
P55				(TI13)/(TO13)
P56				(SNZOUT1)
P57				(SNZOUT0)
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	($\overline{\text{SCK00}}$)/(SCL00)
P61				(SI00)/(SDA00)/(RXD0)
P62				(SO00)/(TXD0)/SCLA0
P63				($\overline{\text{SSI00}}$)/SDAA0
P64				(SNZOUT3)
P65				(SNZOUT2)
P66				(TI00)/(TO00)
P67				(TI02)/(TO02)

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

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(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Input port	KR0/INTP8/SI11/SDA11/SNZOUT4
P71				KR1/INTP6/$\overline{\text{SCK11}}$/SCL11/SNZOUT5
P72				KR2/(CTXD0)/SO11/SNZOUT6
P73				KR3/(CRXD0)/$\overline{\text{SSI11}}$/SNZOUT7
P74				KR4/(SO10)/(TXD1)
P75				KR5/(SI10)/(RXD1)
P76				KR6/($\overline{\text{SCK10}}$)
P77				KR7/($\overline{\text{SSI10}}$)
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2
P81				ANI3
P82				ANI4
P83				ANI5
P84				ANI6
P85				ANI7
P86				ANI8
P87				ANI9
P90	I/O	Port 9 P90 to P97 can be set to analog input. For P96 and P97, use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI10
P91				ANI11
P92				ANI12
P93				ANI13
P94				ANI14
P95				ANI15
P96				ANI26
P97				ANI27
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120, P125, and P126, use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O		Analog input port	ANI24/TI03/TO03/TRDIOB0/$\overline{\text{SSI01}}$/INTP1/SNZOUT1
P126			Input port	(TI01)/(TO01)
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

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2.1.3 RL78/F13 (LIN incorporated) 80-pin products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P01				(TI04)/(TO04)
P02				(TI06)/(TO06)
P10	I/O	Port 1 Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P10 to P17 can be set to N-ch open-drain output. For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJO0/$\overline{\text{SCK10}}$/SCL10
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/RXD1
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/TXD1/SNZOUT3
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/SDA01/LTXD0
P14				TI06/TO06/TRDIOC0/$\overline{\text{SCK01}}$/SCL01/LRXD0
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/(TRDCLK0)/SO00/TXD0/TOOLTXD/RTC1HZ
P16				TI02/TO02/TRDIOC1/SI00/SDA00/RXD0/TOOLRXD
P17				TI00/TO00/TRDIOB1/$\overline{\text{SCK00}}$/SCL00/INTP3
P30	I/O	Port 3 Input of P30 can be set to TTL input buffer. P33 and P34 can be set to analog input. For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. For input to P30, the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/$\overline{\text{SSI00}}$/INTP2/SNZOUT0
P31				STOPST/(INTP2)
P32				INTP7
P33			Analog input port	AVREFP/ANI0
P34				AVREFM/ANI1
P40	I/O	Port 4 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P43, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P44				(TI07)/(TO07)
P45				(TI10)/(TO10)
P46				(TI12)/(TO12)
P47				—
P50	I/O	Port 5 Use of an on-chip pull-up resistor can be specified by a software setting. For input to P50 and P52 to P54, the threshold level can be specified. Input of P54 can be set to TTL input buffer.	Input port	($\overline{\text{SSI01}}$)/(INTP3)
P51				(SO01)/INTP11
P52				($\overline{\text{SCK01}}$)/(STOPST)
P53				(SI01)/INTP10
P54				(TI11)/(TO11)/$\overline{\text{SSI10}}$
P55				(TI13)/(TO13)
P56				(SNZOUT1)
P57				(SNZOUT0)
P60	I/O	Port 6 Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P60 to P63 can be set to N-ch open-drain output. For input to P60 to P63, the threshold level can be specified.	Input port	($\overline{\text{SCK00}}$)/(SCL00)
P61				(SI00)/(SDA00)/(RXD0)
P62				(SO00)/(TXD0)/SCLA0
P63				($\overline{\text{SSI00}}$)/SDAA0
P64				(SNZOUT3)
P65				(SNZOUT2)
P66				(TI00)/(TO00)
P67				(TI02)/(TO02)

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

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(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 Input of P70, P71, and P73 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. Output from P70 to P72 can be set to N-ch open-drain output. For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Input port	KR0/INTP8/SI11/SDA11/SNZOUT4
P71				KR1/INTP6/$\overline{\text{SCK11}}$/SCL11/SNZOUT5
P72				KR2/SO11/SNZOUT6
P73				KR3/$\overline{\text{SSI11}}$/SNZOUT7
P74				KR4/(SO10)/(TXD1)
P75				KR5/(SI10)/(RXD1)
P76				KR6/($\overline{\text{SCK10}}$)
P77				KR7/($\overline{\text{SSI10}}$)
P80	I/O	Port 8 P80 to P87 can be set to analog input.	Analog input port	ANI2
P81				ANI3
P82				ANI4
P83				ANI5
P84				ANI6
P85				ANI7
P86				ANI8
P87				ANI9
P90	I/O	Port 9 P90 to P97 can be set to analog input. For P96 and P97, use of an on-chip pull-up resistor can be specified by a software setting.	Analog input port	ANI10
P91				ANI11
P92				ANI12
P93				ANI13
P94				ANI14
P95				ANI15
P96				ANI26
P97				ANI27
P120	I/O	Port 12 Input of P125 can be set to TTL input buffer. P120 and P125 can be set to analog input. For P120, P125, and P126, use of an on-chip pull-up resistor can be specified by a software setting. Output from P120 can be set to N-ch open-drain output. For input to P125, the threshold level can be specified.	Analog input port	ANI25/TI07/TO07/TRDIOD0/SO01/INTP4
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O		Analog input port	ANI24/TI03/TO03/TRDIOB0/$\overline{\text{SSI01}}$/INTP1/SNZOUT1
P126			Input port	(TI01)/(TO01)
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	PCLBUZ0

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIOR).

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2.1.4 Pins for each product (pins other than port pins)

This subchapter shows the pins other than the ports shown in tables 2-2 to 2-4 for each product.
√ indicates the pin that is provided in the product and — indicates the pin that is not provided.

Table 2-2. List of RL78/F14 Pins Other than Port Pins (1/5)

Pin Function	I/O	Function	Pin Count					
			100-pin	80-pin	64-pin	48-pin	32-pin	30-pin
ANI0	Input	A/D converter analog input (V_{DD} connection)	√	√	√	√	√	√
ANI1	Input		√	√	√	√	√	√
ANI2	Input		√	√	√	√	√	√
ANI3	Input		√	√	√	√	√	√
ANI4	Input		√	√	√	√	√	√
ANI5	Input		√	√	√	√	√	√
ANI6	Input		√	√	√	√	√	√
ANI7	Input		√	√	√	√	√	√
ANI8	Input		√	√	√	√	—	√
ANI9	Input		√	√	√	√	—	√
ANI10	Input		√	√	√	√	—	—
ANI11	Input		√	√	√	√	—	—
ANI12	Input		√	√	√	√	—	—
ANI13	Input		√	√	√	—	—	—
ANI14	Input		√	√	√	—	—	—
ANI15	Input		√	√	√	—	—	—
ANI16	Input		√	√ Note 1	√ Note 1	—	—	—
ANI17	Input		√	√ Note 1	—	—	—	—
ANI18	Input		√	—	—	—	—	—
ANI19	Input		√	—	—	—	—	—
ANI20	Input		√	—	—	—	—	—
ANI21	Input		√	—	—	—	—	—
ANI22	Input		√	—	—	—	—	—
ANI23	Input		√	—	—	—	—	—
ANI24	Input	A/D converter analog input (EV_{DD} connection)	√	√	√	√	√	√
ANI25	Input		√	√	√	√	√	√
ANI26	Input		√	√	√	√ Note 1	—	—
ANI27	Input		√	√	—	√ Note 1	—	—
ANI28	Input		√	√ Note 1	—	√ Note 1	—	—
ANI29	Input		√	√ Note 1	—	—	—	—
ANI30	Input		√	√ Note 1	—	—	—	—
IVCMP00	Input	Comparator analog voltage input	√	√	√	√	√	√
IVCMP01	Input		√	√	√	√	√	√
IVCMP02	Input		√	√	√	√	√	√
IVCMP03	Input		√	√	√	√	√	√
IVREF0	Input	Comparator reference voltage input	√	√	√	√	√	√

Note 1. Provided only in Group E products.

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Table 2-2. List of RL78/F14 Pins Other than Port Pins (2/5)

Pin Function	I/O	Function	Pin Count					
			100-pin	80-pin	64-pin	48-pin	32-pin	30-pin
KR0	Input	Key interrupt input	√	√	√	√	√	√
KR1	Input		√	√	√	√	√	√
KR2	Input		√	√	√	√	√	√
KR3	Input		√	√	√	√	√	√
KR4	Input		√	√	√	√	√	√
KR5	Input		√	√	√	√	√	√
KR6	Input		√	√	√	√	—	√
KR7	Input		√	√	√	√	—	√
ANO0	Output	D/A converter output	√	√	√	√	√	√
VCOUT0	Output	Comparator output	√	√	√	√	√	√
TI00	Input	16-bit timer 00 input	√	√	√	√	√	√
TI01	Input	16-bit timer 01 input (8-bit mode available)	√	√	√	√	√	√
TI02	Input	16-bit timer 02 input	√	√	√	√	√	√
TI03	Input	16-bit timer 03 input (8-bit mode available)	√	√	√	√	√	√
TI04	Input	16-bit timer 04 input	√	√	√	√	√	√
TI05	Input	16-bit timer 05 input	√	√	√	√	√	√
TI06	Input	16-bit timer 06 input	√	√	√	√	√	√
TI07	Input	16-bit timer 07 input	√	√	√	√	√	√
TI10	Input	16-bit timer 10 input	√	√	√	√	√	√
TI11	Input	16-bit timer 11 input (8-bit mode available)	√	√	√	√	√	√
TI12	Input	16-bit timer 12 input	√	√	√	√	√	√
TI13	Input	16-bit timer 13 input (8-bit mode available)	√	√	√	√	√	√
TI14	Input	16-bit timer 14 input	√	√ Note 1	√ Note 1	√ Note 1	—	—
TI15	Input	16-bit timer 15 input	√	√ Note 1	√ Note 1	√ Note 1	—	—
TI16	Input	16-bit timer 16 input	√	√ Note 1	√ Note 1	√ Note 1	—	—
TI17	Input	16-bit timer 17 input	√	√ Note 1	√ Note 1	√ Note 1	—	—
TO00	Output	16-bit timer 00 output	√	√	√	√	√	√
TO01	Output	16-bit timer 01 output (8-bit mode available)	√	√	√	√	√	√
TO02	Output	16-bit timer 02 output	√	√	√	√	√	√
TO03	Output	16-bit timer 03 output (8-bit mode available)	√	√	√	√	√	√
TO04	Output	16-bit timer 04 output	√	√	√	√	√	√
TO05	Output	16-bit timer 05 output	√	√	√	√	√	√
TO06	Output	16-bit timer 06 output	√	√	√	√	√	√
TO07	Output	16-bit timer 07 output	√	√	√	√	√	√
TO10	Output	16-bit timer 10 output	√	√	√	√	√	√
TO11	Output	16-bit timer 11 output (8-bit mode available)	√	√	√	√	√	√
TO12	Output	16-bit timer 12 output	√	√	√	√	√	√
TO13	Output	16-bit timer 13 output (8-bit mode available)	√	√	√	√	√	√
TO14	Output	16-bit timer 14 output	√	√ Note 1	√ Note 1	√ Note 1	—	—
TO15	Output	16-bit timer 15 output	√	√ Note 1	√ Note 1	√ Note 1	—	—
TO16	Output	16-bit timer 16 output	√	√ Note 1	√ Note 1	√ Note 1	—	—
TO17	Output	16-bit timer 17 output	√	√ Note 1	√ Note 1	√ Note 1	—	—

Note 1. Provided only in Group E products.

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Table 2-2. List of RL78/F14 Pins Other than Port Pins (3/5)

Pin Function	I/O	Function	Pin Count					
			100-pin	80-pin	64-pin	48-pin	32-pin	30-pin
TRJIO0	I/O	Timer RJ input/output	√	√	√	√	√	√
TRJO0	Output	Timer RJ output	√	√	√	√	√	√
TRDCLK0	Input	Timer RD external clock input	√	√	√	√	√	√
TRDIOA0	I/O	Timer RD0 input/output	√	√	√	√	√	√
TRDIOB0	I/O		√	√	√	√	√	√
TRDIOC0	I/O		√	√	√	√	√	√
TRDIOD0	I/O		√	√	√	√	√	√
TRDIOA1	I/O	Timer RD1 input/output	√	√	√	√	√	√
TRDIOB1	I/O		√	√	√	√	√	√
TRDIOC1	I/O		√	√	√	√	√	√
TRDIOD1	I/O		√	√	√	√	√	√
RXD0	Input	Serial data input to UART0	√	√	√	√	√	√
RXD1	Input	Serial data input to UART1	√	√	√	√	√	√
TXD0	Output	Serial data output from UART0	√	√	√	√	√	√
TXD1	Output	Serial data output from UART1	√	√	√	√	√	√
SCLA0	I/O	Clock input/output for IICA0	√	√	√	√	√	—
SCL00	Output	Clock output from simplified I^2C	√	√	√	√	√	√
SCL01	Output		√	√	√	√	√	√
SCL10	Output		√	√	√	√	√	√
SCL11	Output		√	√	√	√	—	—
SDAA0	I/O	Serial data input/output for IICA0	√	√	√	√	√	—
SDA00	I/O	Serial data input/output for simplified I^2C	√	√	√	√	√	√
SDA01	I/O		√	√	√	√	√	√
SDA10	I/O		√	√	√	√	√	√
SDA11	I/O		√	√	√	√	—	—
$\overline{SCK00}$	I/O	Clock input/output for CSI00	√	√	√	√	√	√
$\overline{SCK01}$	I/O	Clock input/output for CSI01	√	√	√	√	√	√
$\overline{SCK10}$	I/O	Clock input/output for CSI10	√	√	√	√	√	√
$\overline{SCK11}$	I/O	Clock input/output for CSI11	√	√	√	√	—	—
SI00	Input	Serial data input to CSI00	√	√	√	√	√	√
SI01	Input	Serial data input to CSI01	√	√	√	√	√	√
SI10	Input	Serial data input to CSI10	√	√	√	√	√	√
SI11	Input	Serial data input to CSI11	√	√	√	√	—	—
SO00	Output	Serial data output from CSI00	√	√	√	√	√	√
SO01	Output	Serial data output from CSI01	√	√	√	√	√	√
SO10	Output	Serial data output from CSI10	√	√	√	√	√	√
SO11	Output	Serial data output from CSI11	√	√	√	√	—	—
$\overline{SSI00}$	Input	Slave select input to CSI00 (SPI00)	√	√	√	√	√	√
$\overline{SSI01}$	Input	Slave select input to CSI01 (SPI01)	√	√	√	√	√	√
$\overline{SSI10}$	Input	Slave select input to CSI10 (SPI10)	√	√	√	—	—	—
$\overline{SSI11}$	Input	Slave select input to CSI11 (SPI11)	√	√	√	√	—	—
CRXD0	Input	Serial data input to CAN	√	√	√	√	√	√
CTXD0	Output	Serial data output from CAN	√	√	√	√	√	√

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Table 2-2. List of RL78/F14 Pins Other than Port Pins (4/5)

Pin Function	I/O	Function	Pin Count					
			100-pin	80-pin	64-pin	48-pin	32-pin	30-pin
LRXD0	Input	Serial data input to LIN	√	√	√	√	√	√
LRXD1	Input		√	√ Note 1	√ Note 1	√ Note 1	—	—
LTXD0	Output	Serial data output from LIN	√	√	√	√	√	√
LTXD1	Output		√	√ Note 1	√ Note 1	√ Note 1	—	—
INTP0	Input	External interrupt input	√	√	√	√	√	√
INTP1	Input		√	√	√	√	√	√
INTP2	Input		√	√	√	√	√	√
INTP3	Input		√	√	√	√	√	√
INTP4	Input		√	√	√	√	√	√
INTP5	Input		√	√	√	√	√	√
INTP6	Input		√	√	√	√	—	—
INTP7	Input		√	√	√	√	—	—
INTP8	Input		√	√	√	√	—	—
INTP9	Input		√	√	√	√	—	—
INTP10	Input		√	√	√	—	—	—
INTP11	Input		√	√	√	—	—	—
INTP12	Input		√	√ Note 1	√ Note 1	—	—	—
INTP13	Input		√	√ Note 1	—	—	—	—
PCLBUZ0	Output	Clock output/buzzer output 0	√	√	√	√	—	—
RESOUT	Output	Reset output	√	√	√	√	—	—
STOPST	Output	STOP status output	√	√	√	√	—	—
SNZOUT0	Output	SNOOZE status output	√	√	√	√	√	√
SNZOUT1	Output		√	√	√	√	√	√
SNZOUT2	Output		√	√	√	√	√	√
SNZOUT3	Output		√	√	√	√	√	√
SNZOUT4	Output		√	√	√	√	—	—
SNZOUT5	Output		√	√	√	√	—	—
SNZOUT6	Output		√	√	√	√	—	—
SNZOUT7	Output		√	√	√	√	—	—
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√	√	√	√
EXCLK	Input	External clock input for main system clock	√	√	√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	√	√	—	—
X1	—	Resonator connection for main system clock	√	√	√	√	√	√
X2	—		√	√	√	√	√	√
XT1 Note 3	—	Resonator connection for subsystem clock	√	√	√	√	—	—
XT2 Note 3	—		√	√	√	√	—	—
$\overline{\text{RESET}}$	Input	External reset input	√	√	√	√	√	√
REGC	—	Regulator output stabilization capacitance connection for internal operation. Connect to Vss via the capacitor (0.47 to 1 μF).	√	√	√	√	√	√
V_{DD}	—	Positive power supply for the P33, P34, P80 to P87, P90 to P97 Note 2, P100 to P105, P121 to P124, P137, and $\overline{\text{RESET}}$ pins	√	√	√	√	√	√

Notes 1. Provided only in Group E products.

2. In products of Groups A to D, the positive power supply for P96 and P97 is EV_{DD0}.

3. Do not use the XT1 and XT2 pin functions in grade-Y products.

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Table 2-2. List of RL78/F14 Pins Other than Port Pins (5/5)

Pin Function	I/O	Function	Pin Count					
			100-pin	80-pin	64-pin	48-pin	32-pin	30-pin
EV_{DD0}	—	Positive power supply for the pins that are not connected to V_{DD}	√	√	√	—	—	—
EV_{DD1}	—		√	—	—	—	—	—
AV_{REFP}	Input	A/D converter reference voltage (+ side) input	√	√	√	√	√	√
AV_{REFM}	Input	A/D converter reference voltage (- side) input	√	√	√	√	√	√
V_{SS}	—	Ground potential for the P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, and $\overline{RESET}$ pins	√	√	√	√	√	√
EV_{SS0}	—	Ground potential for the pins that are not connected to V_{SS}	√	√	√	—	—	—
EV_{SS1}	—		√	—	—	—	—	—
TOOLRXD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√	√	√
TOOLTXD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√	√	√
TOOL0	I/O	Data input/output for flash memory programmer/debugger	√	√	√	√	√	√

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Table 2-3. List of RL78/F13 (CAN and LIN incorporated) Pins Other than Port Pins (1/4)

Pin Function	I/O	Function	Pin Count				
			80-pin	64-pin	48-pin	32-pin	30-pin
ANI0	Input	A/D converter analog input (V_{DD} connection)	√	√	√	√	√
ANI1	Input		√	√	√	√	√
ANI2	Input		√	√	√	√	√
ANI3	Input		√	√	√	√	√
ANI4	Input		√	√	√	√	√
ANI5	Input		√	√	√	√	√
ANI6	Input		√	√	√	√	√
ANI7	Input		√	√	√	√	√
ANI8	Input		√	√	√	—	√
ANI9	Input		√	√	√	—	√
ANI10	Input		√	√	√	—	—
ANI11	Input		√	√	√	—	—
ANI12	Input		√	√	√	—	—
ANI13	Input		√	√	—	—	—
ANI14	Input		√	√	—	—	—
ANI15	Input		√	√	—	—	—
ANI24	Input	A/D converter analog input (EV_{DD} connection)	√	√	√	√	√
ANI25	Input		√	√	√	√	√
ANI26	Input		√	√	—	—	—
ANI27	Input		√	—	—	—	—
KR0	Input	Key interrupt input	√	√	√	√	√
KR1	Input		√	√	√	√	√
KR2	Input		√	√	√	√	√
KR3	Input		√	√	√	√	√
KR4	Input		√	√	√	√	√
KR5	Input		√	√	√	√	√
KR6	Input		√	√	√	—	√
KR7	Input		√	√	√	—	√
TI00	Input	16-bit timer 00 input	√	√	√	√	√
TI01	Input	16-bit timer 01 input (8-bit mode available)	√	√	√	√	√
TI02	Input	16-bit timer 02 input	√	√	√	√	√
TI03	Input	16-bit timer 03 input (8-bit mode available)	√	√	√	√	√
TI04	Input	16-bit timer 04 input	√	√	√	√	√
TI05	Input	16-bit timer 05 input	√	√	√	√	√
TI06	Input	16-bit timer 06 input	√	√	√	√	√
TI07	Input	16-bit timer 07 input	√	√	√	√	√
TI10	Input	16-bit timer 10 input	√	√	√	√	√
TI11	Input	16-bit timer 11 input (8-bit mode available)	√	√	√	√	√
TI12	Input	16-bit timer 12 input	√	√	√	√	√
TI13	Input	16-bit timer 13 input (8-bit mode available)	√	√	√	√	√
TO00	Output	16-bit timer 00 output	√	√	√	√	√
TO01	Output	16-bit timer 01 output (8-bit mode available)	√	√	√	√	√

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Table 2-3. List of RL78/F13 (CAN and LIN incorporated) Pins Other than Port Pins (2/4)

Pin Function	I/O	Function	Pin Count				
			80-pin	64-pin	48-pin	32-pin	30-pin
TO02	Output	16-bit timer 02 output	√	√	√	√	√
TO03	Output	16-bit timer 03 output (8-bit mode available)	√	√	√	√	√
TO04	Output	16-bit timer 04 output	√	√	√	√	√
TO05	Output	16-bit timer 05 output	√	√	√	√	√
TO06	Output	16-bit timer 06 output	√	√	√	√	√
TO07	Output	16-bit timer 07 output	√	√	√	√	√
TO10	Output	16-bit timer 10 output	√	√	√	√	√
TO11	Output	16-bit timer 11 output (8-bit mode available)	√	√	√	√	√
TO12	Output	16-bit timer 12 output	√	√	√	√	√
TO13	Output	16-bit timer 13 output (8-bit mode available)	√	√	√	√	√
TRJIO0	I/O	Timer RJ input/output	√	√	√	√	√
TRJO0	Output	Timer RJ output	√	√	√	√	√
TRDCLK0	Input	Timer RD external clock input	√	√	√	√	√
TRDIOA0	I/O	Timer RD0 input/output	√	√	√	√	√
TRDIOB0	I/O		√	√	√	√	√
TRDIOC0	I/O		√	√	√	√	√
TRDIOD0	I/O		√	√	√	√	√
TRDIOA1	I/O	Timer RD1 input/output	√	√	√	√	√
TRDIOB1	I/O		√	√	√	√	√
TRDIOC1	I/O		√	√	√	√	√
TRDIOD1	I/O		√	√	√	√	√
RXD0	Input	Serial data input to UART0	√	√	√	√	√
RXD1	Input	Serial data input to UART1	√	√	√	√	√
TXD0	Output	Serial data output from UART0	√	√	√	√	√
TXD1	Output	Serial data output from UART1	√	√	√	√	√
SCLA0	I/O	Clock input/output for IICA0	√	√	√	√	—
SCL00	Output	Clock output from simplified I^2C	√	√	√	√	√
SCL01	Output		√	√	√	√	√
SCL10	Output		√	√	√	√	√
SCL11	Output		√	√	√	—	—
SDAA0	I/O	Serial data input/output for IICA0	√	√	√	√	—
SDA00	I/O	Serial data input/output for simplified I^2C	√	√	√	√	√
SDA01	I/O		√	√	√	√	√
SDA10	I/O		√	√	√	√	√
SDA11	I/O		√	√	√	—	—
$\overline{SCK00}$	I/O	Clock input/output for CSI00	√	√	√	√	√
$\overline{SCK01}$	I/O	Clock input/output for CSI01	√	√	√	√	√
$\overline{SCK10}$	I/O	Clock input/output for CSI10	√	√	√	√	√
$\overline{SCK11}$	I/O	Clock input/output for CSI11	√	√	√	—	—
SI00	Input	Serial data input to CSI00	√	√	√	√	√
SI01	Input	Serial data input to CSI01	√	√	√	√	√
SI10	Input	Serial data input to CSI10	√	√	√	√	√

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Table 2-3. List of RL78/F13 (CAN and LIN incorporated) Pins Other than Port Pins (3/4)

Pin Function	I/O	Function	Pin Count				
			80-pin	64-pin	48-pin	32-pin	30-pin
SI11	Input	Serial data input to CSI11	√	√	√	—	—
SO00	Output	Serial data output from CSI00	√	√	√	√	√
SO01	Output	Serial data output from CSI01	√	√	√	√	√
SO10	Output	Serial data output from CSI10	√	√	√	√	√
SO11	Output	Serial data output from CSI11	√	√	√	—	—
$\overline{\text{SSI00}}$	Input	Slave select input to CSI00 (SPI00)	√	√	√	√	√
$\overline{\text{SSI01}}$	Input	Slave select input to CSI01 (SPI01)	√	√	√	√	√
$\overline{\text{SSI10}}$	Input	Slave select input to CSI10 (SPI10)	√	√	—	—	—
$\overline{\text{SSI11}}$	Input	Slave select input to CSI11 (SPI11)	√	√	√	—	—
CRXD0	Input	Serial data input to CAN	√	√	√	√	√
CTXD0	Output	Serial data output from CAN	√	√	√	√	√
LRXD0	Input	Serial data input to LIN	√	√	√	√	√
LTXD0	Output	Serial data output from LIN	√	√	√	√	√
INTP0	Input	External interrupt input	√	√	√	√	√
INTP1	Input		√	√	√	√	√
INTP2	Input		√	√	√	√	√
INTP3	Input		√	√	√	√	√
INTP4	Input		√	√	√	√	√
INTP5	Input		√	√	√	√	√
INTP6	Input		√	√	√	—	—
INTP7	Input		√	√	√	—	—
INTP8	Input		√	√	√	—	—
INTP9	Input		√	√	√	—	—
INTP10	Input		√	√	—	—	—
INTP11	Input		√	√	—	—	—
PCLBUZ0	Output	Clock output/buzzer output 0	√	√	√	—	—
RESOUT	Output	Reset output	√	√	√	—	—
STOPST	Output	STOP status output	√	√	√	—	—
SNZOUT0	Output	SNOOZE status output	√	√	√	√	√
SNZOUT1	Output		√	√	√	√	√
SNZOUT2	Output		√	√	√	√	√
SNZOUT3	Output		√	√	√	√	√
SNZOUT4	Output		√	√	√	—	—
SNZOUT5	Output		√	√	√	—	—
SNZOUT6	Output		√	√	√	—	—
SNZOUT7	Output		√	√	√	—	—
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√	√	√
EXCLK	Input	External clock input for main system clock	√	√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	√	—	—
X1	—	Resonator connection for main system clock	√	√	√	√	√
X2	—		√	√	√	√	√

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Table 2-3. List of RL78/F13 (CAN and LIN incorporated) Pins Other than Port Pins (4/4)

Pin Function	I/O	Function	Pin Count				
			80-pin	64-pin	48-pin	32-pin	30-pin
XT1[Note]	—	Resonator connection for subsystem clock	√	√	√	—	—
XT2[Note]	—		√	√	√	—	—
$\overline{\text{RESET}}$	Input	External reset input	√	√	√	√	√
REGC	—	Regulator output stabilization capacitance connection for internal operation. Connect to Vss via the capacitor (0.47 to 1 μF).	√	√	√	√	√
V_{DD}	—	Positive power supply for the P33, P34, P80 to P87, P90 to P95, P121 to P124, P137, and $\overline{\text{RESET}}$ pins	√	√	√	√	√
EV_{DD0}	—	Positive power supply for the pins that are not connected to V_{DD}	√	√	—	—	—
AV_{REFP}	Input	A/D converter reference voltage (+ side) input	√	√	√	√	√
AV_{REFM}	Input	A/D converter reference voltage (- side) input	√	√	√	√	√
V_{SS}	—	Ground potential for the P33, P34, P80 to P87, P90 to P95, P121 to P124, P137, and $\overline{\text{RESET}}$ pins	√	√	√	√	√
EV_{SS0}	—	Ground potential for the pins that are not connected to V_{SS}	√	√	—	—	—
TOOLRXD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√	√
TOOLTXD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√	√
TOOL0	I/O	Data input/output for flash memory programmer/debugger	√	√	√	√	√

Note Do not use the XT1 and XT2 pin functions in grade-Y products.

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Table 2-4. List of RL78/F13 (LIN incorporated) Pins Other than Port Pins (1/4)

Pin Function	I/O	Function	Pin Count					
			80-pin	64-pin	48-pin	32-pin	30-pin	20-pin
ANI0	Input	A/D converter analog input (V_{DD} connection)	√	√	√	√	√	√
ANI1	Input		√	√	√	√	√	√
ANI2	Input		√	√	√	√	√	√
ANI3	Input		√	√	√	√	√	√
ANI4	Input		√	√	√	√	√	—
ANI5	Input		√	√	√	√	√	—
ANI6	Input		√	√	√	√	√	—
ANI7	Input		√	√	√	√	√	—
ANI8	Input		√	√	√	—	√	—
ANI9	Input		√	√	√	—	√	—
ANI10	Input		√	√	√	—	—	—
ANI11	Input		√	√	√	—	—	—
ANI12	Input		√	√ Note 1	√ Note 1	—	—	—
ANI13	Input		√	√ Note 1	—	—	—	—
ANI14	Input		√	√ Note 1	—	—	—	—
ANI15	Input		√	√ Note 1	—	—	—	—
ANI24	Input	A/D converter analog input (EV_{DD} connection)	√	√ Note 1	√ Note 1	—	—	—
ANI25	Input		√	√ Note 1	√ Note 1	—	—	—
ANI26	Input		√	√ Note 1	—	—	—	—
ANI27	Input		√	—	—	—	—	—
KR0	Input	Key interrupt input	√	√	√	√	√	√
KR1	Input		√	√	√	√	√	√
KR2	Input		√	√	√	√	√	—
KR3	Input		√	√	√	√	√	—
KR4	Input		√	√	√	√	√	—
KR5	Input		√	√	√	√	√	—
KR6	Input		√	√	√	—	√	—
KR7	Input		√	√	√	—	√	—
TI00	Input	16-bit timer 00 input	√	√	√	√	√	√
TI01	Input	16-bit timer 01 input (8-bit mode available)	√	√	√	√	√	√
TI02	Input	16-bit timer 02 input	√	√	√	√	√	√
TI03	Input	16-bit timer 03 input (8-bit mode available)	√	√	√	√	√	√
TI04	Input	16-bit timer 04 input	√	√	√	√	√	√
TI05	Input	16-bit timer 05 input	√	√	√	√	√	√
TI06	Input	16-bit timer 06 input	√	√	√	√	√	√
TI07	Input	16-bit timer 07 input	√	√	√	√	√	√
TI10	Input	16-bit timer 10 input	√	√ Note 1	√ Note 1	—	—	—
TI11	Input	16-bit timer 11 input (8-bit mode available)	√	√ Note 1	√ Note 1	—	—	—
TI12	Input	16-bit timer 12 input	√	√ Note 1	√ Note 1	—	—	—
TI13	Input	16-bit timer 13 input (8-bit mode available)	√	√ Note 1	√ Note 1	—	—	—

Note 1. Provided only in the products with 96 Kbytes or 128 Kbytes of ROM.

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Table 2-4. List of RL78/F13 (LIN incorporated) Pins Other than Port Pins (2/4)

Pin Function	I/O	Function	Pin Count					
			80-pin	64-pin	48-pin	32-pin	30-pin	20-pin
TO00	Output	16-bit timer 00 output	√	√	√	√	√	√
TO01	Output	16-bit timer 01 output (8-bit mode available)	√	√	√	√	√	√
TO02	Output	16-bit timer 02 output	√	√	√	√	√	√
TO03	Output	16-bit timer 03 output (8-bit mode available)	√	√	√	√	√	√
TO04	Output	16-bit timer 04 output	√	√	√	√	√	√
TO05	Output	16-bit timer 05 output	√	√	√	√	√	√
TO06	Output	16-bit timer 06 output	√	√	√	√	√	√
TO07	Output	16-bit timer 07 output	√	√	√	√	√	√
TO10	Output	16-bit timer 10 output	√	√ Note 1	√ Note 1	—	—	—
TO11	Output	16-bit timer 11 output (8-bit mode available)	√	√ Note 1	√ Note 1	—	—	—
TO12	Output	16-bit timer 12 output	√	√ Note 1	√ Note 1	—	—	—
TO13	Output	16-bit timer 13 output (8-bit mode available)	√	√ Note 1	√ Note 1	—	—	—
TRJIO0	I/O	Timer RJ input/output	√	√	√	√	√	—
TRJO0	Output	Timer RJ output	√	√	√	√	√	—
TRDCLK0	Input	Timer RD external clock input	√	√	√	√	√	√
TRDIOA0	I/O	Timer RD0 input/output	√	√	√	√	√	√
TRDIOB0	I/O		√	√	√	√	√	√
TRDIOC0	I/O		√	√	√	√	√	√
TRDIOD0	I/O		√	√	√	√	√	√
TRDIOA1	I/O	Timer RD1 input/output	√	√	√	√	√	√
TRDIOB1	I/O		√	√	√	√	√	√
TRDIOC1	I/O		√	√	√	√	√	√
TRDIOD1	I/O		√	√	√	√	√	√
RXD0	Input	Serial data input to UART0	√	√	√	√	√	√
RXD1	Input	Serial data input to UART1	√	√ Note 1	√ Note 1	—	—	—
TXD0	Output	Serial data output from UART0	√	√	√	√	√	√
TXD1	Output	Serial data output from UART1	√	√ Note 1	√ Note 1	—	—	—
SCLA0	I/O	Clock input/output for IICA0	√	√ Note 1	√ Note 1	—	—	—
SCL00	Output	Clock output from simplified I^2C	√	√	√	√	√	√
SCL01	Output		√	√	√	√	√	√
SCL10	Output		√	√ Note 1	√ Note 1	—	—	—
SCL11	Output		√	√ Note 1	√ Note 1	—	—	—
SDAA0	I/O	Serial data input/output for IICA0	√	√ Note 1	√ Note 1	—	—	—
SDA00	I/O	Serial data input/output for simplified I^2C	√	√	√	√	√	√
SDA01	I/O		√	√	√	√	√	√
SDA10	I/O		√	√ Note 1	√ Note 1	—	—	—
SDA11	I/O		√	√ Note 1	√ Note 1	—	—	—
$\overline{SCK00}$	I/O	Clock input/output for CSI00	√	√	√	√	√	√
$\overline{SCK01}$	I/O	Clock input/output for CSI01	√	√	√	√	√	√

Note 1. Provided only in the products with 96 Kbytes or 128 Kbytes of ROM.

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Table 2-4. List of RL78/F13 (LIN incorporated) Pins Other than Port Pins (3/4)

Pin Function	I/O	Function	Pin Count					
			80-pin	64-pin	48-pin	32-pin	30-pin	20-pin
$\overline{\text{SCK10}}$	I/O	Clock input/output for CSI10	√	√ Note 1	√ Note 1	—	—	—
$\overline{\text{SCK11}}$	I/O	Clock input/output for CSI11	√	√ Note 1	√ Note 1	—	—	—
SI00	Input	Serial data input to CSI00	√	√	√	√	√	√
SI01	Input	Serial data input to CSI01	√	√	√	√	√	√
SI10	Input	Serial data input to CSI10	√	√ Note 1	√ Note 1	—	—	—
SI11	Input	Serial data input to CSI11	√	√ Note 1	√ Note 1	—	—	—
SO00	Output	Serial data output from CSI00	√	√	√	√	√	√
SO01	Output	Serial data output from CSI01	√	√	√	√	√	√
SO10	Output	Serial data output from CSI10	√	√ Note 1	√ Note 1	—	—	—
SO11	Output	Serial data output from CSI11	√	√ Note 1	√ Note 1	—	—	—
$\overline{\text{SSI00}}$	Input	Slave select input to CSI00 (SPI00)	√	√	√	√	√	√
$\overline{\text{SSI01}}$	Input	Slave select input to CSI01 (SPI01)	√	√	√	√	√	√
$\overline{\text{SSI10}}$	Input	Slave select input to CSI10 (SPI10)	√	√ Note 1	—	—	—	—
$\overline{\text{SSI11}}$	Input	Slave select input to CSI11 (SPI11)	√	√ Note 1	√ Note 1	—	—	—
LRXD0	Input	Serial data input to LIN	√	√	√	√	√	√
LTXD0	Output	Serial data output from LIN	√	√	√	√	√	√
INTP0	Input	External interrupt input	√	√	√	√	√	√
INTP1	Input		√	√	√	√	√	√
INTP2	Input		√	√	√	√	√	√
INTP3	Input		√	√	√	√	√	√
INTP4	Input		√	√	√	√	√	√
INTP5	Input		√	√	√	√	√	—
INTP6	Input		√	√	√	—	—	—
INTP7	Input		√	√	√	—	—	—
INTP8	Input		√	√ Note 1	√ Note 1	—	—	—
INTP9	Input		√	√ Note 1	√ Note 1	—	—	—
INTP10	Input		√	√ Note 1	—	—	—	—
INTP11	Input		√	√ Note 1	—	—	—	—
PCLBUZ0	Output	Clock output/buzzer output 0	√	√	√	—	—	—
RESOUT	Output	Reset output	√	√	√	—	—	—
STOPST	Output	STOP status output	√	√	√	—	—	—
SNZOUT0	Output	SNOOZE status output	√	√	√	√	√	√
SNZOUT1	Output		√	√	√	√	√	√
SNZOUT2	Output		√	√	√	√	√	—
SNZOUT3	Output		√	√	√	√	√	—
SNZOUT4	Output		√	√	√	—	—	—
SNZOUT5	Output		√	√	√	—	—	—
SNZOUT6	Output		√	√	√	—	—	—
SNZOUT7	Output		√	√	√	—	—	—
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√	√	√	√

Note 1. Provided only in the products with 96 Kbytes or 128 Kbytes of ROM.

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Table 2-4. List of RL78/F13 (LIN incorporated) Pins Other than Port Pins (4/4)

Pin Function	I/O	Function	Pin Count					
			80-pin	64-pin	48-pin	32-pin	30-pin	20-pin
EXCLK	Input	External clock input for main system clock	√	√	√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	√	—	—	—
X1	—	Resonator connection for main system clock	√	√	√	√	√	√
X2	—		√	√	√	√	√	√
XT1[Note]	—	Resonator connection for subsystem clock	√	√	√	—	—	—
XT2[Note]	—		√	√	√	—	—	—
$\overline{\text{RESET}}$	Input	External reset input	√	√	√	√	√	√
REGC	—	Regulator output stabilization capacitance connection for internal operation. Connect to Vss via the capacitor (0.47 to 1 μF).	√	√	√	√	√	√
V_{DD}	—	Positive power supply for the P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, and $\overline{\text{RESET}}$ pins	√	√	√	√	√	√
EV_{DD0}	—	Positive power supply for the pins that are not connected to V_{DD}	√	√	—	—	—	—
AV_{REFP}	Input	A/D converter reference voltage (+ side) input	√	√	√	√	√	√
AV_{REFM}	Input	A/D converter reference voltage (- side) input	√	√	√	√	√	√
V_{SS}	—	Ground potential for the P33, P34, P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137, and $\overline{\text{RESET}}$ pins	√	√	√	√	√	√
EV_{SS0}	—	Ground potential for the pins that are not connected to V_{SS}	√	√	—	—	—	—
TOOLRXD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√	√	√
TOOLTXD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√	√	√
TOOL0	I/O	Data input/output for flash memory programmer/debugger	√	√	√	√	√	√

Note Do not use the XT1 and XT2 pin functions in grade-Y products.

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3. ELECTRICAL SPECIFICATIONS (GRADE L)

Cautions 1. RL78/F13 and RL78/F14 have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

3. The pins mounted depending on the product. For details, refer to 1.5 Pin Configurations and 2.1 Pin Function List.

4. The products are classified into the following five groups according to the product type, pin count, and code flash memory size. In this chapter, the products are referred to by group names depending on the content. In this case, refer to the following classification.

Group A: RL78/F13 (LIN incorporated) products with 20, 30, 32, 48, or 64 pins and 16 Kbytes to 64 Kbytes of code flash memory

Group B: RL78/F13 (LIN incorporated) products with 48 or 64 pins and 96 Kbytes to 128 Kbytes of code flash memory or with 80 pins and 64 Kbytes to 128 Kbytes of code flash memory

Group C: RL78/F13 (CAN and LIN incorporated) products with 30, 32, 48, 64, or 80 pins and 32 Kbytes to 128 Kbytes of code flash memory

Group D: RL78/F14 products with 30, 32, 48, 64, or 80 pins and 48 Kbytes to 96 Kbytes of code flash memory

Group E: RL78/F14 products with 48, 64, or 80 pins and 128 Kbytes to 256 Kbytes of code flash memory or with 100 pins and 64 Kbytes to 256 Kbytes of code flash memory

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3.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	V_{SS}		-0.5 to +0.3	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD}+0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 4], P106, P107, P120, P125 to P127, P140, P150 to P157	-0.3 to EV_{DD0}+0.3 and -0.3 to V_{DD}+0.3[Note 2]	V
	V_{I2}	P33, P34, P80 to P87, P90 to P97[Note 4], P100 to P105, P121 to P124, P137, $\overline{\text{RESET}}$	-0.3 to V_{DD}+0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 4], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	-0.3 to EV_{DD0}+0.3 and -0.3 to V_{DD}+0.3[Note 2]	V
	V_{O2}	P33, P34, P80 to P87, P90 to P97[Note 4], P100 to P105	-0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI1}	ANI24 to ANI30	-0.3 to EV_{DD0}+0.3 and -0.3 to $AV_{REF(+)}$+0.3[Notes 2, 3]	V
	V_{AI2}	ANI0 to ANI23	-0.3 to V_{DD}+0.3 and -0.3 to $AV_{REF(+)}$+0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. For pins to be used in A/D conversion, the voltage should not exceed the value $AV_{REF(+)}$ + 0.3.

4. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	-40	mA
		Total of all pins -170 mA	P01, P02, P40 to P47, P92 to P97[Note], P120, P125 to P127, P150 to P153	-70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	-100	mA
	I_{OH2}	Per pin	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	40	mA
		Total of all pins 170 mA	P01, P02, P40 to P47, P92 to P97[Note], P120, P125 to P127, P150 to P153	70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	100	mA
	I_{OL2}	Per pin	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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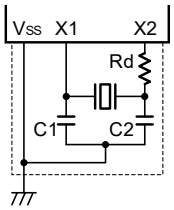
3.2 Oscillator Characteristics

3.2.1 Main System Clock Oscillator Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

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3.2.2 On-chip Oscillator Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Note]	f_{IH}		1		64	MHz
High-speed on-chip oscillator clock frequency accuracy	-		-2		+2	%
Low-speed on-chip oscillator clock frequency	f_{IL}, f_{WDT}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	-		-15		+15	%

Note High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/020C2H) and bits 0 to 2 of the HOCODIV register.

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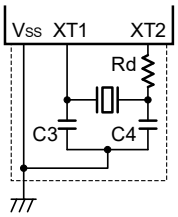
3.2.3 Subsystem Clock Oscillator Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Recommended Circuit	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})	2.7 V ≤ V_{DD} ≤ 5.5 V	29.0	32.768	35.0	kHz

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption and thus required to be adequately evaluated on the system. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

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3.2.4 PLL Circuit Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
PLL input enable clock frequency[Note 1]	f_{PLLI}	PLLMUL = 0	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
		PLLMUL = 1	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
PLL output frequency (center value)	f_{PLL}	PLLMUL = 0	PLLDIV0 = 0	f_{PLLI} × 12/2			MHz
			PLLDIV0 = 1	f_{PLLI} × 12/4			MHz
		PLLMUL = 1	PLLDIV0 = 0	f_{PLLI} × 16/2			MHz
			PLLDIV0 = 1	f_{PLLI} × 16/4			MHz
Long-term jitter[Notes 2, 3]	t_{LJ}	f_{PLL} = 24 MHz (480 counts)		-2		+2	ns
		f_{PLL} = 32 MHz (640 counts)		-2		+2	ns
		f_{PLL} = 48 MHz (960 counts)		-2		+2	ns
		f_{PLL} = 64 MHz (1280 counts)		-2		+2	ns

Notes 1. If the high-speed on-chip oscillator clock is to be selected as the PLL input clock, the minimum and maximum values will reflect the range of accuracy of the oscillation frequency by the high-speed on-chip oscillator clock.

2. Guaranteed by design, but not tested before shipment.

3. Indicates 20 μs.

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3.3 DC Characteristics

3.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **2 PIN FUNCTIONS**.

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 3], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-5.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-3.0	mA
		Per pin for P10, P12, P14, P30,P120,P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-0.6	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-0.2	mA
		Total of P01, P02, P40 to P47, P92 to P97[Note 3], P120, P125 to P127, P150 to P153 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
		Total of P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-50.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-29.0	mA
	I_{OH2}	Per pin for P33, P34, P80 to P87, P90 to P97[Note 3], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V			-0.1	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	2.7 V ≤ V_{DD} ≤ 5.5 V			-2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from pins EV_{DD0}, EV_{DD1} and V_{DD} to an output pin.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode. P10 to P12 and P70 to P72 of the Group A products do not support N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 3], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			8.5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			4.0	mA
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			0.59	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			0.07	mA
		Total of P01, P02, P40 to P47, P92 to P97[Note 3], P120, P125 to P127, P150 to P153 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
		Total of P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			45.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			65.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			50.0	mA
	I_{OL2}	Per pin for P33, P34, P80 to P87, P90 to P97[Note 3], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V			0.4	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	2.7 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows to the EV_{SS0}, EV_{SS1} and V_{SS} pins from an output pin.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.65 EV_{DD0}		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.7 EV_{DD0}		EV_{DD0} Note 1	V
	V_{IH2}	P10, P11, P13, P14, P16, P17, P30, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152, P153 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.8 EV_{DD0}		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.85 EV_{DD0}		EV_{DD0} Note 1	V
	V_{IH3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0} Note 1	V
	V_{IH4} Note 2	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.85 V_{DD}		V_{DD}	V
	V_{IH5}	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.65 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.7 V_{DD}		V_{DD}	V
	V_{IH6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.8 V_{DD}		V_{DD}	V

Notes 1. The maximum value of V_{IH} of the pins P10 to P17, P60 to P63, P70 to P72, and P120 is EV_{DD0}, even in N-ch open-drain mode.

2. P92 to P96 of the Group A products are fixed to Schmitt 1 mode.
P96 and P97 of the Group B, C, and D products are fixed to Schmitt 1 mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.35 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.3 EV_{DD0}	V
	V_{IL2}	P10, P11, P13, P14, P16, P17, P30, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152, P153 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.5 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.4 EV_{DD0}	V
	V_{IL3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
	V_{IL4} Note	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.5 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.4 V_{DD}	V
	V_{IL5}	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.35 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.3 V_{DD}	V
	V_{IL6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V

Note P92 to P96 of the Group A products are fixed to Schmitt 1 mode.
P96 and P97 of the Group B, C, and D products are fixed to Schmitt 1 mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -5.0 mA	EV_{DD0}-0.9			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0}-0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.0 mA	EV_{DD0}-0.5			V
	V_{OH2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V I_{OH2} = -100 μA	V_{DD}-0.5			V
	V_{OH3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = -0.6 mA	EV_{DD0}-0.8			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = -0.2 mA	EV_{DD0}-0.5			V
Output voltage, low	V_{OL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.6 mA			0.8	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.07 mA			0.5	V

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (6/6)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{DD0}				1	μA
	I_{LIH2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105, P137, $\overline{RESET}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{SS0}				-1	μA
	I_{LIL2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105, P137, $\overline{RESET}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97, P100 to P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{SS0}, in input port		10	20	100	kΩ

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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3.3.2 Supply Current Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/3)

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 64 MHz	f_{CLK} = 32 MHz Notes 3, 4		6.5	14.0	mA
					f_{IH} = 32 MHz	f_{CLK} = f_{IH} Notes 3, 4		6.1	13.0	mA
					f_{IH} = 1 MHz	f_{CLK} = f_{IH} Notes 3, 4		1.0	2.5	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		4.2	9.0	mA
					f_{MX} = 1 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.9	2.5	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 64 MHz, f_{MX} = 8 MHz	f_{CLK} = 32 MHz Notes 3, 6		6.4	14.0	mA
					f_{PLL} = 32 MHz, f_{MX} = 8 MHz	f_{CLK} = 32 MHz Notes 3, 6		6.3	13.5	mA
					f_{PLL} = 32 MHz, f_{MX} = 4 MHz	f_{CLK} = 32 MHz Notes 3, 6		6.1	13.0	mA
				Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7				
					Groups A to D			6.0	50.0	μA
					Group E			6.0	70.0	μA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8				
					Groups A to D			3.0	40.0	μA
					Group E			3.0	60.0	μA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

Remarks 1. f_{MX}: High-speed system clock frequency

2. f_{SUB}: Subsystem clock frequency

3. f_{PLL}: PLL clock frequency

4. f_{IH}: High-speed on-chip oscillator clock frequency

5. f_{IL}: Low-speed on-chip oscillator clock frequency

6. f_{CLK}: CPU/peripheral hardware clock frequency

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 3]	I_{DD2}	HALT mode[Note 2]	High-speed on-chip oscillator clock operation	f_{IH} = 64 MHz	f_{CLK} = 32 MHz [Note 5]		1.2	10.0	mA
				f_{IH} = 32 MHz	f_{CLK} = f_{IH}[Note 5]		1.0	9.0	mA
				f_{IH} = 1 MHz	f_{CLK} = f_{IH}[Note 5]		0.3	1.5	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX}[Note 6]		0.6	6.0	mA
				f_{MX} = 1 MHz	f_{CLK} = f_{MX}[Note 6]		0.2	1.5	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 64 MHz, f_{MX} = 8 MHz	f_{CLK} = 32 MHz [Note 7]		1.1	10.0	mA
				f_{PLL} = 32 MHz, f_{MX} = 8 MHz	f_{CLK} = 32 MHz [Note 7]		1.0	9.5	mA
				f_{PLL} = 32 MHz, f_{MX} = 4 MHz	f_{CLK} = 32 MHz [Note 7]		0.8	9.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB}[Note 8]				
				Groups A to D			0.7	45.0	μA
				Group E			0.7	65.0	
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL}[Note 9]				
				Groups A to D			0.7	35.0	μA
				Group E			0.7	55.0	
	I_{DD3}	STOP mode[Note 4]	T_A = +25°C	Groups A to D			0.5		μA
				Group E			0.5		
			T_A = +50°C	Groups A to D				2.5	
				Group E				4.5	
			T_A = +70°C	Groups A to D				4.5	
				Group E				8.0	
			T_A = +105°C	Groups A to D				30.0	
				Group E				50.0	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

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8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency
2. f_{SUB}: Subsystem clock frequency
3. f_{PLL}: PLL clock frequency
4. f_{IH}: High-speed on-chip oscillator clock frequency
5. f_{IL}: Low-speed on-chip oscillator clock frequency
6. f_{CLK}: CPU/peripheral hardware clock frequency

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 2]	I_{SNOZ}	SNOOZE mode	A/D converter operation	During mode transition			1.0	1.2	mA
				During conversion	Low-voltage mode AV_{REFP} = V_{DD} = 5.0 V		2.1	2.5	mA
			DTC operation				4.5		mA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. The values below the MAX. column include the STOP leakage current.

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
		When internal reference voltage is selected Note 5			75.0		μA
LVD operating current	I_{LVD} Note 4				0.08		μA
Temperature sensor operating current	I_{TMPS}				75.0		μA
D/A converter operating current	I_{DAC}	Per channel			0.8	1.5	mA
Comparator operating current	I_{CMP}				50.0		μA
BGO operating current	I_{BGO} Note 6				2.50	12.20	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

5. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

6. Current increased by the BGO operation. The current value is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in operation mode or HALT mode.

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3.4 AC Characteristics

3.4.1 Basic Operation

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	High-speed on-chip oscillator clock operation		0.03125		1	μs
		High-speed system clock operation		0.05		1	μs
		PLL clock operation		0.03125		1	μs
		Subsystem clock operation		28.5	30.5	34.5	μs
		Low-speed on-chip oscillator clock operation			66.6		μs
		In self programming mode		0.03125		1	μs
CPU/peripheral hardware clock frequency	f_{CLK}			0.03125		66.6	μs
External system clock frequency	f_{EX}			1.0		20.0	MHz
	f_{EXS}			29		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}			$1/f_{MCK}+10$			ns
TO00 to TO07, TO10 to TO17 output frequency	f_{TO}	All TO pins, Normal slew rate, C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		TO01, TO06, TO07, TO11, TO13 only, Special slew rate, C = 30 pF				2	MHz
PCLBUZ0 output frequency	f_{PCL}	Normal slew rate C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		Special slew rate C = 30 pF				2	MHz
Timer RJ input cycle	t_C	TRJIO0		100			ns
Timer RJ input high-level width, low-level width	t_{WH}, t_{WL}	TRJIO0		40			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP13 Note		1			μs
KR0 to KR7 key interrupt input low-level width	t_{KR}			250			ns
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

Note Pins $\overline{RESET}$, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

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(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

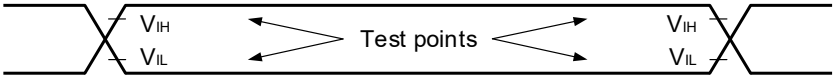
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Port output rise time, port output fall time	t_{RO}, t_{FO}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P96, P97, P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			25	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V		25 Note	60	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			100	ns

Note T_A = +25°C, EV_{DD0} = 5.0 V

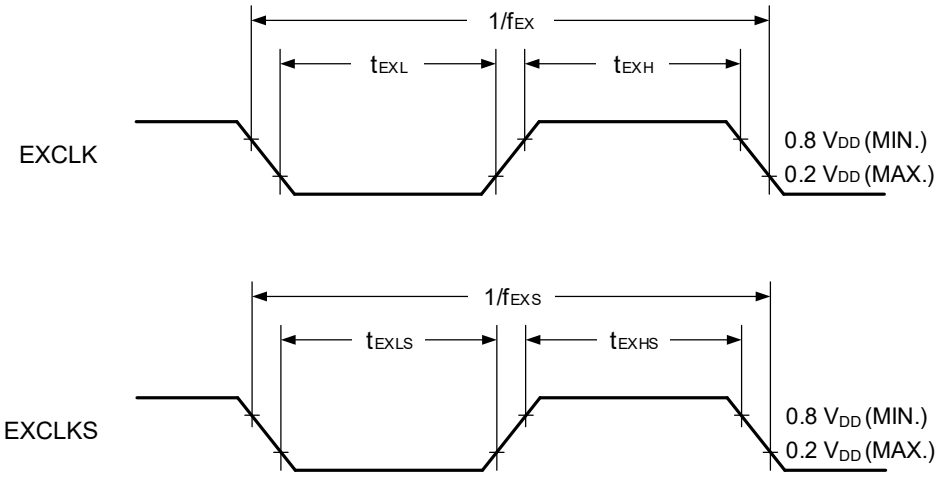
Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

AC Timing Test Points



External System Clock Timing



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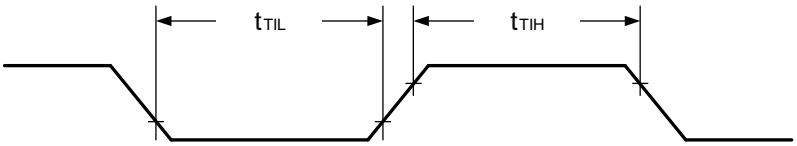
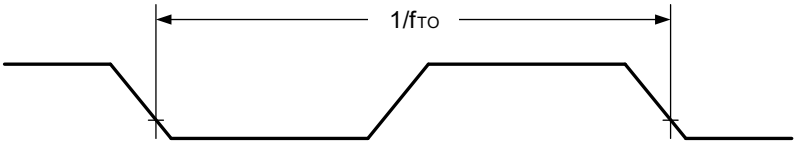
TI/TO Timing

TI00 to TI07, TI10 to TI17

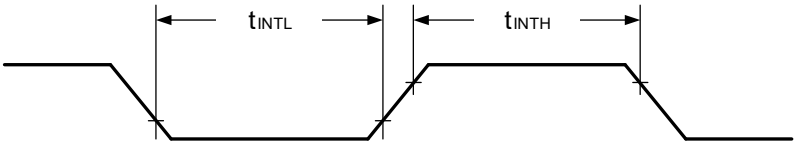


TO00 to TO07, TO10 to TO17



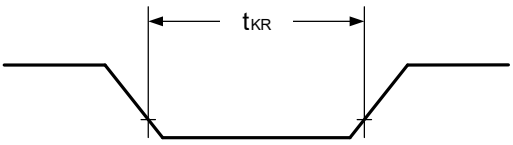
Interrupt Request Input Timing

INTP0 to INTP13



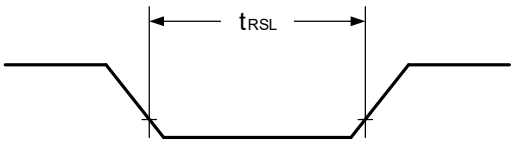
Key Interrupt Input Timing

KR0 to KR7



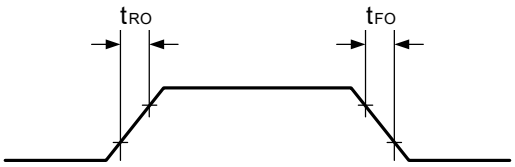
$\overline{\text{RESET}}$ Input Timing

$\overline{\text{RESET}}$



Output Rising and Falling Timing

Output pin



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3.5 Peripheral Functions Characteristics

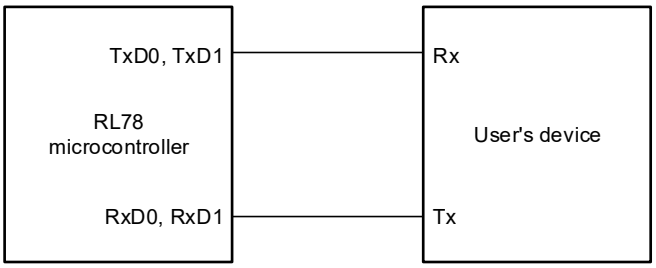
3.5.1 Serial Array Unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

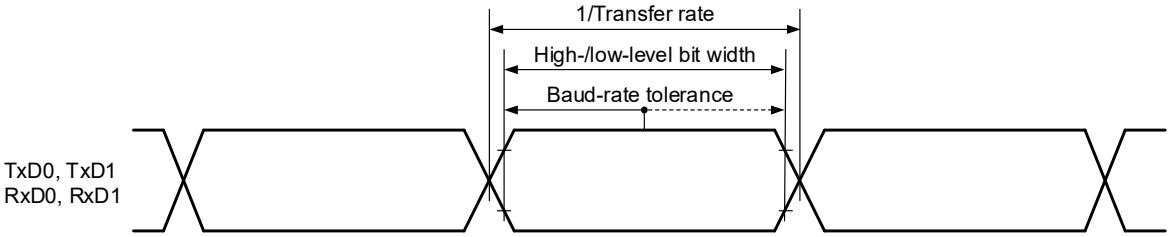
(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-					f_{MCK}/6	bps
		f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}	Normal slew rate			5.3	Mbps
			Special slew rate			2	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxD0 pin and RxD1 pin and normal output mode for the TxD0 pin and TxD1 pin.

Remark f_{MCK}: Serial array unit operation clock frequency

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(2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}		125 Note 5			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	t_{KCY1}/2 – 12			ns
		2.7 V ≤ EV_{DD0} < 4.0 V	t_{KCY1}/2 – 18			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	44			ns
		2.7 V ≤ EV_{DD0} < 4.0 V	55			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 2	t_{KSI1}		30			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

<R> **5.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

Caution Select the normal input buffer for the SIp pin and normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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(3) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, special slew rate)

(T_A = -40 to +105°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}		500 Note 5			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 – 60			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}		120			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 2	t_{KSI1}		80			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			90	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

<R> **5.** t_{KCY1} ≥ 4/ f_{MCK} must also be satisfied.

Caution Select the normal input buffer for the SIp pin and normal output mode and special slew rate for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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(4) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, normal slew rate)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}			8/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			1/f_{MCK} + 20			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]	4.0V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5V			2/f_{MCK} + 44	ns
			2.7V ≤ V_{DD} = EV_{DD0} = EV_{DD1} < 4.0V			2/f_{MCK} + 57	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp, $\overline{SCKp}$ and $\overline{SSIp}$ pins and normal output mode for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

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(5) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, special slew rate)

(T_A = -40 to +105°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	20 MHz < f_{MCK}	10/f_{MCK}			ns
		10 MHz < f_{MCK} ≤ 20 MHz	8/f_{MCK}			ns
		f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)Note1	t_{SIK2}		1/f_{MCK} + 50			ns
SIp hold time (from $\overline{SCKp}$↑)Note 2	t_{KSI2}		1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp outputNote 3	t_{KSO2}	C = 30 pFNote 4			2/f_{MCK} + 80	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0	120			ns
		DAP = 1	1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0	1/f_{MCK} + 120			ns
		DAP = 1	120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp, $\overline{SCKp}$ and $\overline{SSIp}$ pins and normal output mode and special slew rate for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

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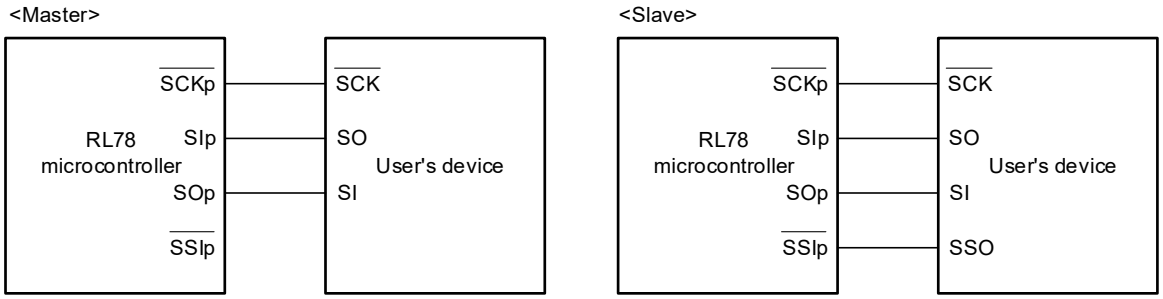
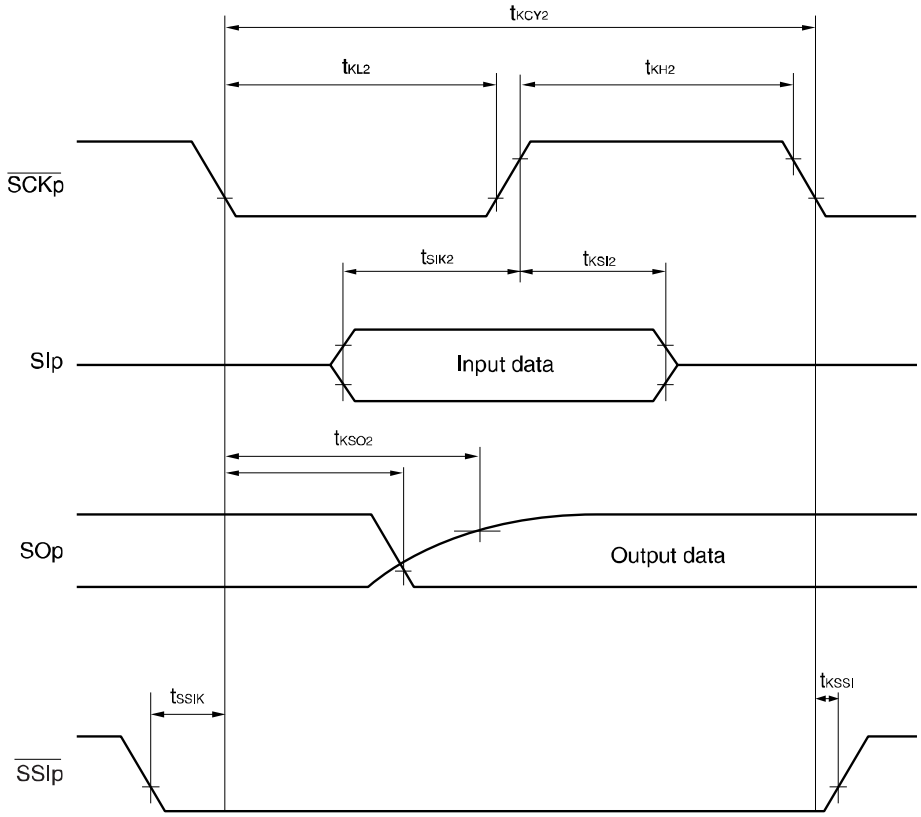
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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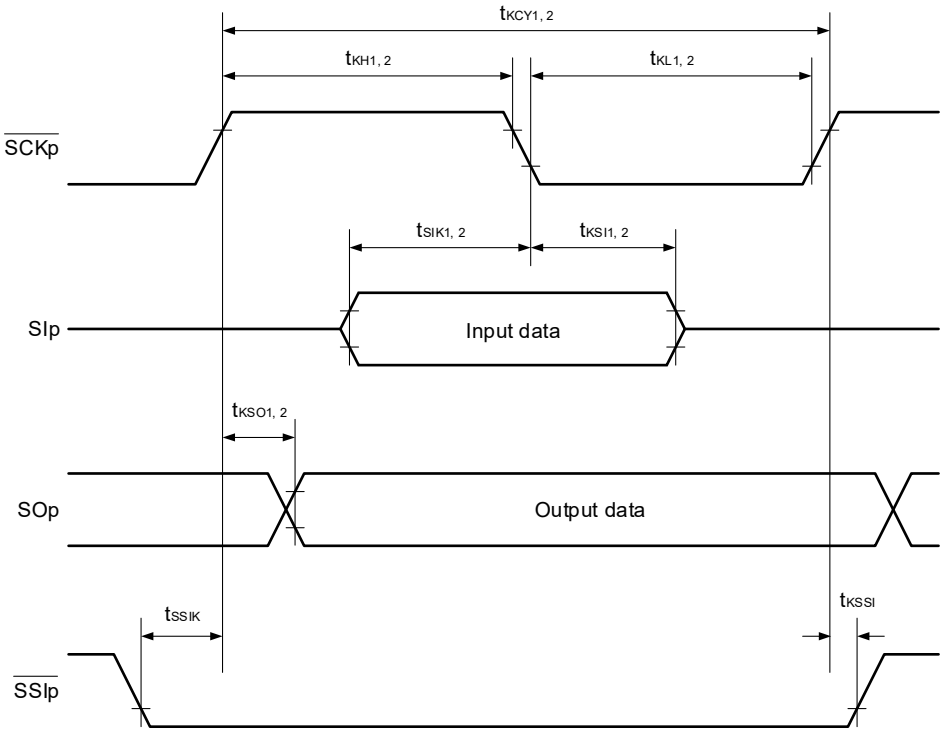
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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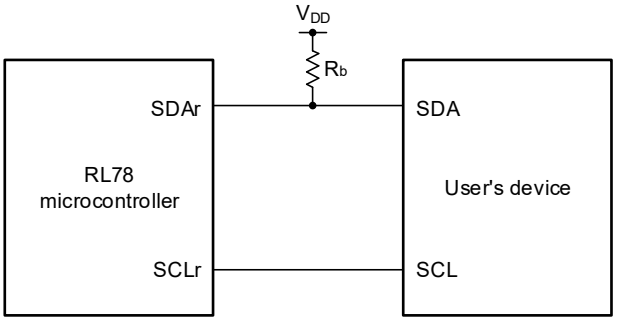
(6) During communication at same potential (simplified I²C mode)
(SDAr: N-ch open-drain output (EV_{DD0} tolerance) mode, SCLr: normal output mode)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

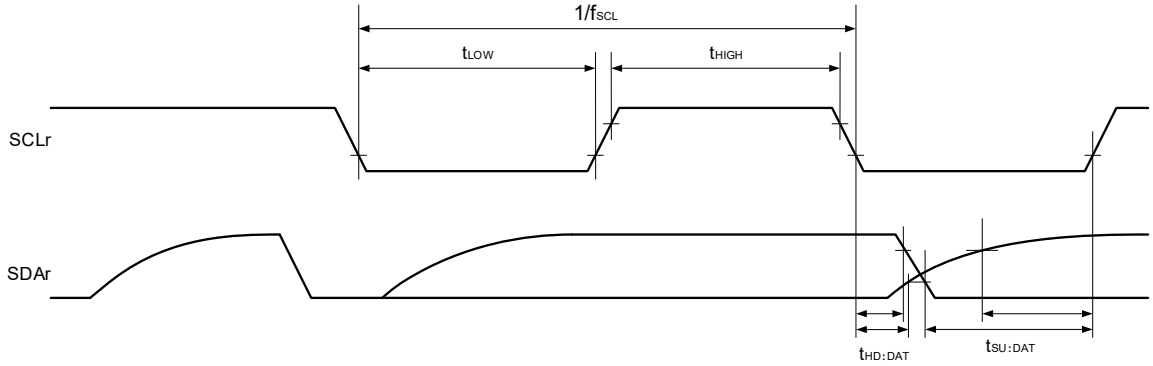
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f_{SCL}				1000[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}		475			ns
Hold time when SCLr = "H"	t_{HIGH}		475			ns
Data setup time (reception)	$t_{SU:DAT}$		$1/f_{MCK}$ + 85			ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 50 pF, R_b = 2.7 kΩ	0		305	ns

Note $f_{SCL} \leq f_{MCK}/4$ must also be satisfied.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and normal output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

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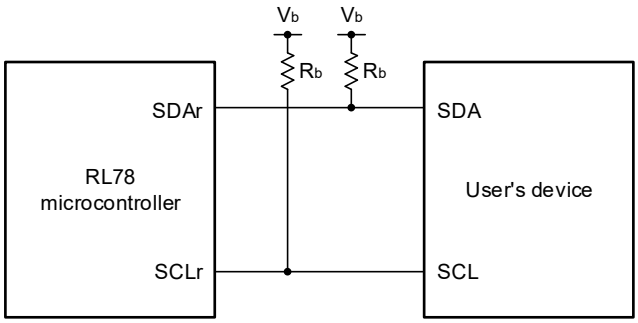
(7) During communication at same potential (simplified I²C mode) (SDAr and SCLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}			400[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1300		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	600		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Data setup time (reception)	$t_{SU: DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1/f_{MCK} + 120		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 270		ns
Data hold time (transmission)	$t_{HD: DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 2.7 kΩ	0	300	ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

Simplified I²C mode connection diagram (during communication at same potential)



Caution Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

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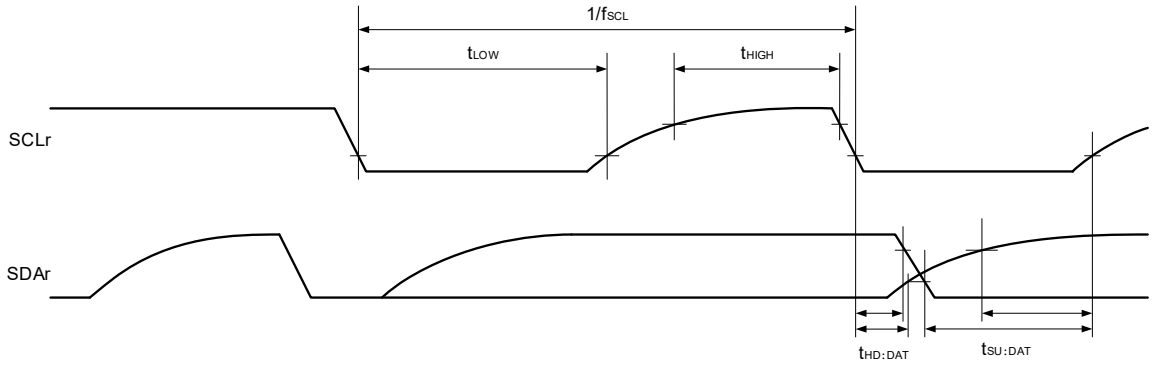
Simplified I^{2}C mode serial transfer timing (during communication at same potential)



Remark r: IICr (r = 00, 01, 10, 11)

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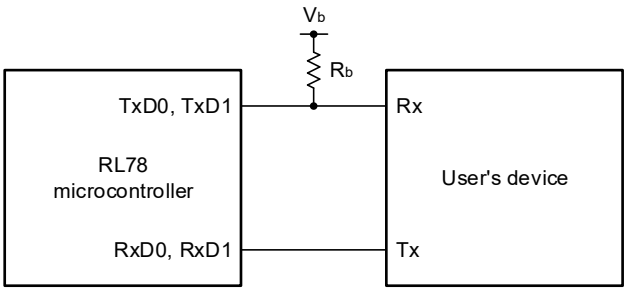
(8) Communication at different potential (UART mode) (TxD output buffer: N-ch open-drain, RxD input buffer: TTL)

(T_A = -40 to +105°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

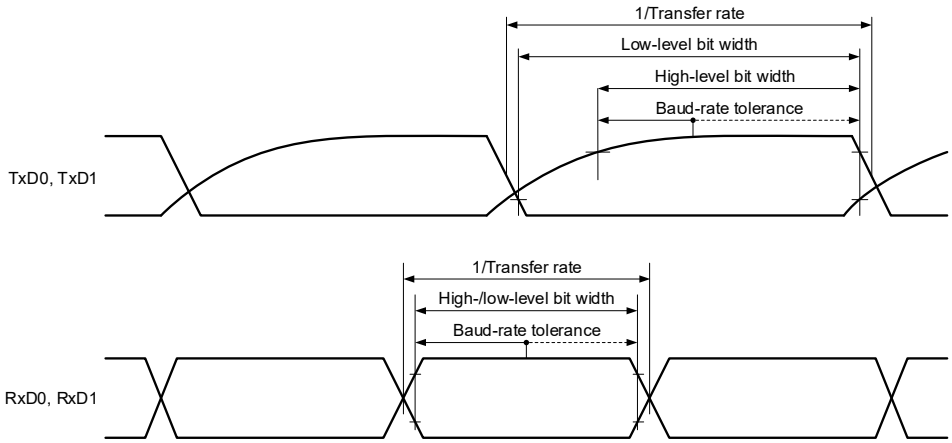
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate	–	Reception	2.7 V ≤ V_b ≤ EV_{DD0}, V_{IH} = 2.2 V, V_{IL} = 0.8 V				f_{MCK}/6	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF)			5.3	Mbps
		Transmission	2.7 V ≤ V_b ≤ EV_{DD0}, V_{OH} = 2.2 V, V_{OL} = 0.8 V				Smaller number of the values given by f_{MCK}/6 and expression 1 is applicable.	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF) Normal slew rate			5.3	Mbps

Note Expression 1: Maximum transfer rate = $1 / [\{-C_b \times R_b \times \ln (1 - 2.2/V_b)\} \times 3]$

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxD0 pin and RxD1 pin and N-ch open-drain output mode for the TxD0 pin and TxD1 pin.

Remarks 1. R_b [Ω]: Communication line (TxD) pull-up resistance, C_b [F]: Communication line (TxD) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

Downloaded from Arrow.com.

(9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)

(T_A = -40 to +105°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	400 Note3			ns
$\overline{\text{SCKp}}$ high-level width	t_{KH1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75			ns
$\overline{\text{SCKp}}$ low-level width	t_{KL1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 20			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
SIp setup time (to $\overline{\text{SCKp}}$↓) Note 2	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 1	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
SIp hold time (from $\overline{\text{SCKp}}$↓) Note 2	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note1	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
Delay time from $\overline{\text{SCKp}}$↑ to SOp output Note2	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

<R> **3.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

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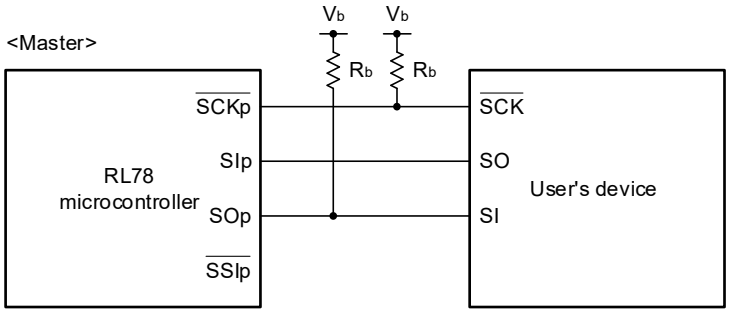
CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp pin and N-ch open-drain output mode for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remarks 1. R_b [Ω]: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, C_b [F]: Communication line (SOp, $\overline{\text{SCKp}}$) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:

When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

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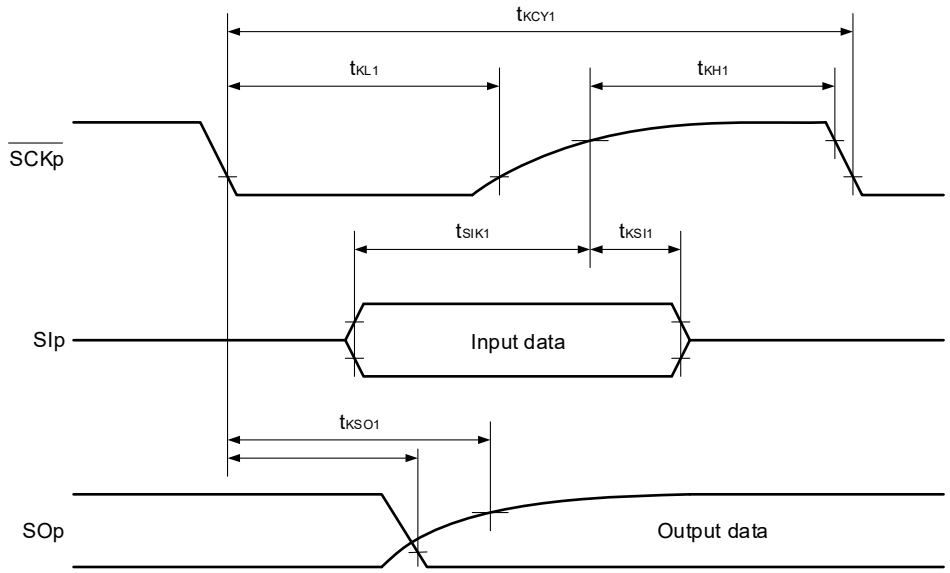
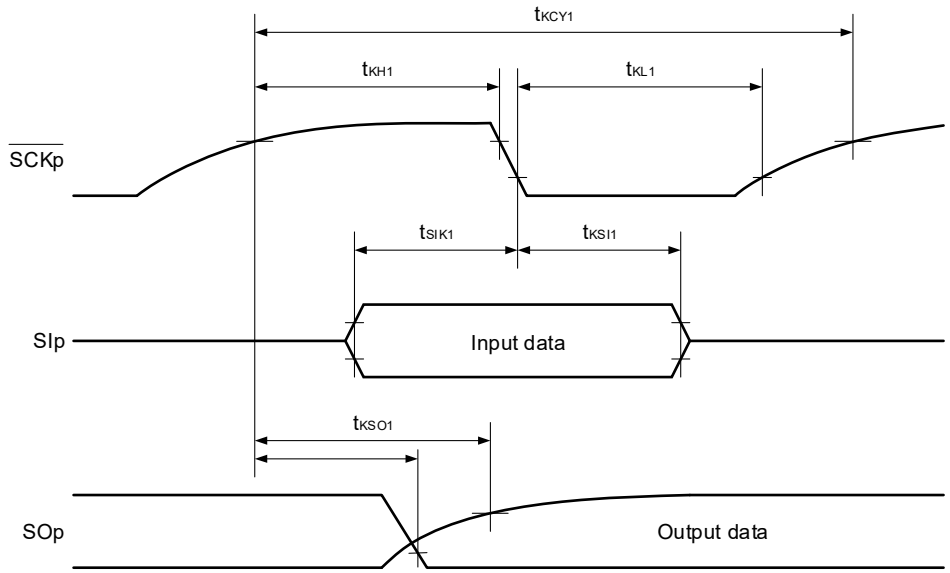
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



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(10) During communication at different potential (3-V supply system) (CSI mode) (slave mode, $\overline{\text{SCKp}}$ … external clock input, normal slew rate)

(T_A = -40 to +105°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY2}	2.7 V ≤ V_b ≤ V_{DD}	24 MHz < f_{MCK}	14/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_b ≤ V_{DD}		t_{KCY2}/2 – 20			ns
SIp setup time (to $\overline{\text{SCKp}}$↑)[Note 1]	t_{SIK2}			90			ns
SIp hold time (from $\overline{\text{SCKp}}$↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output[Note 3]	t_{KSO2}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
$\overline{\text{SSIp}}$ setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
$\overline{\text{SSIp}}$ hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

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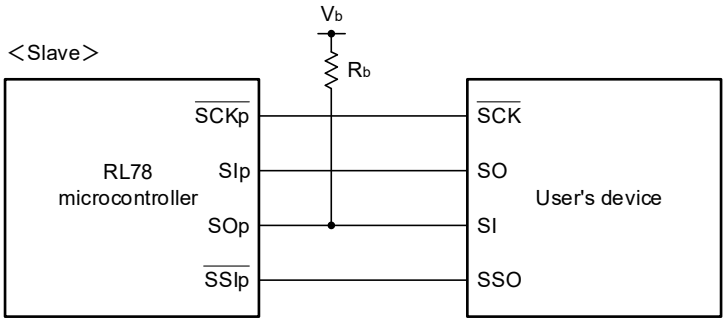
CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp, $\overline{\text{SCKp}}$ and $\overline{\text{SSIp}}$ pins and N-ch open-drain output mode for the SOp pin.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

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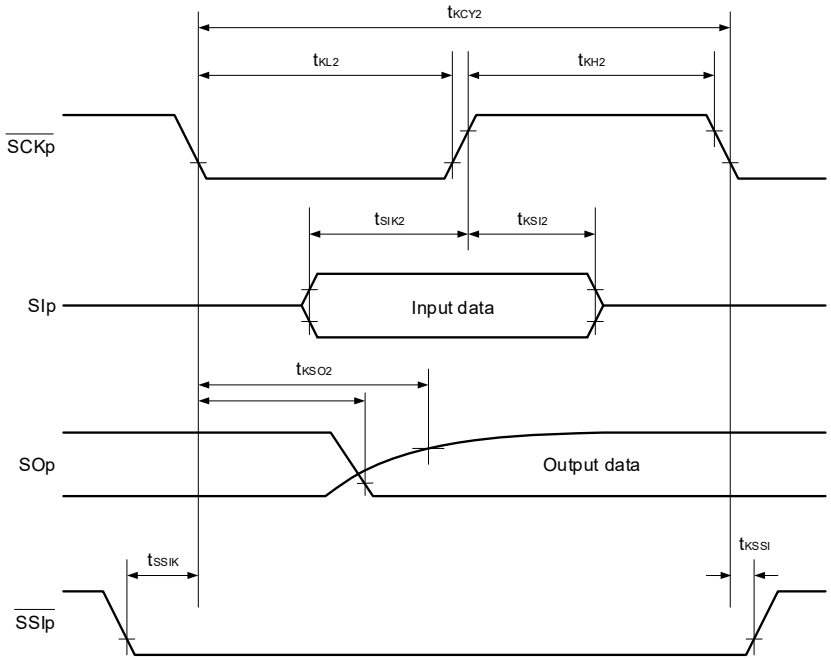
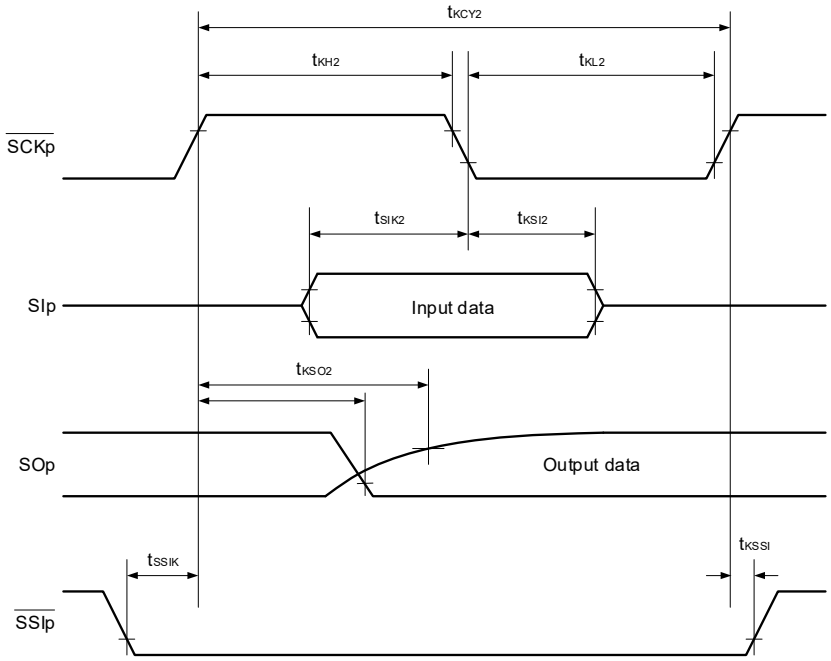
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



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(11) During communication at different potential (3-V supply system) (simplified I²C mode) (SDAr: TTL input buffer mode or N-ch open-drain output (EV_{DD0} tolerance) mode, SCLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

(T_A = -40 to +105°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	135 + 1/f_{MCK}		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	140	ns

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

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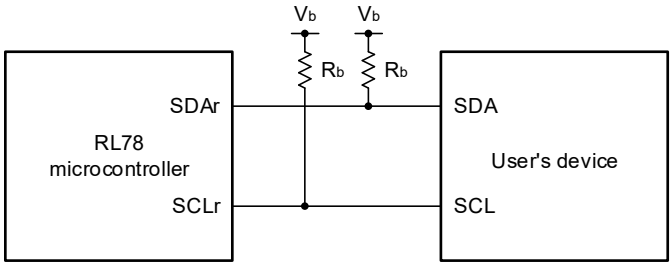
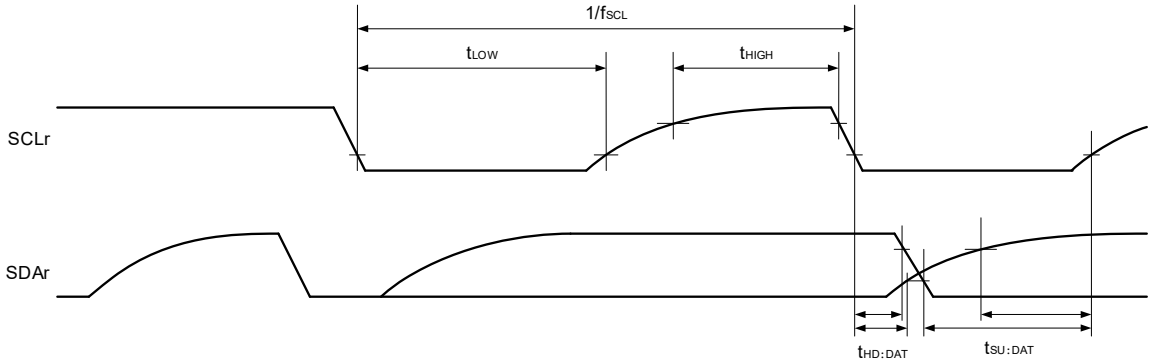
Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open-drain output mode for the SDAr pin and N-ch open-drain output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

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3.5.2 Serial Interface IICA

<R>

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: 10 MHz ≤ f_{MCK}					0	1000	kHz
		Fast mode: 3.5 MHz ≤ f_{MCK}			0	400			kHz
		Normal mode: 1 MHz ≤ f_{MCK}	0	100					kHz
Setup time of restart condition Note 1	$t_{SU:STA}$		4.7		0.6		0.26		μs
Hold time	$t_{HD:STA}$		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	0	0.9	0		μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		μs
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

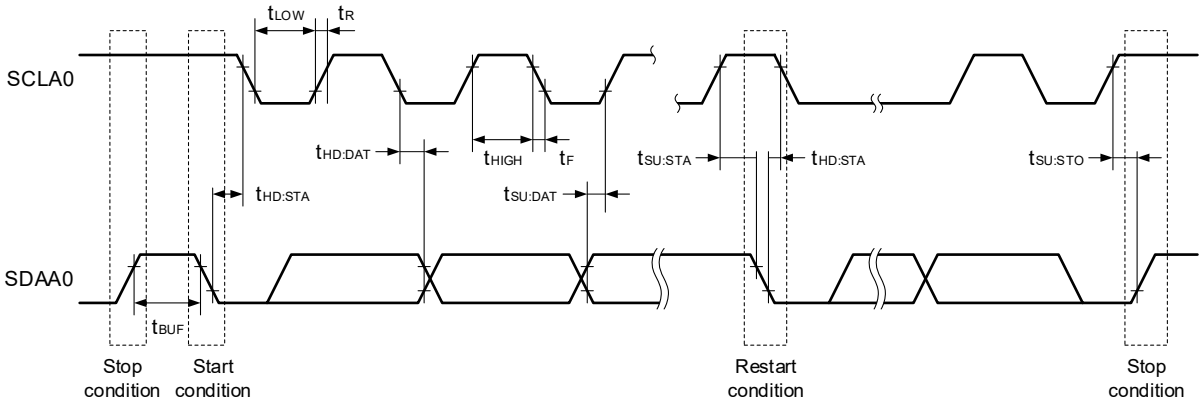
Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



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3.5.3 On-chip Debug (UART)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-		115.2 k		1 M	bps

3.5.4 LIN/UART Module (RLIN3) UART Mode

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 to 32 MHz			5333	kbps
		SNOOZE mode	LIN communication clock source (f_{CLK}): 1 to 32 MHz FRQSEL4 = 0 in the user option byte (000C2H/020C2H)			4.8	
			LIN communication clock source (f_{CLK}): 1 to 32 MHz FRQSEL4 = 1 in the user option byte (000C2H/020C2H)			2.4	

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3.6 Analog Characteristics

3.6.1 A/D Converter Characteristics

(1) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI23 (power supply: V_{DD})

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±3.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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(2) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI24 to ANI30 (power supply: EV_{DD0})

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±4.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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(3) When AV_{REF} (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), AV_{REF} (-) = V_{SS} (ADREFM = 0), target ANI pin: ANI0 to ANI23, ANI24 to ANI30

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution ANI0 to ANI23	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±5.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.5	LSB
		10-bit resolution ANI24 to ANI30	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±6.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.50	%FSR
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.50	%FSR
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI23[Note 3]		0		V_{DD}	V
		ANI24 to ANI30[Note 3]		EV_{SS}		EV_{DD0}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. The number of pins depends on the product. For details, refer to **2.1 Pin Function List**.

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(4) When AV_{REF} (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI0, ANI2 to ANI23, ANI24 to ANI30

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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3.6.2 Temperatures Sensor Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.1		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 D/A Converter Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs

3.6.4 Comparator Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±40	mV
Input voltage range	V_{ICMP}		0		V_{DD}	V
Response time	t_{CR}, t_{CF}	Input amplitude ±100 mV		70	200	ns
Stabilization wait time during input channel switching[Note 1]	t_{WAIT}	Input amplitude ±100 mV	300			ns
Operation stabilization wait time[Note 2]	t_{CMP}	3.3 V ≤ V_{DD} ≤ 5.5 V	1			μs
		2.7 V ≤ V_{DD} < 3.3 V	3			μs

Notes 1. Period of time from when the comparator input channel is switched until the comparator is switched to output

2. Period of time from when the comparator operation is enabled (HCMPON bit in CMPCTL is set to 1) until the comparator satisfies the DC/AC characteristics.

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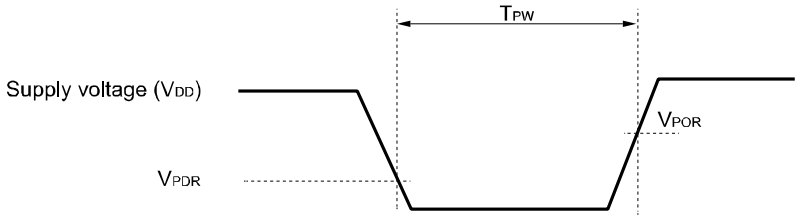
3.6.5 POR Circuit Characteristics

(T_A = -40 to +105°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage[Note 1]	V_{POR}	Power supply rise time	1.48	1.56	1.62	V
	V_{PDR}	Power supply fall time	1.47	1.55	1.61	V
Minimum pulse width[Note 2]	T_{PW}		300			μs
Detection delay time	T_{PD}				350	μs

Notes 1. This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}.



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3.6.6 LVD Circuit Characteristics

(1) LVD detection voltage of interrupt mode or reset mode

(T_A = -40 to +105°C, $V_{PDR} \le EV_{DD0} = EV_{DD1} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	4.62	4.74	4.84	V
			Power supply fall time	4.52	4.64	4.74	V
		V_{LVD1}	Power supply rise time	4.50	4.62	4.72	V
			Power supply fall time	4.40	4.52	4.62	V
		V_{LVD2}	Power supply rise time	4.30	4.42	4.51	V
			Power supply fall time	4.21	4.32	4.41	V
		V_{LVD3}	Power supply rise time	3.13	3.22	3.29	V
			Power supply fall time	3.07	3.15	3.22	V
		V_{LVD4}	Power supply rise time	2.95	3.02	3.09	V
			Power supply fall time	2.89	2.96	3.02	V
		V_{LVD5}	Power supply rise time	2.74	2.81	2.87	V
			Power supply fall time	2.68 Note	2.75	2.81	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

Note The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

(2) LVD detection voltage of interrupt & reset mode

(T_A = -40 to +105°C, $V_{PDR} \le EV_{DD0} = EV_{DD1} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 0, 1 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	2.81	V
	V_{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.51	V
			Falling interrupt voltage	4.21	4.32	4.41	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 0 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	2.81	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.72	V
			Falling interrupt voltage	4.40	4.52	4.62	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	2.81	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.29	V
			Falling interrupt voltage	3.07	3.15	3.22	V
	V_{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.84	V
			Falling interrupt voltage	4.52	4.64	4.74	V

Notes 1. These values indicate setting values of option bytes.

2. The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

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3.7 Power Supply Voltage Rising Time

(T_A = -40 to +105°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope	S_{vrmax}	0 V → V_{DD} (VPOC2 = 0 or 1[Note 2])			50[Note 3]	V/ms
Minimum power supply voltage rising slope [Note 1]	S_{vrmin}	0 V → 2.7 V	6.5			V/ms

Notes 1. The minimum power supply voltage rising slope is applied only under the following condition.
When the voltage detection (LVD) circuit is not used (VPOC2 = 1) and an external reset circuit is not used or when a reset is not effected until V_{DD} = 2.7 V.

2. These values indicate setting values of option bytes.

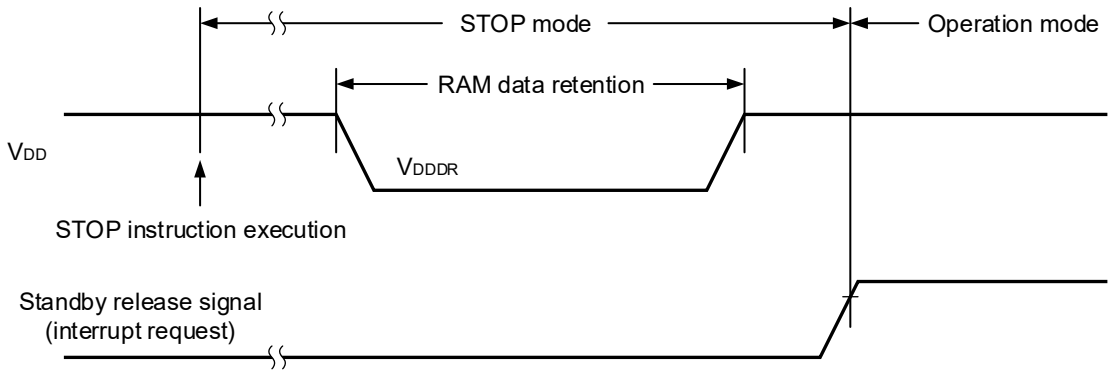
3. If the power supply drops below V_{PDR} and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to 0 V.

3.8 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



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3.9 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = +85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 20 years T_A = +85°C Note 4	10,000			
		Retained for 5 years T_A = +85°C Note 4	100,000			
Erase time	T_{erasa}	Block erase	5			ms
Write time	T_{wrwa}	1 word write	10			μs

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The specified data retention time is given under the condition that the average temperature (T_A) is 85°C or below.

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4. ELECTRICAL SPECIFICATIONS (GRADE K)

Cautions 1. RL78/F13 and RL78/F14 have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

3. The pins mounted depending on the product. For details, refer to 1.5 Pin Configurations and 2.1 Pin Function List.

4. The products are classified into the following five groups according to the product type, pin count, and code flash memory size. In this chapter, the products are referred to by group names depending on the content. In this case, refer to the following classification.

Group A: RL78/F13 (LIN incorporated) products with 20, 30, 32, 48, or 64 pins and 16 Kbytes to 64 Kbytes of code flash memory

Group B: RL78/F13 (LIN incorporated) products with 48 or 64 pins and 96 Kbytes to 128 Kbytes of code flash memory or with 80 pins and 64 Kbytes to 128 Kbytes of code flash memory

Group C: RL78/F13 (CAN and LIN incorporated) products with 30, 32, 48, 64, or 80 pins and 32 Kbytes to 128 Kbytes of code flash memory

Group D: RL78/F14 products with 30, 32, 48, 64, or 80 pins and 48 Kbytes to 96 Kbytes of code flash memory

Group E: RL78/F14 products with 48, 64, or 80 pins and 128 Kbytes to 256 Kbytes of code flash memory or with 100 pins and 64 Kbytes to 256 Kbytes of code flash memory

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4.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	V_{SS}		-0.5 to +0.3	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD}+0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 4], P106, P107, P120, P125 to P127, P140, P150 to P157	-0.3 to EV_{DD0}+0.3 and -0.3 to V_{DD}+0.3[Note 2]	V
	V_{I2}	P33, P34, P80 to P87, P90 to P97[Note 4], P100 to P105, P121 to P124, P137, $\overline{\text{RESET}}$	-0.3 to V_{DD}+0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 4], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	-0.3 to EV_{DD0}+0.3 and -0.3 to V_{DD}+0.3[Note 2]	V
	V_{O2}	P33, P34, P80 to P87, P90 to P97[Note 4], P100 to P105	-0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI1}	ANI24 to ANI30	-0.3 to EV_{DD0}+0.3 and -0.3 to $AV_{REF(+)}$+0.3[Notes 2, 3]	V
	V_{AI2}	ANI0 to ANI23	-0.3 to V_{DD}+0.3 and -0.3 to $AV_{REF(+)}$+0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. For pins to be used in A/D conversion, the voltage should not exceed the value $AV_{REF(+)}$ + 0.3.

4. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	-40	mA
		Total of all pins -170 mA	P01, P02, P40 to P47, P92 to P97[Note], P120, P125 to P127, P150 to P153	-70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	-100	mA
	I_{OH2}	Per pin	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	40	mA
		Total of all pins 170 mA	P01, P02, P40 to P47, P92 to P97[Note], P120, P125 to P127, P150 to P153	70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	100	mA
	I_{OL2}	Per pin	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +125	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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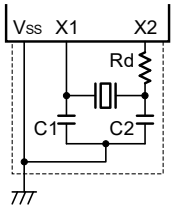
4.2 Oscillator Characteristics

4.2.1 Main System Clock Oscillator Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

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4.2.2 On-chip Oscillator Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Note]	f_{IH}		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy	-		-3		+3	%
Low-speed on-chip oscillator clock frequency	f_{IL}, f_{WDT}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	-		-15		+15	%

Note High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/020C2H) and bits 0 to 2 of the HOCODIV register.

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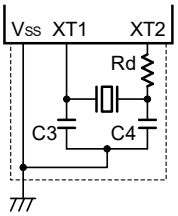
4.2.3 Subsystem Clock Oscillator Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Recommended Circuit	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})	2.7 V ≤ V_{DD} ≤ 5.5 V	29.0	32.768	35.0	kHz

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption and thus required to be adequately evaluated on the system. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

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4.2.4 PLL Circuit Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
PLL input enable clock frequency[Note 1]	f_{PLLI}	PLLMUL = 0	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
		PLLMUL = 1	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
PLL output frequency (center value)	f_{PLL}	PLLMUL = 0	PLLDIV0 = 0	f_{PLLI} × 12/2			MHz
			PLLDIV0 = 1	f_{PLLI} × 12/4			MHz
		PLLMUL = 1 [Note 4]	PLLDIV0 = 0 [Note 4]	f_{PLLI} × 16/2			MHz
			PLLDIV0 = 1	f_{PLLI} × 16/4			MHz
Long-term jitter[Notes 2, 3]	t_{LJ}	f_{PLL} = 24 MHz (480 counts)		-2		+2	ns
		f_{PLL} = 32 MHz (640 counts)		-2		+2	ns
		f_{PLL} = 48 MHz (960 counts)		-2		+2	ns

Notes 1. If the high-speed on-chip oscillator clock is to be selected as the PLL input clock, the minimum and maximum values will reflect the range of accuracy of the oscillation frequency by the high-speed on-chip oscillator clock.

2. Guaranteed by design, but not tested before shipment.

3. Indicates 20 μs.

4. Setting of PLLMUL = 1 and PLLDIV0 = 0 is prohibited when f_{PLLI} > 6 MHz.

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4.3 DC Characteristics

4.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **2. PIN FUNCTIONS**.

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 3], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-5.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-3.0	mA
		Per pin for P10, P12, P14, P30,P120,P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-0.6	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-0.2	mA
		Total of P01, P02, P40 to P47, P92 to P97[Note 3], P120, P125 to P127, P150 to P153 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
		Total of P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-42.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-29.0	mA
	I_{OH2}	Per pin for P33, P34, P80 to P87, P90 to P97[Note 3], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V			-0.1	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	2.7 V ≤ V_{DD} ≤ 5.5 V			-2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from pins EV_{DD0}, EV_{DD1} and V_{DD} to an output pin.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where n = 80% and I_{OH} = -10.0 mA

Total output current of pins = $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode. P10 to P12 and P70 to P72 of the Group A products do not support N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 3], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			8.5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			4.0	mA
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			0.59	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			0.07	mA
		Total of P01, P02, P40 to P47, P92 to P97[Note 3], P120, P125 to P127, P150 to P153 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
		Total of P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			45.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			65.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			50.0	mA
	I_{OL2}	Per pin for P33, P34, P80 to P87, P90 to P97[Note 3], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V			0.4	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	2.7 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows to the EV_{SS0}, EV_{SS1} and V_{SS} pins from an output pin.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.65 EV_{DD0}		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.7 EV_{DD0}		EV_{DD0} Note 1	V
	V_{IH2}	P10, P11, P13, P14, P16, P17, P30, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152, P153 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.8 EV_{DD0}		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.85 EV_{DD0}		EV_{DD0} Note 1	V
	V_{IH3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0} Note 1	V
	V_{IH4} Note 2	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.85 V_{DD}		V_{DD}	V
	V_{IH5}	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.65 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.7 V_{DD}		V_{DD}	V
	V_{IH6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.8 V_{DD}		V_{DD}	V

Notes 1. The maximum value of V_{IH} of the pins P10 to P17, P60 to P63, P70 to P72, and P120 is EV_{DD0}, even in N-ch open-drain mode.

2. P92 to P96 of the Group A products are fixed to Schmitt 1 mode.
P96 and P97 of the Group B, C, and D products are fixed to Schmitt 1 mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.35 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.3 EV_{DD0}	V
	V_{IL2}	P10, P11, P13, P14, P16, P17, P30, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152, P153 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.5 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.4 EV_{DD0}	V
	V_{IL3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
	V_{IL4} Note	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.5 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.4 V_{DD}	V
	V_{IL5}	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.35 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.3 V_{DD}	V
	V_{IL6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V

Note P92 to P96 of the Group A products are fixed to Schmitt 1 mode.
P96 and P97 of the Group B, C, and D products are fixed to Schmitt 1 mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -5.0 mA	EV_{DD0}-0.9			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0}-0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.0 mA	EV_{DD0}-0.5			V
	V_{OH2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V I_{OH2} = -100 μA	V_{DD}-0.5			V
	V_{OH3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = -0.6 mA	EV_{DD0}-0.8			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = -0.2 mA	EV_{DD0}-0.5			V
Output voltage, low	V_{OL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.6 mA			0.8	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.07 mA			0.5	V

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (6/6)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{DD0}				1	μA
	I_{LIH2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105, P137, $\overline{RESET}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{SS0}				-1	μA
	I_{LIL2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105, P137, $\overline{RESET}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97, P100 to P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{SS0}, in input port		10	20	100	kΩ

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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4.3.2 Supply Current Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/3)

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 48 MHz	f_{CLK} = 24 MHz Notes 3, 4		5.1	12.0	mA
					f_{IH} = 24 MHz	f_{CLK} = f_{IH} Notes 3, 4		4.8	11.0	mA
					f_{IH} = 1 MHz	f_{CLK} = f_{IH} Notes 3, 4		1.0	2.5	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		4.2	9.0	mA
					f_{MX} = 1 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.9	2.5	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 48 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz Notes 3, 6		5.0	12.0	mA
					f_{PLL} = 24 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz Notes 3, 6		4.9	11.0	mA
					f_{PLL} = 24 MHz, f_{MX} = 4 MHz	f_{CLK} = 24 MHz Notes 3, 6		4.7	11.0	mA
				Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7				
					Groups A to D			6.0	80.0	μA
					Group E			6.0	120.0	μA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8				
					Groups A to D			3.0	70.0	μA
					Group E			3.0	110.0	μA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

Remarks 1. f_{MX}: High-speed system clock frequency

2. f_{SUB}: Subsystem clock frequency

3. f_{PLL}: PLL clock frequency

4. f_{IH}: High-speed on-chip oscillator clock frequency

5. f_{IL}: Low-speed on-chip oscillator clock frequency

6. f_{CLK}: CPU/peripheral hardware clock frequency

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 3]	I_{DD2}	HALT mode[Note 2]	High-speed on-chip oscillator clock operation	f_{IH} = 48 MHz	f_{CLK} = 24 MHz [Note 5]		0.9	8.0	mA
				f_{IH} = 24 MHz	f_{CLK} = f_{IH} [Note 5]		0.7	7.0	mA
				f_{IH} = 1 MHz	f_{CLK} = f_{IH} [Note 5]		0.3	1.5	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} [Note 6]		0.6	6.0	mA
				f_{MX} = 1 MHz	f_{CLK} = f_{MX} [Note 6]		0.2	1.5	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 48 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz [Note 7]		0.9	8.0	mA
				f_{PLL} = 24 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz [Note 7]		0.8	7.0	mA
				f_{PLL} = 24 MHz, f_{MX} = 4 MHz	f_{CLK} = 24 MHz [Note 7]		0.6	7.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} [Note 8]				
				Groups A to D			0.7	75.0	μA
				Group E			0.7	115.0	
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} [Note 9]				
				Groups A to D			0.7	65.0	μA
				Group E			0.7	105.0	
	I_{DD3}	STOP mode[Note 4]	T_A = +25°C	Groups A to D			0.5		μA
				Group E			0.5		
			T_A = +50°C	Groups A to D				2.5	
				Group E				4.5	
			T_A = +70°C	Groups A to D				4.5	
				Group E				8.0	
			T_A = +105°C	Groups A to D				30.0	
				Group E				50.0	
			T_A = +125°C	Groups A to D				60.0	
				Group E				100.0	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

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7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency
2. f_{SUB}: Subsystem clock frequency
3. f_{PLL}: PLL clock frequency
4. f_{IH}: High-speed on-chip oscillator clock frequency
5. f_{IL}: Low-speed on-chip oscillator clock frequency
6. f_{CLK}: CPU/peripheral hardware clock frequency

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 2]	I_{SNOZ}	SNOOZE mode	A/D converter operation	During mode transition			1.0	1.2	mA
				During conversion	Low-voltage mode AV_{REFP} = V_{DD} = 5.0 V		2.1	2.5	mA
			DTC operation				4.5		mA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. The values below the MAX. column include the STOP leakage current.

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
		When internal reference voltage is selected Note 5			75.0		μA
LVD operating current	I_{LVD} Note 4				0.08		μA
Temperature sensor operating current	I_{TMPS}				75.0		μA
D/A converter operating current	I_{DAC}	Per channel			0.8	1.5	mA
Comparator operating current	I_{CMP}				50.0		μA
BGO operating current	I_{BGO} Note 6				2.50	12.20	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

5. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

6. Current increased by the BGO operation. The current value is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in operation mode or HALT mode.

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4.4 AC Characteristics

4.4.1 Basic Operation

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	High-speed on-chip oscillator clock operation		0.04166		1	μs
		High-speed system clock operation		0.05		1	μs
		PLL clock operation		0.04166		1	μs
		Subsystem clock operation		28.5	30.5	34.5	μs
		Low-speed on-chip oscillator clock operation			66.6		μs
		In self programming mode		0.04166		1	μs
CPU/peripheral hardware clock frequency	f_{CLK}			0.04166		66.6	μs
External system clock frequency	f_{EX}			1.0		20.0	MHz
	f_{EXS}			29		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}			$1/f_{MCK}+10$			ns
TO00 to TO07, TO10 to TO17 output frequency	f_{TO}	All TO pins, Normal slew rate, C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			12	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			6	MHz
		TO01, TO06, TO07, TO11, TO13 only, Special slew rate, C = 30 pF				2	MHz
PCLBUZ0 output frequency	f_{PCL}	Normal slew rate C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			12	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			6	MHz
		Special slew rate C = 30 pF				2	MHz
Timer RJ input cycle	t_C	TRJIO0		100			ns
Timer RJ input high-level width, low-level width	t_{WH}, t_{WL}	TRJIO0		40			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP13 Note		1			μs
KR0 to KR7 key interrupt input low-level width	t_{KR}			250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Note Pins $\overline{\text{RESET}}$, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

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(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

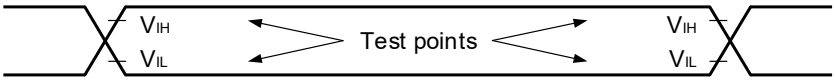
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Port output rise time, port output fall time	t_{RO}, t_{FO}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P96, P97, P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			25	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V		25 Note	60	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			100	ns

Note T_A = +25°C, EV_{DD0} = 5.0 V

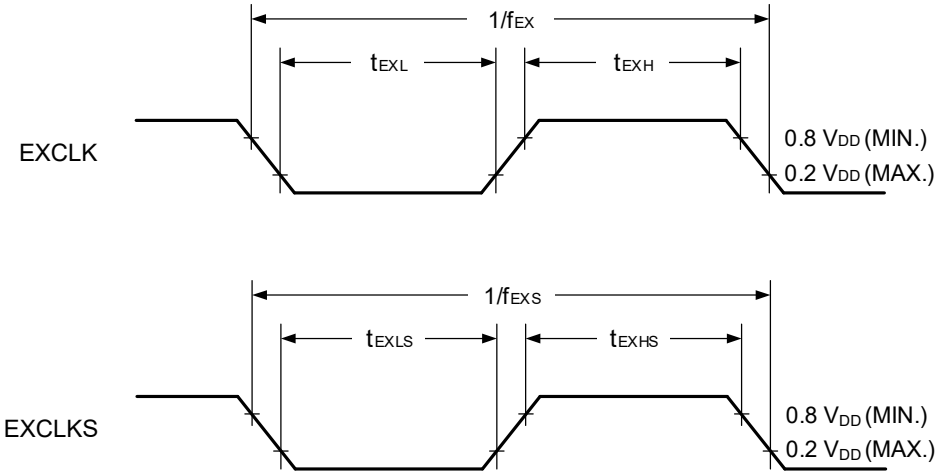
Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

AC Timing Test Points



External System Clock Timing



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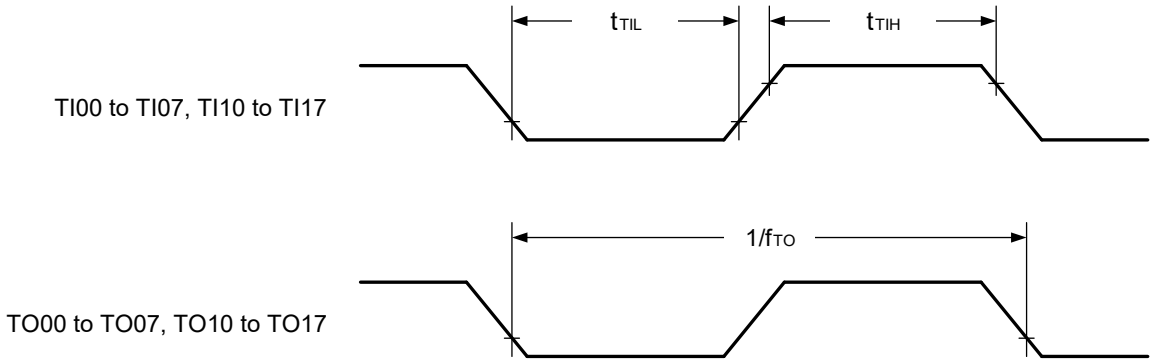
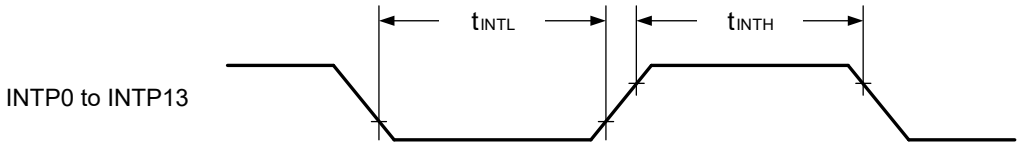
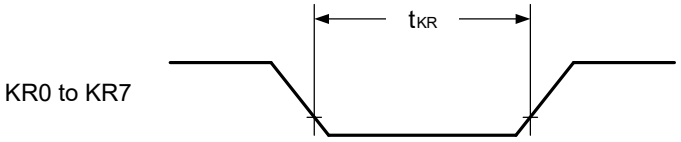
TI/TO Timing



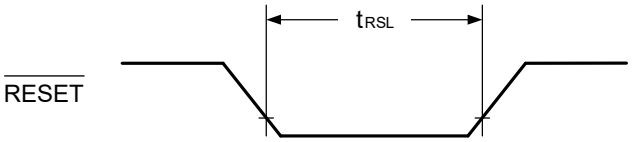
Interrupt Request Input Timing



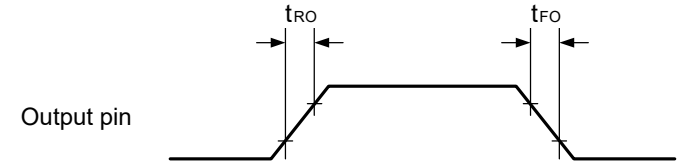
Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Output Rising and Falling Timing



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4.5 Peripheral Functions Characteristics

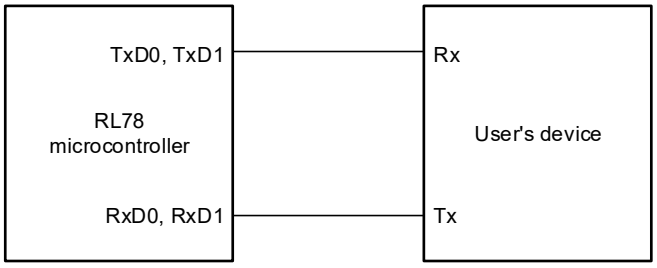
4.5.1 Serial Array Unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

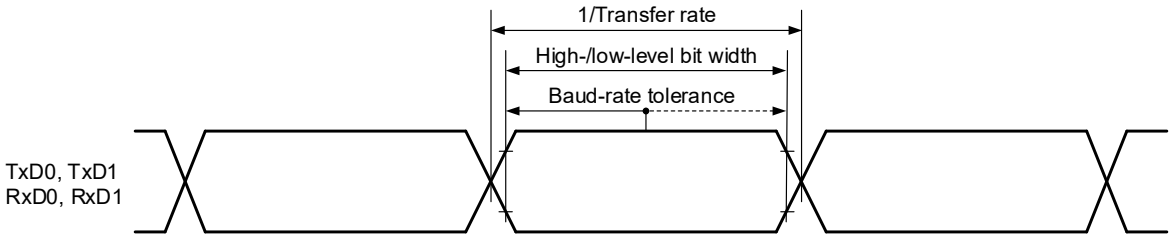
(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-					f_{MCK}/6	bps
		f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}	Normal slew rate			4	Mbps
			Special slew rate			2	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxD0 pin and RxD1 pin and normal output mode for the TxD0 pin and TxD1 pin.

Remark f_{MCK}: Serial array unit operation clock frequency

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(2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}		166.6 Note 5			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	t_{KCY1}/2 – 12			ns
		2.7 V ≤ EV_{DD0} < 4.0 V	t_{KCY1}/2 – 18			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	55			ns
		2.7 V ≤ EV_{DD0} < 4.0 V	66			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 2	t_{KSI1}		30			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

<R> **5.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

Caution Select the normal input buffer for the SIp pin and normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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(3) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, special slew rate)

(T_A = -40 to +125°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}		500 Note 5			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 – 60			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}		120			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 2	t_{KSI1}		80			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			90	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

<R> **5.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

Caution Select the normal input buffer for the SIp pin and normal output mode and special slew rate for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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(4) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, normal slew rate)

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}			8/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)Note 1	t_{SIK2}			1/f_{MCK} + 20			ns
SIp hold time (from $\overline{SCKp}$↑)Note 2	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from $\overline{SCKp}$↓ to SOp outputNote 3	t_{KSO2}	C = 30 pF Note 4	4.0V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5V			2/f_{MCK} + 44	ns
			2.7V ≤ V_{DD} = EV_{DD0} = EV_{DD1} < 4.0V			2/f_{MCK} + 57	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp, $\overline{SCKp}$ and $\overline{SSIp}$ pins and normal output mode for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

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(5) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, special slew rate)

(T_A = -40 to +125°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	20 MHz < f_{MCK}	10/f_{MCK}			ns
		10 MHz < f_{MCK} ≤ 20 MHz	8/f_{MCK}			ns
		f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)Note1	t_{SIK2}		1/f_{MCK} + 50			ns
SIp hold time (from $\overline{SCKp}$↑)Note 2	t_{KSI2}		1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp outputNote 3	t_{KSO2}	C = 30 pFNote 4			2/f_{MCK} + 80	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0	120			ns
		DAP = 1	1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0	1/f_{MCK} + 120			ns
		DAP = 1	120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp, $\overline{SCKp}$ and $\overline{SSIp}$ pins and normal output mode and special slew rate for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

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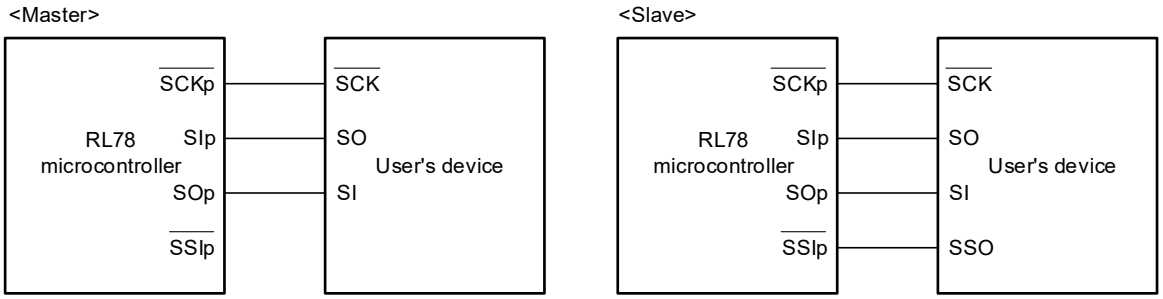
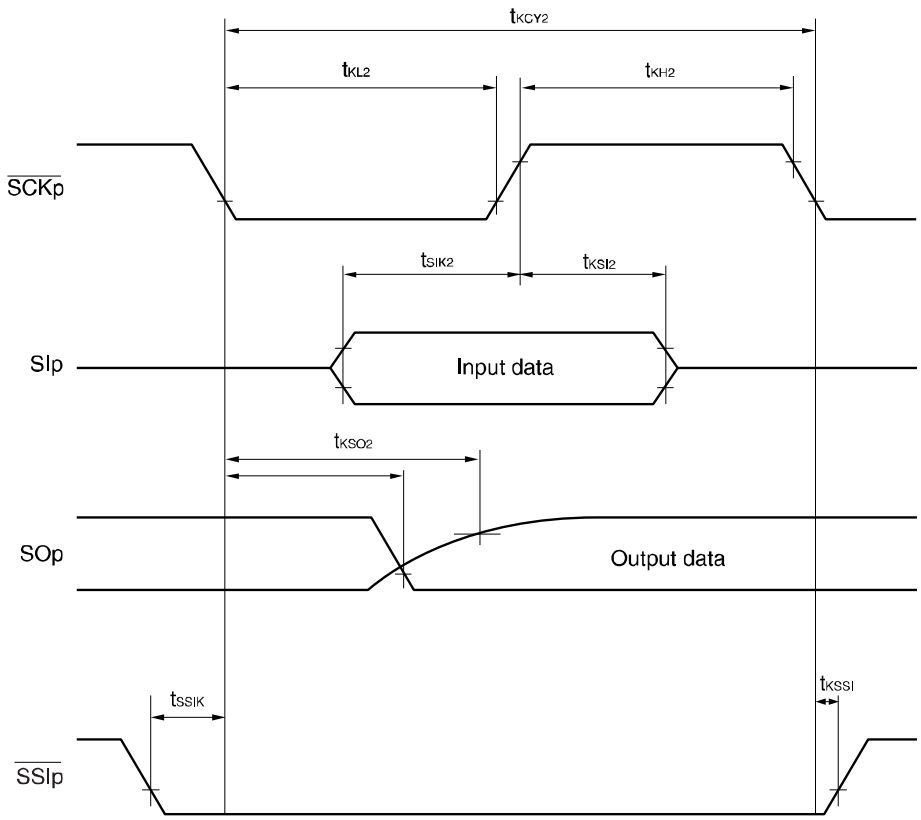
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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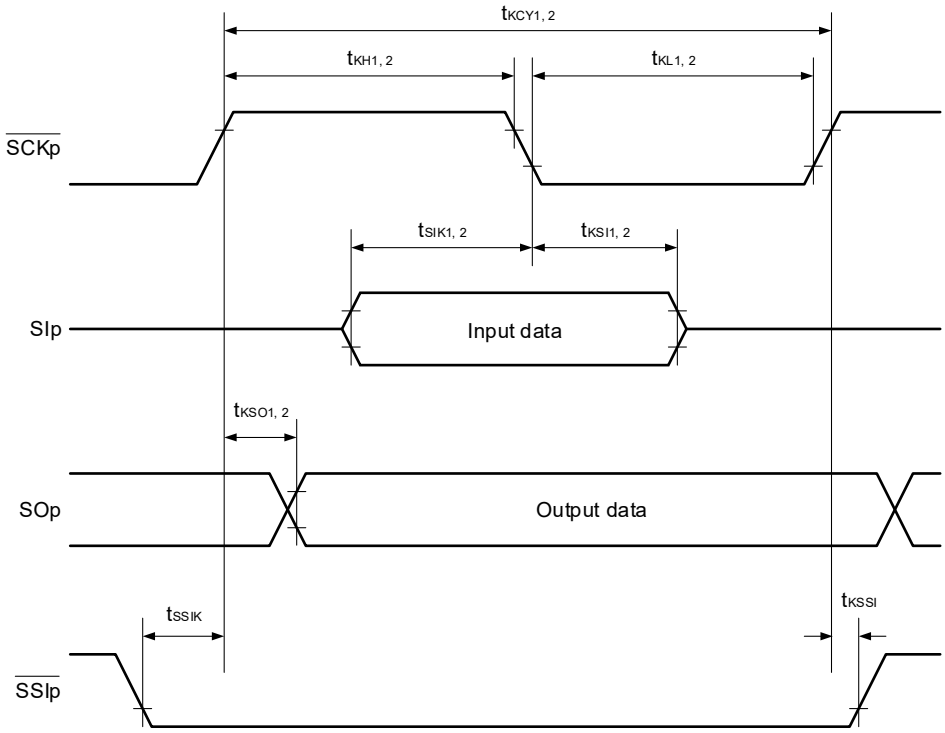
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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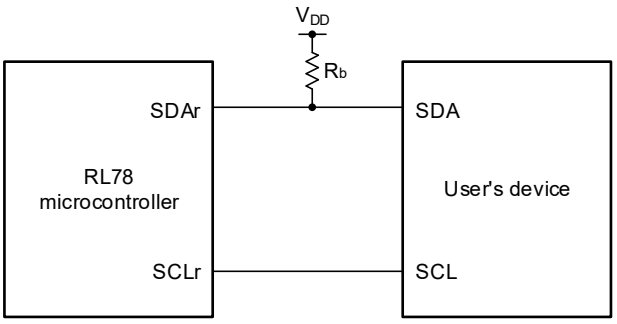
(6) During communication at same potential (simplified I²C mode)
(SDAr: N-ch open-drain output (EV_{DD0} tolerance) mode, SCLr: normal output mode)

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

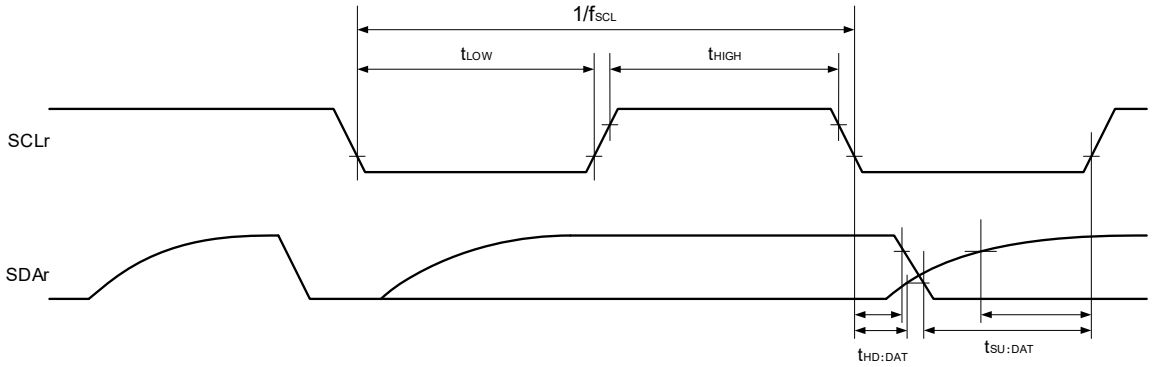
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f_{SCL}				1000[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}		475			ns
Hold time when SCLr = "H"	t_{HIGH}		475			ns
Data setup time (reception)	$t_{SU:DAT}$		$1/f_{MCK}$ + 85			ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 50 pF, R_b = 2.7 kΩ	0		305	ns

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and normal output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

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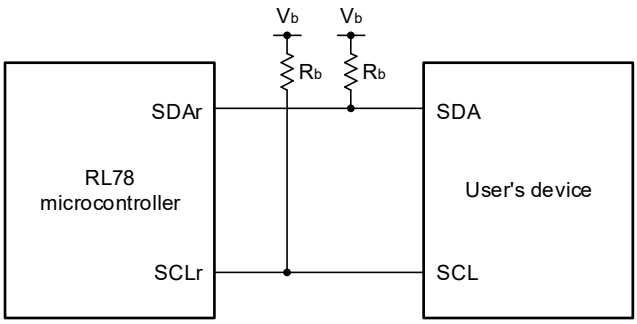
(7) During communication at same potential (simplified I²C mode) (SDAr and SCLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}			400[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1300		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	600		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1/f_{MCK} + 120		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 270		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	0	300	ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

Simplified I²C mode connection diagram (during communication at same potential)



Caution Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

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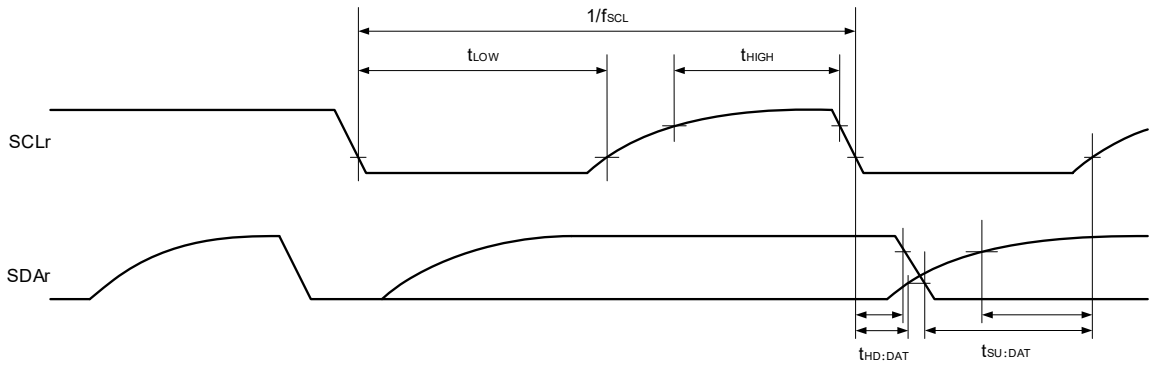
Simplified I²C mode serial transfer timing (during communication at same potential)



Remark r: IICr (r = 00, 01, 10, 11)

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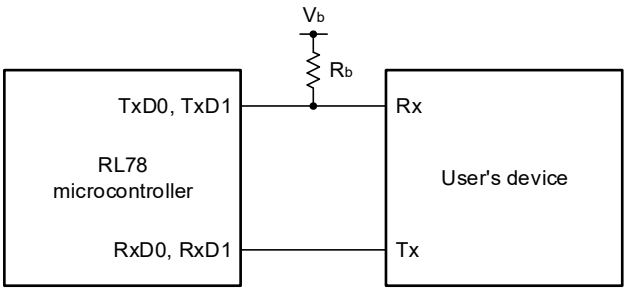
(8) Communication at different potential (UART mode) (TxD output buffer: N-ch open-drain, RxD input buffer: TTL)

(T_A = -40 to +125°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

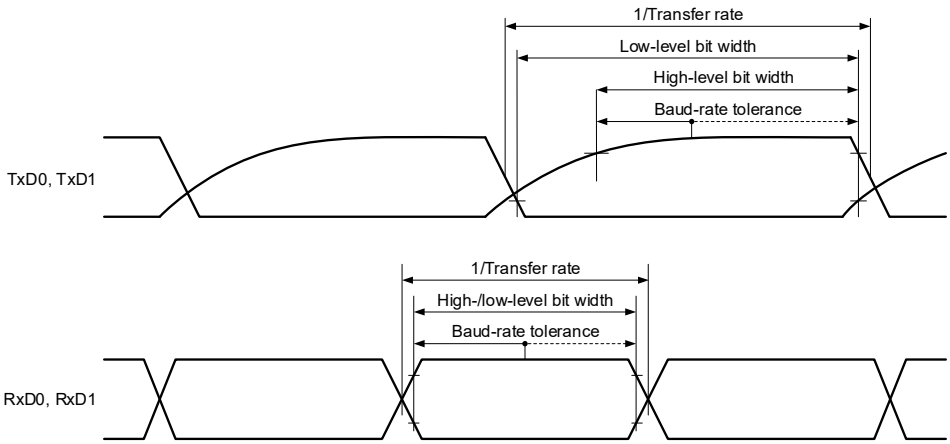
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate	–	Reception	2.7 V ≤ V_b ≤ EV_{DD0}, V_{IH} = 2.2 V, V_{IL} = 0.8 V				f_{MCK}/6	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF)			4.0	Mbps
		Transmission	2.7 V ≤ V_b ≤ EV_{DD0}, V_{OH} = 2.2 V, V_{OL} = 0.8 V				Smaller number of the values given by f_{MCK}/6 and expression 1 is applicable.	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF) Normal slew rate			4.0	Mbps

Note Expression 1: Maximum transfer rate = $1 / [\{-C_b \times R_b \times I_n (1 - 2.2/V_b)\} \times 3]$

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxD0 pin and RxD1 pin and N-ch open-drain output mode for the TxD0 pin and TxD1 pin.

Remarks 1. R_b [Ω]: Communication line (TxD) pull-up resistance, C_b [F]: Communication line (TxD) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

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(9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)

(T_A = -40 to +125°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	400[Note3]			ns
$\overline{\text{SCKp}}$ high-level width	t_{KH1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75			ns
$\overline{\text{SCKp}}$ low-level width	t_{KL1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 20			ns
SIp setup time (to $\overline{\text{SCKp}}$↑)[Note 1]	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
SIp setup time (to $\overline{\text{SCKp}}$↓)[Note 2]	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
SIp hold time (from $\overline{\text{SCKp}}$↑)[Note 1]	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
SIp hold time (from $\overline{\text{SCKp}}$↓)[Note 2]	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output[Note1]	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
Delay time from $\overline{\text{SCKp}}$↑ to SOp output[Note2]	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

<R> **3.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

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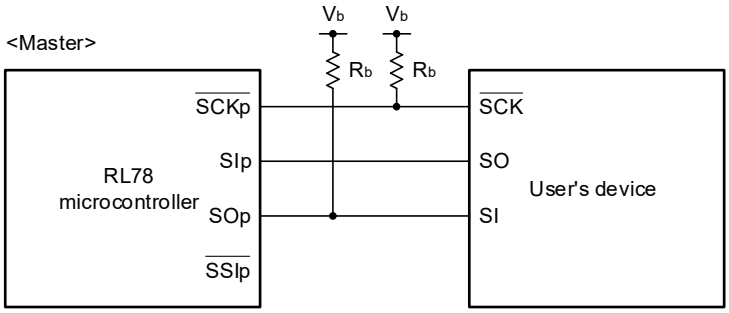
CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp pin and N-ch open-drain output mode for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remarks 1. R_b [Ω]: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, C_b [F]: Communication line (SOp, $\overline{\text{SCKp}}$) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:

When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

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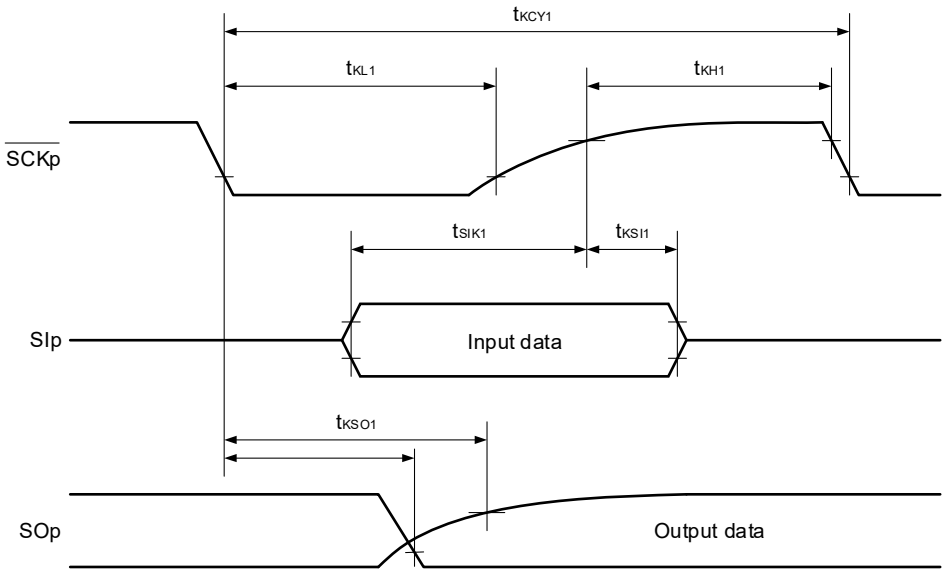
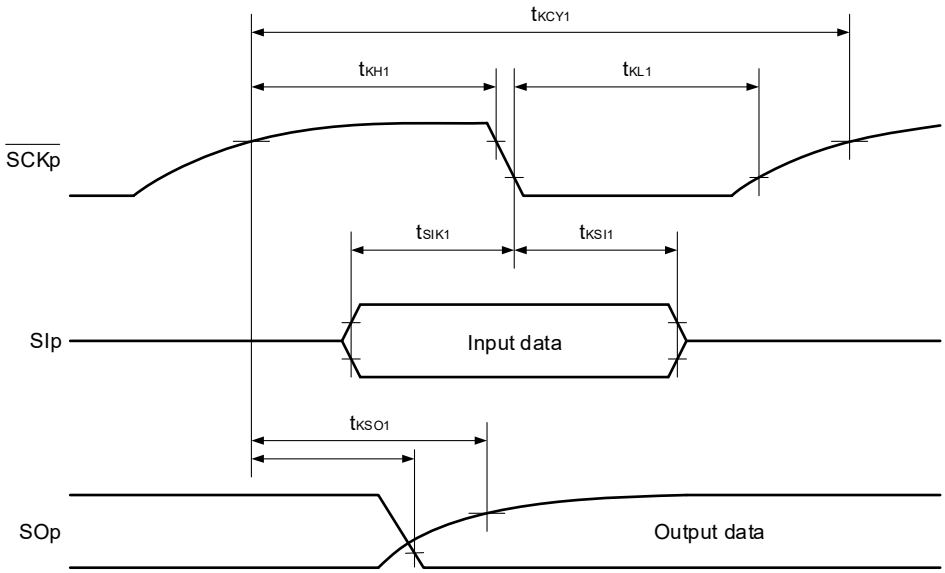
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



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(10) During communication at different potential (3-V supply system) (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, normal slew rate)

(T_A = -40 to +125°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	2.7 V ≤ V_b ≤ V_{DD}	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_b ≤ V_{DD}		t_{KCY2}/2 – 20			ns
SIp setup time (to $\overline{SCKp}$↑)Note 1	t_{SIK2}			90			ns
SIp hold time (from $\overline{SCKp}$↑)Note 2	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp outputNote 3	t_{KSO2}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

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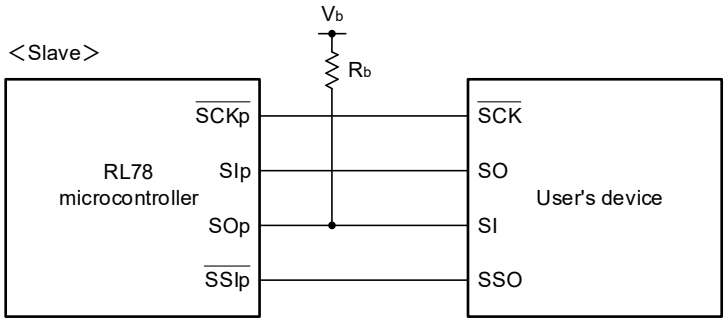
CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp, $\overline{\text{SCKp}}$ and $\overline{\text{SSIp}}$ pins and N-ch open-drain output mode for the SOp pin.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

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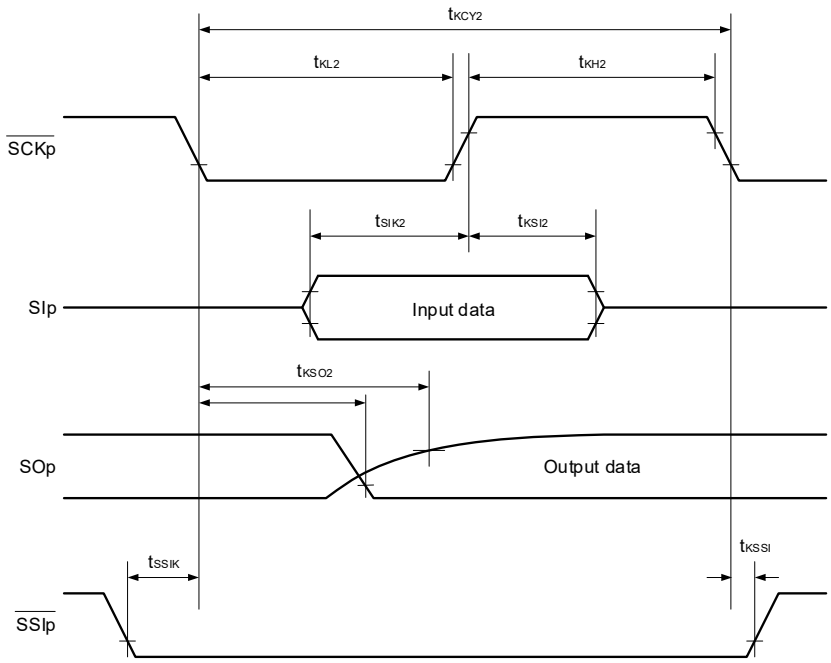
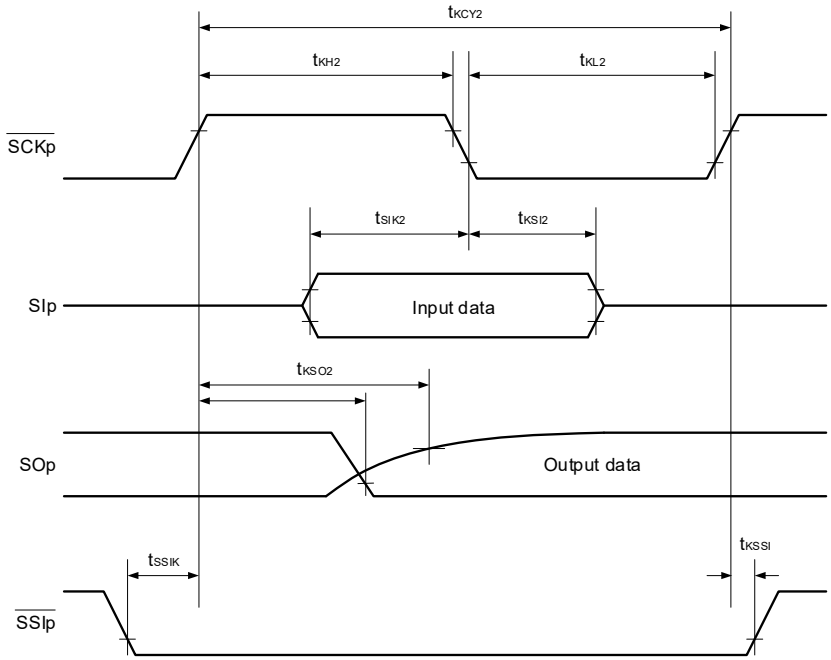
CSI mode serial transfer timing (slave mode) (during communication at different potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (slave mode) (during communication at different potential)

(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



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(11) During communication at different potential (3-V supply system) (simplified I²C mode)
(SDAr: TTL input buffer mode or N-ch open-drain output (EV_{DD0} tolerance) mode, SCLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

(T_A = -40 to +125°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	135 + 1/f_{MCK}		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	140	ns

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

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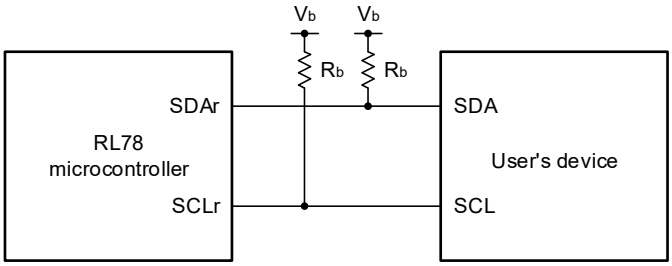
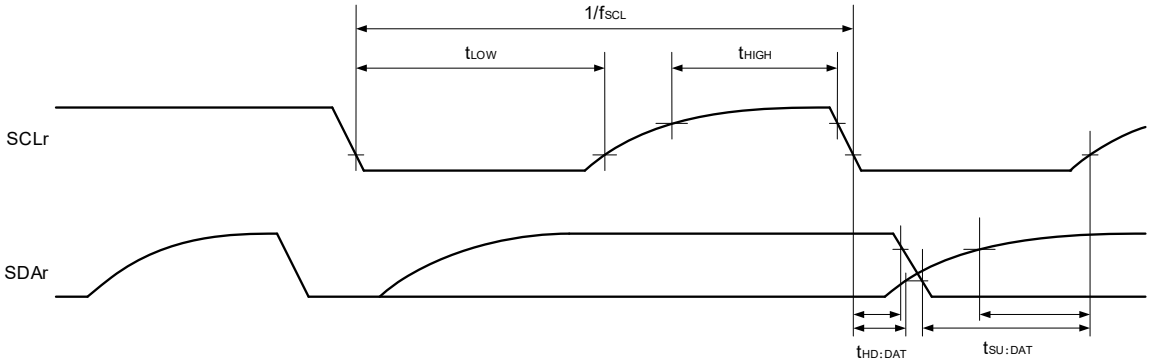
Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open-drain output mode for the SDAr pin and N-ch open-drain output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

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4.5.2 Serial Interface IICA

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

<R>

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: 10 MHz ≤ f_{MCK}					0	1000	kHz
		Fast mode: 3.5 MHz ≤ f_{MCK}			0	400			kHz
		Normal mode: 1 MHz ≤ f_{MCK}	0	100					kHz
Setup time of restart condition[Note 1]	$t_{SU:STA}$		4.7		0.6		0.26		μs
Hold time	$t_{HD:STA}$		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	0		μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		μs
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

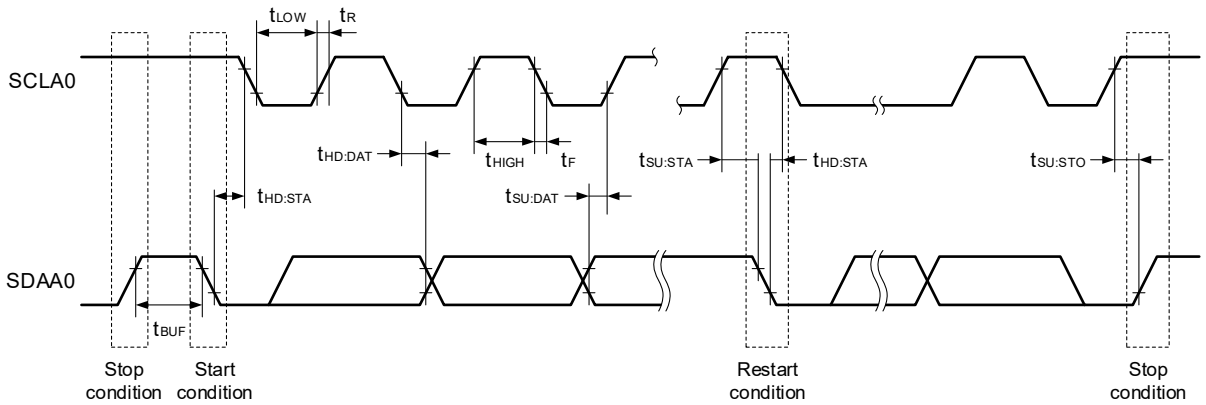
Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



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4.5.3 On-chip Debug (UART)

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-		115.2 k		1 M	bps

4.5.4 LIN/UART Module (RLIN3) UART Mode

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 to 24 MHz			4000	kbps
		SNOOZE mode	LIN communication clock source (f_{CLK}): 1 to 24 MHz FRQSEL4 = 0 in the user option byte (000C2H/020C2H)			4.8	
			LIN communication clock source (f_{CLK}): 1 to 24 MHz FRQSEL4 = 1 in the user option byte (000C2H/020C2H)			2.4	

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4.6 Analog Characteristics

4.6.1 A/D Converter Characteristics

(1) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI23 (power supply: V_{DD})

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±3.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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(2) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI24 to ANI30 (power supply: EV_{DD0})

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±4.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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(3) When AV_{REF} (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), AV_{REF} (-) = V_{SS} (ADREFM = 0), target ANI pin: ANI0 to ANI23, ANI24 to ANI30

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution ANI0 to ANI23	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±5.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.5	LSB
		10-bit resolution ANI24 to ANI30	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±6.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.50	%FSR
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.50	%FSR
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI23[Note 3]		0		V_{DD}	V
		ANI24 to ANI30[Note 3]		EV_{SS}		EV_{DD0}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. The number of pins depends on the product. For details, refer to **2.1 Pin Function List**.

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(4) When AV_{REF} (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI0, ANI2 to ANI23, ANI24 to ANI30

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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4.6.2 Temperatures Sensor Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.1		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

4.6.3 D/A Converter Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs

4.6.4 Comparator Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±40	mV
Input voltage range	V_{ICMP}		0		V_{DD}	V
Response time	t_{CR}, t_{CF}	Input amplitude ±100 mV		70	200	ns
Stabilization wait time during input channel switching[Note 1]	t_{WAIT}	Input amplitude ±100 mV	300			ns
Operation stabilization wait time[Note 2]	t_{CMP}	3.3 V ≤ V_{DD} ≤ 5.5 V	1			μs
		2.7 V ≤ V_{DD} < 3.3 V	3			μs

Notes 1. Period of time from when the comparator input channel is switched until the comparator is switched to output

2. Period of time from when the comparator operation is enabled (HCMPON bit in CMPCTL is set to 1) until the comparator satisfies the DC/AC characteristics.

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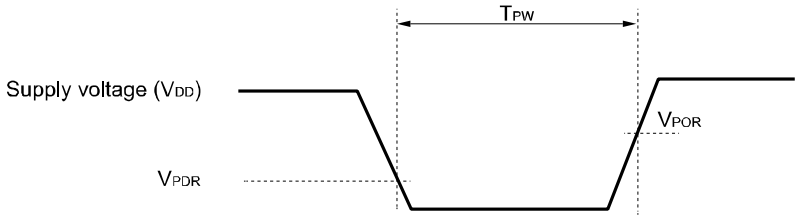
4.6.5 POR Circuit Characteristics

(T_A = -40 to +125°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage[Note 1]	V_{POR}	Power supply rise time	1.48	1.56	1.62	V
	V_{PDR}	Power supply fall time	1.47	1.55	1.61	V
Minimum pulse width[Note 2]	T_{PW}		300			μs
Detection delay time	T_{PD}				350	μs

Notes 1. This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}.



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4.6.6 LVD Circuit Characteristics

(1) LVD detection voltage of interrupt mode or reset mode

(T_A = -40 to +125°C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	4.62	4.74	4.94	V
			Power supply fall time	4.52	4.64	4.84	V
		V_{LVD1}	Power supply rise time	4.50	4.62	4.82	V
			Power supply fall time	4.40	4.52	4.71	V
		V_{LVD2}	Power supply rise time	4.30	4.42	4.61	V
			Power supply fall time	4.21	4.32	4.51	V
		V_{LVD3}	Power supply rise time	3.13	3.22	3.39	V
			Power supply fall time	3.07	3.15	3.31	V
		V_{LVD4}	Power supply rise time	2.95	3.02	3.17	V
			Power supply fall time	2.89	2.96	3.09	V
		V_{LVD5}	Power supply rise time	2.74	2.81	2.95	V
			Power supply fall time	2.68 Note	2.75	2.88	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

Note The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

(2) LVD detection voltage of interrupt & reset mode

(T_A = -40 to +125°C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 0, 1 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	2.88	V
	V_{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.61	V
			Falling interrupt voltage	4.21	4.32	4.51	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 0 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	2.88	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	4.82	V
			Falling interrupt voltage	4.40	4.52	4.71	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	2.88	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.39	V
			Falling interrupt voltage	3.07	3.15	3.31	V
	V_{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	4.94	V
			Falling interrupt voltage	4.52	4.64	4.84	V

Notes 1. These values indicate setting values of option bytes.

2. The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

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4.7 Power Supply Voltage Rising Time

(T_A = -40 to +125°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope	S_{vrmax}	0 V → V_{DD} (VPOC2 = 0 or 1[Note 2])			50[Note 3]	V/ms
Minimum power supply voltage rising slope [Note 1]	S_{vrmin}	0 V → 2.7 V	6.5			V/ms

Notes 1. The minimum power supply voltage rising slope is applied only under the following condition.
When the voltage detection (LVD) circuit is not used (VPOC2 = 1) and an external reset circuit is not used or when a reset is not effected until V_{DD} = 2.7 V.

2. These values indicate setting values of option bytes.

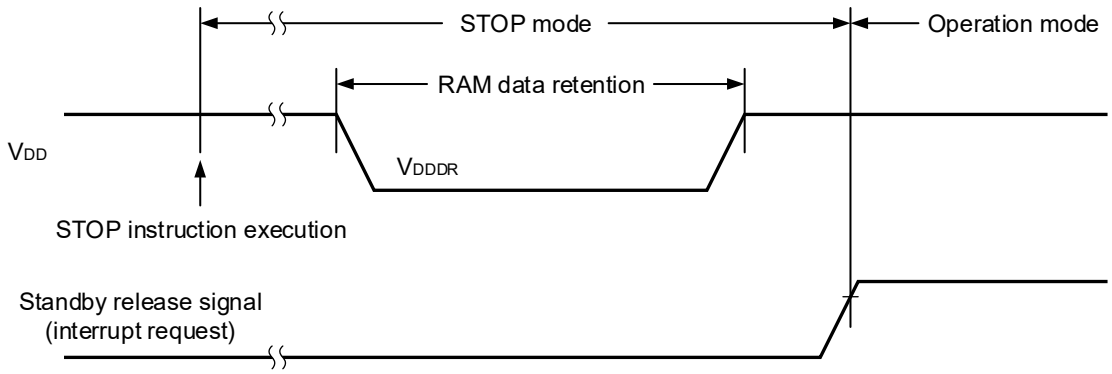
3. If the power supply drops below V_{PDR} and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to 0 V.

4.8 RAM Data Retention Characteristics

(T_A = -40 to +125°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



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4.9 Flash Memory Programming Characteristics

(T_A = -40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = +85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 20 years T_A = +85°C Note 4	10,000			
		Retained for 5 years T_A = +85°C Note 4	100,000			
Erase time	T_{erasa}	Block erase	5			ms
Write time	T_{wrwa}	1 word write	10			μs

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The specified data retention time is given under the condition that the average temperature (T_A) is 85°C or below.

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5. ELECTRICAL SPECIFICATIONS (GRADE Y)

Cautions 1. RL78/F13 and RL78/F14 have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

3. The pins mounted depending on the product. For details, refer to 1.5 Pin Configurations and 2.1 Pin Function List.

4. The products are classified into the following five groups according to the product type, pin count, and code flash memory size. In this chapter, the products are referred to by group names depending on the content. In this case, refer to the following classification.

Group A: RL78/F13 (LIN incorporated) products with 20, 30, 32, 48, or 64 pins and 16 Kbytes to 64 Kbytes of code flash memory

Group B: RL78/F13 (LIN incorporated) products with 48 or 64 pins and 96 Kbytes to 128 Kbytes of code flash memory or with 80 pins and 64 Kbytes to 128 Kbytes of code flash memory

Group C: RL78/F13 (CAN and LIN incorporated) products with 30, 32, 48, 64, or 80 pins and 32 Kbytes to 128 Kbytes of code flash memory

Group D: RL78/F14 products with 30, 32, 48, 64, or 80 pins and 48 Kbytes to 96 Kbytes of code flash memory

Group E: RL78/F14 products with 48, 64, or 80 pins and 128 Kbytes to 256 Kbytes of code flash memory or with 100 pins and 64 Kbytes to 256 Kbytes of code flash memory

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5.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	V_{SS}		-0.5 to +0.3	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD}+0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 4], P106, P107, P120, P125 to P127, P140, P150 to P157	-0.3 to EV_{DD0}+0.3 and -0.3 to V_{DD}+0.3[Note 2]	V
	V_{I2}	P33, P34, P80 to P87, P90 to P97[Note 4], P100 to P105, P121 to P124, P137, $\overline{\text{RESET}}$	-0.3 to V_{DD}+0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 4], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	-0.3 to EV_{DD0}+0.3 and -0.3 to V_{DD}+0.3[Note 2]	V
	V_{O2}	P33, P34, P80 to P87, P90 to P97[Note 4], P100 to P105	-0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI1}	ANI24 to ANI30	-0.3 to EV_{DD0}+0.3 and -0.3 to $AV_{REF(+)}$+0.3[Notes 2, 3]	V
	V_{AI2}	ANI0 to ANI23	-0.3 to V_{DD}+0.3 and -0.3 to $AV_{REF(+)}$+0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. For pins to be used in A/D conversion, the voltage should not exceed the value $AV_{REF(+)}$ + 0.3.

4. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 1], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	-40	mA
		Total of all pins -170 mA	P01, P02, P40 to P47, P92 to P97[Note 1], P120, P125 to P127, P150 to P153	-70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	-100	mA
	I_{OH2}	Per pin	P33, P34, P80 to P87, P90 to P97[Note 1], P100 to P105	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 1], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	40	mA
		Total of all pins 170 mA	P01, P02, P40 to P47, P92 to P97[Note 1], P120, P125 to P127, P150 to P153	70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	100	mA
	I_{OL2}	Per pin	P33, P34, P80 to P87, P90 to P97[Note 1], P100 to P105	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +150	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note 1. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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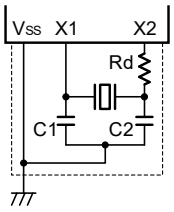
5.2 Oscillator Characteristics

5.2.1 Main System Clock Oscillator Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

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5.2.2 On-chip Oscillator Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Note]	f_{IH}		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy	-		-5		+5	%
Low-speed on-chip oscillator clock frequency	f_{IL}, f_{WDT}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	-		-15		+15	%

Note High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/020C2H) and bits 0 to 2 of the HOCODIV register.

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5.2.3 Subsystem Clock Oscillator Characteristics

Do not use the XT1 oscillator.

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5.2.4 PLL Circuit Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
PLL input enable clock frequency[Note 1]	f_{PLLI}	PLLMUL = 0	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
		PLLMUL = 1	PLLDIV0 = 0	3.92	4.0	4.08	MHz
			PLLDIV0 = 1	7.84	8.0	8.16	MHz
PLL output frequency (center value)	f_{PLL}	PLLMUL = 0	PLLDIV0 = 0	f_{PLLI} × 12/2			MHz
			PLLDIV0 = 1	f_{PLLI} × 12/4			MHz
		PLLMUL = 1 [Note 4]	PLLDIV0 = 0 [Note 4]	f_{PLLI} × 16/2			MHz
			PLLDIV0 = 1	f_{PLLI} × 16/4			MHz
Long-term jitter[Notes 2, 3]	t_{LJ}	f_{PLL} = 24 MHz (480 counts)		-2		+2	ns
		f_{PLL} = 32 MHz (640 counts)		-2		+2	ns
		f_{PLL} = 48 MHz (960 counts)		-2		+2	ns

Notes 1. If the high-speed on-chip oscillator clock is to be selected as the PLL input clock, the minimum and maximum values will reflect the range of accuracy of the oscillation frequency by the high-speed on-chip oscillator clock.

2. Guaranteed by design, but not tested before shipment.

3. Indicates 20 μs.

4. Setting of PLLMUL = 1 and PLLDIV0 = 0 is prohibited when f_{PLLI} > 6 MHz.

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5.3 DC Characteristics

5.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **2. PIN FUNCTIONS**.

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 3], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-5.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-3.0	mA
		Per pin for P10, P12, P14, P30,P120,P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-0.6	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-0.2	mA
		Total of P01, P02, P40 to P47, P92 to P97[Note 3], P120, P125 to P127, P150 to P153 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
		Total of P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-32.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-29.0	mA
	I_{OH2}	Per pin for P33, P34, P80 to P87, P90 to P97[Note 3], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V			-0.1	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	2.7 V ≤ V_{DD} ≤ 5.5 V			-2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from pins EV_{DD0}, EV_{DD1} and V_{DD} to an output pin.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%.

The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode. P10 to P12 and P70 to P72 of the Group A products do not support N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note 3], P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			8.5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			4.0	mA
		Per pin for P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			0.59	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			0.07	mA
		Total of P01, P02, P40 to P47, P92 to P97[Note 3], P120, P125 to P127, P150 to P153 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
		Total of P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			35.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			30.0	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			55.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			45.0	mA
	I_{OL2}	Per pin for P33, P34, P80 to P87, P90 to P97[Note 3], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V			0.4	mA
		Total of all pins (for duty factors ≤ 70%[Note 2])	2.7 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows to the EV_{SS0}, EV_{SS1} and V_{SS} pins from an output pin.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.65 EV_{DD0}		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.7 EV_{DD0}		EV_{DD0} Note 1	V
	V_{IH2}	P10, P11, P13, P14, P16, P17, P30, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152, P153 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.8 EV_{DD0}		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.85 EV_{DD0}		EV_{DD0} Note 1	V
	V_{IH3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0} Note 1	V
			2.7 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0} Note 1	V
	V_{IH4} Note 2	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.85 V_{DD}		V_{DD}	V
	V_{IH5}	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.65 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.7 V_{DD}		V_{DD}	V
	V_{IH6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.8 V_{DD}		V_{DD}	V

Notes 1. The maximum value of V_{IH} of the pins P10 to P17, P60 to P63, P70 to P72, and P120 is EV_{DD0}, even in N-ch open-drain mode.

2. P92 to P96 of the Group A products are fixed to Schmitt 1 mode.
P96 and P97 of the Group B, C, and D products are fixed to Schmitt 1 mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.35 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.3 EV_{DD0}	V
	V_{IL2}	P10, P11, P13, P14, P16, P17, P30, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P125, P150, P152, P153 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.5 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.4 EV_{DD0}	V
	V_{IL3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
	V_{IL4} Note	P33, P34, P80 to P87, P90 to P97, P100 to P105, P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.5 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.4 V_{DD}	V
	V_{IL5}	$\overline{\text{RESET}}$ (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.35 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.3 V_{DD}	V
	V_{IL6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V

Note P92 to P96 of the Group A products are fixed to Schmitt 1 mode.
P96 and P97 of the Group B, C, and D products are fixed to Schmitt 1 mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/6)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -5.0 mA	EV_{DD0}-0.9			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0}-0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.0 mA	EV_{DD0}-0.5			V
	V_{OH2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V I_{OH2} = -100 μA	V_{DD}-0.5			V
	V_{OH3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = -0.6 mA	EV_{DD0}-0.8			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = -0.2 mA	EV_{DD0}-0.5			V
Output voltage, low	V_{OL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105	2.7 V ≤ V_{DD} ≤ 5.5 V I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.6 mA			0.8	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.07 mA			0.5	V

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (6/6)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{DD0}				1	μA
	I_{LIH2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105, P137, $\overline{RESET}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97[Note], P106, P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{SS0}				-1	μA
	I_{LIL2}	P33, P34, P80 to P87, P90 to P97[Note], P100 to P105, P137, $\overline{RESET}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97, P100 to P107, P120, P125 to P127, P140, P150 to P157	V_I = EV_{SS0}, in input port		10	20	100	kΩ

Note For pin I/O buffer power supplies, refer to **Table 2-1 Pin I/O Buffer Power Supplies**.

Caution P10 to P17, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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5.3.2 Supply Current Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/3)

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 48 MHz	f_{CLK} = 24 MHz Notes 3, 4		5.1	12.5	mA
					f_{IH} = 24 MHz	f_{CLK} = f_{IH} Notes 3, 4		4.8	11.5	mA
					f_{IH} = 1 MHz	f_{CLK} = f_{IH} Notes 3, 4		1.0	2.6	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		4.2	9.5	mA
					f_{MX} = 1 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.9	2.6	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 48 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz Notes 3, 6		5.0	12.5	mA
					f_{PLL} = 24 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz Notes 3, 6		4.9	11.5	mA
					f_{PLL} = 24 MHz, f_{MX} = 4 MHz	f_{CLK} = 24 MHz Notes 3, 6		4.7	11.5	mA
				Subsystem clock operation (f_{SUB} = f_{EXS})	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7				
						Groups A to D		6.0	170.0	μA
						Group E		6.0	270.0	μA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8				
						Groups A to D		3.0	160.0	μA
						Group E		3.0	260.0	μA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

Remarks 1. f_{MX}: High-speed system clock frequency

2. f_{SUB}: Subsystem clock frequency

3. f_{EXS}: External subsystem clock frequency

4. f_{PLL}: PLL clock frequency

5. f_{IH}: High-speed on-chip oscillator clock frequency

6. f_{IL}: Low-speed on-chip oscillator clock frequency

7. f_{CLK}: CPU/peripheral hardware clock frequency

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 3]	I_{DD2}	HALT mode[Note 2]	High-speed on-chip oscillator clock operation	f_{IH} = 48 MHz	f_{CLK} = 24 MHz [Note 5]		0.9	8.5	mA
				f_{IH} = 24 MHz	f_{CLK} = f_{IH} [Note 5]		0.7	7.5	mA
				f_{IH} = 1 MHz	f_{CLK} = f_{IH} [Note 5]		0.3	1.6	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} [Note 6]		0.6	6.5	mA
				f_{MX} = 1 MHz	f_{CLK} = f_{MX} [Note 6]		0.2	1.6	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 48 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz [Note 7]		0.9	8.5	mA
				f_{PLL} = 24 MHz, f_{MX} = 8 MHz	f_{CLK} = 24 MHz [Note 7]		0.8	7.5	mA
				f_{PLL} = 24 MHz, f_{MX} = 4 MHz	f_{CLK} = 24 MHz [Note 7]		0.6	7.5	mA
			Subsystem clock operation (f_{SUB} = f_{EXS})	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} [Note 8]				
				Groups A to D			0.7	165.0	μA
				Group E			0.7	265.0	
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} [Note 9]				
				Groups A to D			0.7	155.0	μA
				Group E			0.7	255.0	
	I_{DD3}	STOP mode[Note 4]	T_A = +25°C	Groups A to D			0.5		μA
				Group E			0.5		
			T_A = +50°C	Groups A to D				2.5	
				Group E				4.5	
			T_A = +70°C	Groups A to D				4.5	
				Group E				8.0	
			T_A = +105°C	Groups A to D				30.0	
				Group E				50.0	
			T_A = +125°C	Groups A to D				60.0	
				Group E				100.0	
			T_A = +150°C	Groups A to D				150.0	
				Group E				250.0	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

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6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped.

Remarks
1. f_{MX}: High-speed system clock frequency
2. f_{SUB}: Subsystem clock frequency
3. f_{EXS}: External subsystem clock frequency
4. f_{PLL}: PLL clock frequency
5. f_{IH}: High-speed on-chip oscillator clock frequency
6. f_{IL}: Low-speed on-chip oscillator clock frequency
7. f_{CLK}: CPU/peripheral hardware clock frequency

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 2]	I_{SNOZ}	SNOOZE mode	A/D converter operation	During mode transition			1.0	1.3	mA
				During conversion	Low-voltage mode AV_{REFP} = V_{DD} = 5.0 V		2.1	2.6	mA
			DTC operation				4.5		mA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. The values below the MAX. column include the STOP leakage current.

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
		When internal reference voltage is selected Note 5			75.0		μA
LVD operating current	I_{LVD} Note 4				0.08		μA
Temperature sensor operating current	I_{TMPS}				75.0		μA
D/A converter operating current	I_{DAC}	Per channel			0.8	1.5	mA
Comparator operating current	I_{CMP}				50.0		μA
BGO operating current	I_{BGO} Note 6				2.50	12.20	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

5. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

6. Current increased by the BGO operation. The current value is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in operation mode or HALT mode.

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5.4 AC Characteristics

5.4.1 Basic Operation

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	High-speed on-chip oscillator clock operation		0.04166		1	μs
		High-speed system clock operation		0.05		1	μs
		PLL clock operation		0.04166		1	μs
		Subsystem clock operation		28.5	30.5	34.5	μs
		Low-speed on-chip oscillator clock operation			66.6		μs
		In self programming mode		0.04166		1	μs
CPU/peripheral hardware clock frequency	f_{CLK}			0.04166		66.6	μs
External system clock frequency	f_{EX}			1.0		20.0	MHz
	f_{EXS}			29		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}			$1/f_{MCK}+10$			ns
TO00 to TO07, TO10 to TO17 output frequency	f_{TO}	All TO pins, Normal slew rate, C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			12	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			6	MHz
		TO01, TO06, TO07, TO11, TO13 only, Special slew rate, C = 30 pF				2	MHz
PCLBUZ0 output frequency	f_{PCL}	Normal slew rate C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			12	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			6	MHz
		Special slew rate C = 30 pF				2	MHz
Timer RJ input cycle	t_C	TRJIO0		100			ns
Timer RJ input high-level width, low-level width	t_{WH}, t_{WL}	TRJIO0		40			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP13 Note		1			μs
KR0 to KR7 key interrupt input low-level width	t_{KR}			250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Note Pins $\overline{\text{RESET}}$, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

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(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

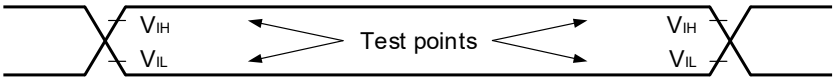
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Port output rise time, port output fall time	t_{RO}, t_{FO}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P96, P97, P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			25	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V		25 Note	60	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			100	ns

Note T_A = +25°C, EV_{DD0} = 5.0 V

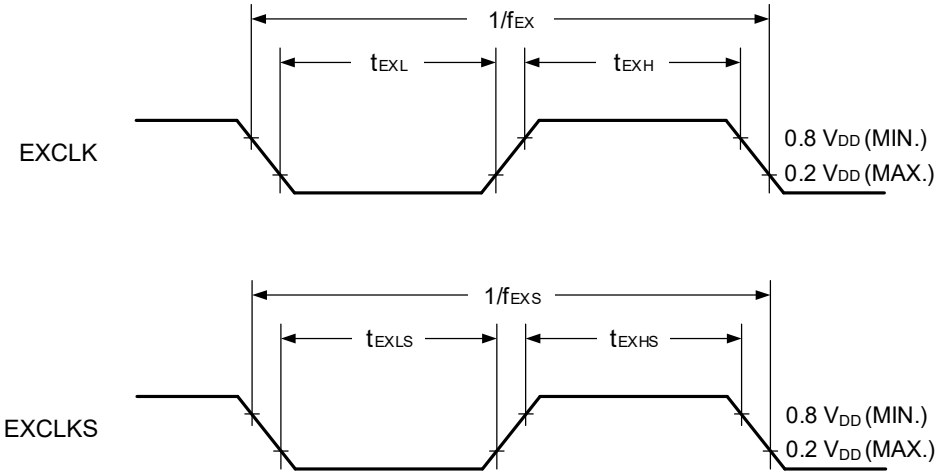
Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

AC Timing Test Points



External System Clock Timing



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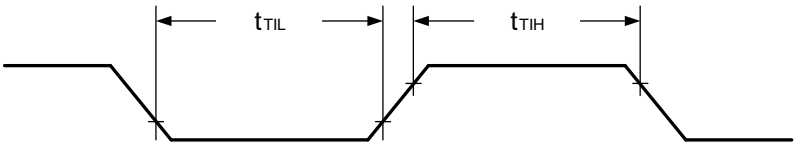
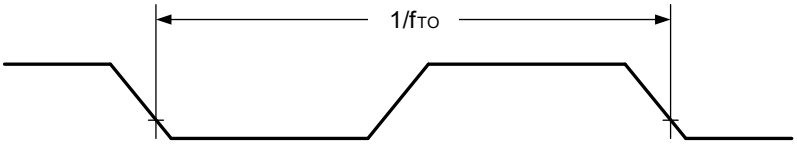
TI/TO Timing

TI00 to TI07, TI10 to TI17

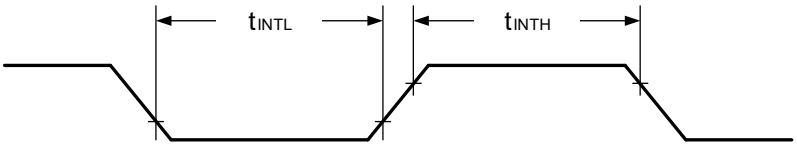


TO00 to TO07, TO10 to TO17



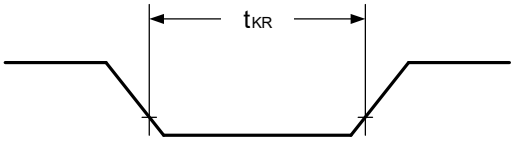
Interrupt Request Input Timing

INTP0 to INTP13



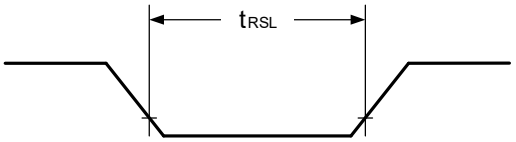
Key Interrupt Input Timing

KR0 to KR7



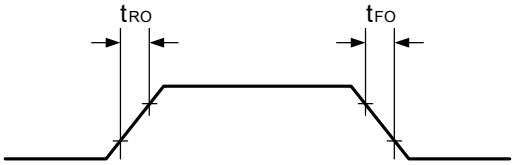
RESET Input Timing

$\overline{\text{RESET}}$



Output Rising and Falling Timing

Output pin



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5.5 Peripheral Functions Characteristics

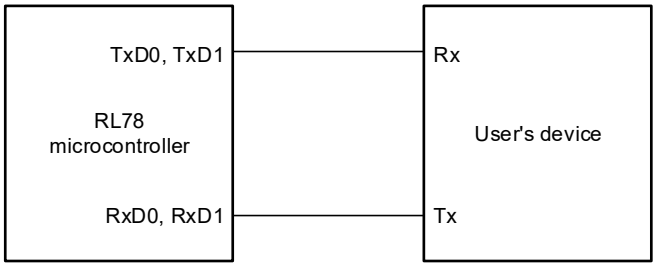
5.5.1 Serial Array Unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

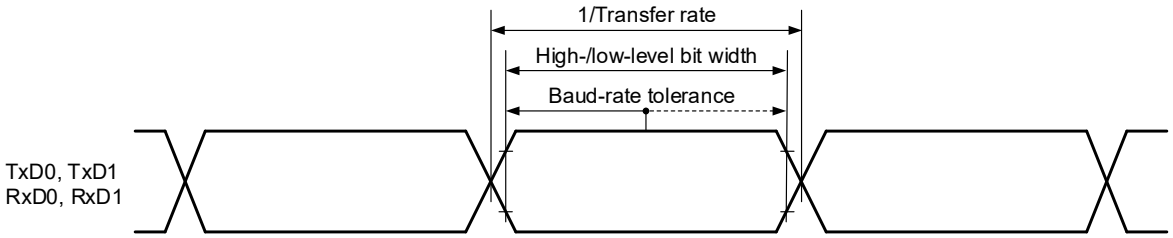
(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-					f_{MCK}/6	bps
		f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}	Normal slew rate			4	Mbps
			Special slew rate			2	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxD0 pin and RxD1 pin and normal output mode for the TxD0 pin and TxD1 pin.

Remark f_{MCK}: Serial array unit operation clock frequency

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(2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}		166.6 Note 5			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	t_{KCY1}/2 – 12			ns
		2.7 V ≤ EV_{DD0} < 4.0 V	t_{KCY1}/2 – 18			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	55			ns
		2.7 V ≤ EV_{DD0} < 4.0 V	66			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 2	t_{KSI1}		30			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

<R> **5.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

Caution Select the normal input buffer for the SIp pin and normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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(3) During communication at same potential (CSI mode) (master mode, $\overline{SCKp}$ … internal clock output, special slew rate)

(T_A = -40 to +150°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}		500 Note 5			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 – 60			ns
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK1}		120			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}		80			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			90	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

<R> **5.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

Caution Select the normal input buffer for the SIp pin and normal output mode and special slew rate for the SOp pin and $\overline{SCKp}$ pin.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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(4) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, normal slew rate)

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}			8/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			1/f_{MCK} + 20			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]	4.0V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5V			2/f_{MCK} + 44	ns
			2.7V ≤ V_{DD} = EV_{DD0} = EV_{DD1} < 4.0V			2/f_{MCK} + 60	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp, $\overline{SCKp}$ and $\overline{SSIp}$ pins and normal output mode for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

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(5) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$ … external clock input, special slew rate)

(T_A = -40 to +150°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	20 MHz < f_{MCK}	10/f_{MCK}			ns
		10 MHz < f_{MCK} ≤ 20 MHz	8/f_{MCK}			ns
		f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-level width, low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)Note1	t_{SIK2}		80			ns
SIp hold time (from $\overline{SCKp}$↑)Note 2	t_{KSI2}		1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp outputNote 3	t_{KSO2}	C = 30 pFNote 4			2/f_{MCK} + 80	ns
$\overline{SSIp}$ setup time	t_{SSIK}	DAP = 0	120			ns
		DAP = 1	1/f_{MCK} + 120			ns
$\overline{SSIp}$ hold time	t_{KSSI}	DAP = 0	1/f_{MCK} + 120			ns
		DAP = 1	120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp, $\overline{SCKp}$ and $\overline{SSIp}$ pins and normal output mode and special slew rate for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

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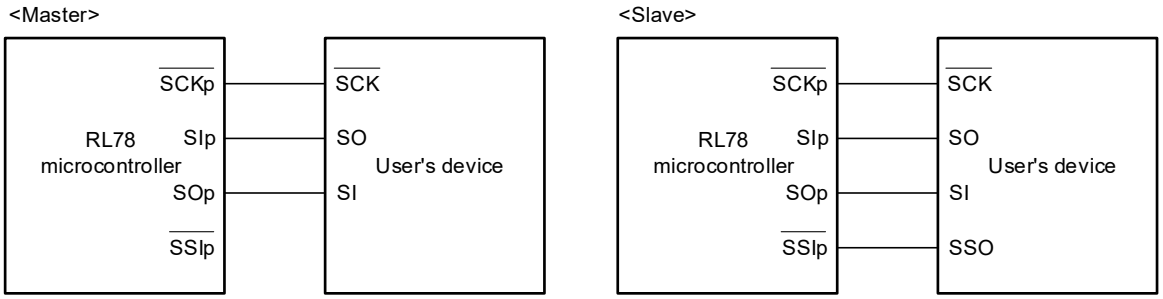
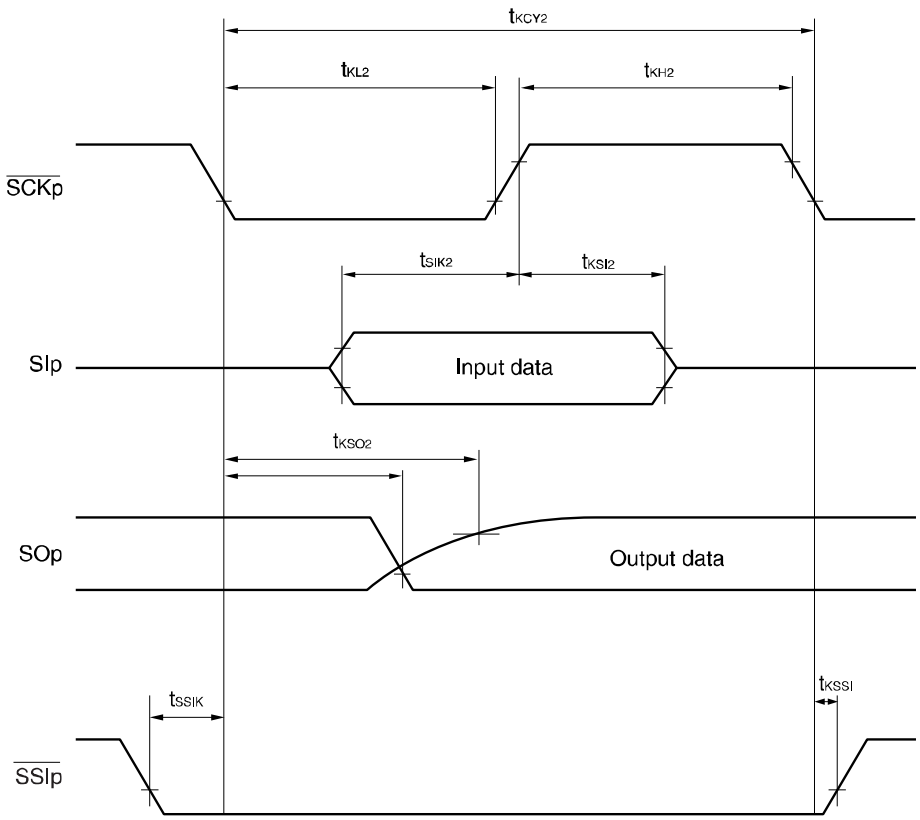
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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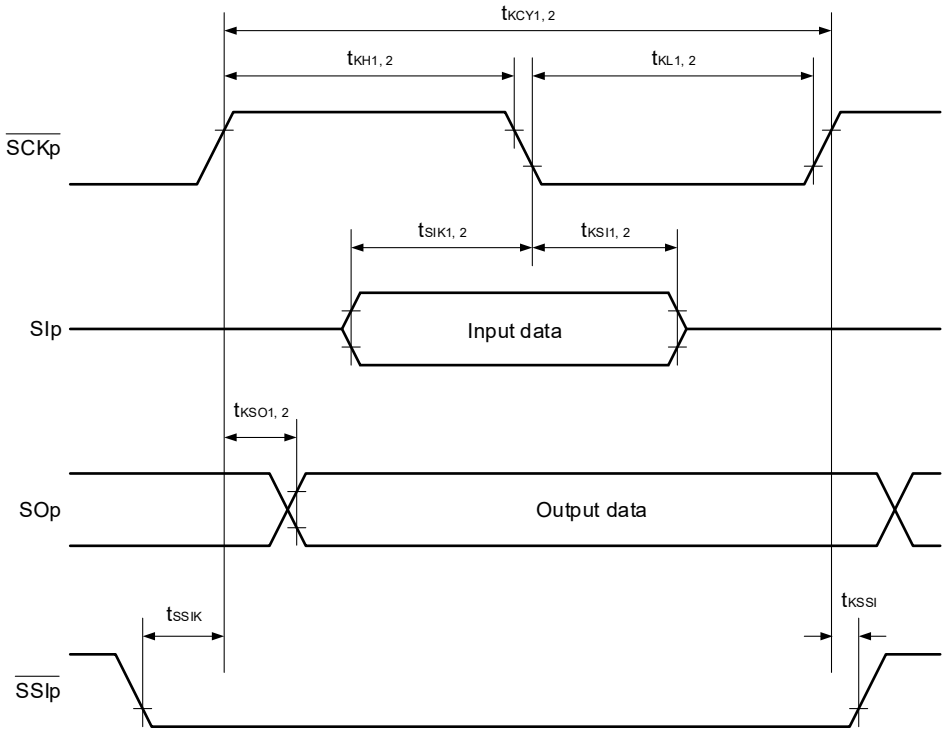
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

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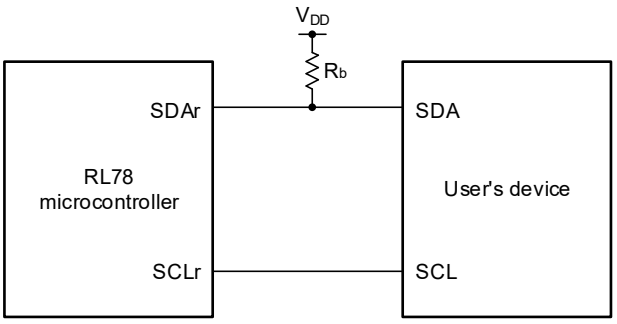
(6) During communication at same potential (simplified I²C mode)
(SDAr: N-ch open-drain output (EV_{DD0} tolerance) mode, SCLr: normal output mode)

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

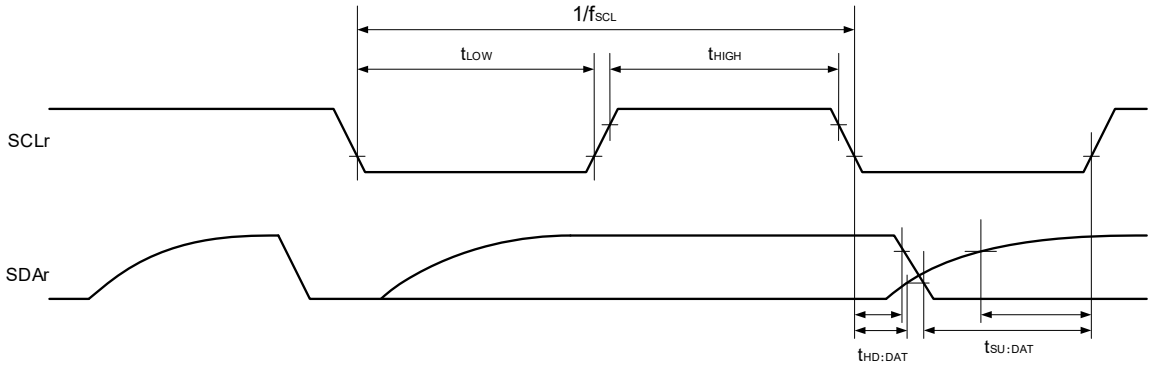
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f_{SCL}				1000[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}		475			ns
Hold time when SCLr = "H"	t_{HIGH}		475			ns
Data setup time (reception)	$t_{SU:DAT}$		$1/f_{MCK}$ + 85			ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 50 pF, R_b = 2.7 kΩ	0		305	ns

Note f_{SCL} ≤ $f_{MCK}/4$ must also be satisfied.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and normal output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

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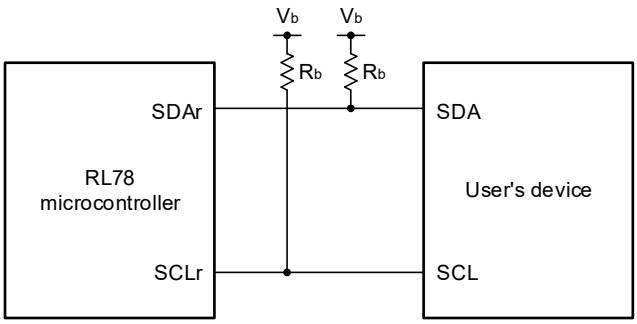
(7) During communication at same potential (simplified I²C mode) (SDAr and SCLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}			400[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1300		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	600		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1/f_{MCK} + 120		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 270		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 2.7 kΩ	0	300	ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

Simplified I²C mode connection diagram (during communication at same potential)



Caution Select the normal input buffer and N-ch open-drain output mode for the SDAr pin and SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

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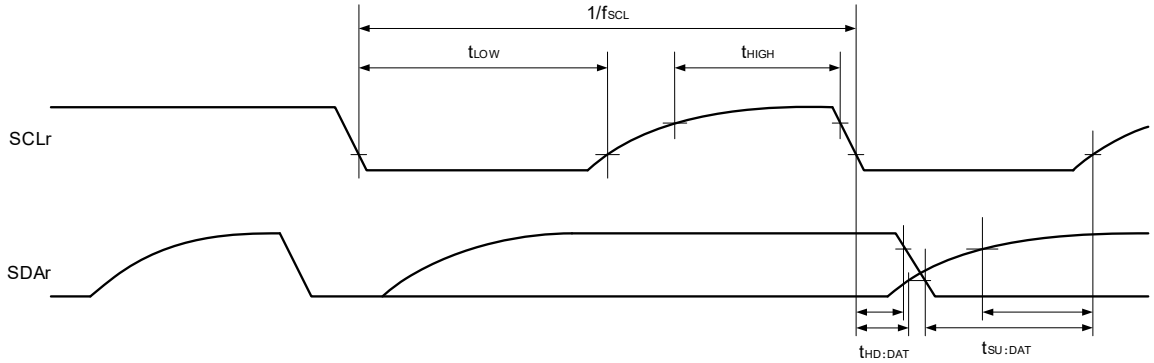
Simplified I²C mode serial transfer timing (during communication at same potential)



Remark r: IICr (r = 00, 01, 10, 11)

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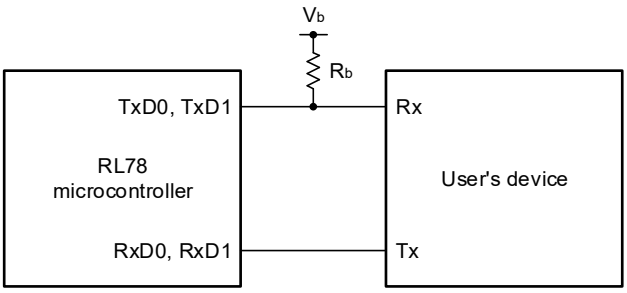
(8) Communication at different potential (UART mode) (TxD output buffer: N-ch open-drain, RxD input buffer: TTL)

(T_A = -40 to +150°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

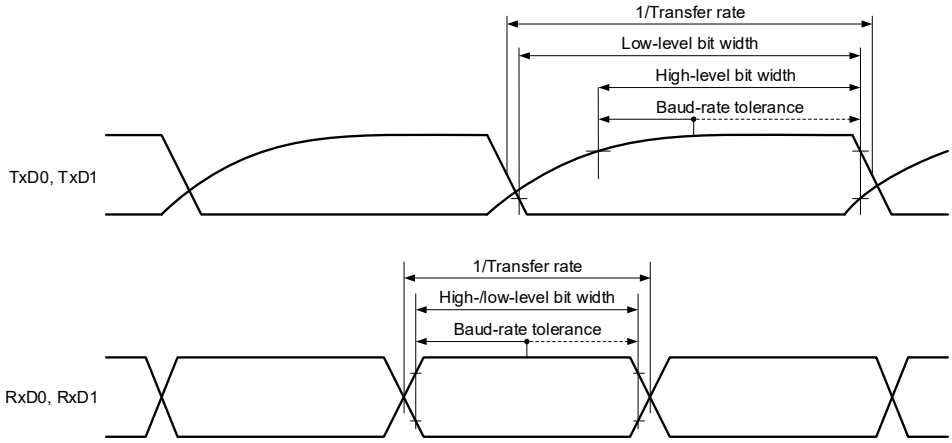
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate	–	Reception	2.7 V ≤ V_b ≤ EV_{DD0}, V_{IH} = 2.2 V, V_{IL} = 0.8 V				f_{MCK}/6	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF)			4.0	Mbps
		Transmission	2.7 V ≤ V_b ≤ EV_{DD0}, V_{OH} = 2.2 V, V_{OL} = 0.8 V				Smaller number of the values given by f_{MCK}/6 and expression 1 is applicable.	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF) Normal slew rate			4.0	Mbps

Note Expression 1: Maximum transfer rate = $1 / [\{-C_b \times R_b \times \ln (1 - 2.2/V_b)\} \times 3]$

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxD0 pin and RxD1 pin and N-ch open-drain output mode for the TxD0 pin and TxD1 pin.

Remarks 1. R_b [Ω]: Communication line (TxD) pull-up resistance, C_b [F]: Communication line (TxD) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

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(9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)

(T_A = -40 to +150°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

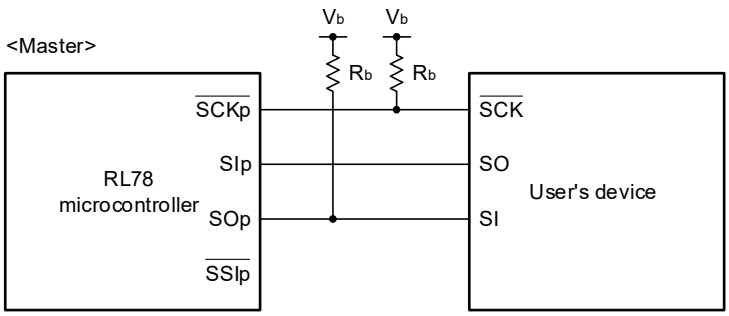
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	400 Note3			ns
$\overline{\text{SCKp}}$ high-level width	t_{KH1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75			ns
$\overline{\text{SCKp}}$ low-level width	t_{KL1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 20			ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 1	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
SIp setup time (to $\overline{\text{SCKp}}$↓) Note 2	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 1	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
SIp hold time (from $\overline{\text{SCKp}}$↓) Note 2	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note1	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
Delay time from $\overline{\text{SCKp}}$↑ to SOp output Note2	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

<R> **3.** t_{KCY1} ≥ 4/f_{MCK} must also be satisfied.

CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp pin and N-ch open-drain output mode for the SOp pin and $\overline{\text{SCKp}}$ pin.

Remarks 1. R_b [Ω]: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, C_b [F]: Communication line (SOp, $\overline{\text{SCKp}}$) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:

When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

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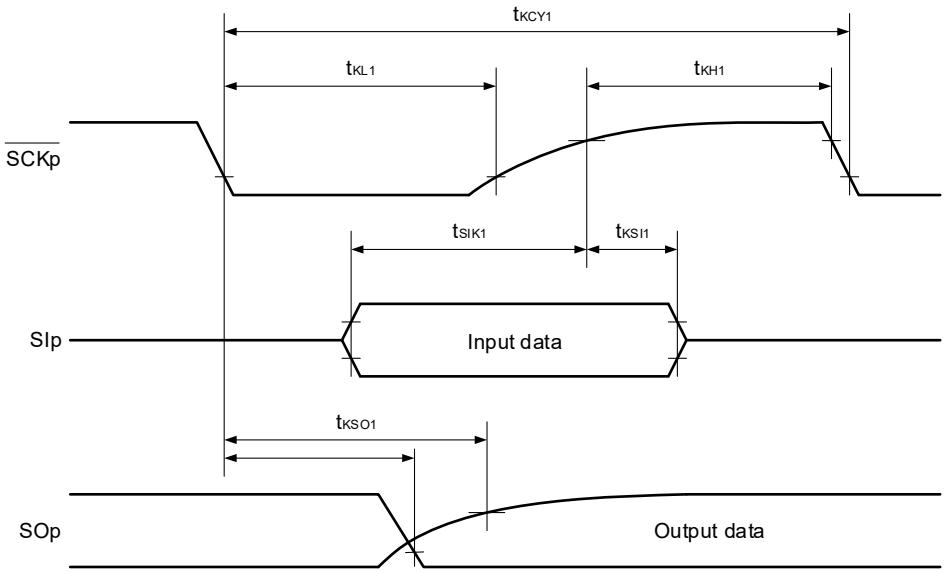
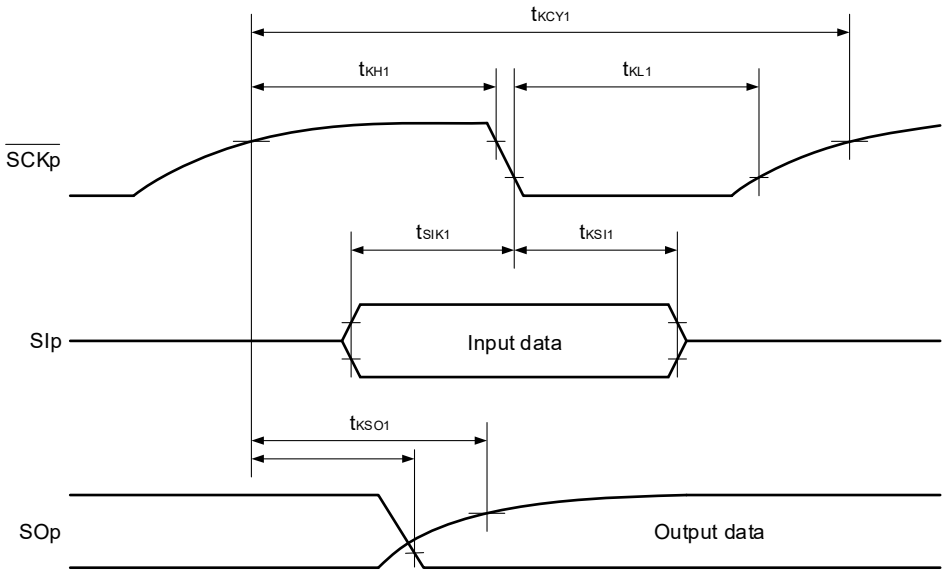
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



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(10) During communication at different potential (3-V supply system) (CSI mode) (slave mode, $\overline{\text{SCKp}}$ … external clock input, normal slew rate)

(T_A = -40 to +150°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	t_{KCY2}	2.7 V ≤ V_b ≤ V_{DD}	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
$\overline{\text{SCKp}}$ high-level width, low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_b ≤ V_{DD}		t_{KCY2}/2 – 20			ns
SIp setup time (to $\overline{\text{SCKp}}$↑)[Note 1]	t_{SIK2}			90			ns
SIp hold time (from $\overline{\text{SCKp}}$↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output[Note 3]	t_{KSO2}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
$\overline{\text{SSIp}}$ setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
$\overline{\text{SSIp}}$ hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

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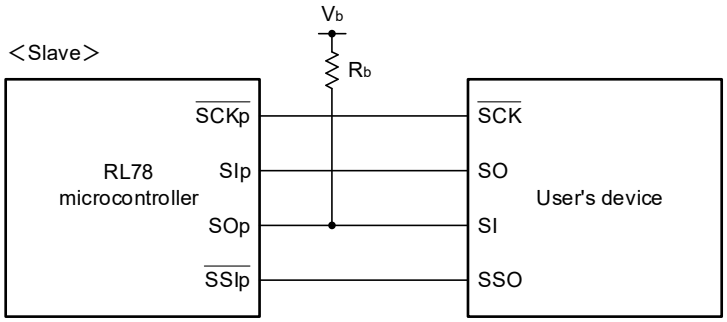
CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp, $\overline{\text{SCKp}}$ and $\overline{\text{SSIp}}$ pins and N-ch open-drain output mode for the SOp pin.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:

When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

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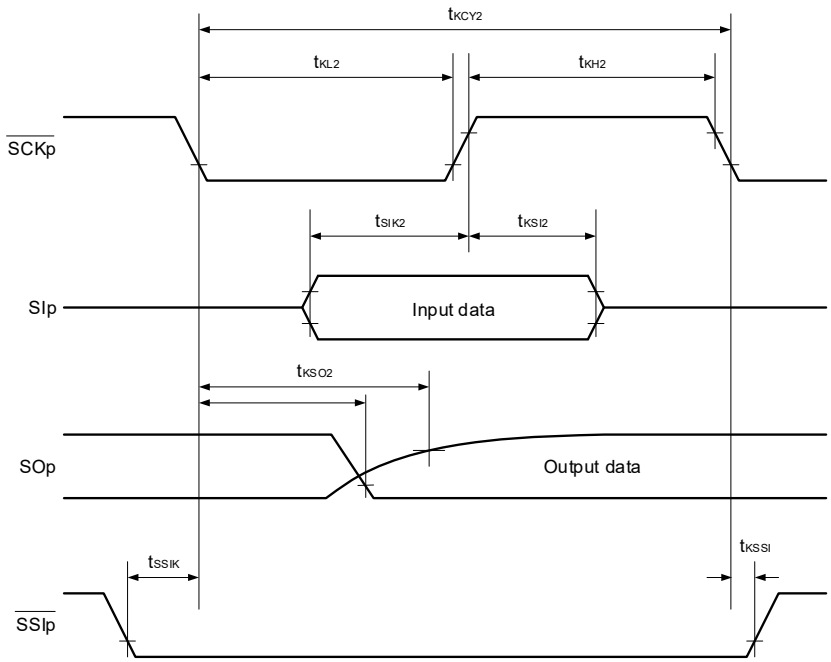
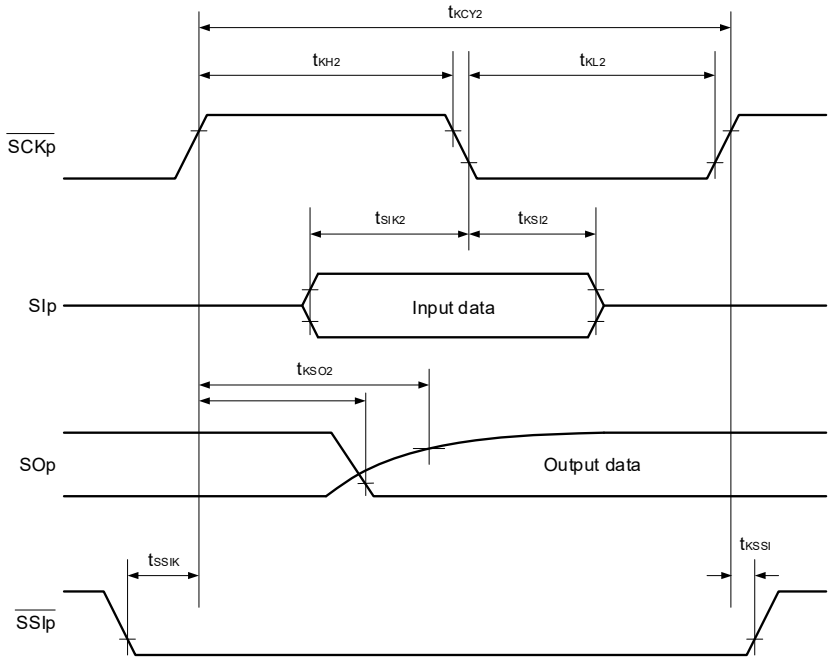
CSI mode serial transfer timing (slave mode) (during communication at different potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (slave mode) (during communication at different potential)

(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



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(11) During communication at different potential (3-V supply system) (simplified I²C mode)
(SDAr: TTL input buffer mode or N-ch open-drain output (EV_{DD0} tolerance) mode, SCLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

(T_A = -40 to +150°C, 4.0 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400[Note]	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	135 + 1/f_{MCK}		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	140	ns

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

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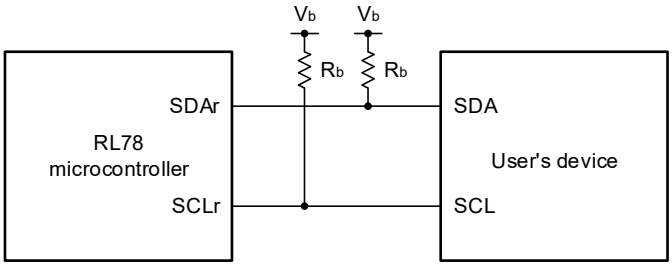
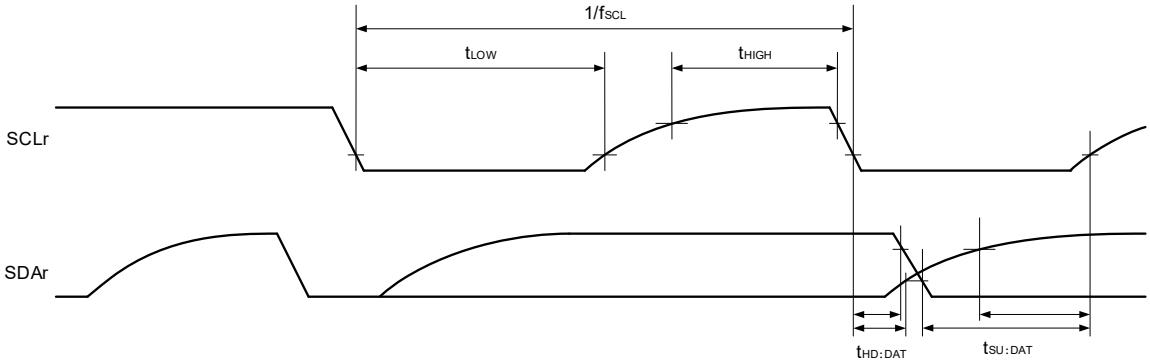
Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open-drain output mode for the SDAr pin and N-ch open-drain output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b [F]: Communication line (SDAr, SCLr) load capacitance, V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

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5.5.2 Serial Interface IICA

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

<R>

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: 10 MHz ≤ f_{MCK}					0	1000	kHz
		Fast mode: 3.5 MHz ≤ f_{MCK}			0	400			kHz
		Normal mode: 1 MHz ≤ f_{MCK}	0	100					kHz
Setup time of restart condition[Note 1]	$t_{SU:STA}$		4.7		0.6		0.26		μs
Hold time	$t_{HD:STA}$		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	0		μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		μs
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

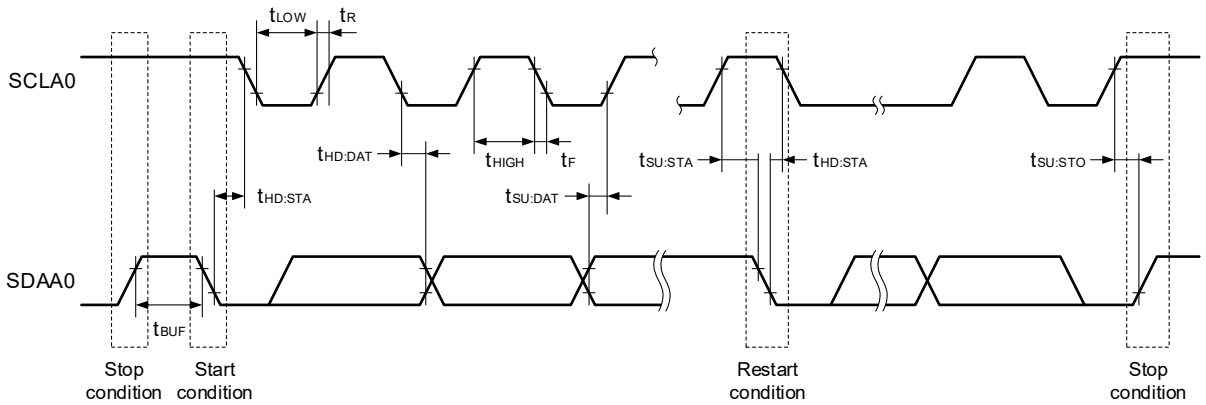
Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



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5.5.3 On-chip Debug (UART)

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-		115.2 k		1 M	bps

5.5.4 LIN/UART Module (RLIN3) UART Mode

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 to 24 MHz			4000	kbps
		SNOOZE mode	LIN communication clock source (f_{CLK}): 1 to 24 MHz FRQSEL4 = 0 in the user option byte (000C2H/020C2H)			2.4	
			LIN communication clock source (f_{CLK}): 1 to 24 MHz FRQSEL4 = 1 in the user option byte (000C2H/020C2H)			1.2	

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5.6 Analog Characteristics

5.6.1 A/D Converter Characteristics

(1) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI23 (power supply: V_{DD})

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±3.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.52	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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(2) When AV_{REF} (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI24 to ANI30 (power supply: EV_{DD0})

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±4.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.52	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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(3) When AV_{REF} (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), AV_{REF} (-) = V_{SS} (ADREFM = 0), target ANI pin: ANI0 to ANI23, ANI24 to ANI30

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution ANI0 to ANI23	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±5.0	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±5.5	LSB
		10-bit resolution ANI24 to ANI30	4.0 V ≤ V_{DD} ≤ 5.5 V		±1.2	±6.5	LSB
			2.7 V ≤ V_{DD} < 4.0 V		±1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution	4.0 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 4.0 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.50	%FSR
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.50	%FSR
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution ANI0 to ANI23	2.7 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
		10-bit resolution ANI24 to ANI30	2.7 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI23[Note 3]		0		V_{DD}	V
		ANI24 to ANI30[Note 3]		EV_{SS}		EV_{DD0}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.38	1.45	1.52	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. The number of pins depends on the product. For details, refer to **2.1 Pin Function List**.

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(4) When AV_{REF} (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AV_{REF} (-) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI0, ANI2 to ANI23, ANI24 to ANI30

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.52	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

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5.6.2 Temperatures Sensor Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.1		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.52	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

5.6.3 D/A Converter Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.7 V ≤ V_{DD} ≤ 5.5 V			-2.5/+3.0	LSB
		Rload = 8 MΩ	2.7 V ≤ V_{DD} ≤ 5.5 V			-2.5/+3.0	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs

5.6.4 Comparator Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±90	mV
Input voltage range	V_{ICMP}		0		V_{DD}	V
Response time	t_{CR}, t_{CF}	Input amplitude ±100 mV		70	700	ns
Stabilization wait time during input channel switching[Note 1]	t_{WAIT}	Input amplitude ±100 mV	800			ns
Operation stabilization wait time[Note 2]	t_{CMP}	3.3 V ≤ V_{DD} ≤ 5.5 V	1			μs
		2.7 V ≤ V_{DD} < 3.3 V	3			μs

Notes 1. Period of time from when the comparator input channel is switched until the comparator is switched to output

2. Period of time from when the comparator operation is enabled (HCMPON bit in CMPCTL is set to 1) until the comparator satisfies the DC/AC characteristics.

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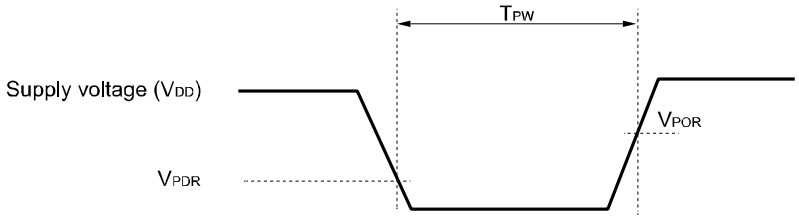
5.6.5 POR Circuit Characteristics

(T_A = -40 to +150°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage[Note 1]	V_{POR}	Power supply rise time	1.48	1.56	1.67	V
	V_{PDR}	Power supply fall time	1.47	1.55	1.66	V
Minimum pulse width[Note 2]	T_{PW}		300			μs
Detection delay time	T_{PD}				350	μs

Notes 1. This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}.



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5.6.6 LVD Circuit Characteristics

(1) LVD detection voltage of interrupt mode or reset mode

(T_A = -40 to +150°C, $V_{PDR} \le EV_{DD0} = EV_{DD1} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	4.62	4.74	5.22	V
			Power supply fall time	4.52	4.64	5.11	V
		V_{LVD1}	Power supply rise time	4.50	4.62	5.09	V
			Power supply fall time	4.40	4.52	4.98	V
		V_{LVD2}	Power supply rise time	4.30	4.42	4.87	V
			Power supply fall time	4.21	4.32	4.76	V
		V_{LVD3}	Power supply rise time	3.13	3.22	3.66	V
			Power supply fall time	3.07	3.15	3.47	V
		V_{LVD4}	Power supply rise time	2.95	3.02	3.44	V
			Power supply fall time	2.89	2.96	3.23	V
		V_{LVD5}	Power supply rise time	2.74	2.81	3.22	V
			Power supply fall time	2.68 Note	2.75	3.00	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

Note The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

(2) LVD detection voltage of interrupt & reset mode

(T_A = -40 to +150°C, $V_{PDR} \le EV_{DD0} = EV_{DD1} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 0, 1 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	3.00	V
	V_{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.87	V
			Falling interrupt voltage	4.21	4.32	4.76	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 0 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	3.00	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	5.09	V
			Falling interrupt voltage	4.40	4.52	4.98	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1 Note 1, falling reset voltage: 2.75 V		2.68 Note 2	2.75	3.00	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.66	V
			Falling interrupt voltage	3.07	3.15	3.47	V
	V_{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	5.22	V
			Falling interrupt voltage	4.52	4.64	5.11	V

Notes 1. These values indicate setting values of option bytes.

2. The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

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5.7 Power Supply Voltage Rising Time

(T_A = -40 to +150°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope	S_{vrmax}	0 V → V_{DD} (VPOC2 = 0 or 1[Note 2])			50[Note 3]	V/ms
Minimum power supply voltage rising slope [Note 1]	S_{vrmin}	0 V → 2.7 V	6.5			V/ms

Notes 1. The minimum power supply voltage rising slope is applied only under the following condition.
When the voltage detection (LVD) circuit is not used (VPOC2 = 1) and an external reset circuit is not used or when a reset is not effected until V_{DD} = 2.7 V.

2. These values indicate setting values of option bytes.

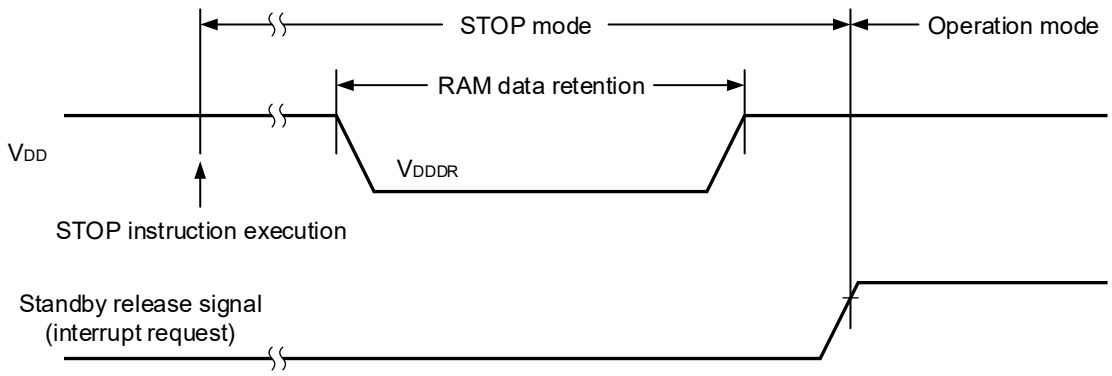
3. If the power supply drops below V_{PDR} and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to 0 V.

5.8 RAM Data Retention Characteristics

(T_A = -40 to +150°C, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



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5.9 Flash Memory Programming Characteristics

(T_A = -40 to +150°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = +85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 20 years T_A = +85°C Note 4	10,000			
		Retained for 5 years T_A = +85°C Note 4	100,000			
Erase time	T_{erasa}	Block erase	5			ms
Write time	T_{wrwa}	1 word write	10			μs

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The specified data retention time is given under the condition that the average temperature (T_A) is 85°C or below.

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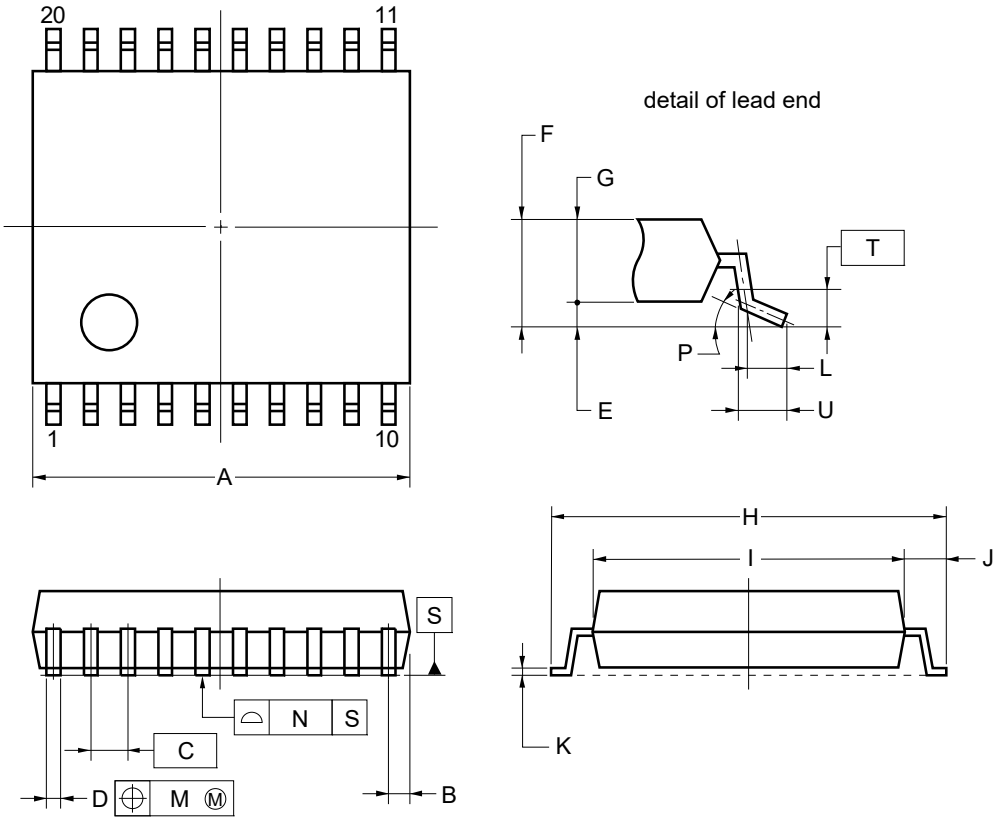
6. PACKAGE DRAWING

<R> The package types for 20-pin, 30-pin, and 32-pin products vary depending on the order name.
Please refer to the product packaging information on Renesas website for more information.

6.1 20-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

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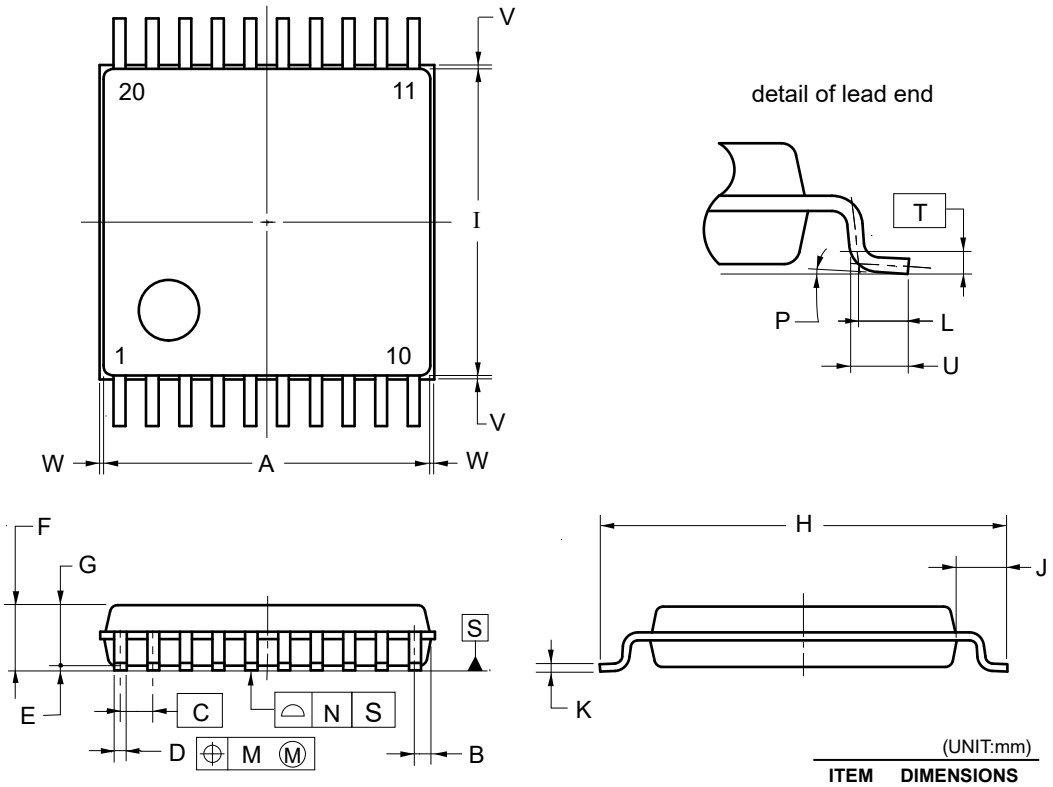
<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-6.10x6.5-0.65	PLSP0020JC-B	P20MC-65-CAA-1	0.12



(UNIT:mm)

ITEM	DIMENSIONS
A	6.50±0.10
B	0.325
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

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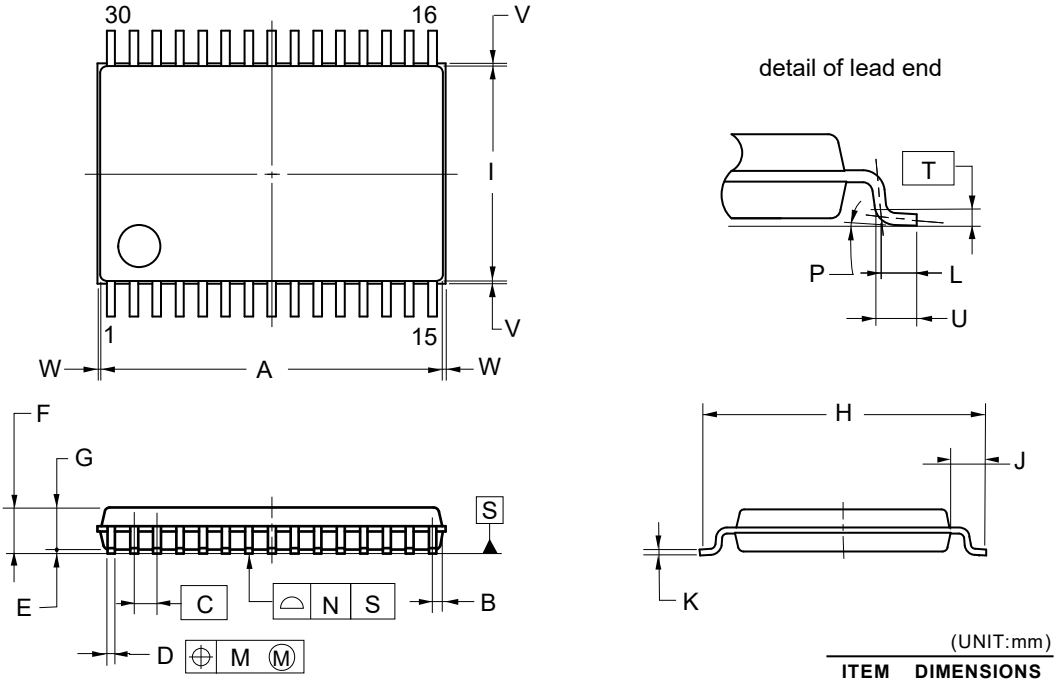
6.2 30-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-6.1x9.7-0.65	PLSP0030JB-A	P30MC-65-CAB-2	0.18



(UNIT:mm)

ITEM	DIMENSIONS
A	9.70±0.10
B	0.30
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition .

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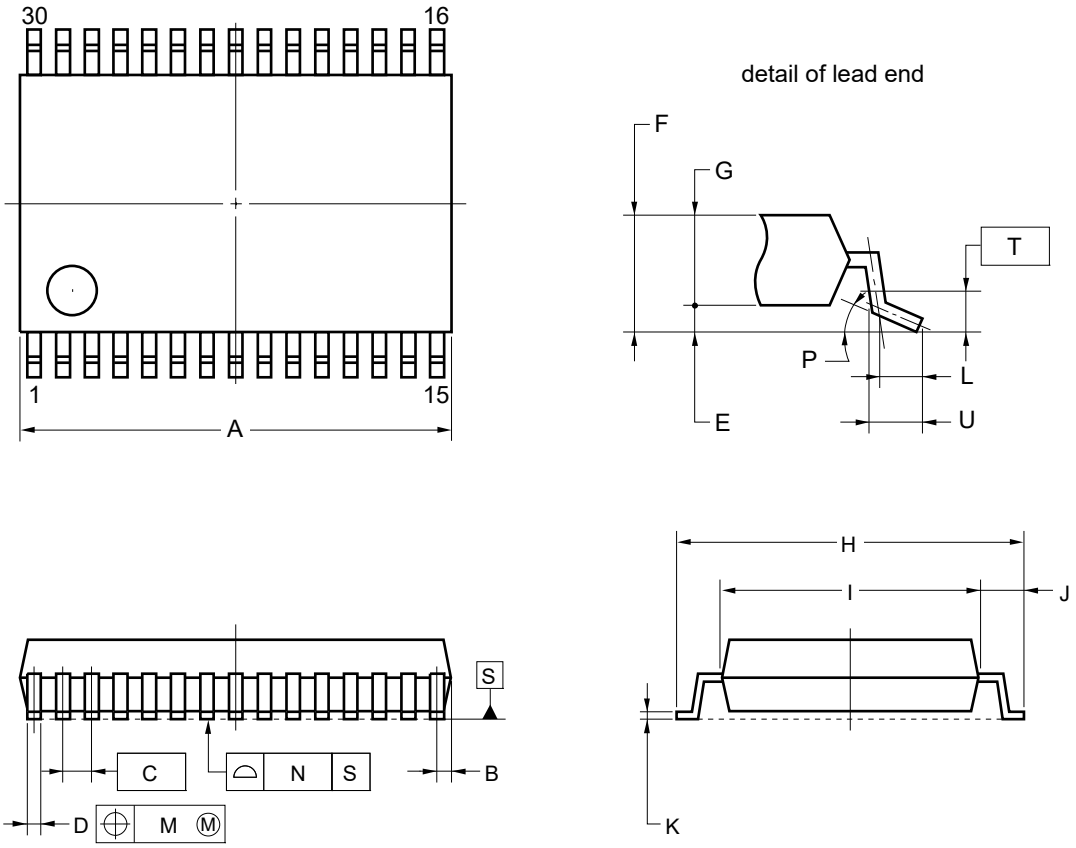
<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

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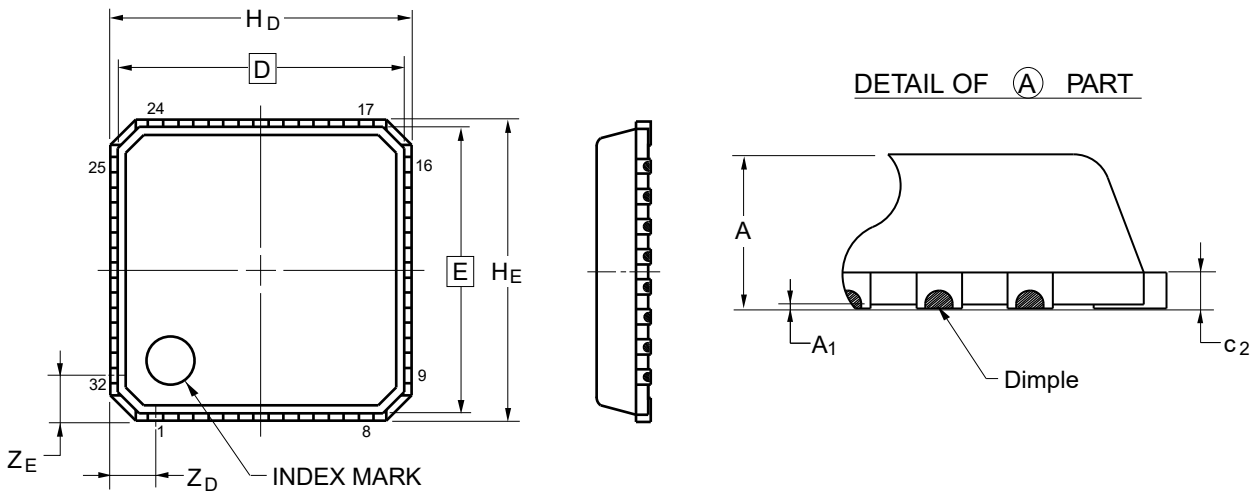
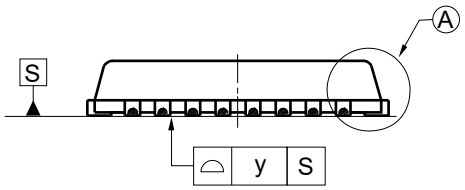
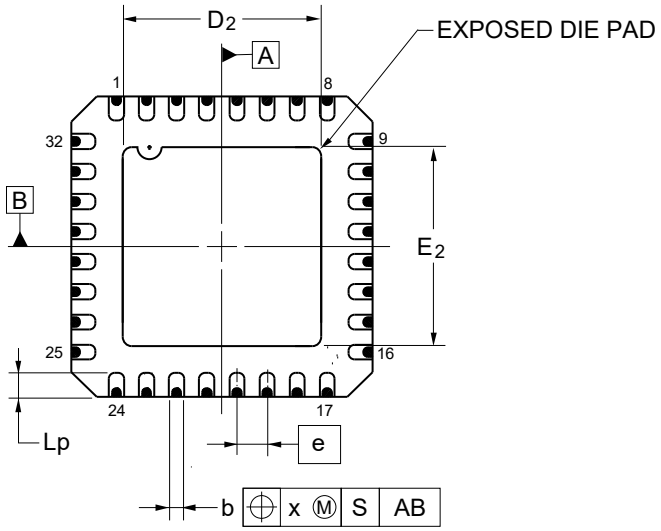
6.3 32-pin products

<R>

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN32-5x5-0.50	PVQN0032KD-A	P32K9-50A-BAH	0.058







Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.75	—
E	—	4.75	—
A	—	—	0.90
A_1	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.05
H_D	4.95	5.00	5.05
H_E	4.95	5.00	5.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.19	0.20	0.21
D_2	—	3.30	—
E_2	—	3.30	—

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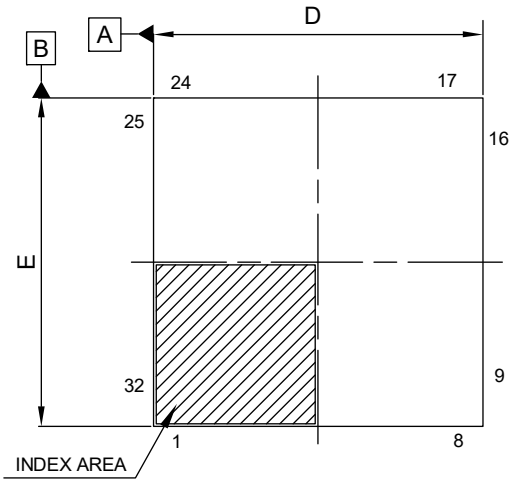
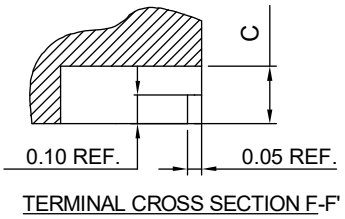
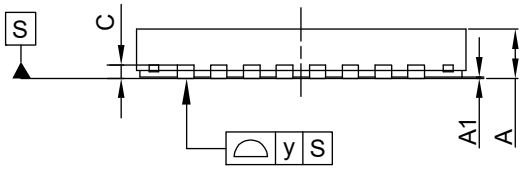
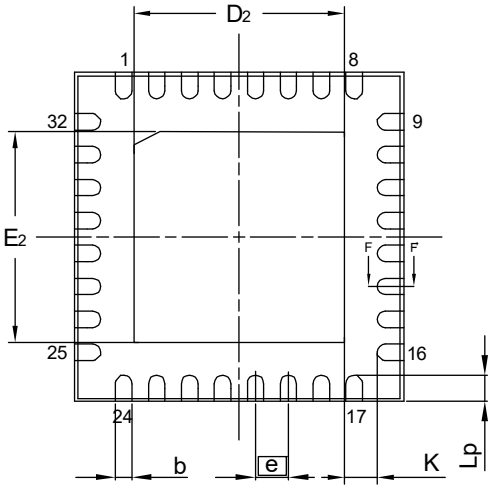
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KH-A	0.06









Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	4.85	5.00	5.15
E	4.85	5.00	5.15
A	—	—	0.80
A_1	0.00	—	0.05
b	0.18	0.25	0.30
e	0.50 BSC		
Lp	0.35	0.40	0.45
y	—	—	0.08
c	—	0.20	—
K	0.20	—	—
D_2	—	3.20	—
E_2	—	3.20	—

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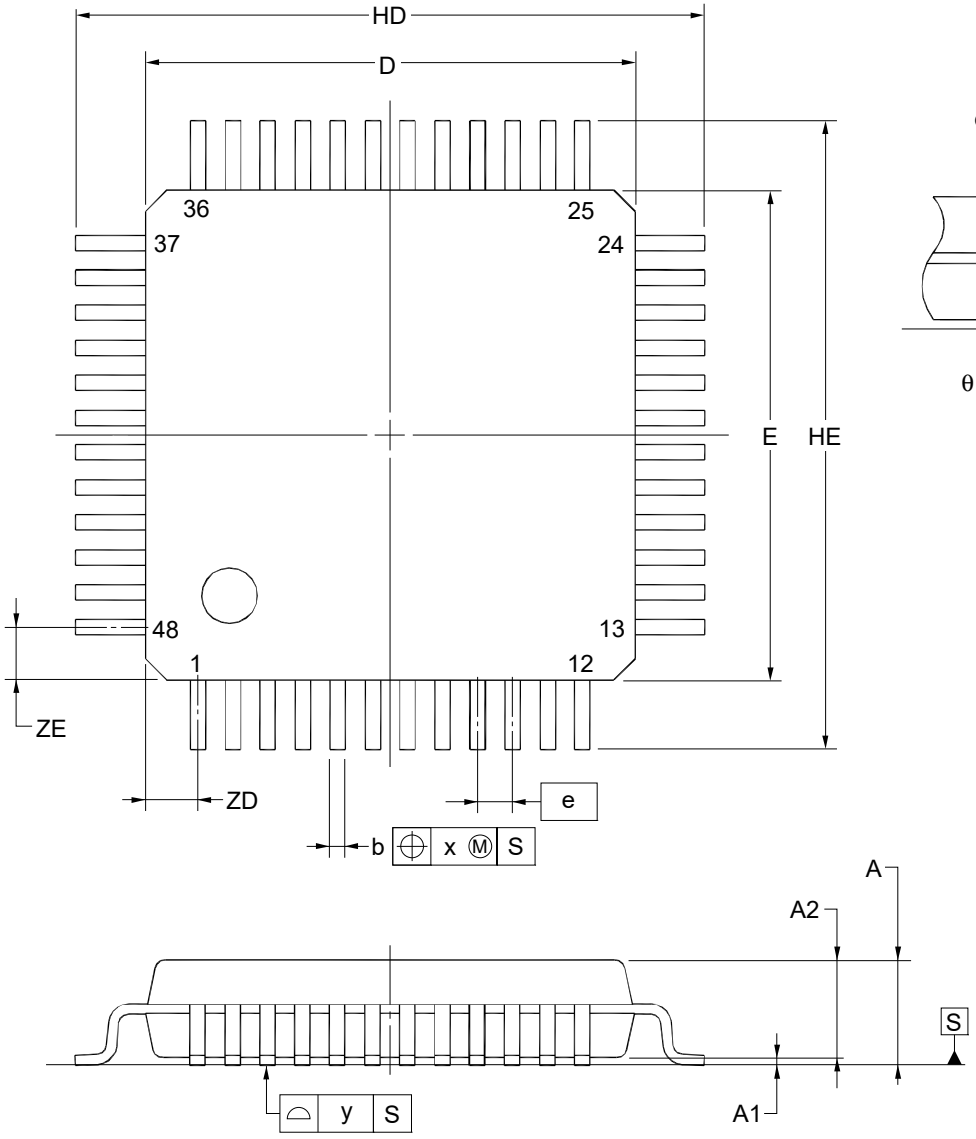
6.4 48-pin products

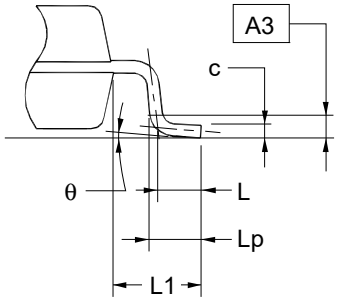
<R> **6.4.1 48-pin LFQFP**

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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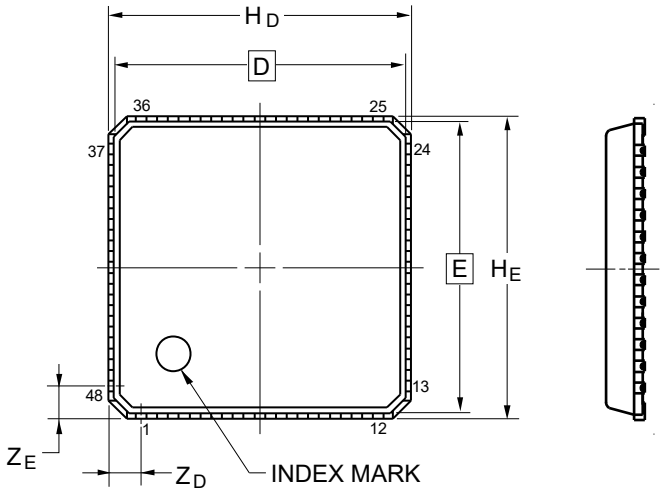
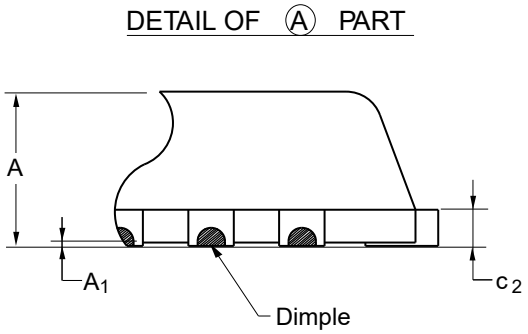
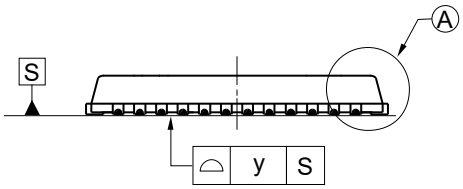
<R> **6.4.2 48-pin HVQFN**

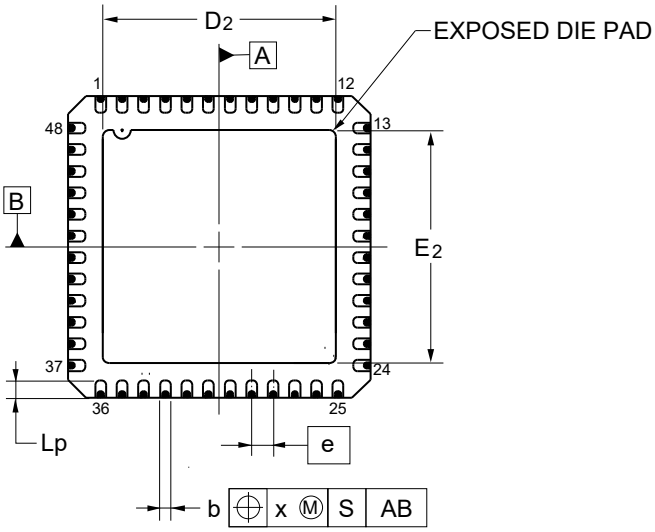
<R>

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN48-7x7-0.50	PVQN0048KG-A	P48K9-50A-BAJ	0.13









Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.75	—
E	—	6.75	—
A	—	—	0.90
A_1	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.05
H_D	6.95	7.00	7.05
H_E	6.95	7.00	7.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.19	0.20	0.21
D_2	—	5.40	—
E_2	—	5.40	—

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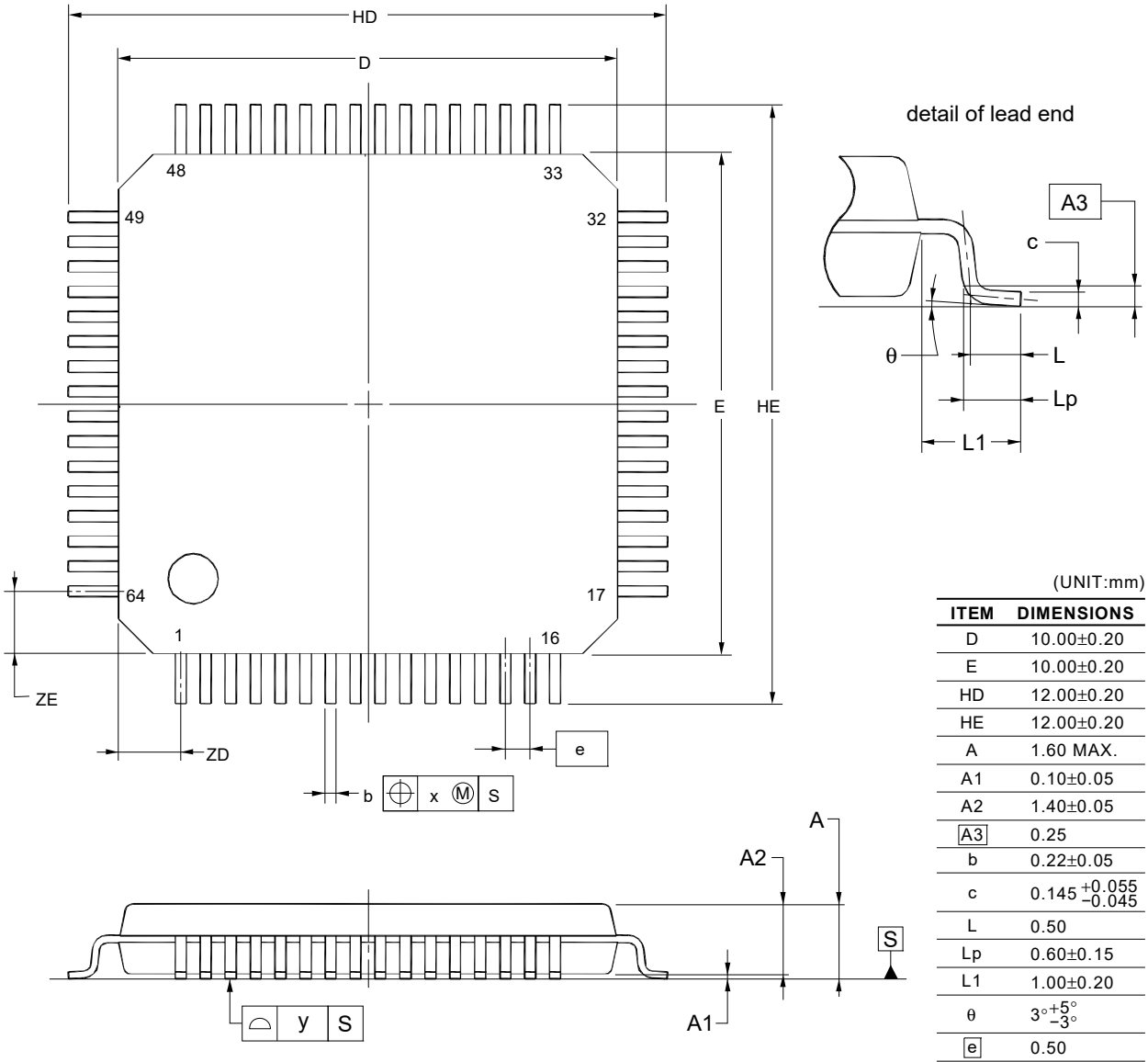
6.5 64-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU	0.35



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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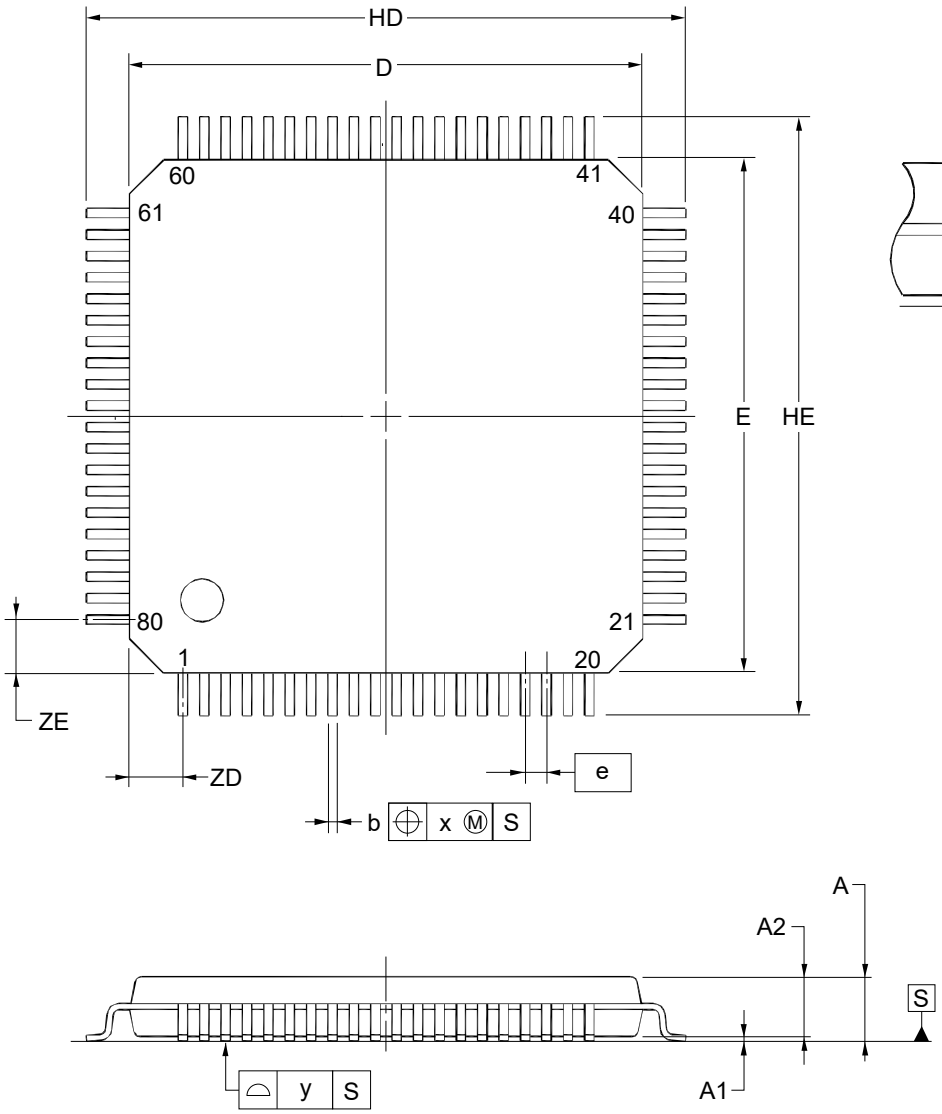
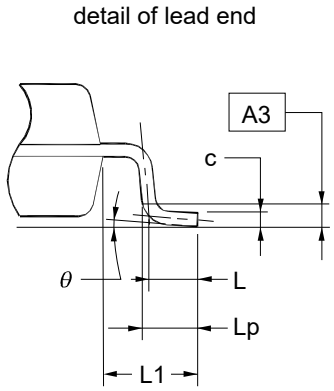
6.6 80-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU	0.53





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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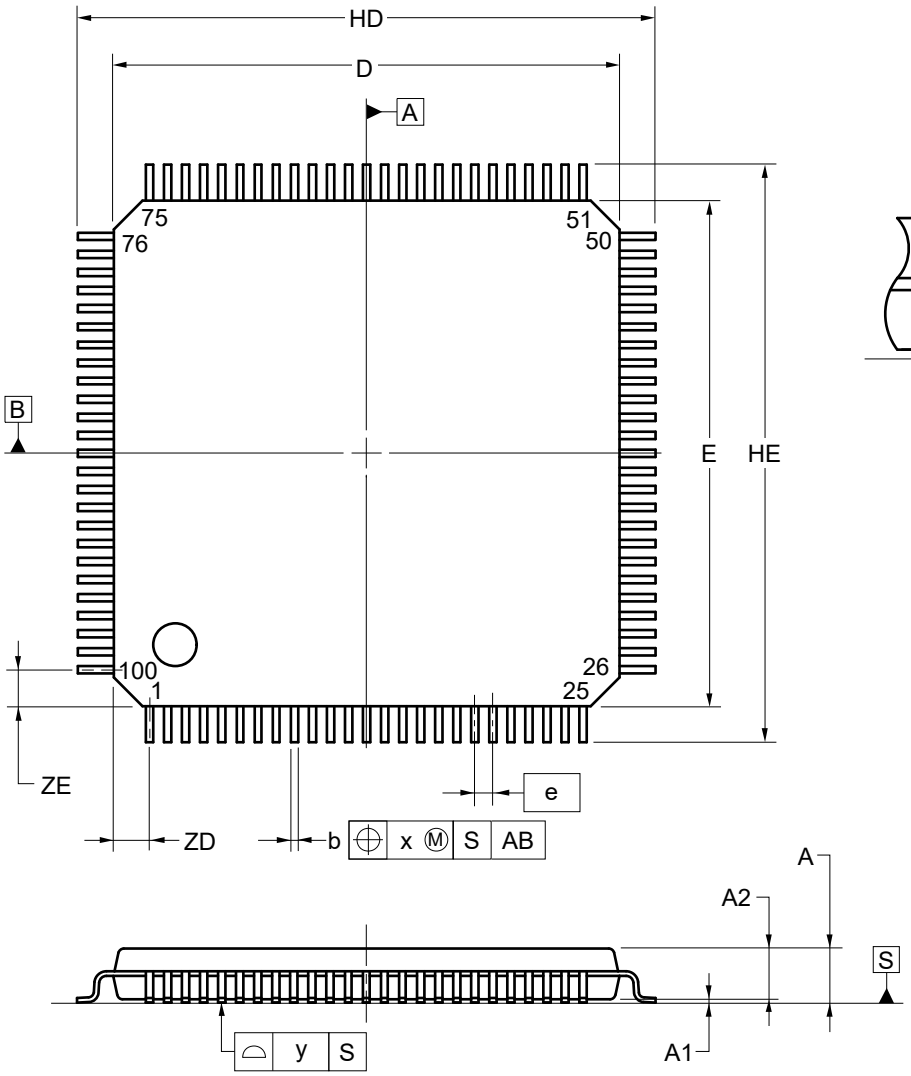
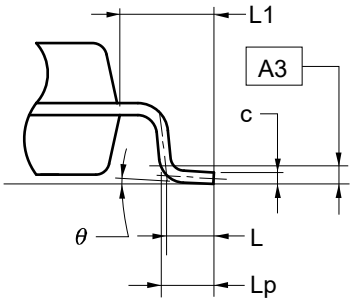
6.7 100-pin products

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14X14-0.50	PLQP0100KE-A	P100GC-50-GBR	0.69



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

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REVISION HISTORY	RL78/F13, F14 Datasheet

Rev	Date	Description	
		Page	Summary
2.20	Dec 27, 2024	–	First edition issued.
2.30	Aug 31, 2025	2	Modification of Table 1-1. RL78/F14 Lineup
		2	Modification of Table 1-2. RL78/F13 (CAN and LIN incorporated) Lineup
		2	Modification of Table 1-3. RL78/F13 (LIN incorporated) Lineup
		31	Modification of 1.5.1 RL78/F14 Pin Configuration for 100-pin Products
		32	Modification of 1.5.2 RL78/F14 Pin Configuration for 80-pin Products
		33	Modification of 1.5.3 RL78/F13 Pin Configuration for 80-pin Products
		34	Modification of 1.5.4 RL78/F14 Pin Configuration for 64-pin Products
		35	Modification of 1.5.5 RL78/F13 Pin Configuration for 64-pin Product
		36	Modification of 1.5.6 RL78/F14 Pin Configuration for 48-pin Products
		37	Modification of 1.5.7 RL78/F13 Pin Configuration for 48-pin Products
		38	Modification of 1.5.8 RL78/F14 Pin Configuration for 32-pin Products
		39	Modification of 1.5.9 RL78/F13 Pin Configuration for 32-pin Products
		40	Modification of 1.5.10 RL78/F14 Pin Configuration for 30-pin Products
		41	Modification of 1.5.11 RL78/F13 Pin Configuration for 30-pin Products
		42	Modification of 1.5.12 RL78/F13 Pin Configuration for 20-pin Products
		43	Modification of Table 1-7. Order Information for RL78/F14
		44	Modification of Table 1-8. Order Information for RL78/F13 (CAN and LIN incorporated)
		45	Modification of Table 1-9. Order Information for RL78/F13 (LIN incorporated)
		89	Modification of Notes 5 in (2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)
		90	Modification of Notes 5 in (3) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, special slew rate)
		99	Modification of Notes 3 in (9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)
		107	Modification of table 3.5.2 Serial Interface IICA
		140	Modification of Notes 5 in (2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)
		141	Modification of Notes 5 in (3) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, special slew rate)
		150	Modification of Notes 3 in (9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)
		158	Modification of table 4.5.2 Serial Interface IICA
		191	Modification of Notes 5 in (2) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)
		192	Modification of Notes 5 in (3) During communication at same potential (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, special slew rate)
		201	Modification of Notes 3 in (9) During communication at different potential (3-V supply system) (CSI mode) (master mode, $\overline{\text{SCKp}}$ … internal clock output, normal slew rate)
		208	Modification of table 5.5.2 Serial Interface IICA
		219	Addition of explanation in 6 PACKAGE DRAWING
		219	Addition of PLSP0020JC-A in 6.1 20-pin products
		220	Modification of PLSP0020JC-B in 6.1 20-pin products
		221	Modification of PLSP0030JB-A in 6.2 30-pin products
		222	Addition of PLSP0030JB-B in 6.2 30-pin products
		223	Modification of PVQN0032KD-A in 6.3 32-pin products
		224	Addition of PWQN0032KH-A in 6.3 32-pin products
		225	Modification of title in 6.4.1 48-pin LFQFP
		225	Modification of PLQP0048KF-A in 6.4.1 48-pin LFQFP
		226	Modification of title in 6.4.2 48-pin HVQFN

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Rev	Date	Description	
		Page	Summary
2.30	Aug 31, 2025	226	Modification of PVQN0048KG-A in 6.4.2 48-pin HVQFN
		227	Modification of PLQP0064KF-A in 6.5 64-pin products
		228	Modification of PLQP0080KE-A in 6.6 80-pin products
		229	Modification of PLQP0100KE-A in 6.7 100-pin products

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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