# STM32WB09xE

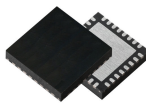## Ultra-low power wireless 32-bit MCU Arm®-based Cortex®-M0+ with Bluetooth® LE and 2.4 GHz radio solution

WLCSP36 (2.83 mm x 2.99 mm)

VFQFPN32 5x5 mm

| Product summary | |
|---|---|
| STM32WB09xE | STM32WB09KE |
| | STM32WB09TE |

### Features

- Includes ST state-of-the-art patented technology
- Bluetooth® LE
  - LE 2M
  - LE Coded
  - Extended Advertising
  - LE Channel Classification
  - Direction Finding
  - LE Data Packet Length Extension
  - LE Secure Connections
  - Link Layer Privacy
  - Periodic Advertising
  - Periodic Advertising with Responses
  - Advertising Coding selection
  - Encrypted Advertising Data
  - LE L2CAP Connection-Oriented Channel
  - LE Power Control
  - Enhanced Attribute Protocol
  - Connection Subrating
  - Isochronous Channels
  - Qualified against Bluetooth® Core 5.4
- Radio
  - RX sensitivity level: -97 dBm @ 1 Mbit/s, -104 dBm @ 125 Kbit/s (long range)
  - Programmable output power up to +8 dBm (at antenna connector)
  - 128 physical connections
  - Data rate supported: 2 Mbit/s, 1 Mbit/s, 500 Kbit/s and 125 Kbit/s
  - Integrated balun
  - Support for external PA and LNA
  - BlueNRG core coprocessor (DMA based) for Bluetooth® LE time critical operations
  - 2.4 GHz proprietary radio driver
  - Suitable for systems requiring compliance with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 part 15, ARIB STD-T66
  - Available integrated passive device (IPD) companion chip for optimized matching and filtering

www.st.com

- Ultra-low power radio performance
    - 12 nA in Shutdown mode (1.8 V)
    - 0.9 µA in Deepstop mode (with external LSE, radio wakeup source and RAM retained, 1.8 V)
    - 1.2 µA in Deepstop mode (with internal LSI, radio wakeup source and RAM retained, 1.8 V)
    - 4.9 mA peak current in TX (@0 dBm, 3.3 V)
    - 3.6 mA peak current in RX (@ sensitivity level, 3.3 V)
- High performance and ultra-low power 32-bit Arm® Cortex®-M0+ , running up to 64 MHz
- Dynamic current consumption: 14.47 µA/MHz
- Operating supply voltage: from 1.7 to 3.6 V
- -40 ºC to 105 ºC temperature range
- Supply and reset management
    - High efficiency embedded SMPS step-down converter with intelligent bypass mode
    - Ultra-low power power-on-reset (POR) and power-down-reset (PDR)
    - Programmable voltage detector (PVD)
- Clock sources
    - 64 MHz PLL
    - Fail safe 32 MHz crystal oscillator with integrated trimming capacitors
    - 32 kHz crystal oscillator
    - Internal low-power 32 kHz RO
- On-chip non-volatile flash memory of 512 Kbytes with page protection against R/W
- On-chip RAM of 64 Kbytes and 4 Kbytes PKA RAM
- One-time-programmable (OTP) memory area of 1 Kbytes
- Embedded UART bootloader
- Ultra-low power modes with or without timer and RAM retention
- Quadrature decoder
- Enhanced security mechanisms such as:
    - Flash read/write protection
    - SWD disabling
    - Secure bootloader
- Security features
    - True random number generator (TRNG) compliant with NIST special publication 800-90B
    - Hardware encryption AES maximum 128-bit security co-processor
    - Hardware public key accelerator (PKA)
    - Cryptographic algorithms: RSA, Diffie-Helman, ECC over GF(p)
    - CRC calculation unit
    - 64-bit unique ID
- System peripherals
    - 1x DMA controller with 8 channels supporting ADC, SPI, I2C, USART, LPUART, Timers
    - 1x SPI with I$^2$S interface multiplexed
    - 1x I$^2$C (SMBus/PMBus)
    - 1x LPUART (low power)
    - 1x USART (ISO 7816 smartcard mode, IrDA, SPI master and modbus)
    - 1x independent WDG
    - 1x real time clock (RTC)
    - 1x independent SysTick
    - 1x 16-bit, four channels general purpose timer
    - 2x 16-bit, two channels general purpose timer
    - Infrared interface

- Up to 20 fast I/Os
    - all of them with wakeup capability
    - all of them retain state in low-power mode
    - all of them 5 V tolerant
- Analog peripherals
    - 12-bit ADC with 8 input channels, up to 16 bits with a down sampler
    - Battery monitoring
    - Analog watchdog
- Development support
    - Serial wire debug (SWD)
    - 4 breakpoints and two watchpoints
- All packages are ECOPACK2 compliant

## Applications

- Industrial
- Home and industrial automation
- Asset tracking, ID location, real-time locating system
- Smart lighting
- Fitness,wellness and sports
- Healthcare, consumer medical
- Security/proximity
- Remote control
- Assisted living
- Mobile phone peripherals
- PC peripherals

# 1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WB09xE microcontrollers, based on Arm® core.

This document must be read in conjunction with the STM32WB09xE reference manual (RM0505).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32WB09xE errata sheet (ES0584).

For information on the Arm® Cortex®-M0+ core, refer to the Cortex®-M0+ technical reference manual, available from the www.arm.com website.

For information on Bluetooth® refer to www.bluetooth.com website.

*Note:* *Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

# 2    Description

The STM32WB09xE is an ultra-low power programmable Bluetooth® LE wireless SoC solution. It embeds STMicroelectronics' state-of-art 2.4 GHz RF radio peripherals, optimized for ultra-low-power consumption and excellent radio performance, for unparalleled battery lifetime.

It is compliant with Bluetooth® LE SIG core specification version 5.4 addressing point-to-point connectivity and Bluetooth® Mesh networking and allows large-scale device networks to be established in a reliable way. The STM32WB09xE is also suitable for 2.4 GHz proprietary radio wireless communication to address ultra-low latency applications.

The STM32WB09xE embeds an Arm® Cortex®-M0+ microprocessor that can operate up to 64 MHz and also the radio core coprocessor (DMA based) for Bluetooth® LE timing critical operations.

In addition, the STM32WB09xE provides enhanced security hardware support by dedicated hardware functions: true random number generator (TRNG) supporting NIST special publication 800-90B, security c0-processor for 128-bit AES encryption, CRC calculation unit, 64-bit unique ID, flash memory read and write protection, and a public key accelerator (PKA).

The PKA supports: modular arithmetic including exponentiation with maximum modulo size of 3136 bits, elliptic curves over prime field scalar multiplication, ECDSA signature, ECDSA verification with maximum modulo size of 521 bits CRC calculation unit, security level allowing constant time operations.

The STM32WB09xE can be configured to support standalone or network processor applications. In the first configuration, the STM32WB09xE operates as a single device running the application code and the Bluetooth® LE stack.

The STM32WB09xE embeds the following high-speed memory types: 512-Kbyte flash memory, 64-Kbyte RAM, 1-Kbyte one-time-programmable (OTP) memory area, and 7-Kbyte ROM (ST reserved area).

Direct data transfer between memory and peripherals and from memory-to-memory is supported by eight DMA channels with a full flexible channel mapping by the DMAMUX peripheral.

The STM32WB09xE embeds a 12-bit ADC, allowing measurements of up to eight external sources and up to three internal sources, including battery monitoring and a temperature sensor.

The STM32WB09xE has a low-power RTC and one advanced 16-bit timer.

The STM32WB09xE features standard and advanced communication interfaces: 1x SPI-I2, LPUART, 1x USART supporting ISO 7816 (SmartCard mode), IrDA and Modbus mode, 2x I$^2$C supporting SMBus/PMBus.

The STM32WB09xE operates in the -40 to +105 °C (+125 °C junction) temperature range from a 1.7 V to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The STM32WB09xE integrates a high efficiency SMPS step-down converter and an integrated PDR circuitry with a fixed threshold that generates a device reset when the VDD drops under 1.65 V.

The STM32WB09xE is available in two package types: VFQFPN32 and WLCSP36. Both versions support up to 20 I/Os.

**Table 1. STM32WB09xE device features and peripheral counts**

| Feature | | STM32WB09KE | STM32WB09TE |
|---|---|---|---|
| Flash memory density | | 512 Kbytes | |
| SRAM density | SRAM0 | 16 Kbytes | |
| | SRAM1 | 16 Kbytes | |
| | SRAM2 | 16 Kbytes | |
| | SRAM3 | 16 Kbytes | |
| Bluetooth LE | | Yes | |
| 2.4 GHz proprietary radio | | Yes | |
| Timers | General purpose | 1x 16-bit, four channels and 2x 16-bit, two channels | |
| | 2.4 GHz proprietary radio timer low power | 32-bit | |
| | SysTick | 1 | |

| Feature | | STM32WB09KE | STM32WB09TE |
|---|---|---|---|
| Communication interfaces | SPI | 1 with I2S feature | |
| | I2C | 1 | |
| | USART | 1 | |
| | LPUART | 1 | |
| RTC | | Yes | |
| Wake-up pins | | 20 | |
| GPIOs | | 20 | |
| 12-bit ADC | | 1 (8 channels) | |
| True random number generator | | Yes | |
| AES | | Yes | |
| Public key accelerator (PKA) | | Yes | |
| Maximum CPU frequency | | 64 MHz | |
| Operating temperature | | -40 ºC to 105 ºC temperature range | |
| Operating voltage | | 1.7 to 3.6 V | |
| Package | | VFQFPN32 | WLCSP36 |

**Figure 1. STM3WB09xE block diagram**
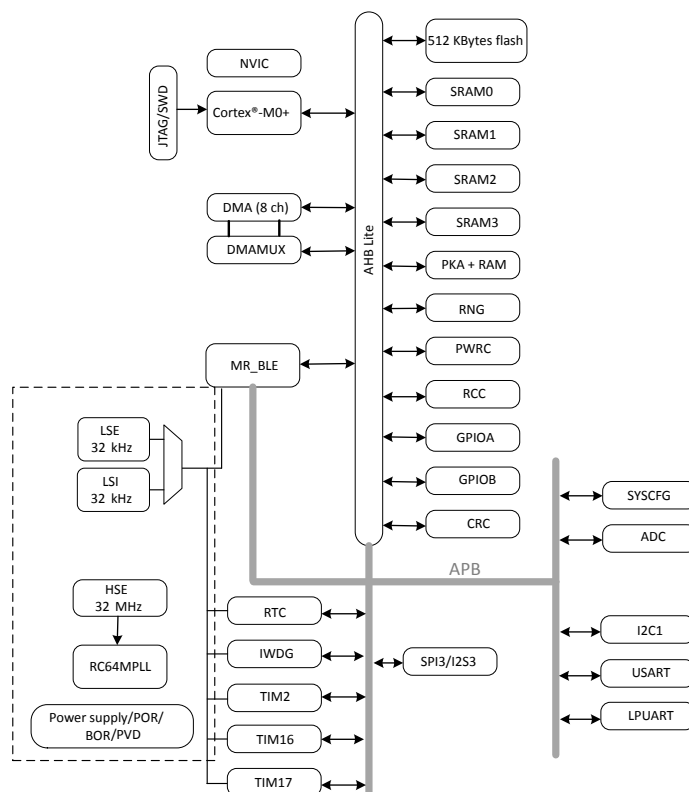


DT57462V1

# 3 Functional overview

## 3.1 Arm® Cortex®–M0+ core with MPU

The STM3WB09xE contains an Arm® Cortex®-M0+ microprocessor core. The Arm® Cortex®-M0+ was developed to provide a low-cost platform that meets the needs of CPU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. The Arm® Cortex®-M0+ can run from 1 MHz up to 64 MHz.

The Arm® Cortex®-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The interrupts are handled by the Arm® Cortex®-M0+ nested vector interrupt controller (NVIC). The NVIC controls specific Arm® Cortex®-M0+ interrupts as well as the STM3WB09xE peripheral interrupts. With its embedded Arm® core, the STM3WB09xE family is compatible with all ARM® tools and software.

## 3.2 System architecture

The main system consists of 32-bit multilayer AHB bus matrix that interconnects:

- Three masters:
  - CPU (Cortex®-M0+) core S-bus
  - DMA1
  - Radio system
- Nine slaves:
  - Internal flash memory on CPU (Cortex®-M0+) S bus
  - Internal SRAM0 (16 Kbytes )
  - Internal SRAM1 (16 Kbytes )
  - Internal SRAM2 (16 Kbytes )
  - Internal SRAM3 (16 Kbytes )
  - APB0 peripherals (through an AHB to APB bridge)
  - APB1 peripherals (through an AHB to APB bridge)
  - AHB0 peripherals
  - AHBRF including AHB to APB bridge and radio peripherals (connected to APB2)

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. **Bus matrix**
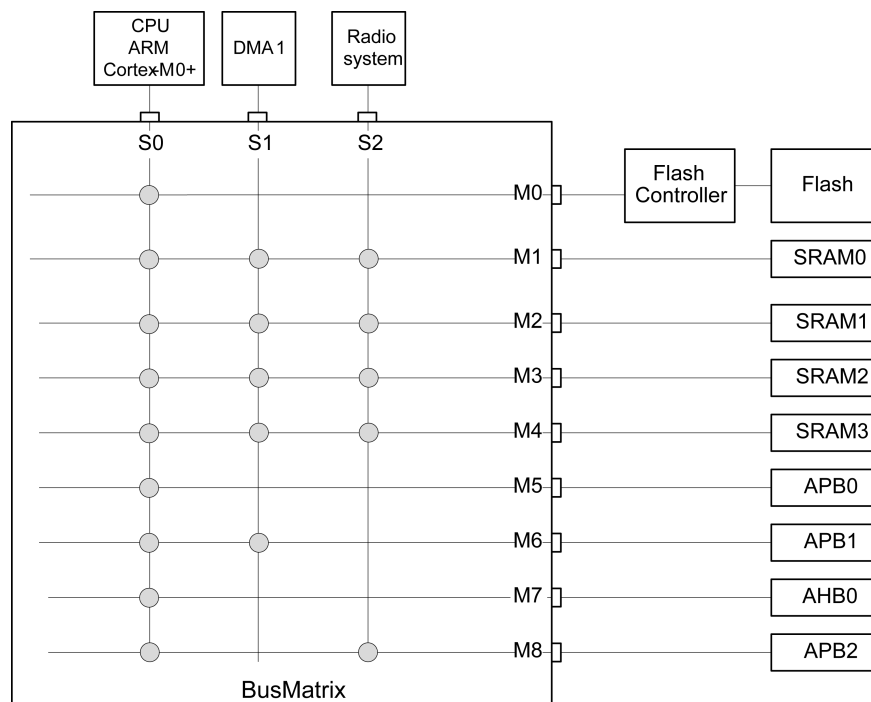


## 3.3 Memory protection unit (MPU)

The MPU is used to manage accesses to memory to prevent one task from accidentally corrupting the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area settings, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 3.4 Memories

### 3.4.1 Embedded flash memory

The flash controller implements the erase and program flash memory operation. The flash controller also implements the read and write protection.

The flash memory features are:
- Memory organization:
  – 1 bank of 512 Kbytes
  – Page size: 2 Kbytes
  – Page number 256
- 32-bit wide data read
- 32-bit wide data write
- Page erase and mass erase

The flash controller features are:
- Flash memory read operations: single read or mass read
- Flash memory write operations: single data write or 4x32-bits burst write or mass write

•  Flash memory erase operations: page erase or mass erase
•  Page write protect mechanism: 4 variable-size memory segments

### 3.4.2 Embedded SRAM

The STM3WB09xE has a total of 64 Kbytes of embedded SRAM, split into four banks as shown in the following table:

**Table 2. SRAM overview**

| SRAM bank | Size | Address | Retained in Deepstop |
|-----------|------|---------|----------------------|
| SRAM0 | 16 Kbytes | 0x2000 0000 | Always |
| SRAM1 | 16 Kbytes | 0x2000 4000 | Programmable by the user |
| SRAM2 | 16 Kbytes | 0x2000 8000 | Programmable by the user |
| SRAM3 | 16 Kbytes | 0x2000 C000 | Programmable by the user |

### 3.4.3 Embedded ROM

The STM3WB09xE has a total of 7 Kbytes of embedded ROM. This area is ST reserved and contains:

•  The UART bootloader from which the CPU boots after each reset (first 6 Kbytes of ROM memory)
•  Some ST reserved values including the ADC trimming values (the last 1 Kbytes of ROM memory)

### 3.4.4 Embedded OTP

The one-time-programmable (OTP) is a memory of 1 Kbytes dedicated for user data. The OTP data cannot be erased.

The user can protect the OTP data area by writing the last word at address 0x1000 1BFC and by performing a system reset. This operation freezes the OTP memory from further unwanted write operations.

## 3.5 Security and safety

The STM3WB09xE contains many security blocks for the Bluetooth® LE and the host application.

It includes:

•  Flash read/write protections over accidental and intentional actions
•  As protection against potential hacker attacks, the SWD access can be disabled
•  Secure bootloader
•  Customer storage of the Bluetooth® LE keys
•  True random number generator (TRNG) supporting NIST special publication 800-90B
•  Private key accelerator (PKA) including:
    –  Modular arithmetic including exponentiation with maximum modulo size of 3136 bits
    –  Elliptic curves over prime field scalar multiplication, ECDSA signature, ECDSA verification with maximum modulo size of 521 bits
    –  Security level allowing constant time operations
•  Cyclic redundancy check calculation unit (CRC)

## 3.6 Boot modes

Following CPU boot, the application software can modify the memory map at address 0x0000 0000. This modification is performed by programming the REMAP bit in the flash controller.

The following memory can be remapped:

•  Main flash memory
•  SRAM0 memory

## 3.7 RF subsystem

The STM32WB09xE embeds an ultra-low power radio, compliant with Bluetooth® LE specification. The device radio offers 1 Mbit/s and 2 Mbit/s transfer rates as well as long range options (125 Kbit/s, 500 Kbit/s), supports multiple roles simultaneously acting at the same time as Bluetooth® LE sensor and hub device.

The Bluetooth® LE protocol stack is implemented by an efficient system partitioned as follows:

• Hardware part: BlueCore handling time critical and time consuming Bluetooth® LE protocol parts

• Firmware part: Arm® Cortex®-M0+ core handling non time critical Bluetooth® LE protocol parts

### 3.7.1 RF front-end block diagram

The RF front-end is based on a direct modulation of the carrier in TX, and uses a low IF architecture in RX mode.

Thanks to an internal transformer with RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to 50 Ω). The natural band pass behavior of the internal transformer simplifies outside circuitry aimed at harmonic filtering and out of band interferer rejection.

In transmit mode, the maximum output power is user selectable through the programmable LDO voltage of the power amplifier. A linearized, smoothed analog control offers a clean power ramp-up.

In receive mode, the automatic gain control (AGC) can reduce the chain gain at both RF and IF locations, for optimized interferer rejections. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

**Figure 3. STM3WB09xE RF block diagram**
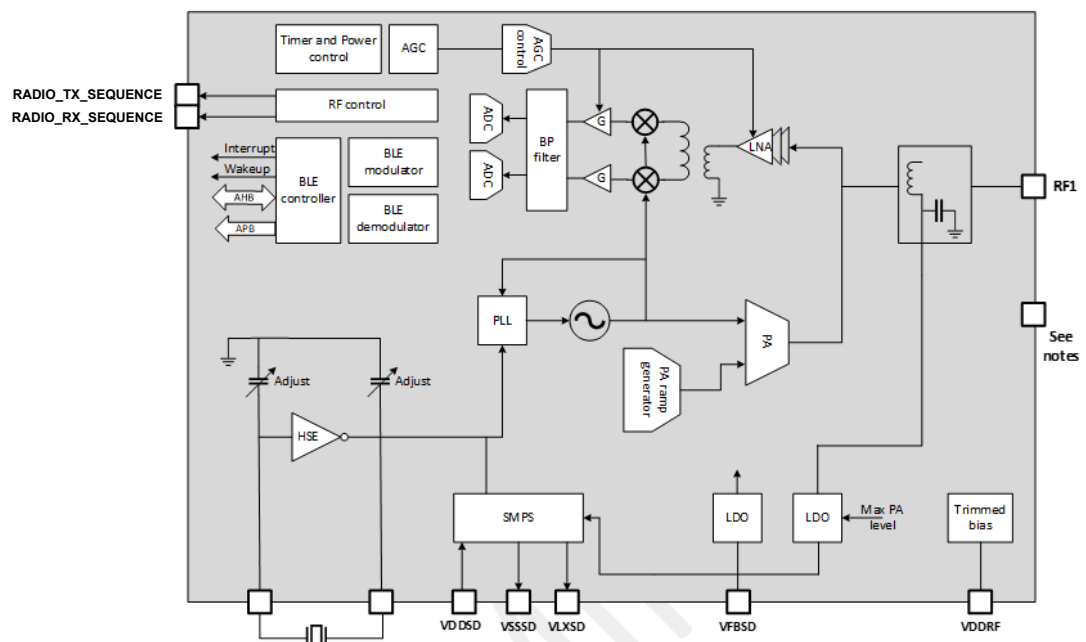


Note:
VFQFPN32: $V_{SS}$ through exposed pad, and $V_{SSRF}$ pins must be connected to ground plane
WLCSP36: $V_{SSRF}$ pins must be connected to ground plane

### 3.7.2 IPDs for STM32WB09xE

The table below lists the available IPD variants for STM32WB09xE device.

**Table 3. IPDs for STM32WB09xE**

| IPD | MCU Package | STM32WB09xxx part number |
|---|---|---|
| MLPF-NRG-01D3 | VFQFPN32 | STM32WB09KEV |
| | WLCSP36 | STM32WB09TEF |

## 3.8 Power supply management

### 3.8.1 SMPS step-down regulator

The device integrates a step-down converter to improve low-power performance when the $V_{DD}$ voltage is high enough. The SMPS output voltage can be programmed from 1.2 V to 1.90 V. It is internally clocked at 4 MHz or 8 MHz.

The device can be operated without the SMPS by just wiring its output to $V_{DD}$. This is the case for applications where the voltage is low, or where the power consumption is not critical.

Except for the configuration SMPS OFF, an L/C BOM must be present on the board and connected to the VFBSD pad.

**Figure 4. Power supply configuration**



SMPS supply configuration          NOSMPS supply configuration
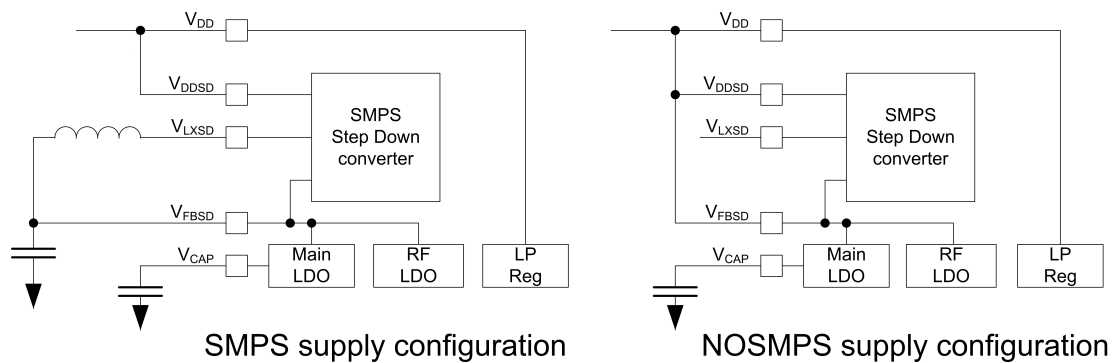
### 3.8.2 Power supply schemes

The STM3WB09xE embeds three power domains:

- $V_{DD33}$ ($V_{DDIO}$ or $V_{DD}$):
    - the voltage range is between 1.7 V and 3.6 V
    - it supplies a part of the I/O ring, the embedded regulators and the system analog peripherals as power management block and embedded oscillators
- $V_{DD12o}$:
    - always-on digital power domain
    - this domain is generally supplied at 1.2 V during active phase of the device
    - this domain is supplied at 1.0 V during low-power mode (Deepstop)
- $V_{DD12i}$:
    - interruptible digital power domain
    - this domain is generally supplied at 1.2 V during active phase of the device
    - this domain is shut down during low-power mode (Deepstop)

**Figure 5. Power supply domain overview**
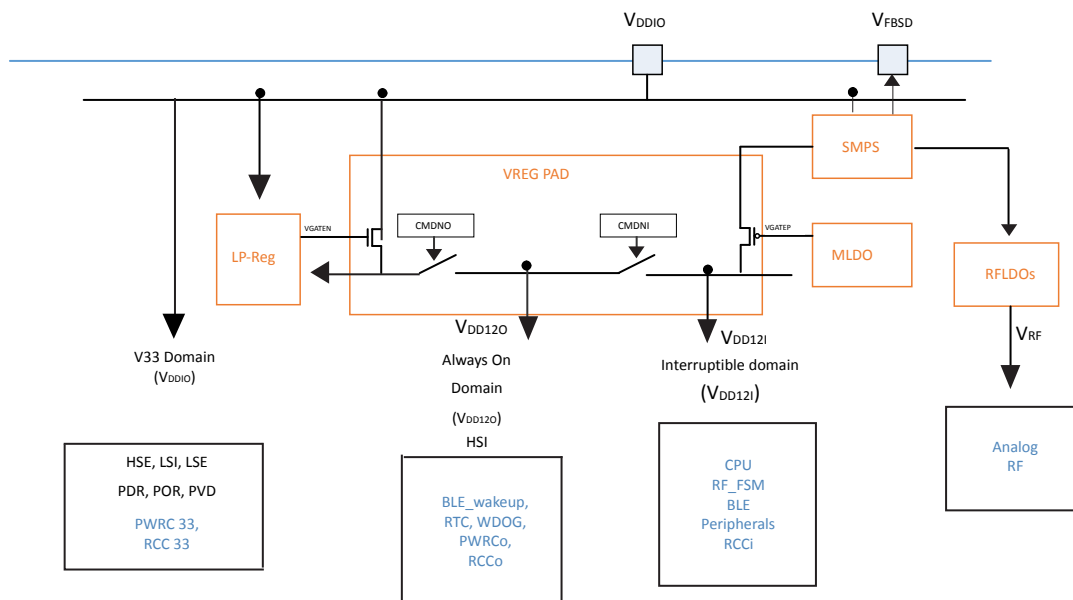


### 3.8.3 Linear voltage regulators

The digital power supplies are provided by different regulators:

- The main LDO (MLDO):
    - it provides 1.2 V from a 1.4-3.3 V input voltage
    - it supplies both $V_{DD12i}$ and $V_{DD12o}$ when the device is active
    - it is disabled during the low-power mode (Deepstop)
- Low-power LDO (LPREG):
    - it stays enabled during both active and low-power phases
    - it provides 1.0 V voltage
    - it is not connected to the digital domain when the device is active
    - it is connected to the $V_{DD12o}$ domain during low-power mode (Deepstop)
- A dedicated LDO (RFLDO) to provide a 1.2 V to the analog RF block

An embedded SMPS step-down converter is available (inserted between the external power and the LDOs).

### 3.8.4 Power supply supervisor

The STM3WB09xE device embeds several power and voltage monitors:

- Power-on-reset (POR): during the power-on, the device remains in reset mode if $V_{DDIO}$ is below a $V_{POR}$ threshold (typically 1.65 V)

- Power-down-reset (PDR): during power-down, the PDR puts the device under reset when the supply voltage ($V_{DD}$) drops below the $V_{PDR}$ threshold (around 20 mV below $V_{POR}$). The PDR feature is always enabled

- Programmable voltage detector (PVD): can be used to monitor the $V_{DDIO}$ (against a programmed threshold) or an external analog input signal. When the feature is enabled and the PVD measures a voltage below the comparator, an interrupt is generated (if unmasked)

## 3.9 Reset management

The STM3WB09xE offers two different resets:

- The PORESETn: this reset is provided by the low-power management unit (LPMU) analog block and corresponds to a POR or PDR root cause. It is linked to power voltage ramp-up or ramp-down. This reset impacts all resources of the STM3WB09xE. The exit from Shutdown mode is equivalent to a POR and thus generates a PORESETn. The PORESETn signal is active when the power supply of the device is below a threshold value or when the regulator does not provide the target voltage.

- The PADRESETn (system reset): this reset is built through several sources:

  – PORESETn

  – Reset due to the watchdog
    The STM3WB09xE device embeds a watchdog timer, which may be used to recover from software crashes

  – Reset due to CPU Lockup
    The Cortex®-M0+ generates a lockup to indicate the core is in the lock-up state resulting from an unrecoverable exception. The lock-up reset is masked if a debugger is connected to the Cortex®-M0+

  – Software system reset
    The system reset request is generated by the debug circuitry of the Cortex®-M0+. The debugger sets the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR). This system reset request through the AIRCR can also be done by the embedded software (into the hardfault handler for instance)

  – Reset from the RSTN external pin
    The RSTN pin toggles to inform that a reset has occurred

This PADRESETn resets all resources of the STM3WB09xE, except:

- Debug features
- Flash controller key management
- RTC timer
- Power controller unit
- Part of the RCC registers

The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of reset from the RSTN external pad, the reset pulse is generated when the pad is asserted low.

## 3.10 Operating modes

Several operating modes are defined for the STM3WB09xE:

- Run mode
- Deepstop mode
- Shutdown mode

**Table 4. Relationship between the low-power modes and functional blocks**

| Mode | Shutdown | Deepstop | Idle | Run |
|---|---|---|---|---|
| CPU | OFF | OFF | OFF | ON |
| Flash | OFF | OFF | ON | ON |
| RAM | OFF | ON/OFF granularity 12 Kbytes | ON/OFF | ON/OFF |
| Radio | OFF | OFF | ON/OFF | ON/OFF |
| Supply system | OFF | OFF | ON ( DC-DC ON/ OFF) | ON ( DC-DC ON/ OFF) |
| Register retention | OFF | ON | ON | ON |
| HS clock | OFF | OFF | ON | ON |
| LS clock | OFF | ON/OFF | ON | ON |

| Mode | Shutdown | Deepstop | Idle | Run |
|---|---|---|---|---|
| Peripherals | OFF | OFF | ON/OFF | ON/OFF |
| Wake-on RTC | OFF | ON/OFF | ON/OFF | NA |
| Wake-on GPIOs | Only from PB0 | ON/OFF | ON/OFF | NA |
| Wake-on reset pin | ON | ON | ON | NA |
| GPIOs configuration retention | Only PWRC pull-up/pull-down | ON | ON | ON |

### 3.10.1 Run mode

In Run mode the STM3WB09xE is fully operational:

- All interfaces are active
- The internal power supplies are active
- The system clock and the bus clock are running
- The CPU core and the radio can be used

The power consumption may be reduced by gating the clock of the unused peripherals.

### 3.10.2 Deepstop mode

The Deepstop is the only low-power mode of the STM3WB09xE allowing the restart from a saved context environment and the application at wakeup to go on running.

The conditions to enter the Deepstop mode are:

- The radio is sleeping (no radio activity)
- The CPU is sleeping (WFI with the SLEEPDEEP bit activated)
- No unmasked wakeup sources are active
- The low-power mode selection (LPMS) bit of the power controller unit is 0 (default)

In Deepstop mode:

- The system and the bus clocks are stopped
- Only the essential digital power domain is ON and supplied at 1.0 V
- The bank RAM0 is kept in retention
- The bank RAM1, RAM2, RAM3 can be in retention or not, depending on the software configuration
- The low-speed clock can be running or stopped, depending on the software configuration:
  - ON or OFF
  - Sourced by LSE or by LSI
- The RTC, IWDG and LPUART stay active, if enabled and the low-speed clock is ON
- The radio wakeup block, including its timer, stayS active (if enabled and the low-speed clock is ON)
- Up to 20 GPIOs retaining their configuration:
  - I/Os retain the Run mode configuration while in Deepstop mode
- Up to 20 I/Os are able to be in output driving:
  - A static low or high level
- Some I/Os can be in output driving:
  - The low speed clock (on PA10)
  - The RTC output (on PA8)

Possible wakeup sources are:

- The radio block is able to generate two events to wake up the system through its embedded wakeup timer running on low-speed clock:
  - Radio wakeup time is reached
  - CPU host wakeup time is reached
- The RTC can generate a wakeup event
- The IWDG can generate a reset event
- The LPUART is able to generate a wakeup event

• All GPIOs can wake up the system

At wakeup, all the hardware resources located in the digital power domain that are OFF during Deepstop mode, are reset. The CPU reboots. The wakeup reason is visible in the register of the power controller.

### 3.10.3 Shutdown mode

The Shutdown mode is the least power consuming mode.

The conditions to enter Shutdown mode are the same conditions needed to enter Deepstop mode except that the LPMS bit of the power controller unit is 1.

In Shutdown mode, the STM3WB09xE is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The STM3WB09xE can enter shutdown mode by internal software sequence. The only way to exit shutdown mode is by asserting and deasserting the RSTN pin or through a configurable pulse on PB0 pin.

In Shutdown mode:

• The system is powered down as both the regulators are OFF

• The $V_{DDIO}$ power domain is ON

• All the clocks are OFF, LSI and LSE are OFF

• The I/Os pull-up and pull-down can be controlled during Shutdown mode, depending on the software configuration

• The only wakeup source is a low pulse on the RSTN pin or a configurable pulse on PB0 pin

• The exit from Shutdown is similar to a POR startup. The PDR feature can be enabled or disabled during Shutdown

## 3.11 Clock management

Three different clock sources may be used to drive the system clock of the STM3WB09xE:

• HSI: high speed internal 64 MHz RC oscillator

• PLL64M: 64 MHz PLL clock

• HSE: high speed 32 MHz external crystal

The STM3WB09xE has also a low-speed clock tree used by some timers in the radio, RTC, IWDG and LPUART.

Three different clock sources can be used for this low-speed clock tree:

• Low-speed internal (LSI): low-speed and low drift internal RC with a fixed frequency between 24 kHz and 49 kHz depending on the sample

• Low-speed external (LSE) from:
    – An external crystal 32.768 kHz
    – A single-ended 32.738 kHz input signal

• A 32 kHz clock obtained by dividing HSI or HSE. In this case, the slow clock is not available in Deepstop low-power mode

By default, after a system reset, all low-speed sources are OFF.

Both the activation and the selection of the slow clock are relevant during the Deepstop mode and at wakeup as slow clock generates a clock for the timers involved in wakeup event generation.

The HSI and the PLL64M clocks are provided by the same analog block called RC64MPLL. The 64 MHz clock output by this block can be:

• A non-accurate clock when no external XO provides an input clock to this block (HSI)

• An accurate clock when the external XO provides the 32 MHz and once its internal PLL is locked (PLL64M)

After reset, the CLK_SYS is divided by four to provide a 16 MHz to the whole system (CPU, DMA, memories and peripherals).

## Figure 6. Clock tree
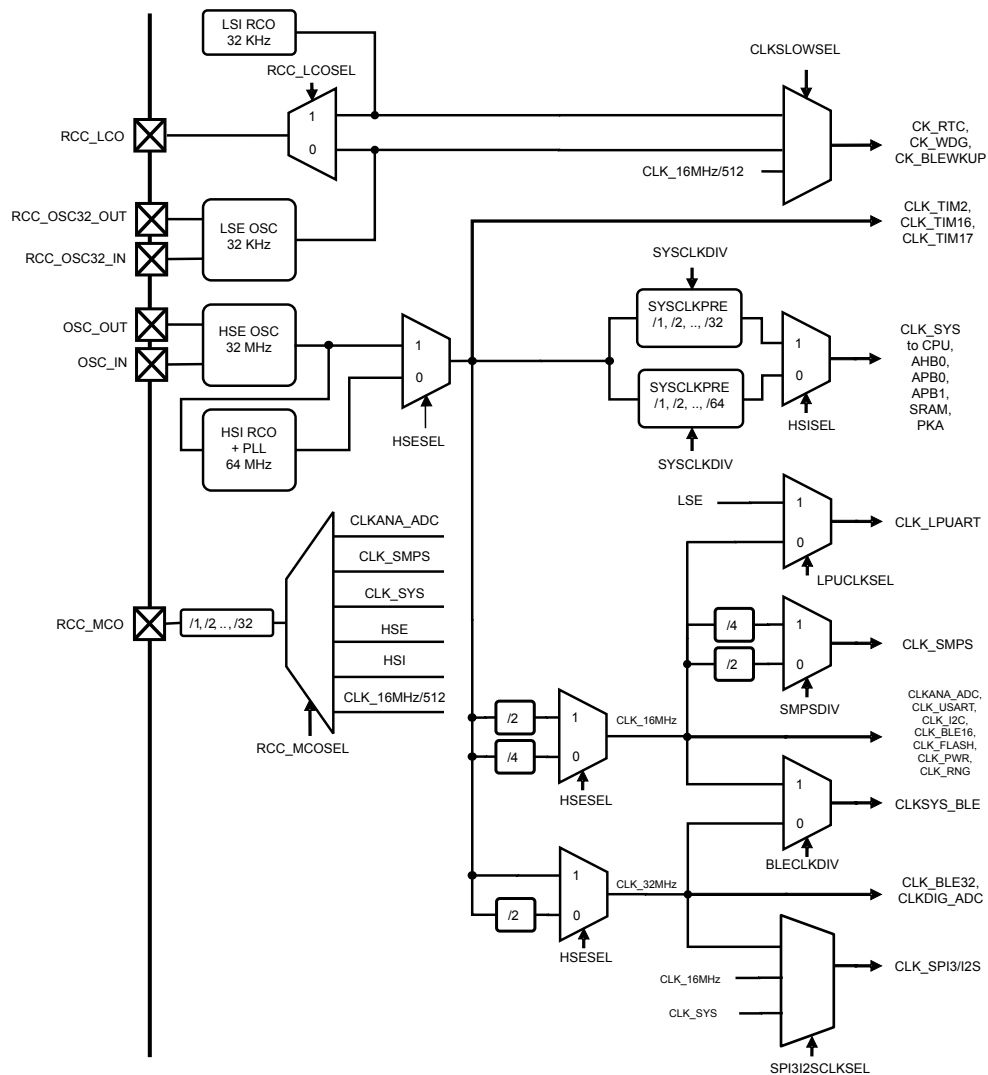


It is possible to output some internal clocks on external pads:

- The low speed clocks can be output on the RCC_LCO I/O
- The high speed clocks can be output on the RCC_MCO I/O

This is possible by programming the associated I/O in the correct alternate function.

Most of the peripherals only use the system clock except:

- $I^2C$, USART: they use an always 16 MHz clock to have a fixed reference clock for baud rate management. The goal is to allow the CPU to boost or slow down the system clock (depending on on-going activities) without impacting a potential on-going serial interface transfer on external I/Os

- LPUART: always uses a 16 MHz clock or LSE to have a fixed reference clock for baud rate management. The goal is to allow the CPU to boost or slow down the system clock (depending on on-going activities) without impacting a potential on-going serial interface transfer on external I/Os.

- SPI: when using the I2S mode, the baud rate is managed through the always 16 MHz or always 32 MHz clock or system clock (CLK_SYS) to reach higher baud rates. When running in other modes than the I2S, the baud rate is managed by the system clock. This implies its baud rate is impacted by dynamic system clock frequency changes.

- TRNG: in parallel with the system clock, the TRNG uses an always 16 MHz clock to generate at a constant frequency the random number whatever the system clock frequency

- Flash controller: in parallel with the system clock, the flash controller uses an always 16 MHz clock to generate specific delays required by the flash memory during programming and erase operations for example
- PKA: in parallel with the system clock, the PKA uses the system clock frequency
- Radio: it does not directly use the system clock for its APB/AHB interfaces, but the system clock with a potential divider (1 or 2 or 4). In parallel, the radio uses an always 16 MHz and an always 32 MHz for modulator, demodulator and to have a fixed reference clock to manage specific delays
- ADC: in parallel with the system clock, ADC uses a 64 MHz prescaled clock running at 16 MHz

## 3.12 General purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB0 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 3.13 Direct memory access (DMA)

The DMA is used in order to provide high-speed data transfer between peripherals and memory as well as memory-to-memory. Data can be quickly moved by DMA without any CPU actions. In this manner, CPU resources are free for other operations.

The DMA controller has eight channels in total. Each has an arbiter to handle the priority among DMA requests.

DMA main features are:

- Eight independently configurable channels (requests)
- Each of the eight channels is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software
- Priorities among requests from channels of DMA are software programmable (four levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, and so on)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer (RAM only)
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to SRAMs and APB1 peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

## 3.14 Nested vectored interrupt controller (NVIC)

The interrupts are handled by the Cortex®-M0+ nested vector interrupt controller (NVIC). NVIC controls specific Cortex®-M0+ interrupts as well as the STM3WB09xE peripheral interrupts.

The NVIC benefits are the following:

- Nested vectored interrupt controller that is an integral part of the Arm® Cortex®-M0+
- Tightly coupled interrupt controller provides low interrupt latency
- Control system exceptions and peripheral interrupts
- NVIC supports 32 vectored interrupts
- Four programmable interrupt priority levels with hardware priority level masking
- Software interrupt generation using the Arm® exceptions SVCall and PendSV
- Support for NMI
- Arm® Cortex® M0+ vector table offset register VTOR implemented

NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

STM32WB09xE
Functional overview

## 3.15 Analog digital converter (ADC)

The STM3WB09xE embeds a 12-bit ADC. The ADC consists of a 12-bit successive approximation analog-to-digital converter (SAR) with 2 x 8 multiplexed channels allowing measurements of up to eight external sources and up to two internal sources.

The ADC main features are:

- Conversion frequency is up to 1 Msps
- Three input voltage ranges are supported (0 - 1.2 V, 0 - 2.4 V, 0 - 3.6 V)
- Up to eight analog single-ended channels or four analog differential inputs or a mix of both
- Temperature sensor conversion
- Battery level conversion up to 3.6 V
- ADC continuous or single mode conversion is possible
- ADC down-sampler for multi-purpose applications to improve analog performance while off-loading the CPU (ratio adjustable from 1 to 128)
- A watchdog feature to inform when data is outside thresholds
- DMA capability
- Interrupt sources with flags.

### 3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

## 3.16 True random number generator (TRNG)

The true random number generator (TRNG) is a hardware module able to generate a random sequence of 128 bits. The TRNG is based on an analog source of entropy composed by free 9 running ring oscillators. The outputs of those oscillators are XORed and sampled for providing random bits, which are then processed by a digital stage.The digital stage is compliant with NIST SP800-90B specifications.

## 3.17 Timers and watchdog

The STM3WB09xE includes three general-purpose timers, one watchdog timer and a SysTick timer.

### 3.17.1 General-purpose timers (TIM2, TIM16, TIM17)

There are up to three general-purpose timers embedded in the STM3WB09xE.

Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
  - Full-featured general-purpose timer
  - Features four independent channels for input capture/output compare, PWM or one-pulse mode output
  - Independent DMA request generation, support of quadrature encoders
- TIM16 and TIM17
  - General-purpose timers with mid-range features:
  - 16-bit auto-reload upcounters and 16-bit prescalers
  - 1 channel and 1 complementary channel
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output
  - The timers have independent DMA request generation
  - The timers are internally connected to generate an infrared interface (IRTIM) for remote control

DS14210 - Rev 6
page 19/73

### 3.17.2 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from the LS clock and it can operate in Deepstop mode. It can also be used as a watchdog to reset the device when a problem occurs.

### 3.17.3 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

## 3.18 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. The RTC provides a time of day/clock/calendar with programmable alarm interrupt. RTC includes also a periodic programmable wakeup flag with interrupt capability. The RTC provides an automatic wakeup to manage all low power modes.

Two 32-bit registers contain seconds, minutes, hours (12- or 24-hour format), day (day of week), date (day of month), month, and year, expressed in binary coded decimal format (BCD). The sub-second value is also available in binary format. Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. Daylight saving time compensation can also be performed. Additional 32-bit registers contain the programmable alarm sub seconds, seconds, minutes, hours, day, and date.

A digital calibration circuit with 0.95 ppm resolution is available to compensate for quartz crystal inaccuracy. After power-on reset, all RTC registers are protected against possible parasitic write accesses. As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under system reset). The RTC counter does not freeze when CPU is halted by a debugger.

## 3.19 Inter-integrated circuit interface (I$^2$C)

The STM3WB09xE embeds ONE I$^2$C. The I$^2$C bus interface handles communications between the microcontroller and the serial I$^2$C bus. It controls all I$^2$C bus-specific sequencing, protocol, arbitration and timing.

The I$^2$C peripheral supports:

- I$^2$C bus specification and user manual rev. 5 compatibilities:
  - Target and controller modes
  - Multicontroller capability
  - Standard-mode (Sm), with a bitrate up to 100 Kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output driver I/Os
  - 7-bit and 10-bit addressing mode
  - Multiple 7-bit target addresses (2 addresses, 1 with configurable mask)
  - All 7-bit address acknowledge mode
  - General call
  - Programmable setup and hold times
  - Easy to use event management
  - Optional clock stretching
  - Software reset
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeouts and idle condition detection
- Power system management protocol (PMBus$^{TM}$) specification rev 1.1 compatibility

- Independent clock: a choice of independent clock sources allowing the I$^2$C communication speed to be independent from the PCLK reprogramming
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

## 3.20 Universal synchronous/asynchronous receiver transmitter (USART)

USART offers flexible full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. USART can communicate with a speed up to 2 Mbit/s. Furthermore, USART can detect and automatically set its own baud rate, based on the reception of a single character.

USART peripheral supports:

- Synchronous one-way communication
- Half-duplex single wire communication
- Local interconnection network (LIN) master/slave capability
- Smart card mode, ISO 7816 compliant protocol
- IrDA (infrared data association) SIR ENDEC specifications
- Modem operations (CTS/RTS)
- RS485 driver enable
- Multiprocessor communications
- SPI-like communication capability

High speed data communication is possible by using DMA (direct memory access) for multibuffer configuration.

## 3.21 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one low-power UART, enabling asynchronous serial communication with minimum power consumption. The LPUART supports half duplex single wire communication and modem operations (CTS/RTS), allowing multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Deepstop mode using baud rates up to 9600 baud. The wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Deepstop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baud rates in Run mode.

The LPUART interfaces can be served by the DMA controller.

## 3.22 Embedded UART bootloader

The STM3WB09xE has a pre-programmed bootloader supporting UART protocol with automatic baud rate detection. The main features of the embedded bootloader are:

- Auto baud rate detection up to 1 Mbit/s
- Flash mass erase, section erase
- Flash programming
- Flash readout protection enable/disable

The pre-programmed bootloader is an application, which is stored in the STM3WB09xE internal ROM at manufacturing time by STMicroelectronics. This application allows upgrading the device flash with a user application using a serial communication channel (UART).

Bootloader is activated by hardware by forcing PA10 high during hardware reset, otherwise, application residing in flash is launched.

## 3.23 Inter-IC sound (I2S)

The STM3WB09xE SPI interface: SPI3 supports the I2S protocol. The I2S interface can operate in slave or master mode with half-duplex communication. It can address four different audio standards:

• Philips I2S standard
• MSB-justified standards (left-justified)
• LSB-justified standards (right-justified)
• PCM standard.

The I2S interfaces DMA capability for transmission and reception.

## 3.24 Serial peripheral interface (SPI)

The STM3WB09xE has one SPI interface (SPI3) allowing communication up to 32 Mbit/s in both master and slave modes. The SPI peripheral supports:

• Master or slave operation
• Multimaster support
• Full-duplex synchronous transfers on three lines
• Half-duplex synchronous transfer on two lines (with bidirectional data line)
• Simplex synchronous transfers on two lines (with unidirectional data line)
• Serial communication with external devices
• NSS management by hardware or software for both master and slave: dynamic change of master/slave operations
• SPI Motorola support
• SPI TI mode support
• Hardware CRC feature for reliable communication

All SPI interfaces can be served by the DMA controller.

## 3.25 Serial wire debug port

The embeds an Arm SWD interface that allows interactive debugging and programming of the device. The interface is composed of only two pins: DEBUG_SWDIO and DEBUG_SWCLK. The enhanced debugging features for developers allow up to four breakpoints and up to two watchpoints.

## 3.26 TX and RX event alert

The STM3WB09xE is provided with the RADIO_TX_SEQUENCE and RADIO_RX_SEQUENCE signals which alert, respectively, transmission and reception activities.

A signal can be enabled for TX and RX on two pins, through alternate functions:

• RADIO_TX_SEQUENCE is available on PA10 (AF2) or PB14 (AF1).
• RADIO_RX_SEQUENCE is available on PA8 (AF2) or PA11 (AF2).

The signal is high when radio is in TX (or RX), low otherwise.

The signals can be used to control external antenna switching and support coexistence with other wireless technologies.

Note: *The RADIO_RF_ACTIVITY signal is used to notify if there is an ongoing RF operation ( either TX or RX). It is a logical OR between the RADIO_RX_SEQUENCE and RADIO_TX_SEQUENCE. This signal can be used to enable an antenna switch component when achieving antenna switching during AoA or AoD operation.*

## 3.27 Direction finding

The STM3WB09xE Bluetooth® radio controller supports the angle of arrival (AoA) and angle of departure (AoD) features by managing:

- the constant tone extension (CTE) inside a packet
- the antenna switching mechanism for both AoA and AoD.

The antenna switching mechanism provides a 7-bit antenna identifier RADIO_ANTENNA_ID[6:0] indicating the antenna number to be used.

In a AoD transmitter or in a AoA receiver, the radio needs to switch antenna during the CTE field of the packet. For this purpose, the RADIO_ANTENNA_ID signal can be enabled on some I/Os, by programming them in the associated alternate function. This signal needs to be provided to an external antenna switching circuit, since RADIO_ANTENNA_ID[0] is the least significant bit and RADIO_ANTENNA _ID[6] the most significant bit of the antenna identifier to be used.

# 4  Pinout, pin description and alternate functions

## 4.1  Pinout/ballout schematics

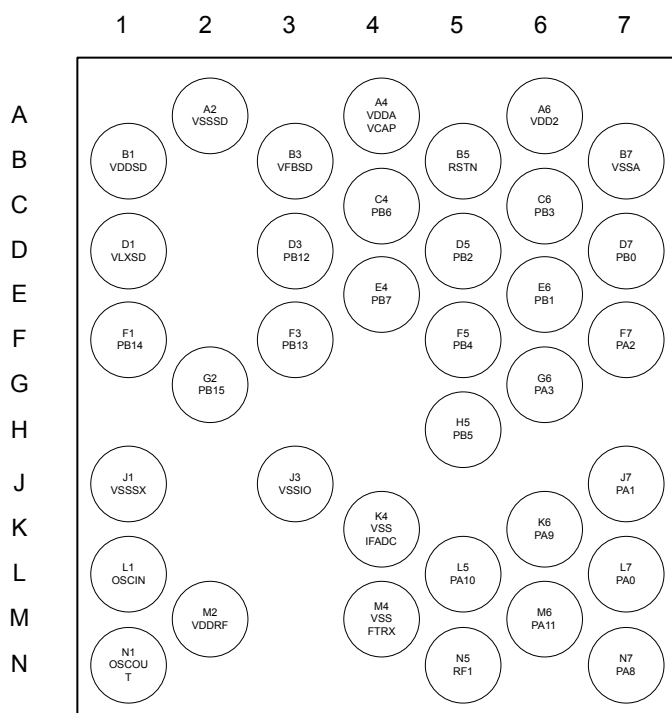The STM3WB09xE comes in two package versions: WLCSP36 offering 20 GPIOs, and VFQFPN32 offering 20 GPIOs.

**Figure 7. VFQFPN32 pinout**
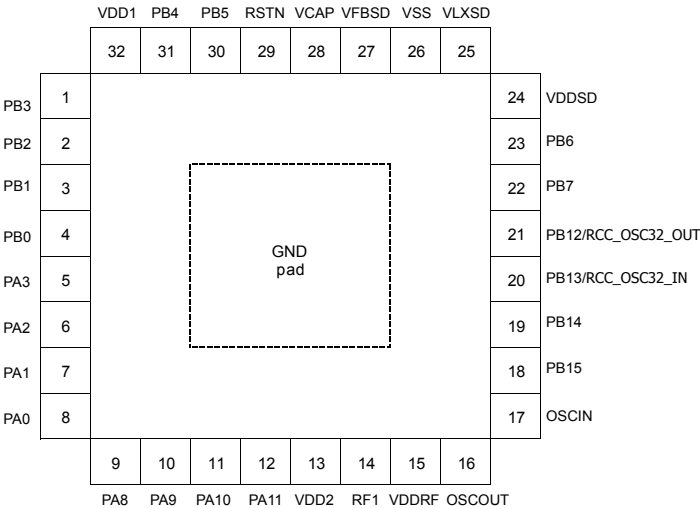
1.  *The above figure shows the package top view.*

Figure 8. **WLCSP36 ballout**



1.  *The above figure shows the package top view.*

## 4.2    Pin description

**Table 5. Legend/abbreviations used in the pinout table**

| Name | Abbreviation | Definition |
|---|---|---|
| Pin name | Unless otherwise specified in brackets below, the pin name and the pin function during and after reset are the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input / output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | TT | 3.6 V tolerant I/O |
| | RF | RF I/O |
| | RST | Bidirectional reset pin with weak pull-up resistor |
| | Options for TT or FT I/Os | |
| | _f[1]. | I/O, Fm+ capable |
| | _a[2]. | I/O, with analog switch function supplied by IO BOOSTER[3] |
| Notes | All I/Os are set as input pullup during and after reset, with the exception of the PA2 (DEBUG_SWDIO) and PA3 (DEBUG_SWCLK) pins which are set, respectively, as alternate function pullup and alternate function pulldown. By default, all I/O pull-ups/pull-downs are controlled by the PWR IP through the PWRC_PUCRx/PWRC_PDCRx registers. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers |
| | Additional functions | Functions directly selected/enabled through peripheral registers |

1.  The related I/O structures in Table 6. Pin description are: FT_f

2.  The related I/O structures in Table 6. Pin description are: FT_a

3.  IO BOOSTER block allows the good behavior of those switches to be guaranteed when the VBAT goes below 2.7 V. Refer to the STM3WB09xE reference Manual (RM0491) for more details.

**Table 6. Pin description**

| Pin number | | Pin name (function after reset) | Pin type | I/O structure | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|
| VFQFPN32 | WLCSP36 | | | | | |
| 1 | C6 | PB3 | I/O | FT_a | USART_CTS, LPUART_TX, SPI3_SCK, TIM2_CH4, TIM17_CH1, RADIO_ANTENNA_ID[3], I2S3_SCK | ADC_VINP0, PWR_WKUP3 |
| 2 | D5 | PB2 | I/O | FT_a | USART_RTS_DE, TIM2_CH3, TIM16_BK, RADIO_ANTENNA_ID[2] | ADC_VINM0, PWR_WKUP2 |
| 3 | E6 | PB1 | I/O | FT_a | USART_CK, TIM2_ETR, TIM16_CH1N, RADIO_ANTENNA_ID[1] | ADC_VINP1, PWR_WKUP1 |
| 4 | D7 | PB0 | I/O | FT_a | USART_RX, LPUART_RTS_DE, TIM16_CH1, RADIO_ANTENNA_ID[0] | ADC_VINM1, PWR_WKUP0 |

| Pin number | | Pin name (function after reset) | Pin type | I/O structure | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|
| VFQFPN32 | WLCSP36 | | | | | |
| 5 | G6 | PA3 | I/O | FT_a | DEBUG_SWCLK, USART_RTS_DE, SPI3_SCK, TIM2_CH2, TIM16_CH1N, I2S3_SCK | ADC_VINP2, PWR_WKUP15 |
| 6 | F7 | PA2 | I/O | FT_a | DEBUG_SWDIO, USART_CK, TIM2_CH1, TIM16_CH1, I2S3_MCK | ADC_VINM2, PWR_WKUP14 |
| 7 | J7 | PA1 | I/O | FT_f | I2C1_SDA, IR_OUT, USART_TX, TIM2_CH4 | PWR_WKUP13 |
| 8 | L7 | PA0 | I/O | FT_f | I2C1_SCL, USART_CTS, IR_OUT, TIM2_CH3 | PWR_WKUP12 |
| 9 | N7 | PA8 | I/O | FT | USART_RX, RADIO_RX_SEQUENCE, SPI3_MISO, TIM2_CH3, TIM16BK | PWR_WKUP8, RTC_OUT |
| 10 | K6 | PA9 | I/O | FT | USART_TX, RTC_OUT, SPI3_NSS, TIM2_CH4, TIM17_CH1, I2S3_WS | PWR_WKUP9 |
| 11 | L5 | PA10 | I/O | FT | LPUART_CTS, RADIO_TX_SEQUENCE, TIM17_CH1N, I2S3_MCK | PWR_WKUP10, RCC_LCO |
| 12 | M6 | PA11 | I/O | FT | RCC_MCO, RADIO_RX_SEQUENCE, SPI3_MOSI, TIM17_BK, I2S3_SD | PWR_WKUP11 |
| 13 | A6 | VDD2 | S | - | - | 1.7-3.6 battery voltage input |
| 14 | N5 | RF1 | I/O | RF | - | RF input/output. Impedance 50 Ω |
| 15 | M2 | VDDRF | S | - | - | 1.7-3.6 battery voltage input |
| 16 | N1 | OSCOUT | I/O | FT_a | - | 32 MHz crystal |
| 17 | L1 | OSCIN | I/O | FT_a | - | 32 MHz crystal |
| 18 | G2 | PB15 | I/O | FT_a | USART_TX | PWR_WKUP19 |
| 19 | F1 | PB14 | I/O | FT_a | RADIO_TX_SEQUENCE, I2C1_SMBA, TIM2_ETR, RCC_MCO, USART_RX | PWR_PVD_IN, PWR_WKUP18 |
| 20 | F3 | PB13 | I/O | FT_a | TIM2_CH4 | RCC_OSC32_IN, PWR_WKUP17 |
| 21 | D3 | PB12 | I/O | FT_a | LPUART_CTS, RCC_LCO, TIM2_CH3 | RCC_OSC32_OUT, PWR_WKUP16 |
| 22 | E4 | PB7 | I/O | FT_f | USART_CTS, I2C1_SDA, LPUART_RX, TIM2_CH2, RF_ACTIVITY | PWR_WKUP7 |
| 23 | C4 | PB6 | I/O | FT_f | I2C1_SCL, LPUART_TX, TIM2_CH1, TIM17_CH1, RADIO_ANTENNA_ID[6] | PWR_WKUP6 |
| 24 | B1 | VDDSD | S | - | - | 1.7-3.6 battery voltage input |
| 25 | D1 | VLXSD | S | - | - | SMPS input/output |
| 26 | A2 | VSSSD | S | - | - | SMPS Ground |

| Pin number | | Pin name (function after reset) | Pin type | I/O structure | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|
| VFQFPN32 | WLCSP36 | | | | | |
| 27 | B3 | VFBSD | S | - | - | SMPS output |
| 28 | A4 | VDDA_VCAP | S | - | - | 1.2 Vdigital core |
| 29 | B5 | RSTN | I/O | RST | - | Reset pin |
| 30 | H5 | PB5 | I/O | FT_a | LPUART_RX, TIM2_CH2, TIM17_BK, RADIO_ANTENNA_ID[5] | PWR_WKUP5, ADC_VINP3 |
| 31 | F5 | PB4 | I/O | FT_a | LPUART_TX, TIM2_CH1, TIM17_CH1N, RADIO_ANTENNA_ID[4] | PWR_WKUP4, ADC_VINM3 |
| 32 | - | VDD1 | S | - | - | 1.7-3.6 battery voltage input |
| - | B7 | VSSA | S | - | - | Ground analog ADC core |
| - | J3 | VSSIO | S | - | - | Ground I/O |
| - | K4 | VSSIFADC | S | - | - | Ground analog RF |
| - | J1 | VSSSX | S | - | - | Ground analog RF |
| - | M4 | VSSRFTRX | S | - | - | Ground analog RF |
| Exposed pad | - | GND | S | - | - | Ground |

## 4.3 Alternate functions

**Table 7. Alternate function port A**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | I2C1/SYS_AF/USART | IR/LPUART/USART | IR/RTC USART/RF | SPI3 | TIM2 | SYS_AF | TIM16/TIM17 | SYS_AF |
| Port A | PA0 | I2C1_SCL | USART_CTS | IR_OUT | - | TIM2_CH3 | - | - | - |
| | PA1 | I2C1_SDA | IR_OUT | USART_TX | - | TIM2_CH4 | - | - | - |
| | PA2 | DEBUG_SWDIO | USART_CK | - | I2S3_MCK | TIM2_CH1 | DEBUG_SWDIO | TIM16_CH1 | DEBUG_SWDIO |
| | PA3 | DEBUG_SWCLK | USART_RTS_DE | - | SPI3_SCK/ I2S3_SCK | TIM2_CH2 | DEBUG_SWCLK | TIM16_CH1N | DEBUG_SWCLK |
| | PA8 | USART_RX | - | RADIO_RX_SEQUENCE | SPI3_MISO | TIM2_CH3 | - | TIM16_BK | - |
| | PA9 | USART_TX | - | RTC_OUT | SPI3_NSS/ I2S3_WS | TIM2_CH4 | - | TIM17_CH1 | - |
| | PA10 | - | LPUART_CTS | RADIO_TX_SEQUENCE | I2S3_MCK | - | - | TIM17_CH1N | - |
| | PA11 | RCC_MCO | - | RADIO_RX_SEQUENCE | SPI3_MOSI/ I2S3_SD | - | - | TIM17_BK | - |

**Table 8. Alternate function port B**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | I2C1/ USART/LPUART | SYS_AF/ LPUART | LPUART/TIM2 TIM16/RIM17 | TIM2/SYS_AF/LPUART | TIM2 | - | RF/USART | - |
| Port B | PB0 | USART_RX | LPUART_RTS_DE | TIM16_CH1 | - | - | - | RADIO_ANTENNA_ID[0] | - |
| | PB1 | USART_CK | - | TIM16_CH1N | TIM2_ETR | - | - | RADIO_ANTENNA_ID[1] | - |
| | PB2 | USART_RTS_DE | - | TIM16_BK | TIM2_CH3 | - | - | RADIO_ANTENNA_ID[2] | - |
| | PB3 | USART_CTS | LPUART_TX | TIM17_CH1 | TIM2_CH4 | SPI3_SCK/ I2S3_SCK | - | RADIO_ANTENNA_ID[3] | - |
| | PB4 | LPUART_TX | - | TIM17_CH1N | - | TIM2_CH1 | - | RADIO_ANTENNA_ID[4] | - |
| | PB5 | LPUART_RX | - | TIM17_BK | - | TIM2_CH2 | - | RADIO_ANTENNA_ID[5] | - |
| | PB6 | I2C1_SCL | - | TIM17_CH1 | LPUART_TX | TIM2_CH1 | - | RADIO_ANTENNA_ID[6] | - |
| | PB7 | I2C1_SDA | - | USART_CTS | LPUART_RX | TIM2_CH2 | - | RADIO_RF_ACTIVITY | - |
| | PB12 | - | RCC_LCO | LPUART_CTS | - | TIM2_CH3 | - | - | - |
| | PB13 | - | - | - | - | TIM2_CH4 | - | - | - |
| | PB14 | I2C1_SMBA | RADIO_TX_SEQUENCE | TIM2_ETR | RCC_MCO | - | - | USART_RX | - |
| | PB15 | - | - | - | - | - | - | USART_TX | - |

# 5 Application circuits

The schematics below are purely indicative.

**Figure 9. Application circuit: DC-DC converter, WLCSP36 package**
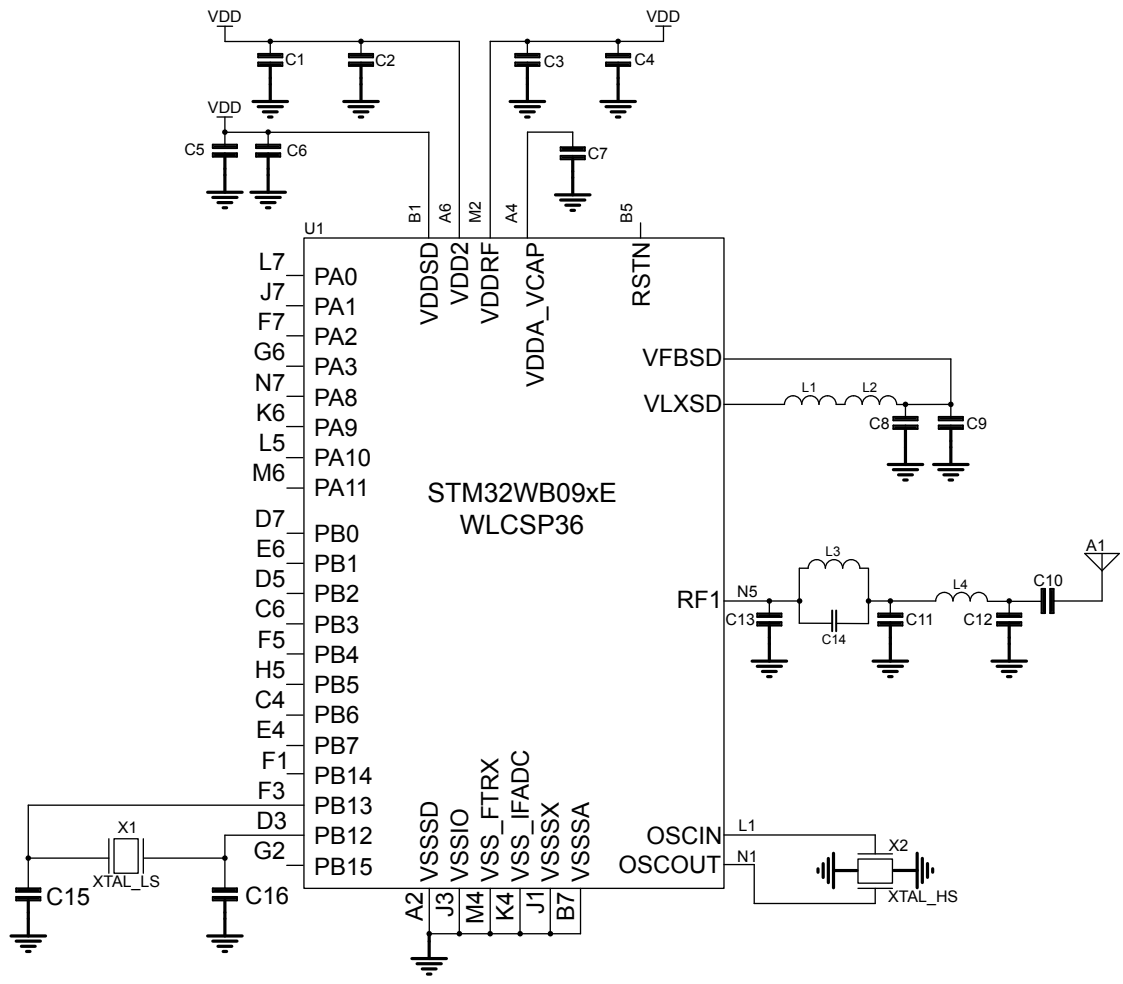
### Figure 10. Application circuit: DC-DC converter, VFQFPN32 package
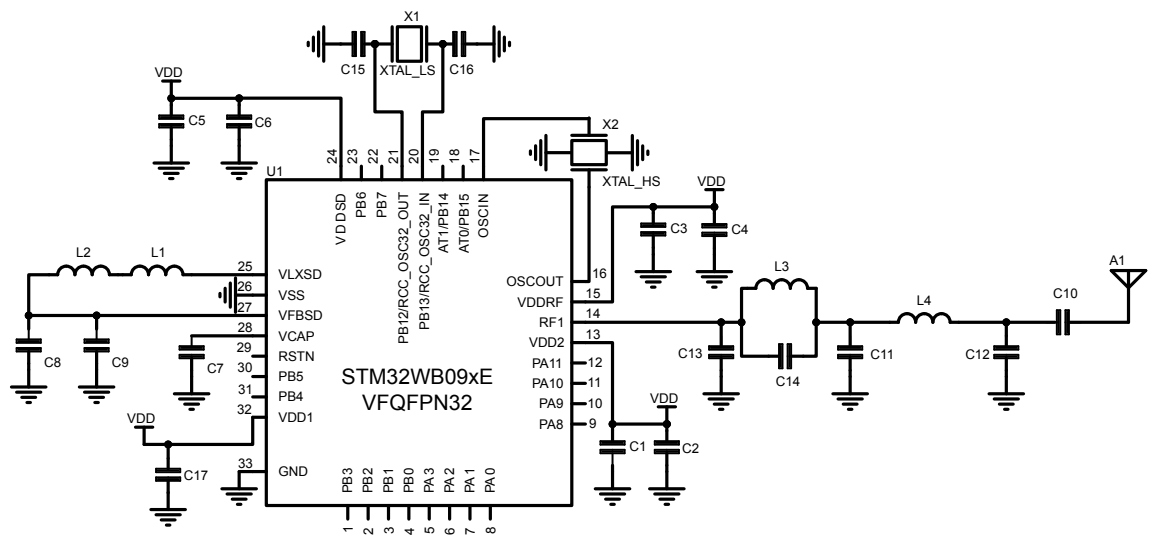
**Table 9. Application circuit external components**

| Component | Description |
|---|---|
| C1 | Decoupling capacitor |
| C2 | Decoupling capacitor |
| C3 | Decoupling capacitor |
| C4 | Decoupling capacitor |
| C5 | Decoupling capacitor |
| C6 | Decoupling capacitor |
| C7 | Main LDO capacitor |
| C8 | DC – DC converter output capacitor |
| C9 | DC – DC converter output capacitor |
| C10 | DC block capacitor |
| C11 | RF matching capacitor |
| C12 | RF Matching capacitor |
| C13 | RF Matching capacitor |
| C14 | RF Matching capacitor |
| C15 | 32 kHz crystal loading capacitor |
| C16 | 32 kHz crystal loading capacitor |
| C17 | Decoupling capacitor |
| L1 | DC-DC converter output inductor |
| L2 | DC-DC converter noise filter |
| L3 | RF matching inductor |
| L4 | RF matching inductor |
| X1 | Low speed crystal |
| X2 | High speed crystal |
| U1 | STM3WB09xE |

Note: *In order to make the board DC–DC OFF, the inductance L1 must be removed and the supply voltage must be applied to the VFBSD pin.*

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to ground (GND).

### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the following standard conditions:

- Ambient temperature is $T_A$ = 25 °C
- Supply voltage is $V_{DD}$: 3.3 V
- System clock frequency is 32 MHz (clock source HSI)
- SMPS clock frequency is 4 MHz

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).
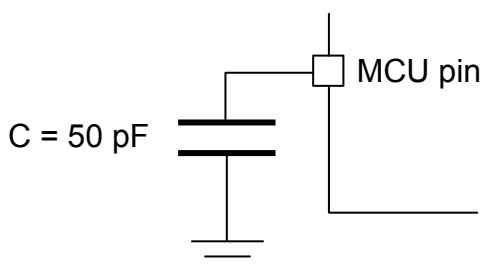
### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are only given as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.
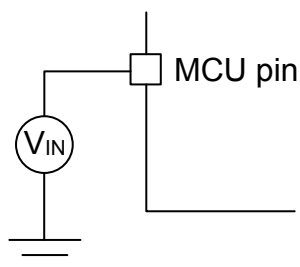
**Figure 11. Pin loading conditions**

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

**Figure 12. Pin input voltage**

## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 10. Voltage characteristics**

| Symbol | Ratings | Min. | Max. | Unit |
|---|---|---|---|---|
| VDD1, VDD2, VDDRF, VDDSD | DC-DC converter supply voltage input and output | -0.3 | +3.9 | V |
| VCAP, VDDA | DC voltage on linear voltage regulator | -0.3 | +1.32 | |
| FXTALOUT, FXTALIN | DC Voltage on HSE | -0.3 | +1.32 | |
| PA0 to PA3, PA8 to PA11, PB0 to PB7, PB14 to PB15 | DC voltage on digital input/output pins | -0.3 | +3.9 | |
| VLXSD, VFBSD | DC voltage on analog pins | | | |
| RCC_OSC32_OUT/PB12, RCC_OSC32_IN/PB13 | DC voltage on XTA | -0.3 | +3.6 | |
| RF1 | DC voltage on RF pin | | +1.4 | - |
| $|\Delta V_{DD}|$ | Variations between different $V_{DDX}$ power pins of the same domain | - | 50 | mV |

*Note:* *All the main power and ground pins must always be connected to the external power supply, in the permitted range.*

**Table 11. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma IV_{DD}$ | Total current into sum of all $V_{DD}$ power lines (source) | 130 | mA |
| $\Sigma IV_{GND}$ | Total current out of sum of all ground lines (sink) | 130 | |
| $IV_{DD(PIN)}$ | Maximum current into each $V_{DD}$ power pin (source) | 100 | |
| $IV_{GND(PIN)}$ | Maximum current out of each ground pin (sink) | 100 | |
| $I_{IO(PIN)}$ | Output current sunk by any I/O and control pin | 20 | |
| | Output current sourced by any I/O and control pin | 20 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all I/Os and control pins | 100 | |
| | Total output current sourced by sum of all I/Os and control pins | 100 | |
| $\Sigma |I_{IN(PIN)}|$ | Total injected current (sum of all I/Os and control pins) | -5/0 | |

**Table 12. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -40 to -125 | °C |
| $T_J$ | Maximum junction temperature | 125 | |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 13. General operating conditions**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|--------|-----------|------------|------|------|------|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 1 | 64 | MHz |
| $f_{PCLK0}$ | Internal APB0 clock | - | 1 | 64 | |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 1 | 64 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 16 | 32 | |
| $V_{DD}$ | Standard operating voltage | - | 1.7 | 3.6 | V |
| $V_{FBSMPS}$ | SMPS feedback voltage | - | 1.4 | 3.6 | |
| $V_{DDRF}$ | Minimum RF voltage | - | 1.7 | 3.6 | |
| $V_{IN}$ | I/O input voltage | - | -0.3 | $V_{DD}$+0.3 | |
| $P_D$ | Power dissipation at $T_A$=105 °C[1] | VFQFPN32 package | - | 30 | mW |
| $T_A$ | Ambient temperature | Maximum power dissipation | -40 | 105 | °C |
| $T_J$ | Junction temperature range | - | -40 | 105 | - |

1. $T_A$ cannot exceed the $T_J$ max.

### 6.3.2 Summary of main performance

**Table 14. Main performance SMPS ON**

| Symbol | Parameter | Test conditions | Typ. VDD = 1.8 V | Typ. VDD = 3.3 V | Unit |
|--------|-----------|-----------------|------------------|------------------|------|
| $I_{CORE}$ | Core current consumption | Shutdown | 12 | 25 | nA |
| | | Deepstop, no timer, wakeup GPIO, RAM0 retained | 0.618 | 0.649 | µA |
| | | Deepstop, no timer, wakeup GPIO, all RAM retained | 0.767 | 0.792 | |
| | | Deepstop (32 kHz LSI), RAM0 retained | 1.103 | 1.197 | |
| | | Deepstop (32 kHz LSI), all RAMs retained | 1.245 | 1.344 | |
| | | Deepstop (32 kHz LSE), RAM0 retained | 0.892 | 0.981 | |
| | | Deepstop (32 kHz LSE), all RAM retained | 0.978 | 1.074 | |
| | | CPU in Run (64 MHz). Dhrystone, clock source PLL64 | 3850 | 2679 | |
| | | CPU in Run (32 MHz). Dhrystone, clock source PLL64 | 2998 | 2216 | |
| | | CPU in RUN (16 MHz). Dhrystone, clock source PLL64 | 2161 | 1759 | |
| | | CPU in RUN (16 MHz). Dhrystone, clock source HSE | 1726 | 1523 | |

| Symbol | Parameter | Test conditions | Typ.<br>VDD = 1.8 V | Typ.<br>VDD = 3.3 V | Unit |
|---|---|---|---|---|---|
| $I_{CORE}$ | Core current consumption | CPU in WFI (64 MHz), all peripherals off, clock source PLL64 | 1860 | 1582 | µA |
| | | CPU in WFI (32 MHz), all peripherals off, clock source PLL64 | 1587 | 1436 | |
| | | CPU in WFI (16 MHz), all peripherals off, clock source PLL64 | 1014 | 1123 | |
| | | CPU in WFI (16 MHz), all peripherals off, clock source Direct HSE | 1447 | 1360 | |
| | | Radio RX at sensitivity level | 6862 | 3693 | |
| | | Radio TX 0 dBm output power | 8669 | 4916 | |
| | | Radio RX at sensitivity level with CPU in WFI (32 MHz), clock source Direct HSE | 7878 | 4815 | |
| | | Radio TX 0 dBm output power with CPU in WFI (32 MHz), clock source Direct HSE | 9683 | 6047 | |
| $I_{DYNAMIC}$ | Dynamic current | Computed value (CPU 64 MHz Dhrystone - CPU 32 MHz Dhrystone) / 32 | 26.63 | 14.47 | µA/MHz |

Table 15. **Main performance SMPS bypassed**

| Symbol | Parameter | Test conditions | Typ.<br>VDD = 1.8 V | Typ.<br>VDD = 3.3 V | Unit |
|---|---|---|---|---|---|
| $I_{CORE}$ | Core current consumption | Shutdown | 12 | 25 | nA |
| | | Deepstop, no timer, wake up GPIO, RAM0 retained | 0.59 | 0.60 | µA |
| | | Deepstop, no timer, wake up GPIO, all RAM retained | 0.72 | 0.74 | |
| | | Deepstop (32 kHz LSI), RAM0 retained | 1.05 | 1.15 | |
| | | Deepstop (32 kHz LSI), all RAMs retained | 1.19 | 1.28 | |
| | | Deepstop (32 kHz LSE ), RAM0 retained | 0.85 | 0.94 | |
| | | Deepstop (32 kHz LSE), all RAM retained | 0.98 | 1.08 | |
| | | CPU in Run (64 MHz). Dhrystone, clock source PLL64 | 4617 | 4635 | |
| | | CPU in Run (32 MHz). Dhrystone, clock source PLL64 | 3532 | 3627 | |
| | | CPU in RUN (16 MHz), all peripherals off, clock source PLL64 | 1930 | 1630 | |
| | | CPU in RUN (16 MHz), all peripherals off, clock source HSE | 1497 | 1395 | |
| | | CPU in WFI (64 MHz), all peripherals off, clock source PLL64 | 1904 | 1926 | |
| | | CPU in WFI (32 MHz), all peripherals off, clock source PLL64 | 1587 | 1436 | |
| | | CPU in WFI (16 MHz), all peripherals off, clock source PLL64 | 1860 | 1583 | |
| | | CPU in WFI (16 MHz), all peripherals off, clock source Direct HSE | 829 | 853 | |
| | | Radio RX at sensitivity level | - | 8301 | |
| | | Radio TX 0 dBm output power | - | 9681 | |
| | | Radio RX at sensitivity level with CPU in WFI (32MHz), clock source Direct HSE | - | 9171 | |

| Symbol | Parameter | Test conditions | Typ.<br>VDD = 1.8 V | Typ.<br>VDD = 3.3 V | Unit |
|---|---|---|---|---|---|
| $I_{CORE}$ | Core current consumption | Radio TX 0 dBm output power with CPU in WFI (32MHz), clock source Direct HSE | - | 10526 | µA |
| $I_{DYNAMIC}$ | Dynamic current | Computed value (CPU 64 MHz Dhrystone - CPU 32 MHz Dhrystone) / 32 | - | 31.5 | µA/MHz |

**Table 16. Peripheral current consumption at VDD = 3.3 V, system clock (32 MHz), SMPS on**

| Parameter | Typ. | Unit |
|---|---|---|
| ADC | 25 | µA |
| DMA | 34 | |
| GPIOA | 1 | |
| GPIOB | 1 | |
| I2C1 | 40 | |
| IWDG | 7 | |
| LPUART | 54 | |
| PKA | 358 | |
| TRNG | 67 | |
| RTC | 10 | |
| SPI3/I2S3 | 38/43 | |
| Systick | 8 | |
| TIM2 | 132 | |
| TIM16 | 80 | |
| TIM17 | 77 | |
| USART | 87 | |
| SYSCFG | 23 | |
| CRC | 6 | |

## 6.3.3 RF general characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

**Table 17. Bluetooth® LE RF general characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{RANGE}$ | Frequency range[1] | - | 2400 | - | 2483.5 | MHz |
| $RF_{CH}$ | RF channel center frequency[1] | - | 2402 | - | 2480 | |
| $PLL_{RES}$ | RF channel spacing[1] | - | - | 2 | - | MHz |
| $\Delta F$ | Frequency deviation[1] | - | - | 250 | - | kHz |
| $\Delta f1$ | Frequency deviation average[1] | - | 450 | - | 550 | kHz |
| $C_{Fdev}$ | Center frequency deviation[1] | During the packet and including both initial frequency offset and drift | - | - | ±150 | kHz |
| $\Delta fa$ | Frequency deviation Δf2 (average) / Δf1 (average)[1] | - | 0.80 | - | - | - |
| $R_{gfsk}$ | On-air data rate[1] | - | 1 | - | 2 | Mbit/s |
| STacc | Symbol time accuracy[1] | - | - | - | ±50 | ppm |
| MOD | Modulation scheme | - | GFSK | | | - |
| BT | Bandwidth-bit period product | - | - | 0.5 | - | - |
| Mindex | Modulation index[1] | - | 0.45 | 0.5 | 0.55 | - |
| PMAX | Maximum output | At antenna connector, VSMPS = 1.9 V, LDO code | - | +8 | - | dBm |
| PMIN | Minimum output | At antenna connector | - | -20 | - | dBm |
| PRFC | RF power accuracy | @ 27 °C | - | ±1.5 | - | dB |
| | | All temperatures | - | ±2.5 | - | |

1. *Tested according to Bluetooth® SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

### 6.3.4 RF transmitter characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

**Table 18. Bluetooth® LE RF transmitter characteristics at 1 Mbit/s not coded**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $P_{BW1M}$ | 6 dB bandwidth for modulated carrier | Using resolution bandwidth of 100 kHz | - | 670 | - | kHz |
| $P_{RF1}$, 1 Ms/s | In-band emission at ±2 MHz[1] | Using resolution bandwidth of 100 kHz and average detector | - | -41 | - | dBm |
| $P_{RF2}$, 1 Ms/s | In-band emission at ±[3+n]MHz, where n=0,1,2..[1] | Using resolution bandwidth of 100 kHz and average detector | - | -45 | - | dBm |
| $PS_{PUR}$ | Spurious emission | Harmonics included. Using resolution bandwidth of 1 MHz and average detector | - | - | -41 | dBm |
| $Freq_{drift}$ | Frequency drift[1] | Integration interval #n – integration interval #0, where n=2,3,4..k | -50 | - | +50 | kHz |
| $IFreq_{drift}$ | Initial carrier frequency drift[1] | Integration interval #1 – integration interval #0 | -23 | - | +23 | kHz |
| $Int_{Freqdrift}$ | Intermediate carrier frequency drift[1] | Integration interval #n – integration interval #(n-5), where n=6,7,8..k | -20 | - | +20 | kHz |
| Drift Rate max | Maximum drift rate[1] | Between any two 10-bit groups separated by 50 µs | -20 | - | +20 | kHz/50 µs |
| $Z_{RF1}$ | Optimum RF load (impedance at RF1 pin) | @ 2440 MHz | - | 40 | - | Ω |

1. *Tested according to Bluetooth® SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

**Table 19. Bluetooth® LE RF transmitter characteristics at 2 Mbit/s not coded**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $P_{BW1M}$ | 6 dB bandwidth for modulated carrier | Using resolution bandwidth of 100 kHz | - | 1140 | - | kHz |
| $P_{RF1}$, 2 Ms/s | In-band emission at ±4 MHz[1] | Using resolution bandwidth of 100 kHz and average detector | - | -47 | - | dBm |
| $P_{RF2}$, 2 Ms/s | In-band emission at±5 MHz[1] | Using resolution bandwidth of 100 kHz and average detector | - | -47 | - | dBm |
| $P_{RF3}$, 2 Ms/s | In-band emission at ±[6+n]MHz, where n=0,1,2..[1] | Using resolution bandwidth of 100 kHz and average detector | - | -48 | - | dBm |
| $P_{SPUR}$ | Spurious emission | Harmonics included. Using resolution bandwidth of 1 MHz and average detector | - | - | -41 | dBm |
| $Freq_{drift}$ | Frequency drift[1] | Integration interval #n – integration interval #0, where n=2,3,4..k | -50 | - | +50 | kHz |
| $IFreq_{drift}$ | Initial carrier frequency drift[1] | Integration interval #1 – integration interval #0 | -23 | - | +23 | kHz |
| $IntFreq_{drift}$ | Intermediate carrier frequency drift[1] | Integration interval #n – integration interval #(n-5), where n=6,7,8..k | -20 | - | +20 | kHz |
| $DriftRate_{max}$ | Maximum drift rate[1] | Between any two 20-bit groups separated by 50 µs | -20 | - | +20 | kHz/50µs |
| $Z_{RF1}$ | Optimum RF load (impedance at RF1 pin) | @ 2440 MHz | - | 40 | - | Ω |

1. *Tested according to Bluetooth® SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

**Table 20. Bluetooth® LE RF transmitter characteristics at 1 Mbit/s LE coded (S=8)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $P_{BW}$ | 6 dB bandwidth for modulated carrier | Using resolution bandwidth of 100 kHz | - | 670 | - | kHz |
| $P_{RF1, LE\ coded}$ | In-band emission at ±2 MHz[1] | Using resolution bandwidth of 100 kHz and average detector | - | -41 | - | dBm |
| $P_{RF2, LE\ coded}$ | In-band emission at ±[3+n] MHz, where n=0,1,2..[1] | Using resolution bandwidth of 100 kHz and average detector | - | -45 | - | dBm |
| $PS_{PUR}$ | Spurious emission | Harmonics included. Using resolution bandwidth of 1 MHz and average detector | - | - | -41 | dBm |
| $Freq_{drift}$ | Frequency drift[1] | Integration interval #n – integration interval #0, where n=1,2,3..k | -50 | - | +50 | kHz |
| $IFreq_{drift}$ | Initial carrier frequency drift[1] | Integration interval #3 – integration interval #0 | -19.2 | - | +19.2 | kHz |
| $IntFreq_{drift}$ | Intermediate carrier frequency drift[1] | Integration interval #n – integration interval #(n-3), where n=7,8,9..k | -19.2 | - | +19.2 | kHz |
| $DriftRate_{max}$ | Maximum drift rate[1] | Between any two 16-bit groups separated by 48 µs | -19.2 | - | +19.2 | kHz/48 µs |
| $Z_{RF1}$ | Optimum RF load (Impedance at RF1 pin) | @ 2440 MHz | - | 40 | - | Ω |

1. *Tested according to Bluetooth® SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

### 6.3.5 RF receiver characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

**Table 21. Bluetooth® LE RF receiver characteristics at 1 Msym/s uncoded**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $RX_{SENS}$ | Sensitivity | PER < 30.8% | - | -97 | - | dBm |
| $P_{SAT}$ | Saturation | PER < 30.8% | - | 8 | - | dBm |
| $Z_{RF1}$ | Optimum RF source (impedance at RF1 pin) | @ 2440 MHz | - | 40 | - | Ω |
| RF selectivity with Bluetooth® LE equal modulation on interfering signal |
| $C/I_{CO-channel}$ | Co-channel interference $f_{RX} = f_{interference}$ | Wanted signal = -67 dBm, PER < 30.8% | - | 8 | - | dBc |
| $C/I_{1\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz | Wanted signal = -67 dBm, PER < 30.8% | - | -1 | - | dBc |
| $C/I_{2\ MHz}$ | Adjacent Interference $f_{interference} = f_{RX} \pm 2$ MHz | Wanted signal = -67 dBm, PER < 30.8% | - | -35 | - | dBc |
| $C/I_{3\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…] | Wanted signal = -67 dBm, PER < 30.8% | - | -47 | - | dBc |
| $C/I_{Image}$ | Image frequency interference $f_{interference} = f_{image}$ | Wanted signal = -67 dBm, PER < 30.8% | - | -25 | - | dBc |
| $C/I_{Image \pm 1\ MHz}$ | Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz | Wanted signal= -67 dBm, PER < 30.8% | - | -25 | - | dBc |
| Out of band blocking (interfering signal CW) |
| $C/I_{Block}$ | Interfering signal frequency 30 MHz – 2000 MHz | Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 10 MHz | - | 5 | - | dB |
| $C/I_{Block}$ | Interfering signal frequency 2003 MHz – 2399 MHz | Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 3 MHz | - | -5 | - | dB |
| $C/I_{Block}$ | Interfering signal frequency 2484 MHz – 2997 MHz | Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 3 MHz | - | -5 | - | dB |
| $C/I_{Block}$ | Interfering signal frequency 3000 MHz – 12.75 GHz | Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 25 MHz | - | 10 | - | dB |
| Intermodulation characteristics (CW signal at $f_1$, Bluetooth® LE interfering signal at $f_2$) |
| P_IM(3) | Input power of IM interferer at 3 and 6 MHz distance from wanted signal | Wanted signal = -64 dBm, PER < 30.8% | - | -27 | - | dBm |
| P_IM(-3) | Input power of IM interferer at -3 and -6 MHz distance from wanted signal | Wanted signal = -64 dBm, PER < 30.8% | - | -40 | - | dBm |
| P_IM(4) | Input power of IM interferer at ±4 and ±8 MHz distance from wanted signal | Wanted signal= -64 dBm, PER < 30.8% | - | -32 | - | dBm |
| P_IM(5) | Input power of IM interferer at ±5 and ±10 MHz distance from wanted signal | Wanted signal = -64 dBm, PER < 30.8% | - | -32 | - | dBm |

**Table 22. Bluetooth® LE RF receiver characteristics at 2 Msym/s uncoded**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RX$_{SENS}$ | Sensitivity | PER < 30.8% | - | -94 | - | dBm |
| P$_{SAT}$ | Saturation | PER < 30.8% | - | 8 | - | dBm |
| Z$_{RF1}$ | Optimum RF source (impedance at RF1 pin) | @ 2440 MHz | - | 40 | - | Ω |
| RF selectivity with Bluetooth® LE equal modulation on interfering signal | | | | | | |
| C/I$_{CO-channel}$ | Co-channel interference $f_{RX} = f_{interference}$ | Wanted signal= -67 dBm, PER < 30.8% | - | 8 | - | dBc |
| C/I$_{2 MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz | Wanted signal = -67 dBm, PER < 30.8% | - | -14 | - | dBc |
| C/I$_{4 MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 4$ MHz | Wanted signal = -67 dBm, PER < 30.8% | - | -41 | - | dBc |
| C/I$_{6 MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm (6+2n)$ MHz [n = 0,1,2…] | Wanted signal = -67 dBm, PER < 30.8% | - | -45 | - | dBc |
| C/I$_{Image}$ | Image frequency interference $f_{interference} = f_{image-2M}$ | Wanted signal = -67 dBm, PER < 30.8% | - | -25 | - | dBc |
| C/I$_{Image\pm1 MHz}$ | Adjacent channel-to-image frequency $f_{interference} = f_{image-2M} \pm 2$ MHz | Wanted signal= -67 dBm, PER < 30.8% | -<br>- | -14 | - | dBc |
| Out of band blocking (interfering signal CW) | | | | | | |
| C/I$_{Block}$ | Interfering signal frequency 30 MHz – 2000 MHz | Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 10 MHz | - | 5 | - | dB |
| C/I$_{Block}$ | Interfering signal frequency 2003 MHz – 2399 MHz | Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 3 MHz | - | -5 | - | dB |
| C/I$_{Block}$ | Interfering signal frequency 2484 MHz – 2997 MHz | Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 3 MHz | - | -5 | - | dB |
| C/I$_{Block}$ | Interfering signal frequency 3000 MHz – 12.75 GHz | Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 25 MHz | - | 10 | - | dB |
| Intermodulation characteristics (CW signal at $f_1$, Bluetooth® LE interfering signal at $f_2$) | | | | | | |
| P_IM(6) | Input power of IM interferer at 6 and 12 MHz distance from wanted signal | Wanted signal= -64 dBm, PER < 30.8% | - | -27 | - | dBm |
| P_IM(-6) | Input power of IM interferer at -6 and -12 MHz distance from wanted signal | Wanted signal= -64 dBm, PER < 30.8% | - | -30 | - | dBm |
| P_IM(8) | Input power of IM interferer at ±8 and ±16 MHz distance from wanted signal | Wanted signal= -64 dBm, PER < 30.8% | - | -30 | - | dBm |
| P_IM(10) | Input power of IM interferer at ±10 and ±20 MHz distance from wanted signal | Wanted signal= -64 dBm, PER < 30.8% | - | -28 | - | dBm |

**Table 23. Bluetooth® LE RF receiver characteristics at 1 Msym/s LE coded (S=2)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $RX_{SENS}$ | Sensitivity | PER < 30.8% | | -100 | - | dBm |
| $P_{SAT}$ | Saturation | PER < 30.8% | - | 8 | - | dBm |
| $Z_{RF1}$ | Optimum RF source (impedance at RF1 pin) | @ 2440 MHz | | 40 | - | Ω |
| RF selectivity with Bluetooth® LE equal modulation on interfering signal | | | | | | |
| $C/I_{CO\text{-channel}}$ | Co-channel interference $f_{RX} = f_{interference}$ | Wanted signal = -72 dBm, PER < 30.8% | | 2 | - | dBc |
| $C/I_{1\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz | Wanted signal = -72 dBm, PER < 30.8% | | -5 | - | dBc |
| $C/I_{2\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz | Wanted signal = -72 dBm, PER < 30.8% | - | -38 | - | dBc |
| $C/I_{3\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…] | Wanted signal = -72 dBm, PER < 30.8% | | -50 | - | dBc |
| $C/I_{Image}$ | Image frequency interference $f_{interference} = f_{image}$ | Wanted signal = -72 dBm, PER < 30.8% | | -30 | - | dBc |
| $C/I_{Image\pm1}$ MHz | Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz | Wanted signal = -72 dBm, PER < 30.8% | | -34 | - | dBc |

**Table 24. Bluetooth® LE RF receiver characteristics at 1 Msym/s LE coded (S=8)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $RX_{SENS}$ | Sensitivity | PER < 30.8% | | -104 | - | dBm |
| $P_{SAT}$ | Saturation | PER < 30.8% | - | 8 | - | dBm |
| $Z_{RF1}$ | Optimum RF source (impedance at RF1 pin) | @ 2440 MHz | | 40 | - | Ω |
| RF selectivity with Bluetooth® LE equal modulation on interfering signal | | | | | | |
| $C/I_{CO\text{-channel}}$ | Co-channel interference $f_{RX} = f_{interference}$ | Wanted signal = -79 dBm, PER < 30.8% | | 1 | - | dBc |
| $C/I_{1\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz | Wanted signal = -79 dBm, PER < 30.8% | | -4 | - | dBc |
| $C/I_{2\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz | Wanted signal = -79 dBm, PER < 30.8% | | -39 | - | dBc |
| $C/I_{3\ MHz}$ | Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…] | Wanted signal = -79 dBm, PER < 30.8% | - | -53 | - | dBc |
| $C/I_{Image}$ | Image frequency interference $f_{interference} = f_{image}$ | Wanted signal = -79 dBm, PER < 30.8% | | -33 | - | dBc |
| $C/I_{Image} \pm 1$ MHz | Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz | Wanted signal = -79 dBm, PER < 30.8% | | -32 | - | dBc |

### 6.3.6 Embedded reset and power control block characteristics

**Table 25. Embedded reset and power control block characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| TRSTTEMPO | Reset temporization after PDR is detected | $V_{DD}$ rising | - | - | 500 | µs |
| $V_{PDR}$ | Power-down reset threshold | - | - | 1.58 | - | |
| $V_{PVD0}$ | PVD0 threshold | PVD0 threshold at the falling edge of $V_{DDIO}$ | - | 2.05 | - | |
| $V_{PVD1}$ | PVD1 threshold | PVD1 threshold at the falling edge of $V_{DDIO}$ | - | 2.21 | - | |
| $V_{PVD2}$ | PVD2 threshold | PVD2 threshold at the falling edge of $V_{DDIO}$ | - | 2.36 | - | |
| $V_{PVD3}$ | PVD3 threshold | PVD3 threshold at the falling edge of $V_{DDIO}$ | - | 2.53 | - | V |
| $V_{PVD4}$ | PVD4 threshold | PVD4 threshold at the falling edge of $V_{DDIO}$ | - | 2.64 | - | |
| $V_{PVD5}$ | PVD5 threshold | PVD5 threshold at the falling edge of $V_{DDIO}$ | - | 2.82 | - | |
| $V_{PVD6}$ | PVD6 threshold | PVD6 threshold at the falling edge of $V_{DDIO}$ | - | 2.91 | - | |
| $V_{PVD7}$ | PVD threshold for $V_{IN\_PVD}$ | PVD7 threshold (VBGP) at the falling edge of $V_{IN\_PVD}$ | - | 1 | - | |

### 6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as: the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

**Table 26. Current consumption**

| Symbol | Parameter | Conditions | Typ. | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$(Run) | Supply current in Run mode[1] | $f_{HCLK}$ = 64 MHz  All peripherals disabled | 2349 | 2428 | 2476 | µA |
| | | $f_{HCLK}$ = 32 MHz  All peripherals disabled | 1964 | 2040 | 2086 | |
| | | $f_{HCLK}$ = 16 MHz  All peripherals disabled | 1617 | 1686 | 1729 | |
| $I_{DD}$(Deepstop) | Supply current in Deepstop[2] | Clock OFF | 742 | 5197 | 12499 | nA |
| | | Clock source LSI | 1290 | 5791 | 13294 | |
| | | Clock source LSI  RTC ON | 1358 | 5900 | 13298 | |
| | | Clock source LSI  IWDG ON | 1300 | 5864 | 13298 | |
| | | Clock source LSI  RTC, LPUART and IWDG ON[3] | 1373 | 5946 | 13395 | |

| Symbol | Parameter | Conditions | Typ. | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25 °C | 85 °C | 105 °C | |
| $I_{DD}$(Deepstop) | Supply current in Deepstop[2] | Clock source LSE | 1023 | 5547 | 12929 | nA |
| | | Clock source LSE RTC ON | 1090 | 5682 | 13007 | |
| | | Clock source LSE IWDG ON | 1043 | 5599 | 13003 | |
| | | Clock source LSE. LPUART ON | 1128 | 5682 | 13035 | |
| | | Clock source LSE RTC, LPUART and IWDG ON | 1212 | 5816 | 13160 | |
| $I_{DD}$(Shutdown) | Supply current in Shutdown | SMPS ON | 20 | 279 | 871 | |
| $I_{DD}$(RST) | Current under reset condition | - | 956 | 1073 | 1160 | µA |

1. *The CPU executes a "while(1)" loop*
2. *The current consumption in Deepstop is measured considering the entire SRAM retained.*
3. *LPUART not functional in deepstop mode with LSI (only LSE)*

### 6.3.8 Wakeup time from low-power modes

The wakeup times reported are the latency between the event and the execution of the instruction. The device goes to low-power mode after WFI (wait for interrupt) instructions.

**Table 27. Low-power mode wakeup timing**

| Symbol | Parameter | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $T_{WUDEEPSTOP}$ | Wakeup time from Deepstop mode to Run mode | Wakeup from GPIO $V_{DD}$ = 3.3 V flash memory | 170 | µs |

### 6.3.9 High speed crystal requirements

The high speed external oscillator must be supplied with an external 32 MHz crystal that is specified for a 6 to 8 pF loading capacitor. The STM32WB09 includes internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one. These internal load capacitors are made by a fixed one, in parallel with a 6-bit binary weighted capacitor bank. Thanks to low CL step size (LSB is typically 0.07 pF), very fine crystal tuning is possible. With a typical XTAL sensitivity of -14 ppm/pF, it is possible to trim a 32 MHz crystal, with a resolution of 1 ppm.

The requirements for the external 32 MHz crystal are reported in the table below.

**Table 28. HSE crystal requirements**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{NOM}$ | Oscillator frequency | - | - | 32 | - | MHz |
| $f_{TOL}$ | Frequency tolerance | Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance | - | - | ±50 | ppm |
| ESR | Equivalent series resistance | - | - | - | 100 | Ω |
| $P_D$ | Drive level | - | - | - | 100 | µW |
| CL | HSE crystal load capacitance | 27 °C, GMCONF = 3 | 5 [1] | 7 [2] | 9.2 [3] | pF |
| CLstep | HSE crystal load capacitance LSB value | 27 °C, GMCONF = 3 XOTUNE code between 32 and 33 | - | 0.07 | - | pF |

1. *XOTUNE programed at minimum code = 0*

2. *XOTUNE programed at center code = 32*

3. *XOTUNE programed at maximum code = 63*

## 6.3.10 Low speed crystal requirements

Low speed clock can be supplied with an external 32.768 kHz crystal oscillator. Requirements for the external 32.768 kHz crystal are reported in the table below.

**Table 29. LSE crystal requirements**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{NOM}$ | Nominal frequency | - | - | 32.768 | - | kHz |
| ESR | Equivalent series resistance | - | - | - | 90 | kΩ |
| $P_D$ | Drive level | - | - | - | 0.1 | µW |
| $G_{mcritmax}$ | Maximum critical crystal $g_m$ | LSEDRIV[1:0] = 00 Low drive capability | - | - | 0.50 | µA/V |
| | | LSEDRIV[1:0] = 01 Medium low drive capability | - | - | 0.75 | |
| | | LSEDRIV[1:0] = 10 Medium high drive capability | - | - | 1.70 | |
| | | LSEDRIV[1:0] = 11 High drive capability | - | - | 2.70 | |

## 6.3.11 High speed ring oscillator characteristics

**Table 30. HSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{NOM}$ | Nominal frequency | - | - | 64 | - | MHz |

## 6.3.12 Low speed ring oscillator characteristics

**Table 31. LSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{NOM}$ | Nominal frequency | $V_{DD}$ =3 .3 V Ambient temperature Typical corner | - | 33 | - | kHz |
| $\Delta F_{RO\_\Delta T}/F_{RO}$ | Frequency spread vs. temperature | Standard deviation | - | 140 | - | ppm/°C |

## 6.3.13 PLL characteristics

Characteristics measured over recommended operating conditions unless otherwise specified.

**Table 32. PLL characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $PN_{SYNTH}$ | RF carrier phase noise | At ±1 MHz offset from carrier (measured at 2.4 GHz) | - | -110 | - | dBc/Hz |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| PN$_{SYNTH}$ | RF carrier phase noise | At 2.4 GHz ±3 MHz offset from carrier (measured at 2.4 GHz) | - | -114 | - | dBc/Hz |
| | | At 2.4 GHz±6 MHz offset from carrier (measured at 2.4 GHz) | - | -128 | - | dBc/Hz |
| | | At ±25 MHz offset from carrier | - | -135 | - | dBc/Hz |
| LOCK$_{TIMETX}$ | PLL lock time to TX | With calibration @2.5 ppm | - | 150 | - | µs |
| LOCK$_{TIMERX}$ | PLL lock time to RX | With calibration @2.5 ppm | - | 110 | - | µs |
| LOCK$_{TIMERXTX}$ | PLL lock time RX to TX | Without calibration @2.5 ppm | - | 47 | - | µs |
| LOCK$_{TIMETXRX}$ | PLL lock time TX to RX | Without calibration @2.5 ppm | - | 32 | - | µs |

### 6.3.14 Flash memory characteristics

The characteristics below are guaranteed by design.

**Table 33. Flash memory characteristics**

| Symbol | Parameter | Test conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| t$_{prog}$ | 32-bit programming time | - | 20 | 40 | µs |
| t$_{prog\_burst}$ | 4x32-bit burst programming time | - | 4x20 | 4x40 | |
| t$_{ERASE}$ | Page (2 kbyte) erase time | - | 20 | 40 | ms |
| t$_{ME}$ | Mass erase time | - | 20 | 40 | |
| I$_{DD}$ | Average consumption from V$_{DD}$ | Write mode | 3 | - | mA |
| | | Erase mode | 3 | - | |
| | | Mass erase | 5 | - | |

**Table 34. Flash memory endurance and data retention**

| Symbol | Parameter | Test conditions | Min. | Unit |
|---|---|---|---|---|
| N$_{END}$ | Endurance | T$_A$ = -40 to +105 °C | 10 | kcycles |
| t$_{RET}$ | Data retention | T$_A$ = 105 °C | 10 | Years |

### 6.3.15 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

**Table 35. ESD absolute maximum ratings**

| Symbol | Parameter | Conditions | Class | Max.[1] | Unit |
|---|---|---|---|---|---|
| V$_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | Conforming to ANSI/ESDA/JEDEC JS-001 | 2 | 2000 | V |
| V$_{ESD(CBM)}$ | Electrostatic discharge voltage (charge device model) | Conforming to ANSI/ESDA/STM5.3.1 JS-002 | C2a | 500 | |

1. Guaranteed by design.

### 6.3.16 I/O port characteristics

Unless otherwise specified, the parameters given in the tables below are derived from tests performed under the conditions summarized in Table 13. All I/Os are designed as CMOS-compliant.

The characteristics below are guaranteed by characterization.

**Table 36. I/O static characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| $V_{IL}$ | I/O input low level voltage | 1.62 V < $V_{DD}$ < 3.6 V | - | - | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | I/O input high level voltage | | 0.7 x $V_{DD}$ | - | - | |
| $I_{lkg}$ | Input leakage current | 0 <= $V_{IN}$ <= Max($V_{DDx}$)[1] | - | - | +/-100 | nA |
| | | Max($V_{DDx}$)[1] <= $V_{IN}$ <= Max($V_{DDx}$)[1] +1 V | - | - | 650 | |
| | | Max($V_{DDx}$)[1] + 1 V < $V_{IN}$ <= 5.5 V | - | - | 200 | |
| $R_{PU}$ | Pull-up resistor | $V_{IN}$ = GND | 25 | 40 | 55 | kΩ |
| $R_{PD}$ | Pull-down resistor | $V_{IN}$ = $V_{DD}$ | 25 | 40 | 55 | |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Max($V_{DDx}$) is the maximum value among all the I/O supplies.

All I/Os are CMOS-compliant (no software configuration required).

GPIOs (general purpose input/outputs) can sink or source up to ±8 mA and sink or source up to ± 20 mA (with a relaxed $V_{OL}$ / $V_{OH}$).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified.

- The sum of currents sourced by all I/Os on $V_{DD}$, plus the maximum consumption of MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating ΣIV$_{DD}$
- The sum of currents sunk by all I/Os on $V_{SS}$, plus the maximum consumption of the MCU sunk on GND, cannot exceed the absolute maximum rating ΣIV$_{GND}$

The characteristics below are guaranteed by characterization.

**Table 37. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|--------|-----------|------------|------|------|------|
| $V_{OL}$ | Output low level voltage for I/O pin | CMOS port[1] \|$I_{IO}$\| = 8 mA $V_{DD}$ ≥ 2.7 V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage for I/O pin | | $V_{DD}$ -0.4 | - | |
| $V_{OL}$ | Output low level voltage for I/O pin | \|$I_{IO}$\| = 20 mA $V_{DD}$ ≥ 2.7 V | - | 1.3 | |
| $V_{OH}$ | Output high level voltage for I/O pin | | $V_{DD}$ -1.3 | - | |
| $V_{OL}$ | Output low level voltage for I/O pin | \|$I_{IO}$\| = 4 mA $V_{DD}$ ≥ 1.62 V | - | 0.4 | |
| $V_{OH}$ | Output high level voltage for I/O pin | | $V_{DD}$-0.45 | - | |

1. CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

### 6.3.17 RSTN pin characteristics

The RSTN pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 13.

The characteristics below are guaranteed by design.

**Table 38. RSTN pin characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit. |
|--------|-----------|-----------------|------|------|------|-------|
| $V_{IL(RSTN)}$ | RSTN input low level voltage | - | - | - | $0.3 \times V_{DD}$ | V |
| $V_{IH(RSTN)}$ | RSTN input high level voltage | - | $0.7 \times V_{DD}$ | - | - | |
| $V_{hys(RSTN)}$ | RSTN Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| RPU | Weak pull-up equivalent resistor | $V_{IN}$=GND | 25 | 40 | 55 | kΩ |

**Figure 13. Recommended RSTN pin protection**
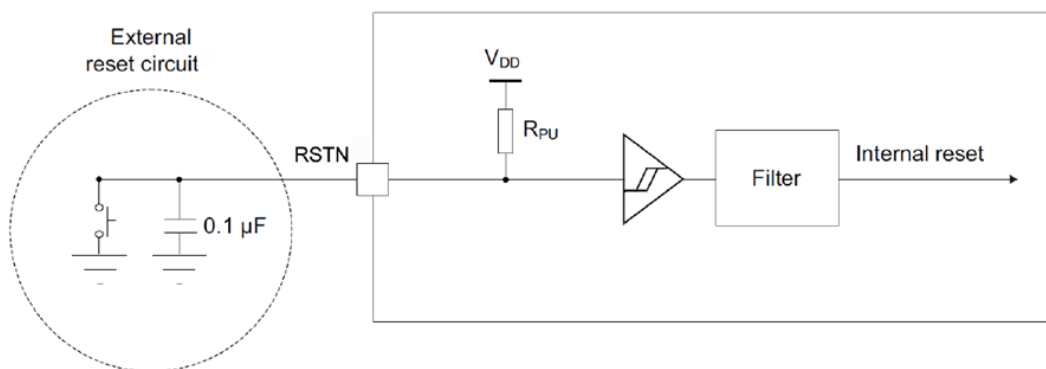


1. The external reset circuit protects the device against parasitic resets.
2. The user must ensure that the level on the RSTN pin can go below the $V_{IL}$(RSTN) max. level specified in the table, otherwise the reset is not taken into account by the device.
3. The external capacitor on RSTN must be placed as close as possible to the device.

## 6.3.18 ADC characteristics

**Table 39. ADC characteristics (HSI must be set to PLL mode)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Units |
|--------|-----------|-----------------|------|------|------|-------|
| Ch_diff_num | Number of channels for differential mode | VFQFPN32, WLCSP36 | - | - | 4 | - |
| Ch_se_num | Number of channels for single ended mode | VFQFPN32, WLCSP36 | - | - | 8 | - |
| IBAT$_{ADCBIAS}$ | ADC biasing consumption at battery | Biasing blocks turned on | - | 145 | - | µA |
| IBAT$_{ADCACTIVE}$ | ADC active consumption at battery | ADC activated in differential mode | - | 185 | - | µA |
| $V_{DDA}$ | Analog supply voltage | - | 1.2 | - | 1.32 | V |
| $R_{AIN}$ | Input impedance | In DC | - | 250 | - | kΩ |
| $R_{in}$ | Internal access resistance | $V_{BOOST}$ is enabled for $V_{BAT}$ < 2.7 V | - | - | 550 | Ω |
| $C_{in}$ | Input sampling capacitor | - | - | 4 | - | pF |
| $T_s$ | Sampling period | Default configuration | - | 1 | - | µs |
| $T_{sw}$ | Sampling time | Default configuration | - | 125 | - | ns |
| DR | Output data rate | - | - | 200 | - | k samples/s |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| FRMT$_{output}$ | Output data format | - | - | 16 | - | bits |
| TL | Latency time | 200 kSps | - | 5 | - | µs |
| T$_{STARTUP}$ | Start-up time | From ADC enable to conversion start | - | - | 1 | µs |
| DNL | Differential non-linearity | - | - | ±0.7 | - | LSB |
| INL | Integral non-linearity | - | - | ±1 | - | LSB |
| SNR Diff | Signal to noise ratio | Differential input @1 kHz, -1 dBFs, F$_S$ = 1 MHz with DF | - | 72 | - | dB |
| STHD Diff | Signal to THD ratio (10 harmonics) | Differential input @1 kHz, -1 dBFs, F$_S$ = 1 MHz with DF | - | 75 | - | dB |
| ENOB Diff | Effective number of bits | Differential input @1 kHz, -1 dBFs, F$_S$ = 1 MHz with DF | - | 11.5 | - | bits |
| SNR SE | Signal-to-noise ratio | Single ended @1 kHz, -1 dBFs, F$_S$ = 1 MHz with DF | - | 70 | - | dB |
| STHD SE | Signal-to THD ratio (10 harmonics) | Single ended @1 kHz, -1 dBFs, F$_S$ = 1 MHz with DF | - | 70 | - | dB |
| ENOB SE | Effective number of bits | Single ended @1 kHz, -1 dBFs, F$_S$ = 1 MHz with DF | - | 11 | - | bits |
| - | ADC_ERR_1V7 | Absolute error when used for battery measurements at 1.7 V, 2.4 V, 3.0 V, 3.6 V | - | 13 | - | mV |
| - | ADC_ERR_2V4 | | - | 0 | - | mV |
| - | ADC_ERR_3V0 | | - | -9 | - | mV |
| - | ADC_ERR_3V6 | | - | -22 | - | mV |

### 6.3.19 Temperature sensor characteristics

#### Table 40. Temperature sensor characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| T$_{rERR}$ | Error in temperature | - | ±4 | - | °C |
| T$_{SLOPE}$ | Average temperature coefficient | - | 8 | - | LSB/°C |
| T$_{ICC}$ | Current consumption | - | 415 | - | µA |
| T$_{TS-out}$ | Output Code at 30°C (+-5°C) | - | - | 2533 | bit |

### 6.3.20 Timer characteristics

The characteristics below are guaranteed by design.

#### Table 41. TIM1 characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| t$_{res(TIM)}$ | Timer resolution time | f$_{TIMxCLK}$ = 64 MHz | - | 15.625 | - | ns |
| R$_{esTIM}$ | Timer resolution | - | - | 16 | - | bit |
| t$_{COUNTER}$ | 16-bit counter clock period | f$_{TIMxCLK}$ = 64 MHz | 0.015625 | - | 1024 | µs |
| t$_{MAX\_COUNT}$ | Maximum possible count time | f$_{TIMxCLK}$= 64 | - | - | 67.10 | s |

**Table 42. IWDG min./max. timeout period at 32 kHz (LSE)**

| Prescaler divider | PR[2:0] bits | Min. timeout RL[11:0] = 0x000 | Max. timeout RL[11:0] = 0xFFF | Unit |
|---|---|---|---|---|
| /4 | 0 | 0.125 | 512 | ms |
| /8 | 1 | 0.250 | 1024 | |
| /16 | 2 | 0.500 | 2048 | |
| /32 | 3 | 1.0 | 4096 | |
| /64 | 4 | 2.0 | 8192 | |
| /128 | 5 | 4.0 | 16384 | |
| /256 | 6 or 7 | 8.0 | 32768 | |

## 6.3.21 I$^2$C interface characteristics

The I$^2$C interface meets the timing requirements of the I$^2$C-Bus specifications and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 Kbit/s
- Fast-mode (Fm): bit rate up to 400 Kbit/s
- Fast-mode plus (Fm+): bit rate up to 1 Mbit/s

SDA and SCL I/O requirements are met with the following restrictions: SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present. The 20 mA output drive requirement in fast-mode plus is supported partially.

This limits the maximum load $C_{load}$ supported in fast-mode plus, given by these formulas:

- $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(min.) = [V_{DD} - V_{OL}(max)] / I_{OL}(max)$

where $R_p$ is the I$^2$C lines pull-up.

All I$^2$C SDA and SCL I/Os embed an analog filter.

The characteristics below are guaranteed by design.

**Table 43. I$^2$C analog filter characteristics**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50 | 110 | ns |

## 6.3.22 SPI characteristics

The parameters for SPI are derived from tests performed according to $f_{PCLKx}$ frequency and supply voltage conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x $V_{DD}$

The characteristics below are guaranteed by design.

**Table 44. SPI characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SPI clock frequency | Master mode | - | - | 32 | MHz |
| | | Slave mode | | | 32[1] | |
| $t_{su}(NSS)$ | NSS setup time | - | $4 / f_{PCLK}$ | - | - | - |
| $t_h(NSS)$ | NSS hold time | - | $2 / f_{PCLK}$ | - | - | - |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|-----------|------------|------|------|------|-------|
| $t_w(SCKH)$ | SCK high and low time | Master mode | $1 / f_{PCLK}$ - 1.5 | $1 / f_{PCLK}$ | $1 / f_{PCLK}$+1 | ns |
| $t_w(SCKL)$ | | | $1 / f_{PCLK}$- 1.5 | $1 / f_{PCLK}$ | $1 / f_{PCLK}$+1 | |
| $t_{su}(MI)$ | Data input set-up time | Master mode | 2 | - | - | |
| $t_{su}(SI)$ | Data input set-up time | Slave mode | 1 | - | - | |
| $t_h(MI)$ | Data input hold time | Master mode | 2 | - | - | |
| $t_h(SI)$ | Data input hold time | Slave mode | 0 | - | - | |
| $t_a(SO)$ | Data output access time | Slave mode | 6 | - | 30 | |
| $t_{dis}(SO)$ | Data output disable time | Slave mode | 6 | - | 32 | |
| $t_v(MO)$ | Data output valid time | Master mode | - | 5 | 9 | |
| $t_v(SO)$ | | Slave mode | - | 12 | 35 | |
| $t_h(MO)$ | Data output hold time | Master mode | 1 | - | - | |
| $t_h(SO)$ | | Slave mode | 6 | - | | |

1. The maximum frequency in slave transmitter mode is determined by the sum of $t_v(SO)$ and $t_{su}(MI)$, which has to fit SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su}(MI)$ = 0 while duty(SCK) = 50 %.

**Figure 14.** SPI timing diagram - slave mode and CPHA = 0
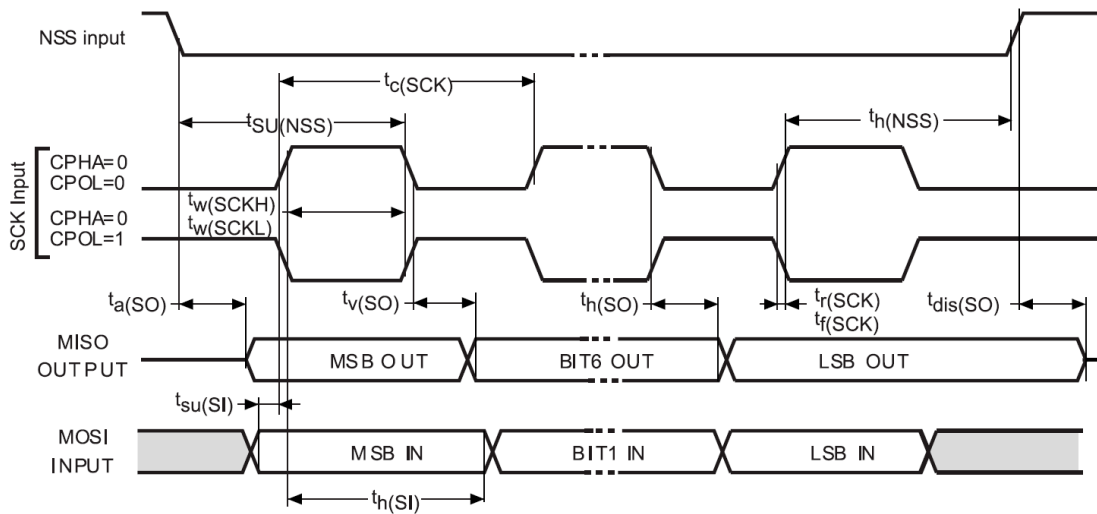
**Figure 15. SPI timing diagram - slave mode and CPHA = 1**
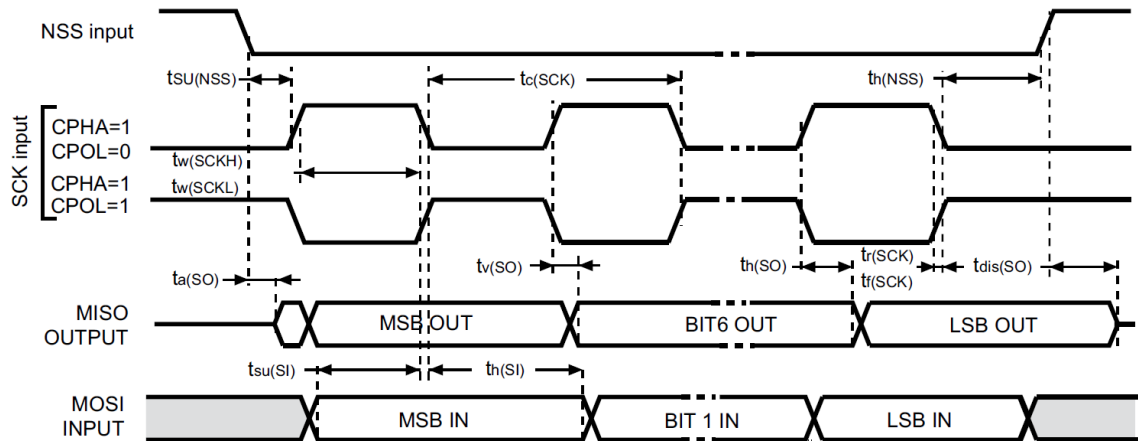


**Figure 16. SPI timing diagram - master mode**
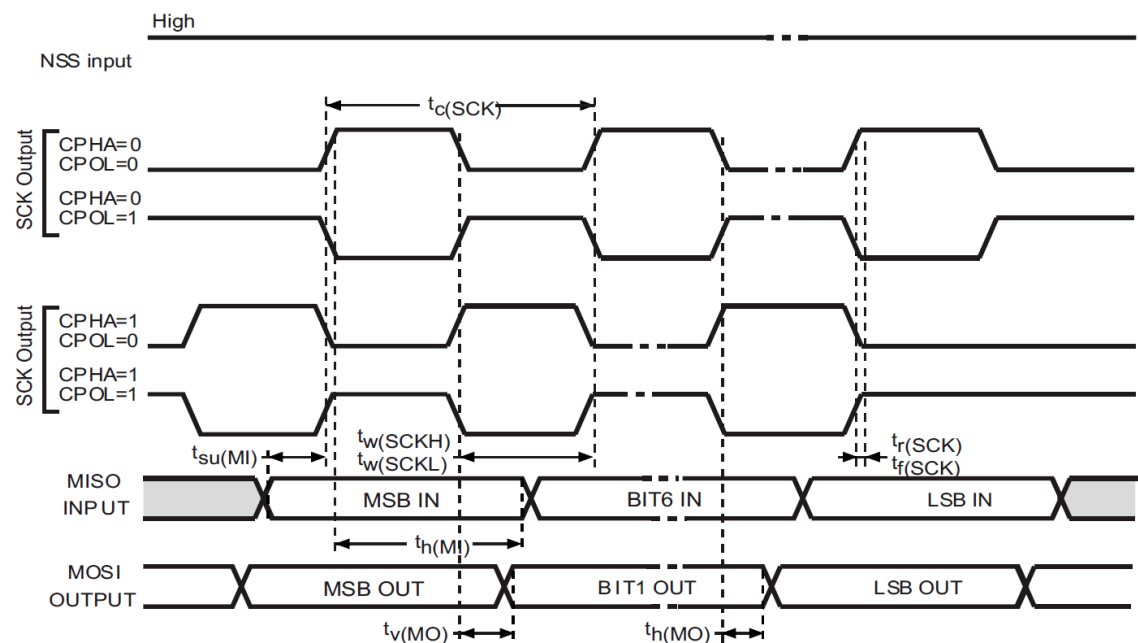
# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK2 packages, depending on their level of environmental compliance. ECOPACK2 specifications, grade definitions and product status are available at: www.st.com. ECOPACK2 is an ST trademark.

## 7.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433 ) available on http://www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example is provided in the corresponding package information subsection.

## 7.2 VFQFPN32 package information (42)

This VFQFPN is a 32 lead, 5 x 5 mm, 0.50 mm pitch, very fine pitch quad flat no lead package.

**Figure 17. VFQFPN32 - Outline**



BOTTOM VIEW
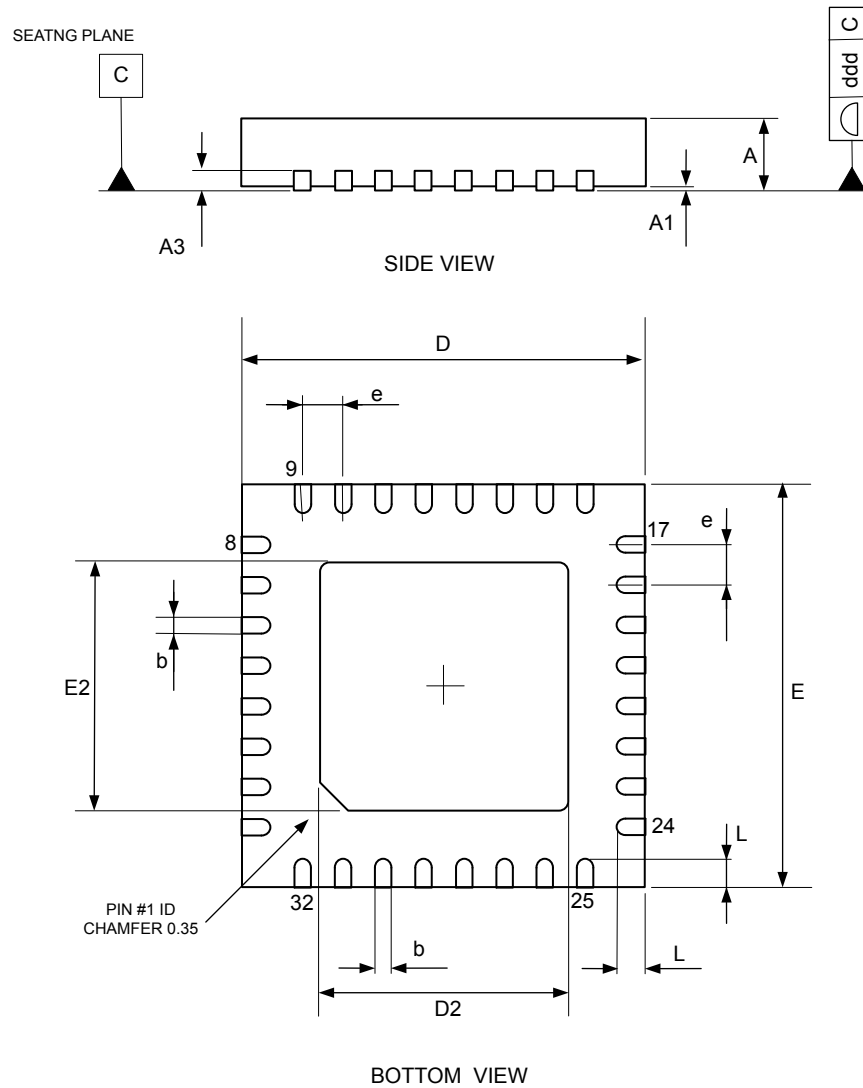
1. Drawing is not to scale.
2. Package outline exclusive of any mold flashes dimensions and metal burrs.
3. Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.

**Table 45. VFQFPN32 - Mechanical data**

| Symbol | Millimetres | | | Inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2] | 0.80 | 0.90 | 1.00 | 0.0315 | 0.0354 | 0.0394 |
| A1 | 0 | - | 0.05 | 0 | - | 0.0020 |
| A3 | - | 0.20 | - | - | 0.008 | - |
| b | 0.18 | 0.25 | 0.30 | 0.0070 | 0.0098 | 0.0118 |
| D | 4.90 | 5.00 | 5.10 | 0.1929 | 0.19 | 0.2008 |
| E | 4.90 | 5.00 | 5.10 | 0.1929 | 0.19 | 0.2008 |
| D2 | 3.60 | 3.70 | 3.80 | 0.1417 | 0.1457 | 0.1496 |
| E2 | 3.60 | 3.70 | 3.80 | 0.1417 | 0.1457 | 0.1496 |
| e | - | 0.50 | - | - | 0.0197 | - |
| L | 0.30 | 0.40 | 0.50 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.05 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 3 decimal digits.

2. VFQFPN stands for thermally Enhanced very thin fine pitch quad flat package No lead . Very thin profile 0.80 < A ≤ 1.00 mm.

**Figure 18. VFQFPN32 - Footprint example**
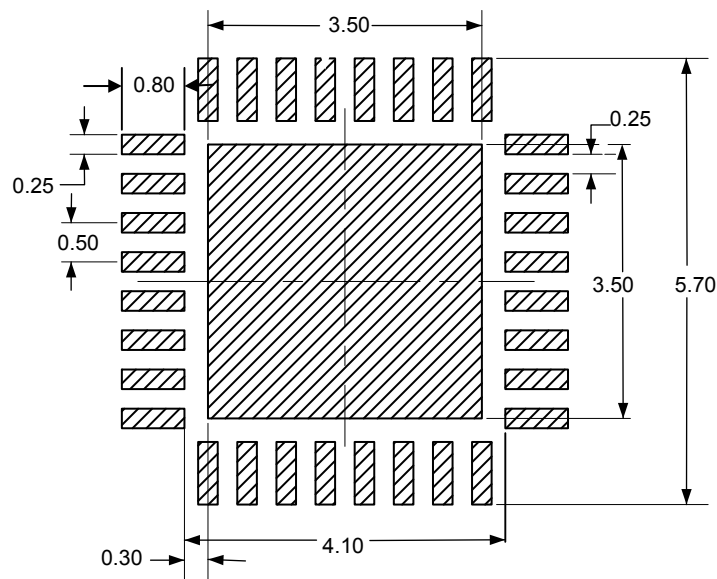


42_VFQFPN32_CALAMBA_FP_V1

## 7.3 WLCSP36 package information (B0LY)

This WLCSP is a 36-ball, 2.83 x 2.99 mm, 0.40 mm pitch, wafer level chip scale package.

**Figure 19. WLCSP36 - Outline**
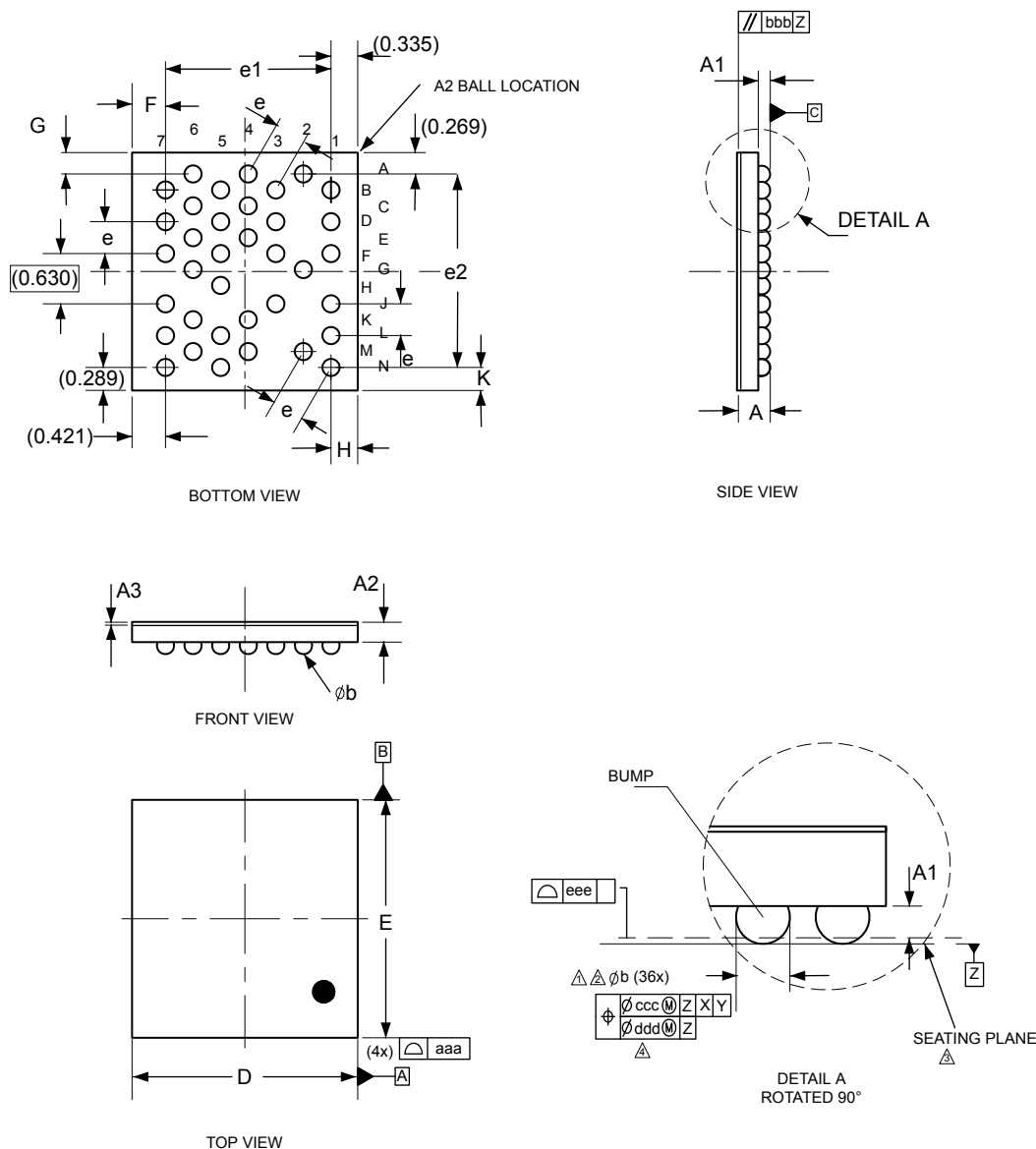


1. *Drawing is not to scale.*

2. *Dimension is measured at the maximum bump diameter parallel to primary datum Z.*

3. *Primary datum Z and seating plane are defined by the spherical crowns of the bump.*

4. *Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.*

**Table 46. WLCSP36 - Mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2] | - | - | 0.43 | - | - | 0.0168 |
| A1 | - | 0.15 | - | - | 0.0059 | - |
| A2 | - | 0.25 | - | - | 0.0098 | - |
| A3[3] | - | 0.025 | - | - | 0.0010 | - |
| b[4] | 0.19 | 0.22 | 0.24 | 0.0076 | 0.0086 | 0.0096 |
| D | 2.81 | 2.83 | 2.85 | 0.1108 | 0.1116 | 0.1124 |
| E | 2.97 | 2.99 | 3.01 | 0.1168 | 0.1176 | 0.1184 |
| e | - | 0.40 | - | - | 0.0157 | - |
| e1 | - | 2.08 | - | - | 0.0818 | - |
| e2 | - | 2.43 | - | - | 0.0957 | - |
| F[5] | - | 0.419 | - | - | 0.0164 | - |
| G[5] | - | 0.269 | - | - | 0.0106 | - |
| H[5] | - | 0.333 | - | - | 0.0131 | - |
| K[5] | - | 0.289 | - | - | 0.0113 | - |
| N | 36 | | | | | |
| aaa | - | - | 0.10 | - | - | 0.004 |
| bbb | - | - | 0.10 | - | - | 0.004 |
| ccc[6] | - | - | 0.10 | - | - | 0.004 |
| [7] | - | - | 0.05 | - | - | 0.002 |
| eee | - | - | 0.05 | - | - | 0.002 |

1. Values in inches are converted from mm and rounded to 3 decimal digits.

2. The maximum total package height is calculated by the RSS method (root sum square) using nominal and tolerances values of A1 and A2.

3. Back side coating. Nominal dimension is rounded to the 3$^{rd}$ decimal place resulting from process capability.

4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

5. Calculated dimensions are rounded to the 3$^{rd}$ decimal place

6. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

7. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 20. WLCSP36 - Footprint example
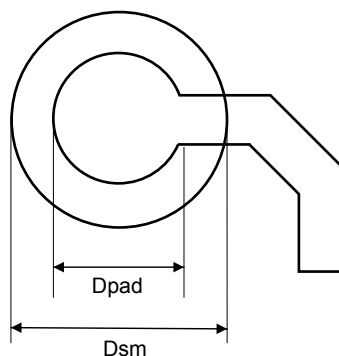


1. Dimensions are expressed in millimeters.

Table 47. WLCSP36 - Example of PCB design rules

| Dimension | Values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0,225 mm |
| Dsm | 0.290 mm typ. (depends on soldermask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

### 7.3.1 Device marking example for WLCSP36

The following figure gives an example of topside marking versus pin 1 position identifier location. The printed markings may differ depending on the supply chain. Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 21. WLCSP36 marking example (package top view)**
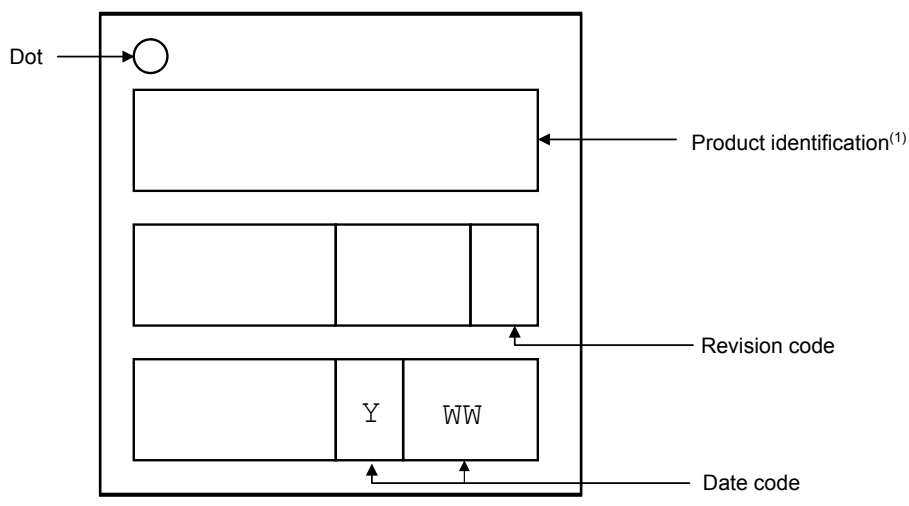


1. Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax.}$) must never exceed the values in general operating conditions.

The maximum chip-junction temperature, $T_J$ max., in degrees Celsius, can be calculated using the equation:

$$T_J\text{max.} = T_A\text{max.} + (PD\text{max} \times \theta JA) \tag{1}$$

where:

- $T_A$ max. is the maximum ambient temperature in °C
- $\Theta JA$ is the package junction-to-ambient thermal resistance, in °C/W
- $P_D$ max. is the sum of $P_{INT}$ max. and $P_{I/O}$ max. ($P_D$ max. = $P_{INT}$ max. + $P_{I/O}$ max.)
- PINT max. is the product of $I_{DD}$ and $V_{DD}$, expressed in Watt. This is the maximum chip internal power

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max. = $\Sigma$ ($V_{OL} \times I_{OL}$) + $\Sigma$ (($V_{DD} - V_{OH}$) × $I_{OH}$)

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the applications.

*Note:* *When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the chip power dissipation. This portion depends mainly on the inductor ESR characteristics.*

*Note:* *As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.*

*Note:* *RF characteristics (such as: sensitivity, Tx power, consumption) are provided up to 85 °C.*

**Table 48. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $\Theta JA$ | Thermal resistance junction-ambient<br>VFQFPN32 - 5 mm x 5 mm | 26.9 | °C/W |

# 8 Ordering information

**Table 49. Ordering information scheme**

| Example: | STM32 | WB | 09 | K | E | V | 6 | TR |
|---|---|---|---|---|---|---|---|---|

**Device family**

STM32 = Arm-based 32-bit microcontroller

**Product type**

WB = wireless Bluetooth®

**Device subfamily**

09 = full set of features

**Pin count**

K = 32 pins

T = 36 pins

**Flash memory size**

E = 512 Kbytes

**Package**[1]

F = WLCSP

V = VFQFPN

**Temperature range**

6 = -40 °C up to +85 °C

7 = -40 °C up to +105 °C

**Packing**

TR = tape and reel

1. ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).

Note:       For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

# 9    Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.

- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.

- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.

- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.

- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

# Revision history

**Table 50. Document revision history**

| Date | Version | Changes |
|---|---|---|
| 21-Sep-2023 | 1 | Initial release. |
| 06-Feb-2024 | 2 | Removed Section 5 Memory mapping.<br>Added Table 1. STM32WB09xE device features and peripheral counts<br>Updated:<br>• Section Features (ultra-low power radio performance figures)<br>• Section 3.11: Clock management<br>• Figure 6. Clock tree<br>• Section 3.25: Serial wire debug port<br>• Section 3.26: TX and RX event alert<br>• Section 3.27: Direction finding<br>• Table 6. Pin description<br>• Table 7. Alternate function port A<br>• Table 8. Alternate function port B<br>• Table 10. Voltage characteristics<br>• Table 14. Main performance SMPS ON<br>• Table 15. Main performance SMPS bypassed |
| 16-Feb-2024 | 3 | • Removed unresolved product link from Product summary.<br>• Replaced generic product path used in document. |
| 11-Jun-2024 | 4 | Updated:<br>• Product status link / summary<br>• Features<br>• Section 1: Introduction<br>• Section 2: Description<br>• Section 3.5: Security and safety<br>• Figure 6. Clock tree<br>• Table 6. Pin description<br>• Table 7. Alternate function port A<br>• Figure 9. Application circuit: DC-DC converter, WLCSP36 package<br>• Figure 10. Application circuit: DC-DC converter, VFQFPN32 package<br>• Table 9. Application circuit external components<br>• Table 29. LSE crystal requirements |
| 03-Sep-2024 | 5 | Updated VFQFPN32 package information (42) |
| 17-Mar-2025 | 6 | Throughout document, replaced the Bluetooth term "Low Energy" with "LE".<br>Updated:<br>• Section Features<br>• Section 3.19: Inter-integrated circuit interface ($I^2C$)<br>• Table 5. Legend/abbreviations used in the pinout table |

# Contents

# List of tables

# List of figures

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.