Data Sheet

LT80602, LT80603

3V to 65V, 2.5A/3.5A/4.5A Synchronous Step-Down Silent Switcher with 8µA Quiescent Current

FEATURES

- **Silent Switcher®** Architecture
  - Ultralow EMI Emissions
  - Spread Spectrum Frequency Modulation
- High Efficiency at High Frequency
- Up to 94.3% at 400kHz, 90% at 2.1MHz, $24V_{IN}$ to $5V_{OUT}$
- Up to 95.6% at 400kHz, 91.1% at 2.1MHz, $48V_{IN}$ to $12V_{OUT}$
- Pin Selectable Fixed 3.3V, Fixed 5V, or Adjustable Output from 0.8V to 99% of V_{IN}
- Low Quiescent Current Burst Mode Operation
  - 8µA I_Q Regulating $24V_{IN}$ to $5V_{OUT}$
- On-the-Fly Mode Change Among Burst Mode, Pulse-Skipping Mode, and FCM
- Built-in Output-Voltage Monitoring and Die Temperature Monitoring with PG/T_J
- 200kHz to 3MHz Adjustable Switching Frequency with External Clock Synchronization
- 80V Transient-Input Tolerant (LT8060xHV)
- Programmable Soft-Start and Tracking
- Small 17-Lead 3mm × 3mm Quad Flat No-lead (QFN)

APPLICATIONS

- General Purpose Step-Down
- Automotive and Industrial Supplies

GENERAL DESCRIPTION

The LT8060x and LT8060xHV step-down regulators **family** feature the Silent Switcher® architecture to minimize electromagnetic interference (EMI) emissions while delivering high efficiency at frequencies up to 3MHz. The LT80602 and LT80602HV deliver up to 2.5A continuous current, the LT80603 and LT80603HV support up to 3.5A, and the LT80603A and LT80603AHV provide up to 4.5A continuous current. An ultralow 8µA quiescent current, with the output in full regulation, enables applications requiring the highest efficiency at light loads. An accurate enable threshold can be set using the EN/UV pin and a resistor at the RT pin to program the switch frequency.

The LT8060x and LT8060xHV enable high-V_{IN} to low-V_{OUT} conversion at high frequency, featuring a production-tested fast minimum top-switch on-time of 25ns (typ). In addition, the device features a PG/T_J pin that can be used to monitor the status of the output voltage or the die temperature. The die temperature monitor allows for direct measurement of the silicon die temperature, enabling a robust and reliable power supply design.

GENERIC PART NUMBER	AbsMax V_{IN}
LT8060x	70V
LT8060xHV	80V

SIMPLIFIED APPLICATION DIAGRAM

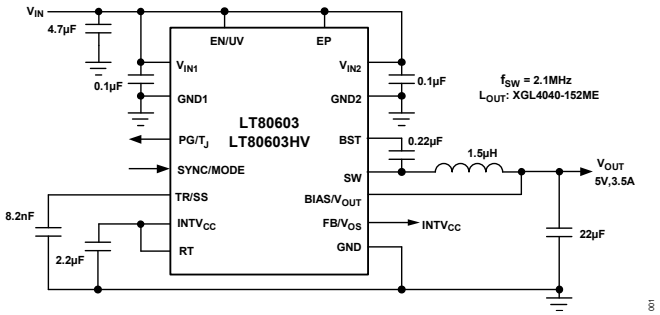


Figure 1. Typical Application Circuit

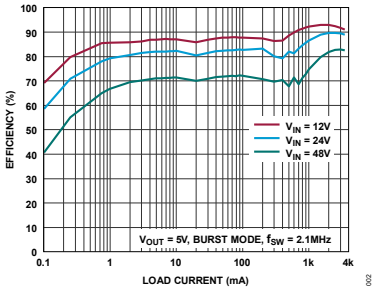


Figure 2. Efficiency vs. Load Current

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/26	Initial release	—
1	4/26	Updated Figure 90 Replaced Figure 94 Updated Ordering Guide	46 50 51
2	7/26	Updated Features and General Description sections Updated Absolute Maximum Ratings section Updated Operation section Updated Figure 73 Updated Ordering Guide	1 9 26 28 51

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SPECIFICATIONS

Table 1. Electrical Characteristics

($V_{IN1} = V_{IN2} = V_{IN} = V_{EN/UV} = 24V$, RT = unconnected ($f_{SW} = 400kHz$), $C_{INTVCC} = 2.2\mu F$, $V_{GND} = V_{GND1} = V_{GND2} = V_{BIAS/VOUT} = 0V$, $V_{SYNC/MODE} = 0V$, $V_{FB/Vos} = 0.84V$, SW = TR/SS = PG/T_J = unconnected, V_{BST} to $V_{SW} = 1.8V$, $T_J = -40°C$ to $+150°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. All voltages are referenced to GND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		3		65	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UV} = 0V$ ($T_A = T_J = +25°C$), $V_{IN} = 12V$		0.75	1.50	µA
		$V_{EN/UV} = 0V$, $V_{IN} = 12V$, LT8060xAFOA/VY+ and LT8060xAFOAH/VY+		0.75	30.00	µA
Input Quiescent Current	$I_{Q\ Burst\ Mode}$	Burst Mode, Not Switching		18.6		µA
		Burst Mode, Not Switching, $V_{BIAS} = 5V$		2.2		µA
	$I_{Q\ Pulse\ Skipping}$	Pulse-Skipping Mode (PSM), Not Switching		0.70	0.96	mA
		Pulse-Skipping Mode, Not Switching, $V_{BIAS} = 5V$		2.72		µA
Input Quiescent Current (See *Figure 82*)	I_{Q_FCM}	Normal Switching Mode		11.85		mA
		Normal Switching Mode, $V_{BIAS} = 5V$		9.53		mA
Input UVLO	$V_{IN_UVLO_R}$	V_{IN} Rising	2.70	2.80	2.92	V
	$V_{IN_UVLO_F}$	V_{IN} Falling	2.45	2.55	2.66	V
ENABLE/UVLO (EN/UV)						
EN/UV Threshold	V_{ENR}	$V_{EN/UV}$ Rising	0.95	1.00	1.05	V
	V_{ENF}	$V_{EN/UV}$ Falling		0.895		V
EN/UV Input Leakage Current	I_{EN}	$V_{EN/UV} = 2V$ ($T_A = T_J = +25°C$)	−50		+50	nA
		$V_{EN/UV} = 2V$, LT8060xAFOA/VY+ and LT8060xAFOAH/VY+ Only	-100		+100	nA
$INTV_{CC}$						
$INTV_{CC}$ Output Voltage Range	V_{INTVCC}	$3 \le V_{IN} \le 65V$, $I_{INTVCC} = 1mA$	1.74	1.80	1.86	V
		$V_{IN} = 3V$, $1mA \le I_{INTVCC} \le 20mA$	1.72	1.80	1.87	V

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(V_{IN1} = V_{IN2} = V_{IN} = $V_{EN/UV}$ = 24V, RT = unconnected (f_{SW} = 400kHz), C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = $V_{BIAS/VOUT}$ = 0V, $V_{SYNC/MODE}$ = 0V , $V_{FB/Vos}$ = 0.84V, SW = TR/SS = PG/T_J = unconnected, V_{BST} to V_{SW} = 1.8V, T_J = −40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS/V_{OUT}						
BIAS/V_{OUT} Operating Voltage Range			2.35		25.00	V
BIAS/V_{OUT} Switchover Threshold		V_{BIAS}/V_{OUT} Rising	2.24	2.30	2.35	V
		V_{BIAS}/V_{OUT} Falling	2.135	2.200	2.250	V
BIAS/V_{OUT} Shutdown Current		$V_{EN/UV}$ = 0V, V_{BIAS}/V_{OUT} = 12V		0		µA
BIAS/V_{OUT} Current Consumption		V_{BIAS}/V_{OUT} = 3.3V, f_{SW} = 2MHz		13		mA
POWER MOSFETS						
High-Side NMOS On-Resistance	R_{DS-ONH}	I_{SW} = 1A, Sourcing		105	200	mΩ
Low-Side NMOS On-Resistance	R_{DS-ONL}	I_{SW} = 1A, Sinking		50	105	mΩ
SW Leakage Current	I_{SW_LKG}	V_{IN} = 65V, V_{SW} = 0V, 65V, T_A = T_J = +25°C	-5.5		+5.5	µA
		V_{IN} = 65V, V_{SW} = 0V, 65V, LT8060xAFOA/VY+ and LT8060xAFOAH/VY+ Only	-20		110	µA
TRACKING and SOFT-START (TR/SS)						
Charging Current	I_{SS}	$V_{TR/SS}$ = 0.3V	4.675	5.000	5.300	µA
TR/SS Pull-Down Resistance		Fault Condition, TR/SS = 0.1V		4		Ω
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}		0.792	0.800	0.808	V
BIAS/V_{OUT} Regulation Voltage		$V_{FB/Vos}$ = $INTV_{CC}$	4.95	5.00	5.05	V
		$V_{FB/Vos}$ = Float	3.26	3.30	3.33	V
FB/V_{OS} Input Bias Current	I_{FB}	$V_{FB/Vos}$ = 1V (T_A = T_J = +25°C)	−50		+50	nA
		$V_{FB/Vos}$ = 1V, LT8060xAFOA/VY+ and LT8060xAFOAH/VY+ Only	-100		+100	nA
SYNC/MODE						
MODE Threshold	$V_{SYNC/MODE-Float}$	SYNC/MODE = Float	0.835		0.935	V
	$V_{SYNC/MODE-High}$	SYNC/MODE = $INTV_{CC}$	1.3			V
	$V_{SYNC/MODE\ -Low}$	SYNC/MODE = GND			0.5	V

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(V_{IN1} = V_{IN2} = V_{IN} = $V_{EN/UV}$ = 24V, RT = unconnected (f_{SW} = 400kHz), C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = $V_{BIAS/VOUT}$ = 0V, $V_{SYNC/MODE}$ = 0V , $V_{FB/Vos}$ = 0.84V, SW = TR/SS = PG/T_J = unconnected, V_{BST} to V_{SW} = 1.8V, T_J = −40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Capture Range	f_{SYNC}	f_{SW} set by RT	1.0 x f_{SW}		1.4 x f_{SW}	kHz
Minimum SYNC High Pulse Width			66			ns
Minimum SYNC Low Pulse Width			66			ns
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$	LT80602 and LT80602HV	4.09	4.81	5.53	A
		LT80603 and LT80603HV	4.75	5.50	6.75	A
		LT80603A and LT80603AHV	5.40	6.30	7.20	A
Bottom Power N-channel Metal-Oxide-Semiconductor (NMOS) Current Limit				3.9		A
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	Pulse-Skipping Mode, Burst Mode		+70		mA
		FCM		−2.5		A
I_{LIM} Blanking Before Device Enters HICCUP	$T_{ILIMBLANK}$ [2]			20		ms
HICCUP Timeout [2]				130		ms
RT						
Switching Frequency	f_{SW}	RT = 78.7kΩ	175	205	237	kHz
		RT = Open	370	400	435	kHz
		RT = 24.9kΩ	760	800	864	kHz
		RT = $INTV_{CC}$	1910	2100	2250	kHz
		RT = 5.23kΩ	2780	3050	3325	kHz
Minimum On-Time	t_{ON-MIN}	All Modes, I_{OUT} = 1A		25	40	ns
Minimum Off-Time	$t_{OFF-MIN}$	All Modes, $V_{IN} \geq V_{IN(MIN)}$		160	190	ns
Maximum High-Side Switch On-Time		All Modes		15		µs
Spread Spectrum Modulation Frequency Range		LT8060xAFOA/VY+ and LT8060xAFOAH/VY+ Only		20		%
Spread Spectrum Modulation Frequency		LT8060xAFOA/VY+ and LT8060xAFOAH/VY+ Only		12		kHz

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(V_{IN1} = V_{IN2} = V_{IN} = $V_{EN/UV}$ = 24V, RT = unconnected (f_{SW} = 400kHz), C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = $V_{BIAS/VOUT}$ = 0V, $V_{SYNC/MODE}$ = 0V , $V_{FB/Vos}$ = 0.84V, SW = TR/SS = PG/T_J = unconnected, V_{BST} to V_{SW} = 1.8V, T_J = −40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted. [1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PG/T$_J$ (OUTPUT VOLTAGE MONITOR OPERATION)						
PG/T_J Output Leakage Current	I_{PGLKG}	T_A = T_J = +25°C, $V_{PG/TJ}$ = 5.5V	−50		+50	nA
		$V_{PG/TJ}$ = 5.5V, LT8060xAFOA/VY+ and LT8060xAFOAH/VY+ Only	-100		+1900	nA
PG/T_J Upper Threshold Offset from V_{FB}/V_{OS}	V_{FB-OV}	V_{FB} Rising	8	10	12	%
PG/T_J Lower Threshold Offset from V_{FB}/V_{OS}	V_{FB-UV}	V_{FB} Falling	−11.0	−8.5	−6.5	%
PG/T_J Delay after FB/Vos Reaches 93% Regulation				200		µs
PG/T_J Pull-Down Resistance					60	Ω
PG/T$_J$ (DIE TEMPERATURE MONITOR OPERATION)						
PG/T_J Pin Voltage	V_{T25}	T_A = +25°C; PG/T_J = 20kΩ, Connected to GND	580	595	610	mV
PG/T_J Pin Voltage Variation with Respect to Die Temperature	dV_{TJ}/dT			2		mV/°C
THERMAL SHUTDOWN (TEMP)						
Thermal Shutdown Threshold		Temperature Rising		175		°C
Thermal Shutdown Hysteresis				10		°C

1 Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.
The device is designed for continuous operation up to T_J = 125°C for 95,000 hours and T_J = 150°C for 5,000 hours.

2 See the *Overcurrent Protection (OCP)/Hiccup Mode* section for more details.

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ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN1}, V_{IN2} to GND (LT8060x)	−0.3V to +70V
V_{IN1}, V_{IN2} to GND (LT8060xHV)	−0.3V to +80V
EN/UV to GND	−0.3V to (V_{IN} + 0.3)V
SW to GND (DC)	-0.3V to (V_{IN} + 0.3)V
SW to GND (LT8060x) (AC, less than 10ns transient)	(V_{IN} + 0.3)V to min (V_{IN} + 5, 70)V
SW to GND (LT8060x) (AC, less than 20ns transient)	−3V to -0.3 V
SW to GND (LT8060xHV) (AC, less than 10ns transient)	(V_{IN} + 0.3)V to min (V_{IN} + 5, 80)V
SW to GND (LT8060xHV) (AC, less than 20ns transient)	−3V to -0.3 V
BIAS/V_{OUT} to GND	−14V to +26.5V
BST to SW	−0.3V to +2.2 V
BST to $INTV_{CC}$ (LT8060x)	−0.3V to +70 V
BST to $INTV_{CC}$ (LT8060xHV)	−0.3V to +80V
FB/VOS, TR/SS, $INTV_{CC}$, RT to GND	−0.3V to +2.2V
PG/T_J to GND	−0.3V to +6V
GND1/GND2 to GND	−0.3V to 0.3V
SYNC/MODE to GND	−0.3V to +6V
SW Total RMS current	6A
Output Short-Circuit Duration	Continuous
Operating Temperature Range[1]	−40°C to +150°C
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Soldering, 10s	+300°C
Soldering Temperature (Reflow)	+260°C

[1] Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

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PIN CONFIGURATION

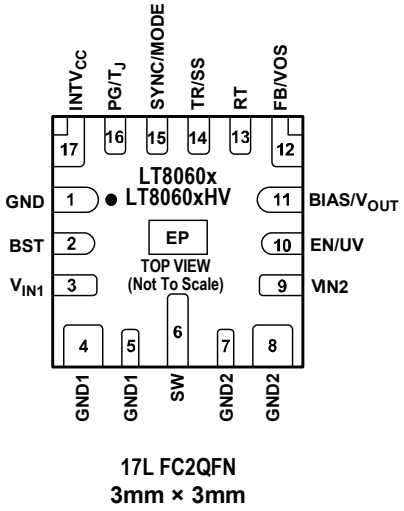


Figure 3. LT8060x and LT8060xHV Pin Configuration

PIN DESCRIPTION

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	GND	LT8060x and LT8060xHV Ground Pin. Connect this pin to the system ground and the ground plane.
2	BST	Boot Strap Capacitor Pin. This pin provides a drive voltage higher than the input voltage to the high-side n-channel metal-oxide semiconductor (NMOS). The boost capacitor between the BST and SW pins should be placed as close as possible to the IC. See the *BST Capacitor Selection* section for more details.
3	V_{IN1}	Power Supply Input Pin. The LT8060x and LT8060xHV require two 0.1µF small-input bypass capacitors. One 0.1µF capacitor should be placed between V_{IN1} (pin 3) and GND1 (pin 4). A second 0.1µF capacitor should be placed between V_{IN2} (pin 9), and GND2 (pin 8). These capacitors must be placed as close as possible to the LT8060x and LT8060xHV. A third larger capacitor of 4.7µF or more should be placed close to the LT8060x and LT8060xHV, with the positive terminal connected to V_{IN1} and V_{IN2}, and the negative terminal connected to ground. See the *Application Information* section for the sample layout.
4, 5	GND1	Power Switch Ground. This pin is the return path of the internal bottom-side power switch. Place the negative terminal of the input capacitor as close to the GND1 pins as possible. Also, be sure to tie GND1 to the ground plane. See the *Application Information* section for the sample layout.
6	SW	Switching Node Pin. Connect SW to the bootstrap capacitor and to the switching side of the inductor. This node should be kept small on the PCB for good performance and low EMI.

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PIN	NAME	DESCRIPTION
7, 8	GND2	Power Switch Ground. This pin is the return path of the internal bottom-side power switch. Also, be sure to tie GND2 to the ground plane. See the *Application Information* section for a sample layout.
9	V_{IN2}	Power Supply Input Pin. The LT8060x and LT8060xHV require two 0.1µF small-input bypass capacitors. One 0.1µF capacitor should be placed between V_{IN1} (pin 3) and GND1 (pin 4). A second 0.1µF capacitor should be placed between V_{IN2} (pin 9) and GND2 (pin 8). These capacitors must be placed as close as possible to the LT8060x and LT8060xHV. A third larger capacitor of 4.7µF or more should be placed close to the LT8060x, and LT8060xHV, with the positive terminal connected to V_{IN1} and V_{IN2}, and the negative terminal connected to ground. See the *Application Information* section for the sample layout.
10	EN/UV	Enable/Undervoltage Lockout Pin. The LT8060x and LT8060xHV are shut down when this pin is low and active when it is high. The enable threshold voltage is 1V rising and 0.9V falling. Tie this pin to V_{IN} if the shutdown feature is not required. To program a V_{IN} threshold below which the LT8060x and LT8060xHV shut down, use an external resistor divider from V_{IN}.
11	BIAS/V_{OUT}	External Bias input for LDO. Connect the BIAS/V_{OUT} pin to the converter output-voltage node for output voltages ranging from 2.35V to 25V for improved efficiency. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin. Connect the BIAS/V_{OUT} pin to GND when this feature is not in use. The BIAS/V_{OUT} pin should be tied to V_{OUT} for programming internal 5V or 3.3V output. See the *INTVcc Regulator* section for more details.
12	FB/V_{OS}	Output Feedback/Fixed Output Voltage Selection Pin. Output is sensed and regulated through this pin, when a resistor divider is connected to this pin from V_{OUT} to GND. This pin can also be used to select the internal V_{OUT} options by either connecting to $INTV_{CC}$ or leaving it floating. Choose maximum R_{FB-TOP} or $R_{FB-BOTTOM}$ such that the maximum effective impedance at FB/V_{OS} is less than 170kΩ.
13	RT	Switching Frequency Programming Input Pin. A resistor is tied between RT and ground to set the switching frequency between 200kHz and 3MHz. Leave the RT pin floating to program the device to 400kHz. Connect the RT pin to $INTV_{CC}$ for programming the device to 2100kHz.
14	TR/SS	Output Tracking and Soft-Start Pin. This pin allows control of the output voltage ramp rate during start-up. A TR/SS voltage below the internal reference voltage of 0.8V forces the LT8060x and LT8060xHV to regulate the feedback node equal to the TR/SS pin voltage. When the TR/SS voltage is above the internal reference voltage of 0.8V, the tracking function is disabled, and the internal reference resumes control of the error amplifier. An internal 5µA pull-up current from INTVcc on this pin allows a capacitor to program the output-voltage slew rate. This pin is pulled to ground with an internal 4Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low-impedance output.
15	SYNC/MODE	Mode Selection Input/ External Clock Synchronization Input Pin. This pin programs four different operating modes:

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PIN	NAME	DESCRIPTION
		▶ Burst Mode. Tie this pin to GND for Burst Mode operation at light loads. This results in ultralow quiescent current. ▶ Pulse-skipping mode. Leave this pin unconnected for pulse-skipping mode. This mode offers full-frequency operation down to low output loads before pulse skipping occurs. ▶ Forced continuous mode (FCM). This mode offers fast transient response and full-frequency operation over a wide load range. Tie this pin to $INTV_{CC}$ or a voltage more than 1.3V for FCM. ▶ Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization, the part operates in forced-continuous mode. See the *Mode Selection and External Clock Synchronization (SYNC/MODE)* section for more details.
16	PG/T_J	Open-Drain Status Output/ Die Temperature Monitor Output Pin. The output voltage status can be monitored by connecting the PG/T_J pin to a power supply through a pull-up resistor. The PG/T_J output is driven low if the feedback node voltage falls below 91.5% of the internal reference voltage (0.8V) or increases above 110% of the internal reference voltage (0.8V). PG/T_J goes high after a delay of 200µs whenever the feedback node voltage reaches within +10%/−8.5% of the internal reference voltage (0.8V). The PG/T_J pin can also be used to monitor the die temperature of the device by connecting a 20kΩ resistor from the PG/T_J pin to GND. See the *Output Power Good and Die Temperature Monitor* section for more details. During fault conditions like thermal shutdown, V_{IN} UVLO, and V_{CC} UVLO, this pin is pulled low, and die temperature monitoring is not supported. The die temperature monitoring is also not supported during low I_Q Burst Mode.
17	$INTV_{CC}$	1.8V Linear Regulator Output Pin. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to GND with at least a 2.2µF low ESR ceramic capacitor placed close to the IC. Do not load the $INTV_{CC}$ pin with external circuitry. See the *INTVcc Regulator* section for more details.
—	EP	Exposed Pad. Internally connected to V_{IN1} and V_{IN2} pins. Always connect EP to the V_{IN1} and V_{IN2} pins on the PCB using a plane. Refer to the *LT80603 evaluation board user guide* for a layout example.

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FUNCTIONAL DIAGRAM

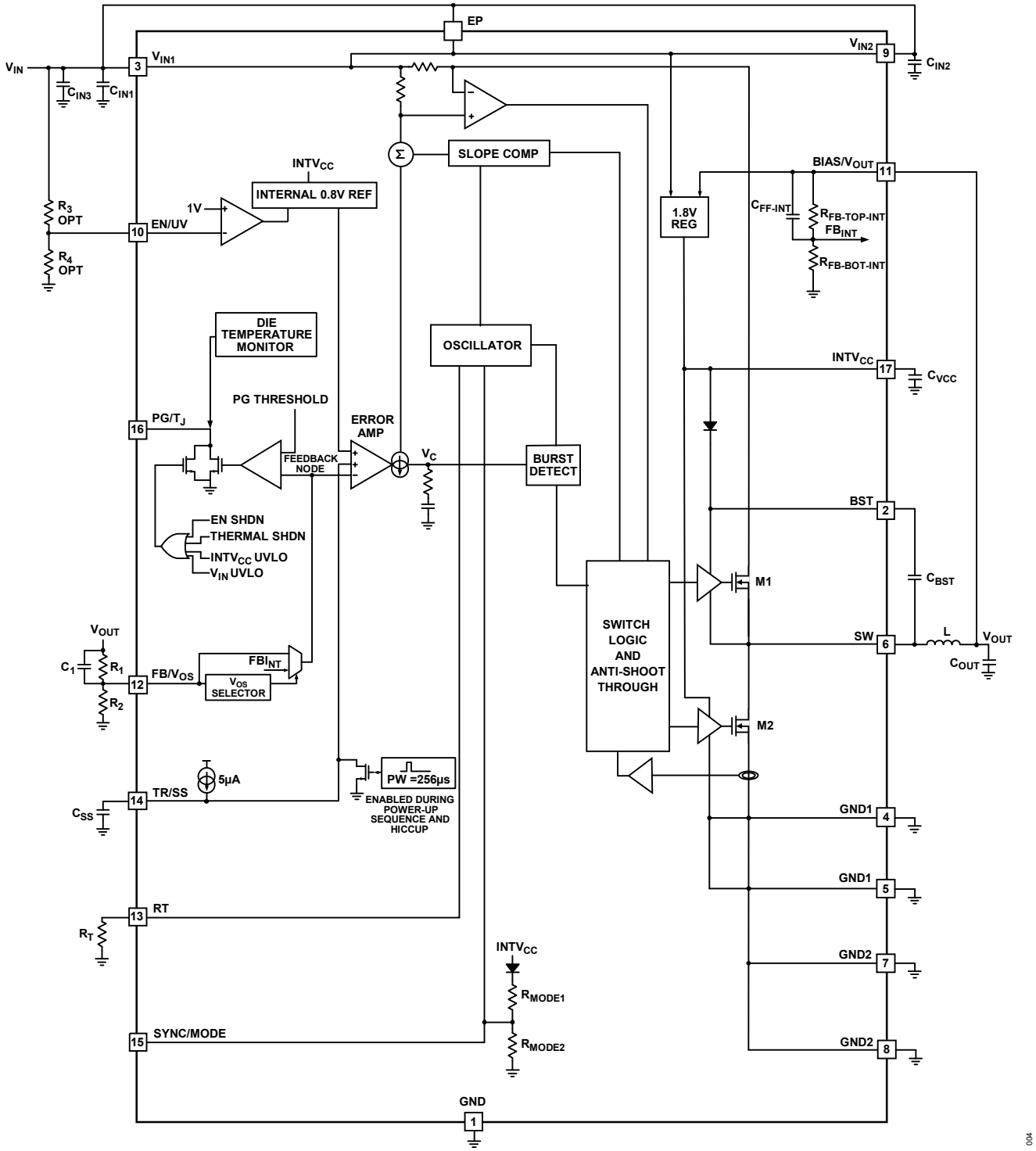


Figure 4. LT8060x and LT8060xHV Functional Diagram

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TYPICAL PERFORMANCE CHARACTERISTICS

(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

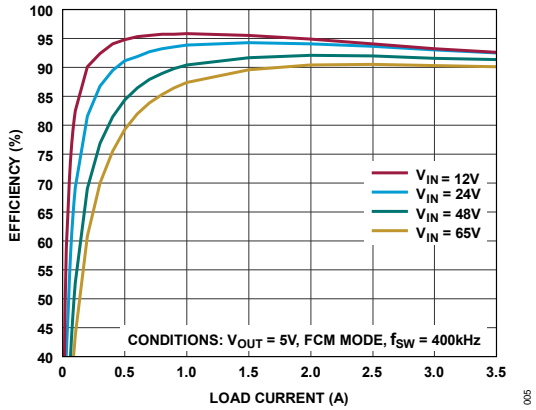


Figure 5. LT80603 Efficiency vs. Load Current (See Figure 82, Typical Application Circuit)

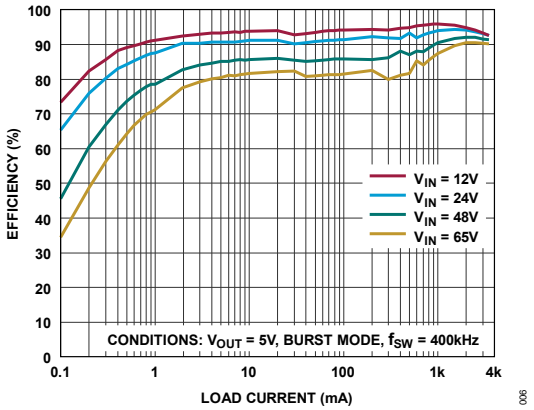


Figure 6. LT80603 Efficiency vs. Load Current (See Figure 82, Typical Application Circuit)

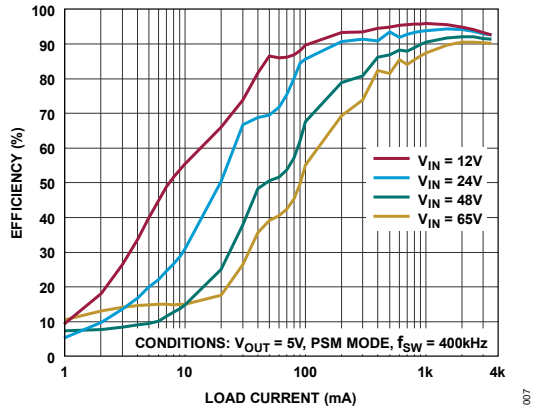


Figure 7. LT80603 Efficiency vs. Load Current (See Figure 82, Typical Application Circuit)

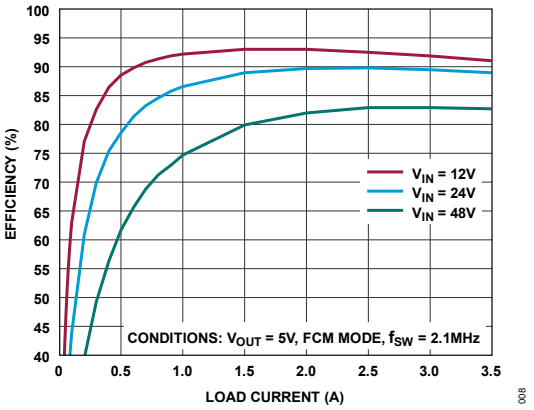


Figure 8. LT80603 Efficiency vs. Load Current (See Figure 81, Typical Application Circuit)

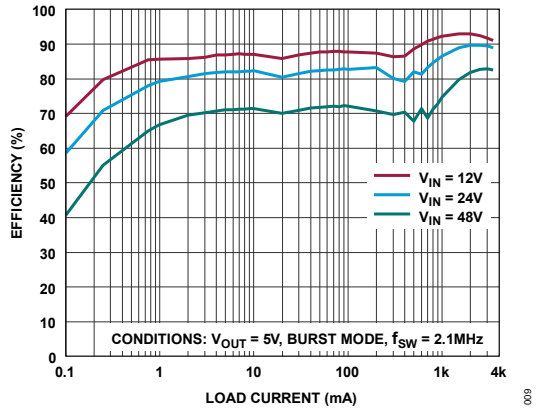


Figure 9. LT80603 Efficiency vs. Load Current (See Figure 81, Typical Application Circuit)

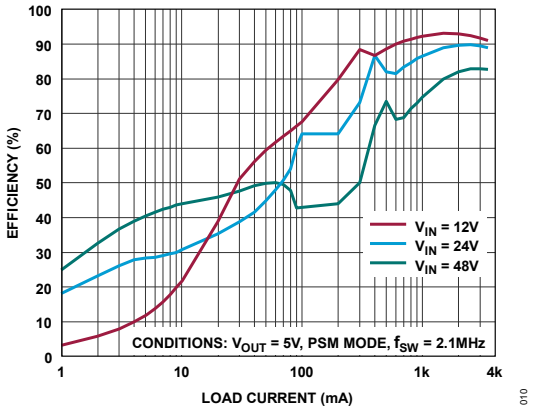


Figure 10. LT80603 Efficiency vs. Load Current (See Figure 81, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

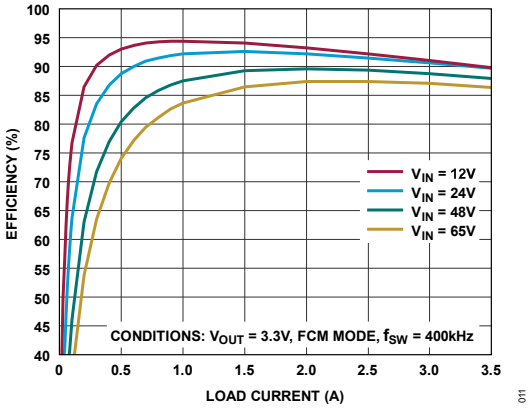


Figure 11. LT80603 Efficiency vs. Load Current (See Figure 86, Typical Application Circuit)

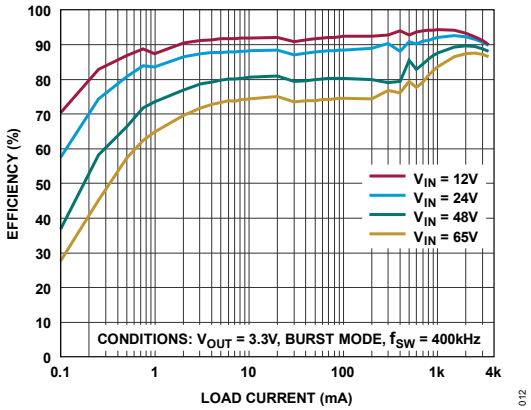


Figure 12. LT80603 Efficiency vs. Load Current (See Figure 86, Typical Application Circuit)

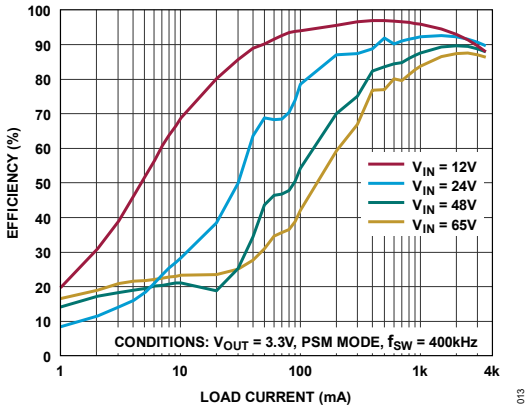


Figure 13. LT80603 Efficiency vs. Load Current (See Figure 86, Typical Application Circuit)

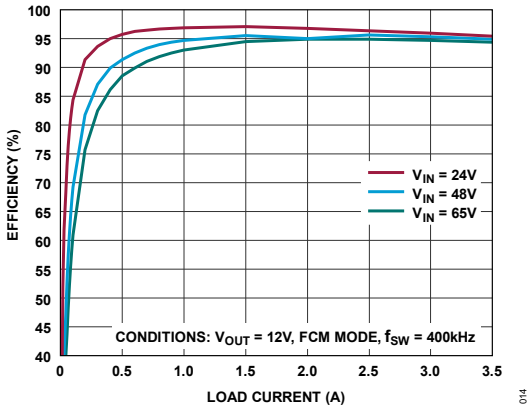


Figure 14. LT80603 Efficiency vs. Load Current (See Figure 84, Typical Application Circuit)

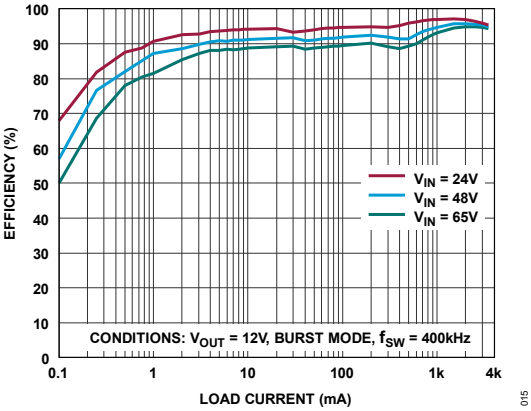


Figure 15. LT80603 Efficiency vs. Load Current (See Figure 84, Typical Application Circuit)

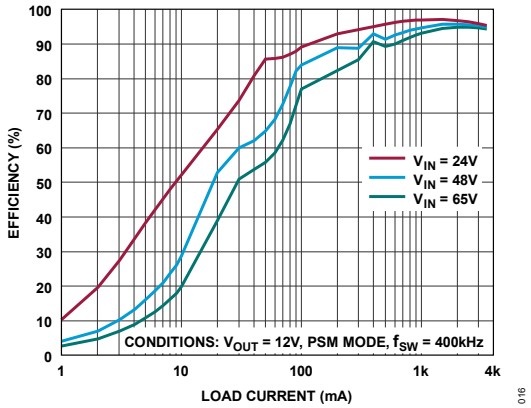


Figure 16. LT80603 Efficiency vs. Load Current (See Figure 84, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

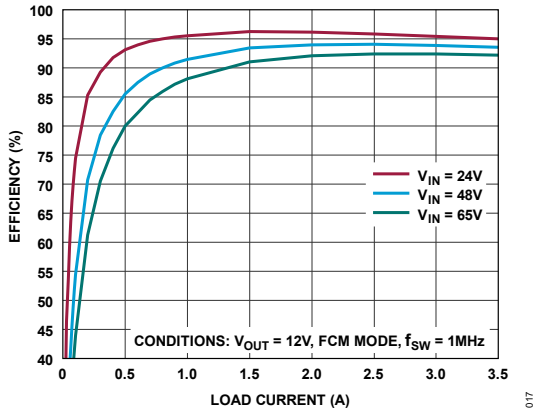


Figure 17. LT80603 Efficiency vs. Load Current

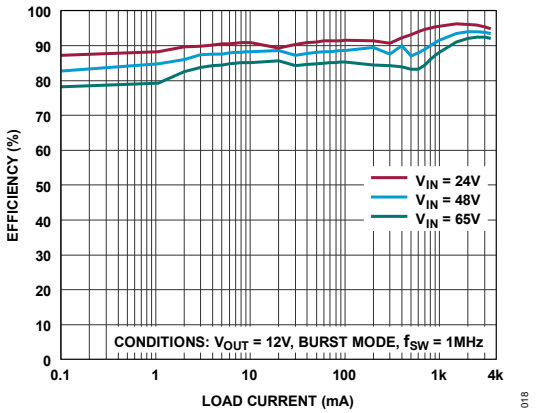


Figure 18. LT80603 Efficiency vs. Load Current

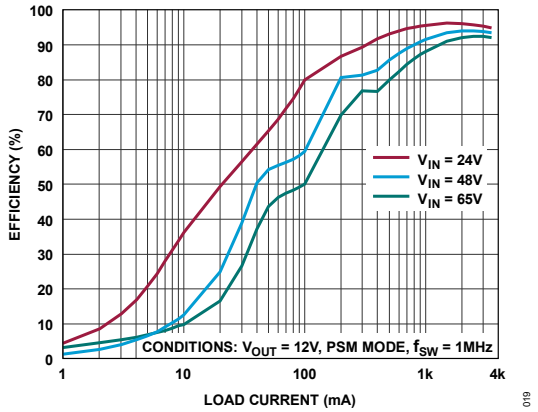


Figure 19. LT80603 Efficiency vs. Load Current

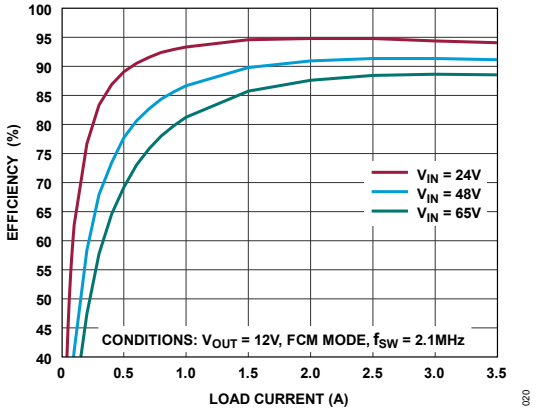


Figure 20. LT80603 Efficiency vs. Load Current (See Figure 83, Typical Application Circuit)

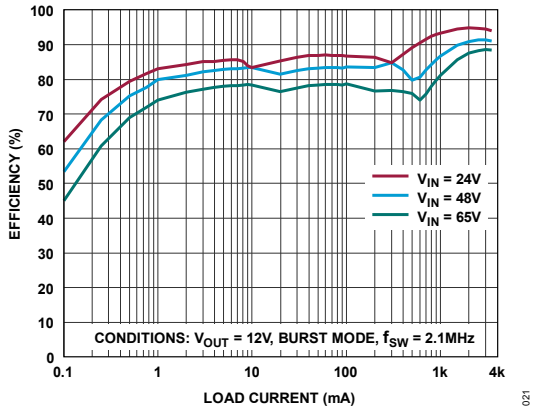


Figure 21. LT80603 Efficiency vs. Load Current (See Figure 83, Typical Application Circuit)

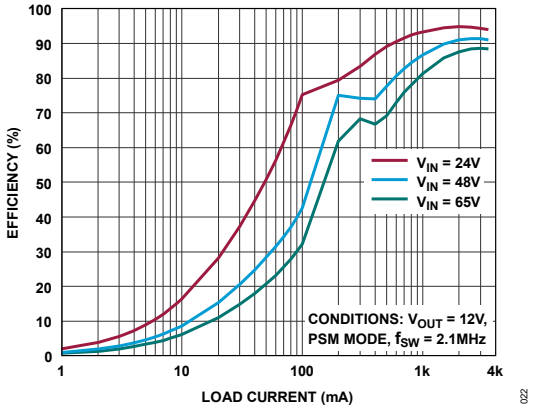


Figure 22. LT80603 Efficiency vs. Load Current (See Figure 83, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

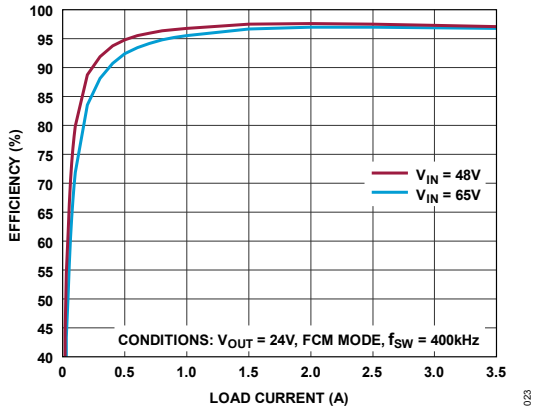


Figure 23. LT80603 Efficiency vs. Load Current (See Figure 88, Typical Application Circuit)

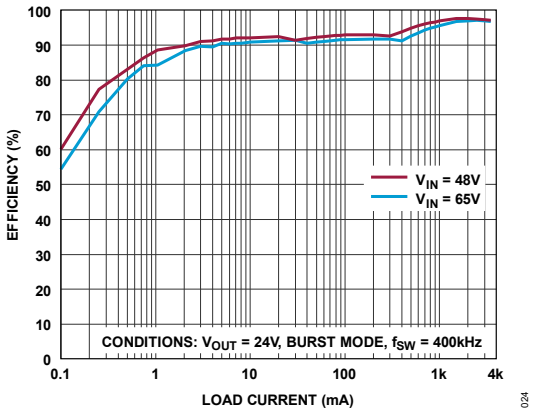


Figure 24. LT80603 Efficiency vs. Load Current (See Figure 88, Typical Application Circuit)

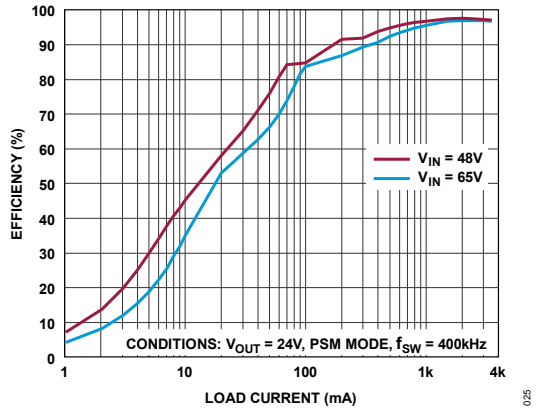


Figure 25. LT80603 Efficiency vs. Load Current (See Figure 88, Typical Application Circuit)

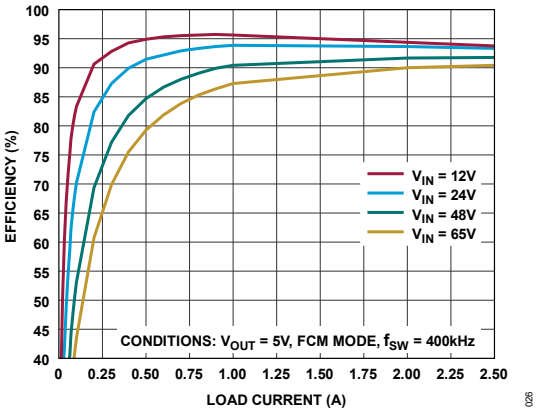


Figure 26. LT80602 Efficiency vs. Load Current

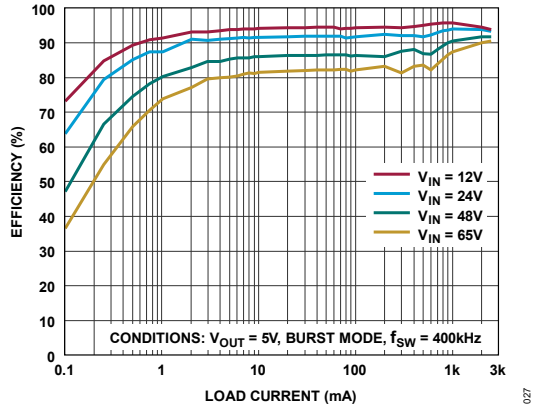


Figure 27. LT80602 Efficiency vs. Load Current

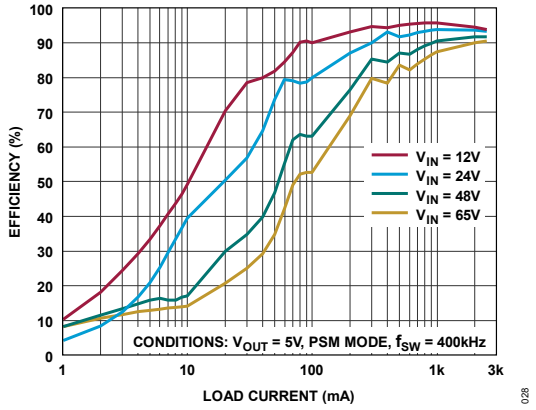


Figure 28. LT80602 Efficiency vs. Load Current

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

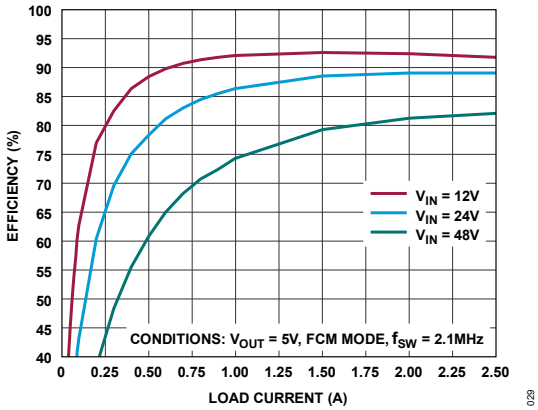


Figure 29. LT80602 Efficiency vs. Load Current

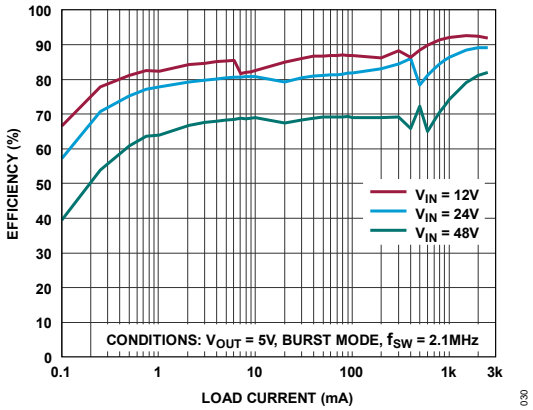


Figure 30. LT80602 Efficiency vs. Load Current

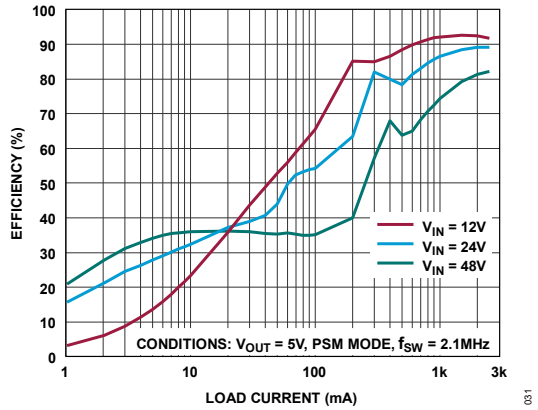


Figure 31. LT80602 Efficiency vs. Load Current

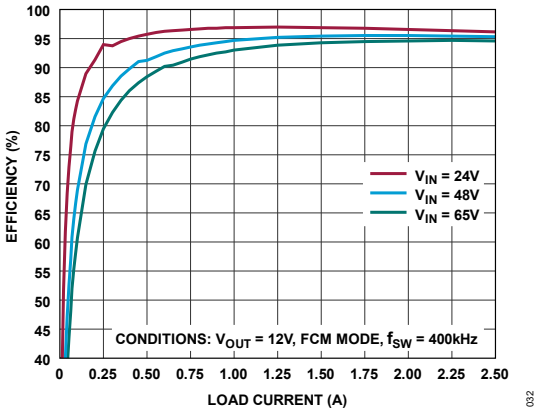


Figure 32. LT80602 Efficiency vs. Load Current

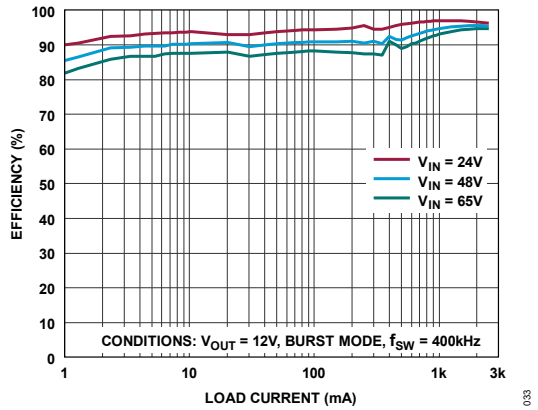


Figure 33. LT80602 Efficiency vs. Load Current

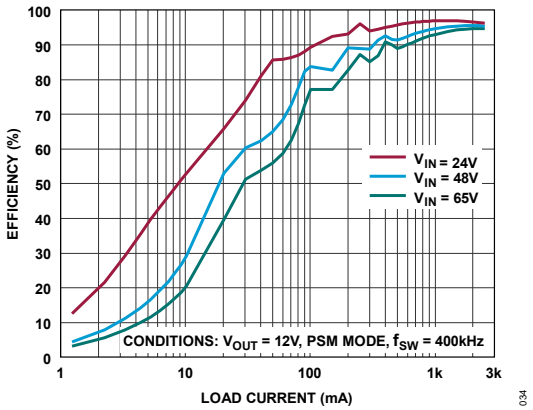


Figure 34. LT80602 Efficiency vs. Load Current

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

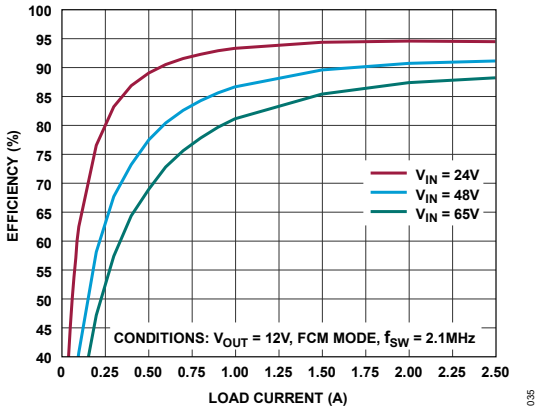


Figure 35. LT80602 Efficiency vs. Load Current

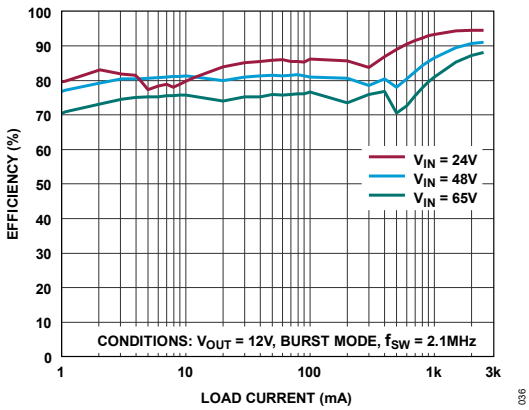


Figure 36. LT80602 Efficiency vs. Load Current

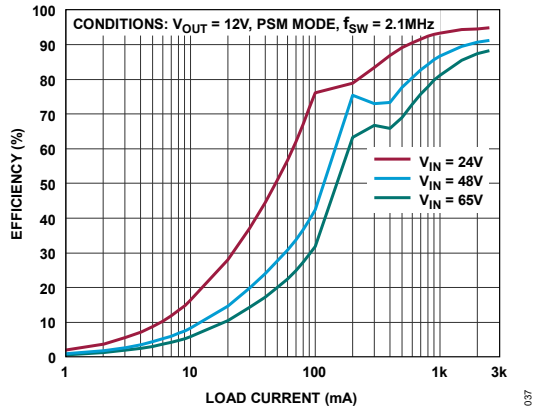


Figure 37. LT80602 Efficiency vs. Load Current

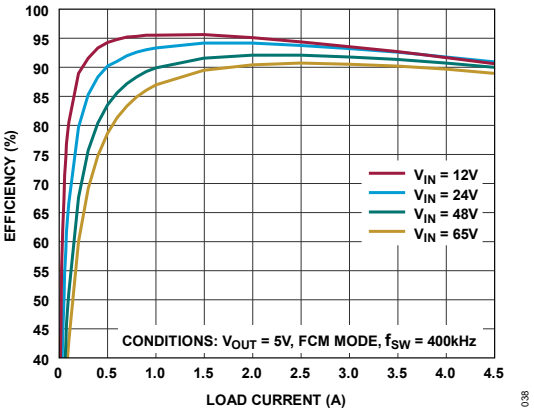


Figure 38. LT80603A Efficiency vs. Load Current

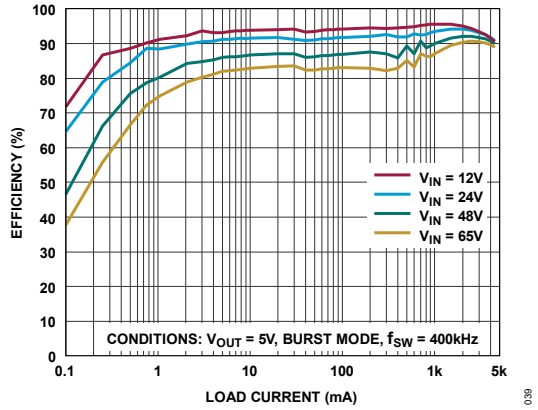


Figure 39. LT80603A Efficiency vs. Load Current

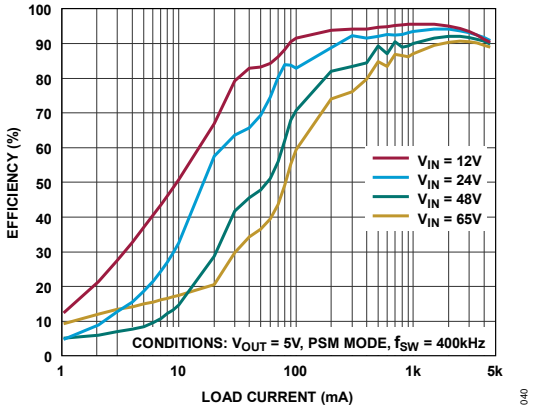


Figure 40. LT80603A Efficiency vs. Load Current

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

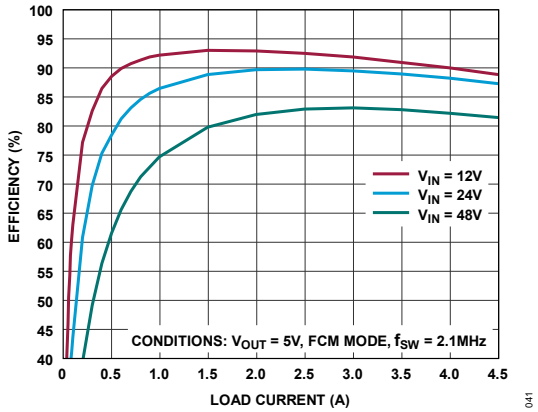


Figure 41. LT80603A Efficiency vs. Load Current

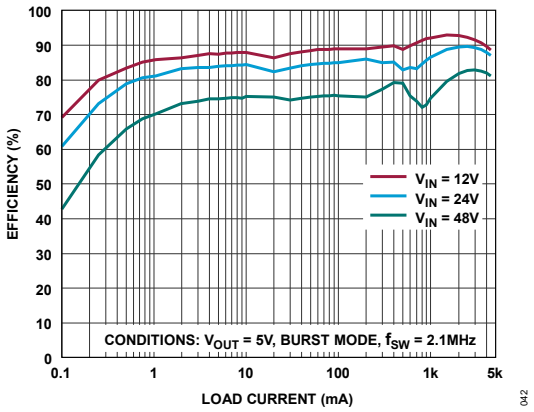


Figure 42. LT80603A Efficiency vs. Load Current

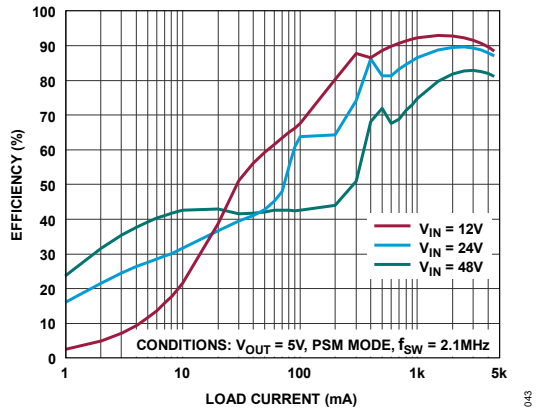


Figure 43. LT80603A Efficiency vs. Load Current

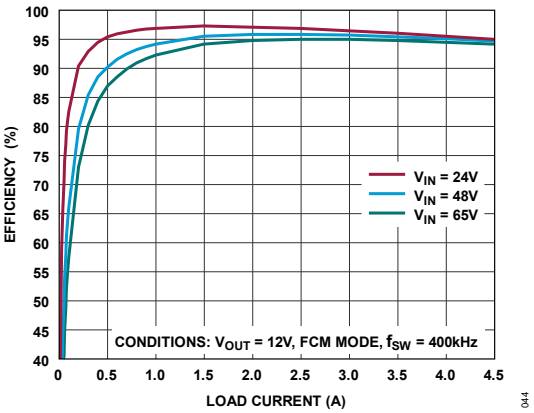


Figure 44. LT80603A Efficiency vs. Load Current

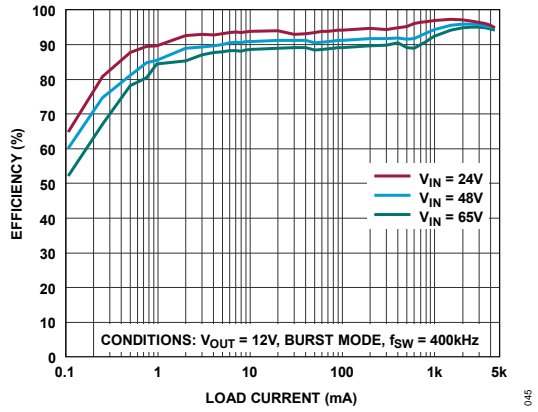


Figure 45. LT80603A Efficiency vs. Load Current

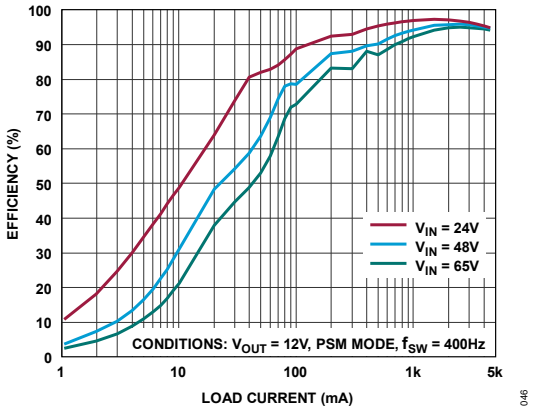


Figure 46. LT80603A Efficiency vs. Load Current

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

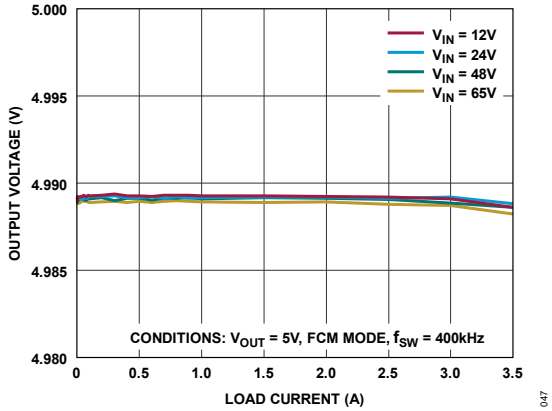


Figure 47. LT80603 Output Voltage vs. Load Current (See Figure 82, Typical Application Circuit)

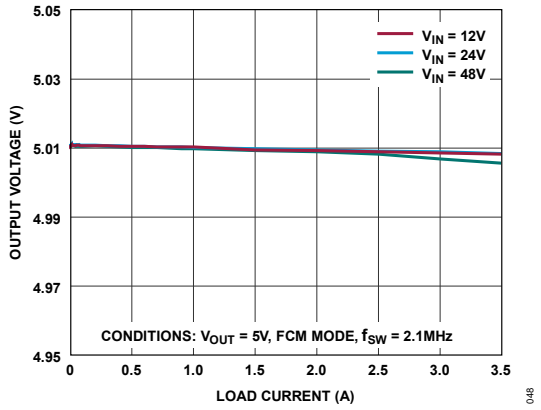


Figure 48. LT80603 Output Voltage vs. Load Current (See Figure 81, Typical Application Circuit)

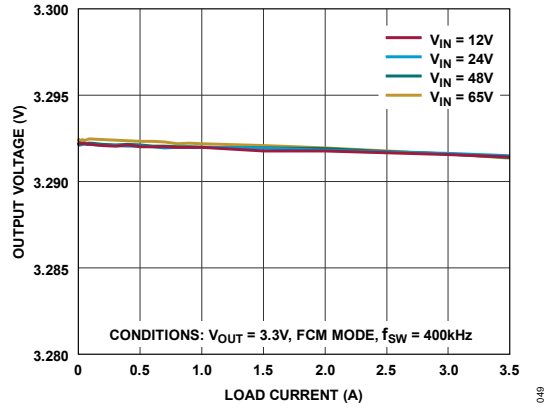


Figure 49. LT80603 Output Voltage vs. Load Current (See Figure 85, Typical Application Circuit)

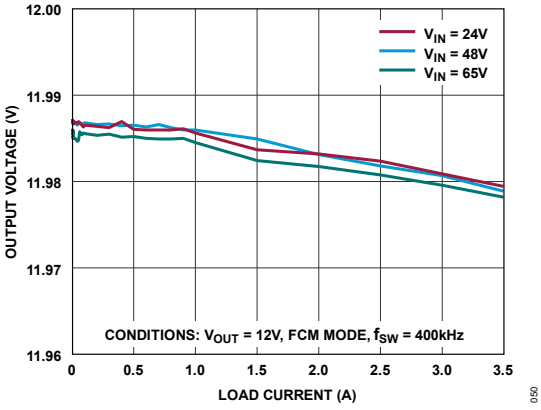


Figure 50. LT80603 Output Voltage vs. Load Current (See Figure 84, Typical Application Circuit)

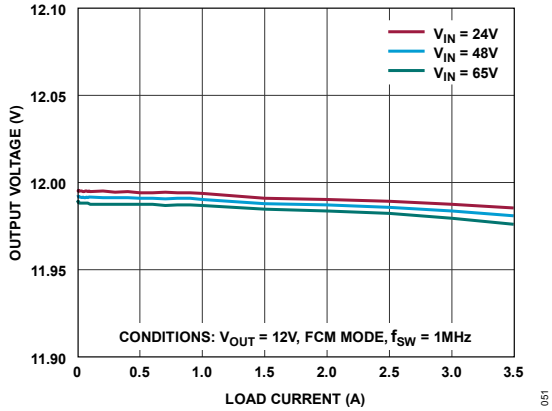


Figure 51. LT80603 Output Voltage vs. Load Current

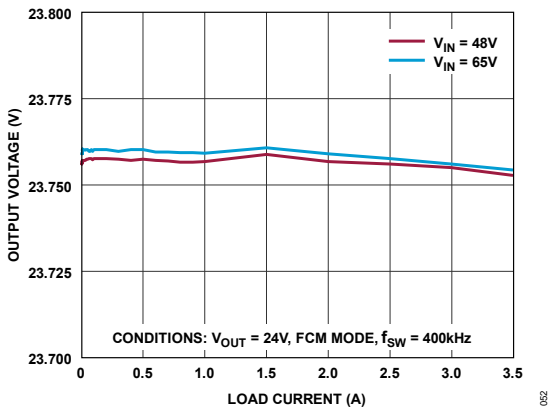


Figure 52. LT80603 Output Voltage vs. Load Current (Figure 88, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

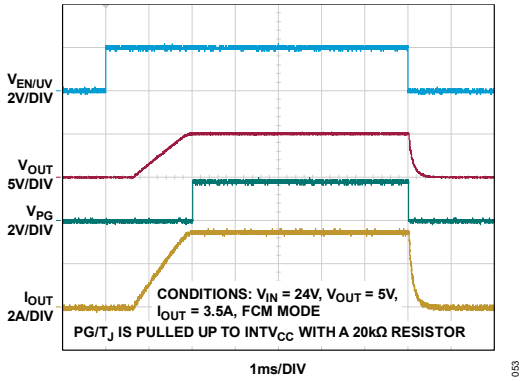


Figure 53. LT80603 Start-up/Shutdown Through EN/UV (See Figure 82, Typical Application Circuit)

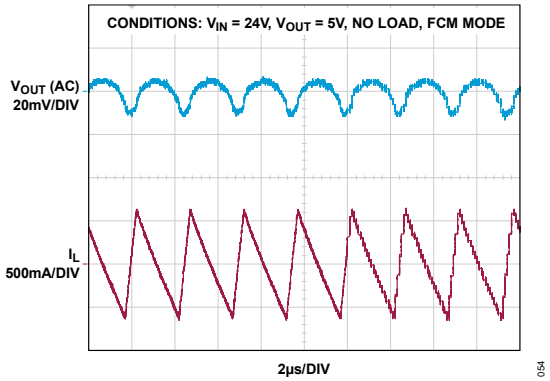


Figure 54. LT80603 Steady-State Switching Waveform (See Figure 82, Typical Application Circuit)

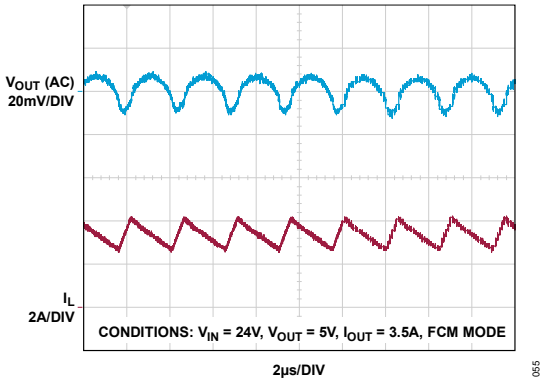


Figure 55. LT80603 Steady-State Switching Waveform (See Figure 82, Typical Application Circuit)

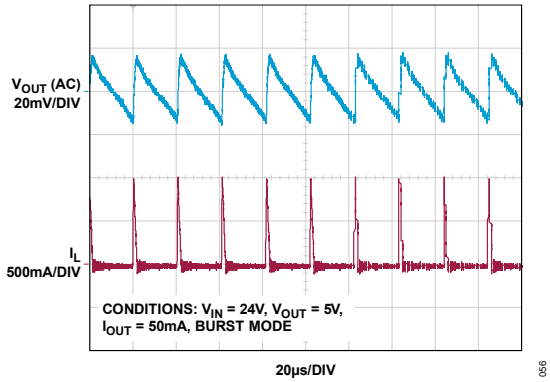


Figure 56. LT80603 Steady-State Switching Waveform (See Figure 82, Typical Application Circuit)

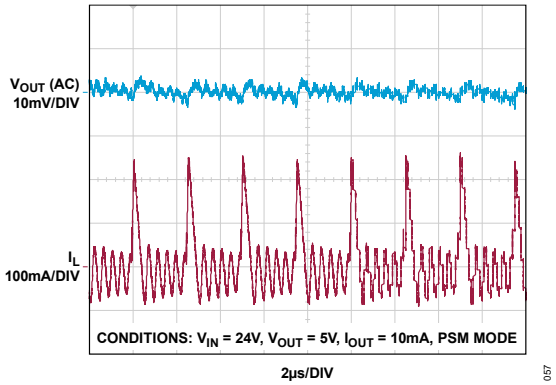


Figure 57. LT80603 Steady-State Switching Waveform (See Figure 82, Typical Application Circuit)

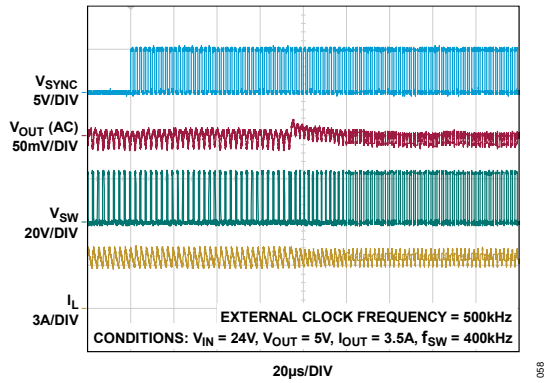


Figure 58. LT80603 External Clock Synchronization (See Figure 82, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

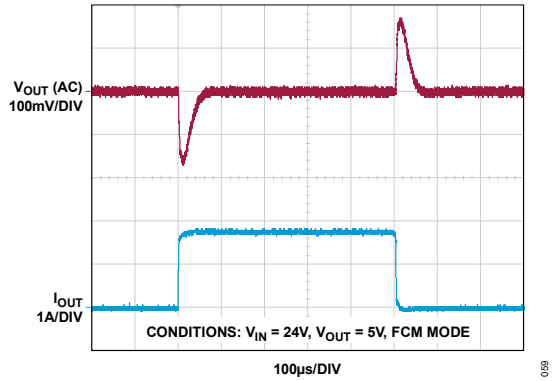


Figure 59. LT80603 Load Current Stepped from 10mA to 1.75A (See Figure 82, Typical Application Circuit)

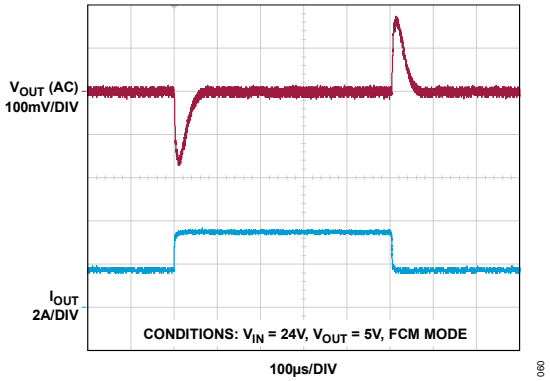


Figure 60. LT80603 Load Current Stepped from 1.75A to 3.5A (See Figure 82, Typical Application Circuit)

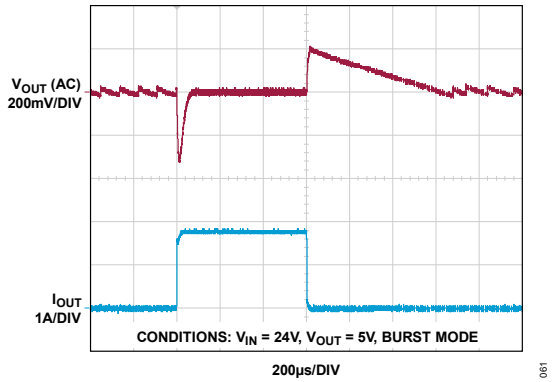


Figure 61. LT80603 Load Current Stepped from 10mA to 1.75A (See Figure 82, Typical Application Circuit)

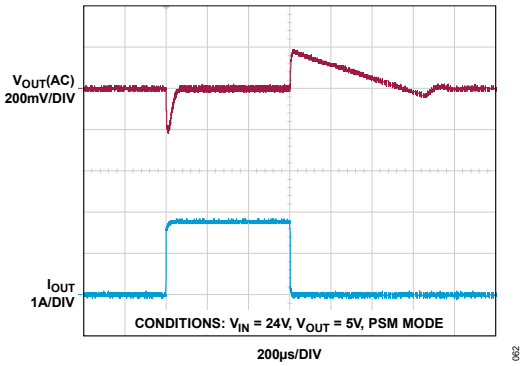


Figure 62. LT80603 Load Current Stepped from 10mA to 1.75A (See Figure 82, Typical Application Circuit)

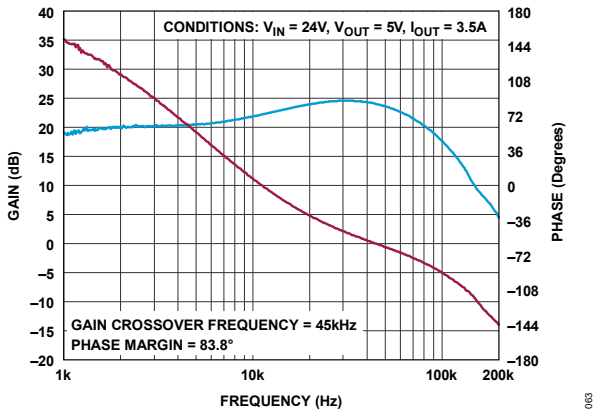


Figure 63. LT80603 Gain/Phase vs. Frequency (See Figure 82, Typical Application Circuit)

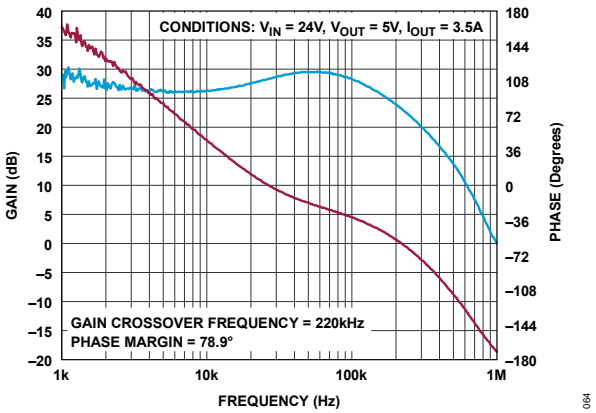


Figure 64. LT80603 Gain/Phase vs. Frequency (See Figure 81, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

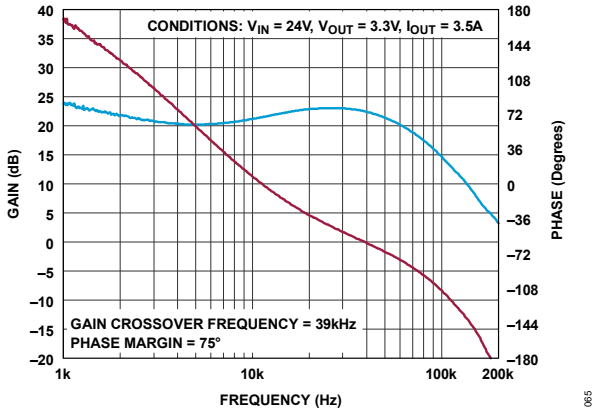


Figure 65. LT80603 Gain/Phase vs. Frequency (Figure 86 Circuit)

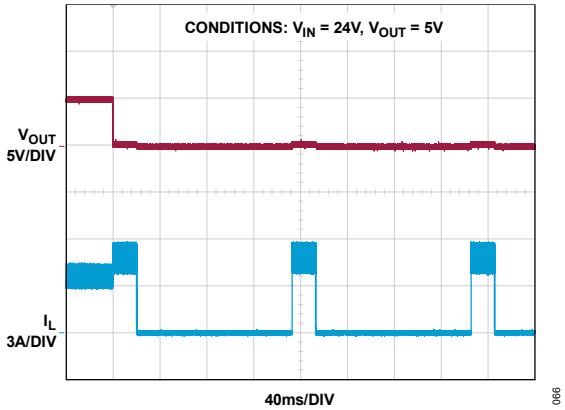


Figure 66. LT80603 Output Short (Figure 82 Circuit)

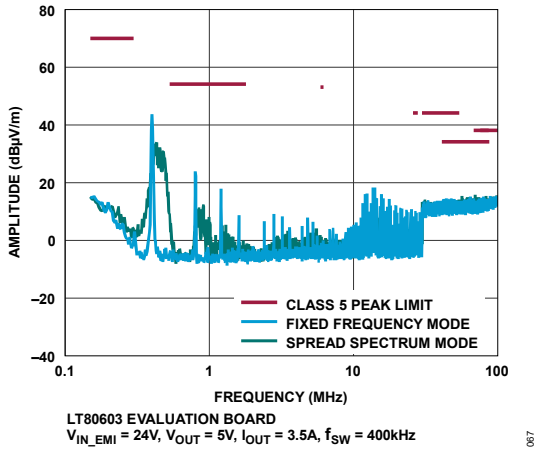


Figure 67. LT80603 CISPR 25 Conducted Emission Test with Class 5 Peak Limits (See Figure 89, Typical Application Circuit)

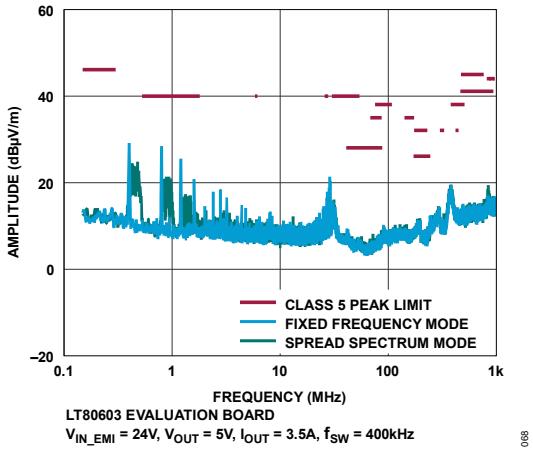


Figure 68.LT80603 CISPR 25 Radiated Emission Test with Class 5 Peak Limits (See Figure 89, Typical Application Circuit)

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(V_{IN} = $V_{EN/UV}$ = 24V, C_{INTVCC} = 2.2µF, V_{GND} = V_{GND1} = V_{GND2} = 0V, V_{BIAS}/V_{OUT} = V_{OUT}, C_{SS} = 8.2nF, T_A = +25°C, unless otherwise noted.)

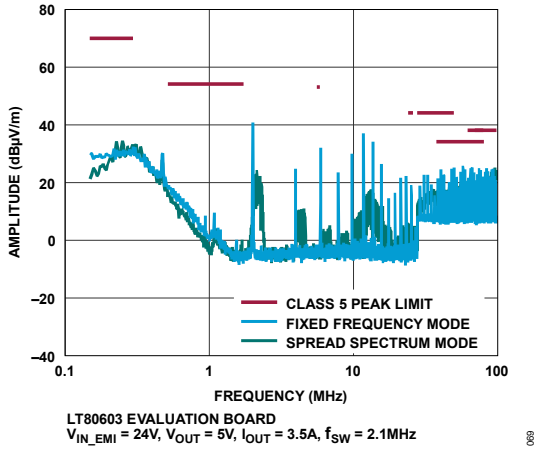


Figure 69. LT80603 CISPR 25 Conducted Emission Test with Class 5 Peak Limits (See Figure 90, Typical Application Circuit)

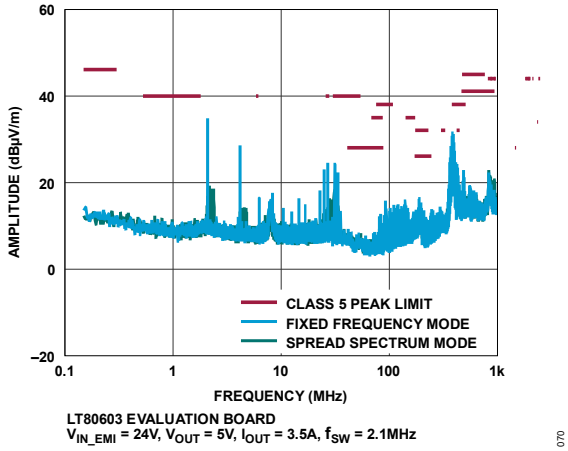


Figure 70. LT80603 CISPR 25 Radiated Emission Test with Class 5 Peak Limits (See Figure 90, Typical Application Circuit)

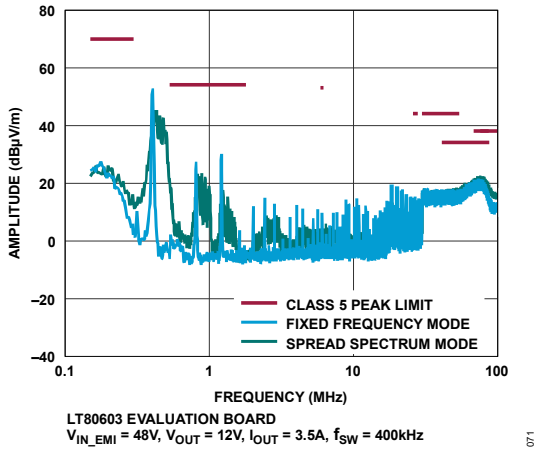


Figure 71.LT80603 CISPR 25 Conducted Emission Test with Class 5 Peak Limits (Figure 91 Circuit)

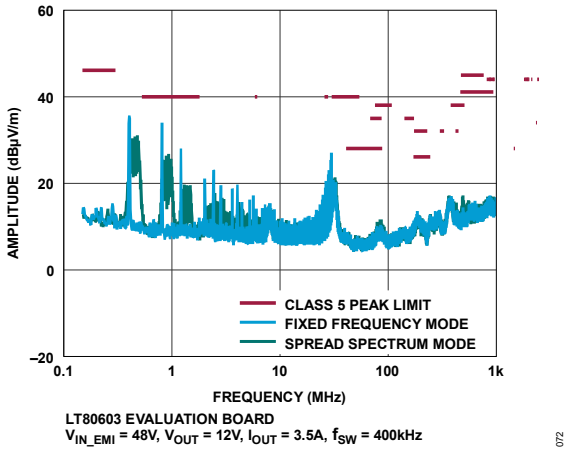


Figure 72. LT80603 CISPR 25 Radiated Emission Test with Class 5 Peak Limits (Figure 91 Circuit)

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OPERATION

The LT8060x and LT8060xHV are monolithic, constant-frequency, current-mode, step-down DC/DC converters. The LT80602 and LT80602HV support up to 2.5A continuous current, the LT80603 and LT80603HV support up to 3.5A, and the LT80603A and LT80603AHV support up to 4.5A continuous current. An oscillator, whose frequency is set by a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. The current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal V_C node. The error amplifier servos the V_C node by comparing the feedback node voltage with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback node voltage relative to the reference, leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins, or in Burst Mode and pulse-skipping mode, the inductor current falls to zero. If overload conditions result in the top switch turning OFF by a peak current limit event, 4.81A (typ) for LT80602 and LT80602HV, 5.5A (typ) for LT80603 and LT80603HV and 6.3A for LT80603A and LT80603AHV, the synchronous low-side power switch turns ON and remains ON, till the current through the synchronous low-side switch current returns to a safe level (3.9A). If the current returns to a safe level (3.9A) within the same clock cycle, then the low-side switch remains ON for the remainder of the clock cycle.

If the EN/UV pin is below the true shutdown voltage (0.45V), the LT8060x and LT8060xHV are shut down and draw 0.75µA from the input. When the EN/UV pin is above 1V, the switching regulator becomes active.

To optimize efficiency at light loads, the LT8060x and LT8060xHV operate in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current consumed by the device. In a typical application, 8µA is consumed from the input supply when regulating with no load. The SYNC/MODE pin is connected to GND to program Burst Mode operation and should be left unconnected to program pulse-skipping mode. For forced continuous mode (FCM), the SYNC/MODE pin should be tied to $INTV_{CC}$ or a voltage greater than 1.3V. If a clock is applied to the SYNC/MODE pin, the device synchronizes to an external clock frequency and operates in forced continuous mode.

While in pulse-skipping mode, the oscillator operates continuously, and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output, and the quiescent current is several hundred µA. The LT8060x and LT8060xHV can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. In FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed. The LT8060x/LT8060xHV can sink current from the output and return this charge to the input in this mode, thereby improving load-step transient response.

To improve EMI performance, LT8060x and LT8060xHV offer spread spectrum mode. This feature varies the clock with a triangular frequency modulation depth of +20%. For example, if the LT8060x and LT8060xHV's frequencies are programmed to switch at 2MHz, spread spectrum mode modulates the oscillator between 2MHz and 2.4MHz. Spread spectrum modulation is available when the device is configured in Pulse-Skipping Mode, FCM, or Burst Mode.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the $BIAS/V_{OUT}$ pin when biased at 2.35V or above. Otherwise, the internal circuitry draws current from V_{IN}. The $BIAS/V_{OUT}$ pin should be connected to V_{OUT} if the LT8060x and LT8060xHV's outputs are programmed at 2.35V to 25V.

Comparators monitoring the FB node voltage pull the PG/T_J pin low if the output voltage varies more than +10% or −8% (typical) from the set point, or if a fault condition is present. In addition, the device features a die temperature monitor to directly measure the silicon die temperature, instead of relying on theoretical estimation, thus enabling robust, reliable power supply design.

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APPLICATION INFORMATION

Low EMI PCB Layout

The LT8060x and LT8060xHV are specifically designed to minimize EMI emissions and maximize efficiency when switching at high frequencies. For optimal performance, the LT8060x and LT8060xHV require the use of multiple V_{IN} bypass capacitors.

Two small 0.1µF capacitors should be placed as close as possible to the LT8060x and LT8060xHV. One capacitor should be tied to V_{IN1} (pin 3) and GND1 (pin 4). A second capacitor should be tied to V_{IN2} (pin 9) and GND2 (pin 8). A third capacitor with a larger value, 4.7µF or higher, should be placed near V_{IN1} or V_{IN2}.

See *Figure 73* for a recommended PCB layout. For more details and PCB design files, refer to the LT80603 evaluation board user guide. Note that large, switched currents flow in the LT80603 V_{IN1}, V_{IN2}, GND1, and GND2 pins, and the input capacitors (C_{IN1}, C_{IN2}). The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN1}, $V_{IN2,}$ and GND1 or GND2 pins. Capacitors with a small case size, such as 0603, are optimal due to the lowest parasitic inductance.

The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible.

Finally, keep the FB/V_{OS} and RT nodes small so that the ground traces shield them from the SW and BST nodes. A bypass capacitor for the $INTV_{CC}$ pin should also be placed close to the pin to reduce the effects of trace impedance. To keep thermal resistance low, extend the ground plane from GND1 and GND2 as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.

Mode Selection and External Clock Synchronization (SYNC/MODE)

The LT8060x and LT8060xHV support forced continuous mode (FCM), Burst (ultralow quiescent current) Mode, and pulse skipping modes of operation. The device enters the programmed mode of operation based on the setting of the MODE/SYNC pin. If the MODE/SYNC pin is high (> $V_{SYNC/MODE-High}$), the device operates in a constant-frequency FCM mode at all loads. If the MODE/SYNC pin is low (< $V_{SYNC/MODE-Low}$), the device operates in Burst Mode at light loads. If the MODE/SYNC pin is left open, the device operates in pulse skip mode at light loads. The device supports on-the-fly mode change. When there is a state transition on the MODE/SYNC pin, the device waits for 60µs and transitions into the mode based on the MODE/SYNC pin voltage at the end of the 60µs period. During sleep mode, transition can be detected only at the next $I_{PK-BURST}$ pulse.

The MODE/SYNC pin can also be used to synchronize the internal oscillator of the device to an external clock in all three modes of operation. To synchronize the LT8060x and LT8060xHV oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys below 0.5V and peaks above 1.3V (up to 5V). The external clock frequency must be between 1.0 × f_{SW} and 1.4 × f_{SW}, where f_{SW} is the programmed switching frequency. When an external clock is applied to the MODE/SYNC pin, if eight or more external clock rising edges are detected in 60µs, the device operates in FCM mode and the internal oscillator frequency changes to the external clock frequency at the end of the 60µs period. When the external clock is removed, the device continues to operate in FCM mode for 60µs and enters a mode based on the SYNC/MODE pin status. The external clock logic high and low pulse widths should be more than 66ns.

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Achieving Ultralow Quiescent Current (Burst Mode Operation)

To enhance efficiency at light loads, the LT8060x and LT8060xHV operate in low-ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing input quiescent current and output voltage ripple. In Burst Mode operation, the LT8060x and LT8060xHV deliver single small pulses of current to the output capacitor, followed by sleep periods in which the output power is supplied by the output capacitor.

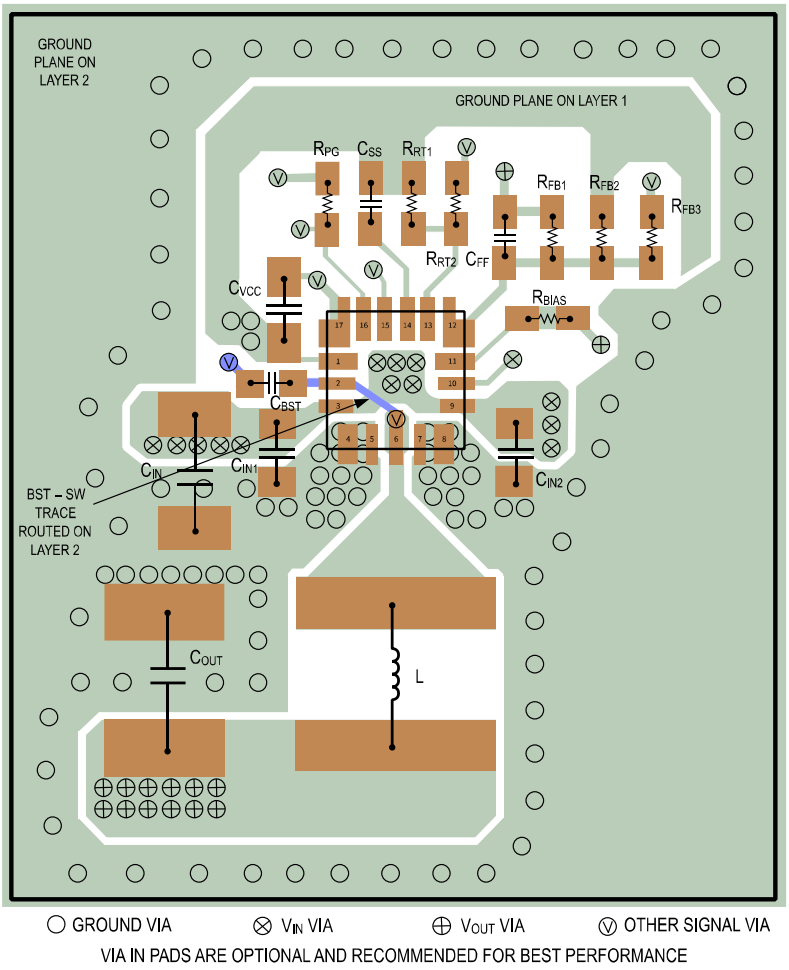


Figure 73. Recommended PCB Layout for the LT80603

In a typical application circuit, the quiescent current can be reduced by connecting the V_{OUT} to the BIAS/V_{OUT} pin. When in sleep mode, the LT8060x and LT8060xHV draw 18.6µA (typ) from the BIAS/V_{OUT} pin and 2.2µA (typ) from the input supply at V_{IN} = 24V. The total current consumed from the input, when the converter is not switching, is approximately given by the equation:

$$I_{QB} = 18.6\mu A \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{\eta}\right) + 2.2\mu A + I_{FB} \quad (1)$$

Input referred FB resistor divider current (I_{FB}) can be calculated using the formulations in the *FB Resistor Network* section. For a 5V application with V_{IN} = 24V, $I_{FB} \cong 1\mu A$, and light load efficiency (η) = 85%, the quiescent current is close to 8µA.

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As the output load decreases, the frequency of single current pulses decreases (see *Figure 74*) and the percentage of time the LT8060x and LT8060xHV are in sleep mode increases, maintaining higher efficiency even at lighter loads. In sleep mode, most of the internal blocks are turned off to minimize quiescent current. The current in the feedback resistor divider must be minimized to improve the quiescent current performance.

To achieve higher light load efficiency, more energy must be delivered to each Burst Mode pulse, such that the LT8060x and LT8060xHV can stay in sleep mode longer between each pulse. This can be achieved using a larger-value inductor and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value is typically used for a high-switching-frequency application, if high-light-load-efficiency is desired, a higher inductor value should be chosen. See the curve in *Typical Performance Characteristics*.

In Burst Mode operation, the current limit of the top switch is approximately 0.85A, 1A, and 1.15A for LT80602, LT80603, and LT80603A, respectively, resulting in low output voltage ripple. Increasing the output capacitance decreases the output ripple proportionally. As the load ramps upward from zero, the switching frequency increases, but only up to the switching frequency programmed by the resistor at the RT pin, as shown in *Figure 74*.

The output load at which the LT8060x and LT8060xHV reach the programmed frequency varies based on input voltage, output voltage, and inductor selection. To select low-ripple Burst Mode operation, connect the SYNC/MODE pin to GND.

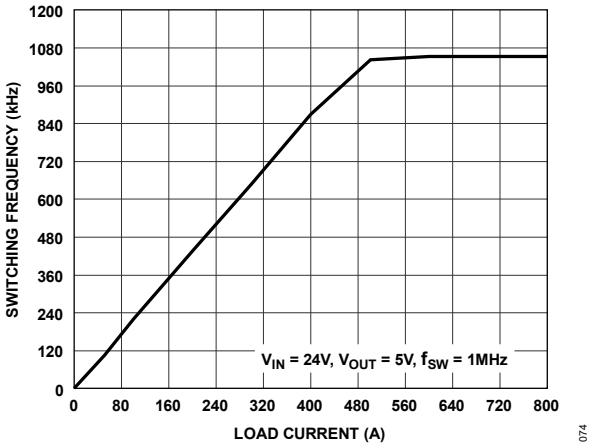


Figure 74. Output Current vs. Switching Frequency

Pulse-Skipping Mode

The pulse-skipping mode of operation features a constant frequency operation down to light loads. In pulse-skipping mode, inductor current is not allowed to go negative. In this mode, much of the internal circuitry is always awake, increasing the quiescent current to several hundred µA. Pulse skip operation offers efficiency performance that lies between the FCM and Burst Modes. The output voltage ripple in pulse skip mode is lower compared to Burst Mode and comparable with FCM mode. To program pulse-skipping mode, leave the SYNC/MODE pin unconnected.

Forced Continuous Mode

In FCM mode, the inductor current is allowed to go negative. FCM operation provides a constant-frequency operation across all loads and is useful in applications sensitive to switching frequency. However, the FCM mode of operation gives lower efficiency at light loads compared to the Burst and pulse-skipping modes of operation. The LT8060x and LT8060xHV can sink current from the output and return this charge to the input in this mode, thus improving load-step transient response (see *Figure 75*). To program FCM, connect the SYNC/MODE pin to $INTV_{CC}$ or a voltage greater than 1.3V. FCM is disabled during soft-start, and the converter operates in pulse-skipping mode. This ensures the converter starts monotonically.

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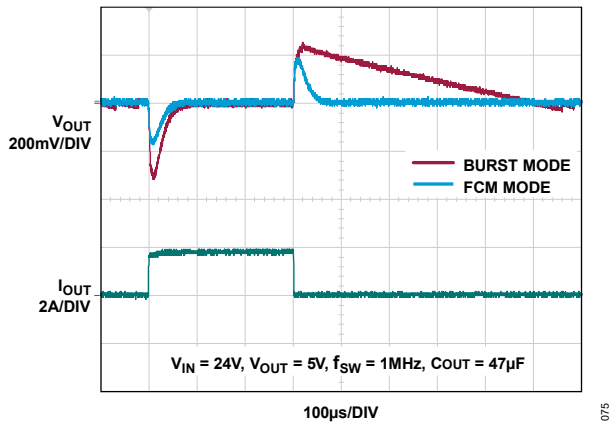


Figure 75. Load-Step Transient Performance with Burst and FCM Modes

Spread Spectrum Mode

The LT8060x and LT8060xHV feature spread spectrum operation to further reduce EMI emissions. In spread spectrum mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by R_T to approximately 20% higher than that value. The modulation frequency is approximately 12kHz. For example, when the LT80603 is programmed to 2MHz, the frequency varies from 2MHz to 2.4MHz at a 12kHz rate. Spread spectrum operation is unavailable when the device is synchronized to an external clock.

Setting the Switching Frequency

The LT8060x and LT8060xHV use a constant-frequency pulse width modulation (PWM) architecture that can be programmed to switch from 200kHz to 3MHz using a resistor tied from the RT pin to ground. *Table 4* shows the necessary R_T values for desired switching frequencies.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T \cong \frac{23.5 - (2.4 \times f_{SW})}{0.09 + f_{SW}} \quad (2)$$

where, R_T is in kΩ and f_{SW} is in MHz. Leaving the RT pin open forces the device to operate at a default switching frequency of 400kHz. Connecting the RT pin to $INTV_{CC}$ forces the device to operate at 2100kHz. See *Table 4* for R_T resistor values for a few common switching frequencies.

Table 4. Switching Frequency vs. R_T Resistor

SWITCHING FREQUENCY (kHz)	R_T RESISTOR (kΩ)
200	78.7
400	OPEN or 46.4
1000	19.1
2100	$INTV_{CC}$ or 8.66
3000	5.23

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Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values can be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated by Equation 3.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)} \times \left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (3)$$

where, V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.15V, respectively, at maximum load), and $t_{ON(MIN)}$ is the minimum top switch on-time (see the *Specifications* section). Equation 3 shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operations, V_{IN} may reach 65V regardless of the R_T value. However, the LT8060x and LT8060xHV reduce switching frequency as necessary to maintain control of the inductor current, ensuring safe operation.

The LT8060x and LT8060xHV are capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode, the LT8060x and LT8060xHV skip switch cycles, resulting in a lower switching frequency than programmed by the R_T resistor.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use Equation 4 to set the switching frequency.

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - (f_{SW} \times t_{OFF-MIN})} - V_{SW(BOT)} + V_{SW(TOP)} \quad (4)$$

where, $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.15V, respectively, at maximum load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency increases the minimum input voltage, below which cycles are dropped to achieve a higher duty cycle.

High Duty Operation

The LT8060x and LT8060xHV feature high-duty operation, which enhances the output-to-input voltage ratio. To regulate the output voltage with an input voltage close to the output voltage, the operating switching frequency is reduced by skipping off-time pulses. The high-duty operation extends the high-side switch on time beyond the programmed switching cycle, until the inductor peak current reaches the reference set by the controller or Burst Mode peak current limit ($I_{PEAK-BURST}$). After the high-side switch is turned off, the low-side switch is turned on, and the next switching cycle starts with the rising edge of the clock signal.

In scenarios where the maximum on-time (15µs + up to one programmed t_{SW}) is reached, the high-side switch is turned off for a minimum off-time ($t_{OFF-MIN}$), and the low-side switch is turned on. After the $t_{OFF-MIN}$, the new switching cycle starts.

When the device is synchronized to an external clock with f_{SYNC} frequency, the operating switching frequency is reduced in discrete fractions of the external clock frequency ($f_{SYNC}/2$, $f_{SYNC}/3$, and so on). SW rising edges are synchronized to the external clock.

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Inductor Selection and Maximum Output Current

The LT8060x and LT8060xHV are designed to minimize solution size by allowing the inductor to be selected based on the output load requirements of the application. During overload or short-circuit conditions, the LT8060x and LT8060xHV safely tolerate operation with a saturated inductor with a high-speed peak-current mode architecture.

For LT8060x and LT8060xHV, a good first choice for the inductor value is calculated by Equation 5.

$$L = \left(\frac{V_{OUT}}{f_{SW}}\right) \times K1 \quad (5)$$

where, f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, and L is the inductor value in µH. K1 = 0.75 for LT80602 and LT80602HV, K1 = 0.65 for LT80603 and LT80603HV, K1 = 0.55 for LT80603A and LT80603AHV.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of the inductor ripple current.

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (6)$$

where, ΔI_L is the inductor ripple current, as calculated in Equation 6, and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 3.5A output should use an inductor with an RMS rating of greater than 3.5A and an I_{SAT} of greater than 5.5A. During long-duration overload or short-circuit conditions, the inductor's root mean square (RMS) rating requirement is greater to avoid overheating of the inductor. To maintain high efficiency, the series resistance (DCR) should be less than 15mΩ, and the core material should be intended for high-frequency applications.

The LT8060x and LT8060xHV limit the peak switch current to protect the switches and the system from overload faults. The typical top switch current limit (I_{LIM}) is 5.5A for the LT80603 and LT80603HV, 4.81A for the LT80602 and LT80602HV, 6.3A for the LT80603A and LT80603AHV. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current (Equation 7).

$$I_{OUT(MAX)} = I_{LIM} - \frac{1}{2}\Delta I_L \quad (7)$$

The peak-to-peak ripple current in the inductor can be calculated using Equation 8.

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (8)$$

where, f_{SW} is the switching frequency of the LT8060x and LT8060xHV, and L is the value of the inductor. Therefore, the maximum output current delivered by the LT8060x and LT8060xHV depends on the switch current limit, inductor value, and input and output voltages. The inductor value may need to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger-value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower, and the LT8060x and LT8060xHV may operate with higher ripple current. This allows the use of a physically smaller inductor, or one with a lower direct current resistance (DCR), resulting in higher efficiency. Be aware that low inductance may reduce the maximum load current.

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For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillation (see Equation 9). Refer to the Analog Devices *Application Note 19* for more details.

$$L_{MIN} = \frac{V_{IN}}{K2 \times f_{SW}} \times (2 \times DC - 1) \quad (9)$$

where, DC is the duty cycle, and f_{SW} is the switching frequency. K2 = 1 for LT80602 and LT80602HV, K2 = 1.2 for LT80603 and LT80603HV, K2 = 1.4 for LT80603A and LT80603AHV.

Input Capacitors

The V_{IN} of the LT8060x and LT8060xHV should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors, 0.1µF, each, should be placed close to the device: one at the V_{IN1}/GND1 pins and a second at the V_{IN2}/GND2 pins. These capacitors should be 0402 or 0603 in size. For automotive applications requiring two series input capacitors, two small capacitors (0402 or 0603) may be placed at each side of the LT8060x and LT8060xHV near the V_{IN1}/GND1 and V_{IN2}/GND2 pins.

A third, larger ceramic capacitor of 4.7µF or greater should be placed close to V_{IN1} or V_{IN2}. See the *Low EMI PCB Layout* section for more details. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations.

Note that a larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low-performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the LT8060x and LT8060xHV circuits are plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8060x and LT8060xHV's voltage rating. Refer to the Analog Devices *Application Note 88* for more details.

In applications where the source is located far from the device input, an appropriate electrolytic capacitor should be added in parallel with the ceramic capacitor to provide the necessary damping to prevent potential oscillations caused by the inductance of the longer input power path and the input ceramic capacitor.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8060x and LT8060xHV to produce the DC output. The second function is to store energy to satisfy transient loads and stabilize the LT8060x and LT8060xHV's control loop. For good starting values, see *Typical application circuits* for LT80603 and LT80603HV, *Table 5* for LT80602 and LT80602HV, *Table 6* for LT80603A and LT80603AHV.

X5R/X7R/X8M ceramic output capacitors have very low equivalent series resistance (ESR) and are preferred for their temperature stability in industrial applications. This choice provides low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and an appropriate feedforward capacitor placed between V_{OUT} and FB/V_{OS}. Increasing the output capacitance also decreases the output voltage ripple. A lower value for the output capacitor can save space and cost, but transient performance suffers and may cause loop instability.

The choice of output capacitance is influenced by the closed-loop bandwidth. When the RT pin is left floating or connected with a resistor to GND, the maximum recommended bandwidth is approximately $f_{SW}/10$ or 80kHz. The LT8060x and LT8060xHV offer a unique feature when the RT pin is connected to $INTV_{CC}$. The internal compensation parameters are selected to facilitate a high bandwidth exceeding 150kHz. This enhanced bandwidth improves the

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transient performance, reduces output capacitance requirement, and minimizes solution size. See *Typical application circuits, Table 5* or *Table 6* for output capacitance in typical application circuits with the RT pin connected to $INTV_{CC}$.

Actual derating of ceramic capacitors under DC bias voltage must be considered when selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

FB Resistor Network

The output voltage can be programmed with a resistor divider between the output and the FB/V_{OS} pin. Choose the resistor values according to Equation 10.

$$R_{FB-TOP} = R_{FB-BOT} \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (10)$$

1% resistors are recommended to maintain output voltage accuracy. Limit the maximum value of R_{FB-TOP} to 1MΩ and R_{FB-BOT} to 205kΩ such that the maximum effective impedance at FB/V_{OS} is less than 170kΩ.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and increases the no-load input current to the device, which is approximately given by Equation 11.

$$I_{FB} = \left(\frac{V_{OUT}}{R_{FB-TOP} + R_{FB-BOT}}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{\eta}\right) \quad (11)$$

where, η is the light load efficiency. For a 5V application with R_{FB-TOP} = 1MΩ and R_{FB-BOT} = 191kΩ, the feedback divider draws 4.2µA. With V_{IN} = 24V and η = 85%, this adds ~1µA to the 7µA (I_{QB}) quiescent current, resulting in 8µA no-load current from the 24V supply. Note that Equation 11 implies that the no-load current is a function of V_{IN}.

When using large FB/V_{OS} resistors, a phase-lead capacitor should be connected from V_{OUT} to FB/V_{OS} to improve loop stability and transient performance. To achieve an optimal transient response with minimum output-voltage deviation or the required phase margin, the value of C_{FF} can be increased or decreased. A very large value of feedforward capacitor increases the bandwidth but provides less phase boost, as the maximum phase boost point shifts to lower frequencies.

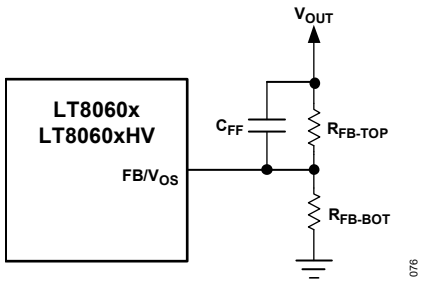


Figure 76. Setting the Output Voltage

Connect FB/V_{OS} to $INTV_{CC}$ to program the internal 5V output and float the FB/V_{OS} pin to program the internal 3.3V output. The BIAS/V_{OUT} pin should always be connected to V_{OUT} when programming the internal 3.3V or 5V output voltages. The internal feedback divider is connected to the BIAS/V_{OUT} pin.

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Table 5. Typical Component Values for LT80602

V_{OUT} (V)	FB/V_{OS}	f_{SW} (kHz)	L_{OUT} (µH)	C_{OUT}	R_{FB-TOP} (kΩ)	R_{FB-BOT} (kΩ)	C_{FF} (pF)	R_T (kΩ)
1.8	External FB Divider	400	3.3	3 × 47µF, 6.3V, 1210 (X7R)	357	287	22	Open
3.3	External FB Divider	400	6.8	1 × 47µF, 10V, 1210 + 1 × 22µF, 10V, 1210 (X7R)	665	216	8.2	Open
3.3	External FB Divider	2100	1.2	1 × 22µF, 1210, 10V (X7R)	665	216	6.8	8.66
5	External FB Divider	400	10	2 × 22µF, 1210, 16V (X7R)	1000	191	5.6	Open
5	External FB Divider	2100	1.8	1 × 22µF, 1210, 16V (X7R)	1000	191	5.6	8.66
12	External FB Divider	400	22	2 × 22µF, 25V, 1210 (X7R)	1000	71.5	8.2	Open
12	External FB Divider	2100	4.7	1 × 10µF, 1210, 25V (X7R)	1000	71.5	6.8	8.66
24	External FB Divider	400	47	3 × 4.7µF, 100V, 1206 (X7R)	1000	34	5.6	Open

Table 6. Typical Component Values for LT80603A

V_{OUT} (V)	FB/V_{OS}	f_{SW} (kHz)	L_{OUT} (µH)	C_{OUT}	R_{FB-TOP} (kΩ)	R_{FB-BOT} (kΩ)	C_{FF} (pF)	R_T (kΩ)
1.8	External FB Divider	400	2.7	5 × 47µF, 6.3V, 1210 (X7R)	357	287	47	Open
3.3	External FB Divider	400	4.7	2 x 47µF, 10V, 1210 + 1 x 22µF, 10V, 1210 (X7R)	665	216	12	Open
3.3	External FB Divider	2100	1	1 x 47µF, 10V, 1210 + 1 x 22µF, 10V, 1210 (X7R)	665	216	22	8.66
5	External FB Divider	400	6.8	2 x 47µF, 10V, 1210 (X7R)	1000	191	8.2	Open
5	External FB Divider	2100	1.5	1 x 47µF, 10V, 1210 (X7R)	1000	191	6.8	8.66
12	External FB Divider	400	22	2 x 22µF, 25V, 1210 (X7R)	1000	71.5	6.8	Open
24	External FB Divider	400	33	2 x 4.7µF, 100V, 1206 (X7R)	1000	34	1.5	Open

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Ceramic Capacitors

Ceramic capacitors are small, robust, and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8060x and LT8060xHV due to their piezoelectric nature. When in Burst Mode operation, the LT8060x and LT8060xHV's switching frequency depends on the load current, and at very light loads, the LT8060x and LT8060xHV can excite the ceramic capacitor at audio frequencies, generating audible noise. As the LT8060x and LT8060xHV operate at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high-performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8060x and LT8060xHV. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high-quality (underdamped) tank circuit. If the LT8060x and LT8060xHV circuits are plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8060x and LT8060xHV's rating. This situation can be easily avoided. Refer to Analog Devices *Application Note 88* for more details.

BST Capacitor Selection

A capacitor between BST and SW provides the current required by the high-side driver and internal circuits operating on the BST to SW rail. In Burst Mode, when the converter is operating at no load, the switching frequency is significantly reduced, resulting in extended intervals of several milliseconds between consecutive pulses. The BST capacitor must be selected appropriately to hold sufficient charge and supply the BST from the SW rail in sleep mode. See *Figure 77* for the minimum recommended capacitance at programmed switching frequency. If the converter is programmed to operate in pulse-skipping or FCM mode, it is recommended to use a 0.1µF BST to SW capacitor.

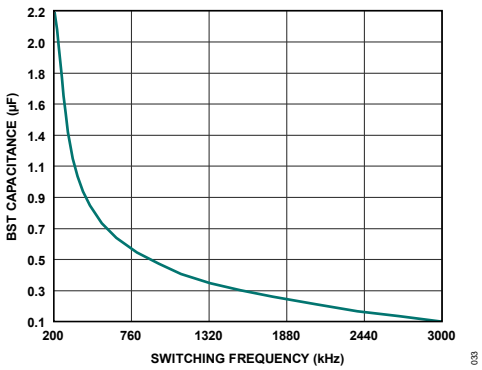


Figure 77.Switching Frequency vs. BST Capacitance

Table 7. Switching Frequency vs. BST Capacitance

Switching Frequency (kHz)	C_{BST} (µF)
200	2.2
400	1
1000	0.47
2100	0.22
3000	0.1

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Enable Pin

The LT8060x and LT8060xHV are in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1V, with a 100mV hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8060x and LT8060xHV to regulate the output only when V_{IN} exceeds a desired voltage (see the *Functional Diagram*). Typically, this threshold, $V_{IN(EN)}$, is used when the input supply is current-limited or has a relatively high source resistance. A switching regulator draws constant power from the source. So, the source current increases as the source voltage drops. This is a negative-resistance load to the source and can cause the source to current-limit or latch low under low-source-voltage conditions. The $V_{IN(EN)}$ threshold ensures the regulator does not operate at source voltages that could cause issues. This threshold can be adjusted by setting R_{EN-TOP} and $R_{EN-BOTTOM}$ values to satisfy Equation 12.

$$R_{EN-BOTTOM} = \frac{R_{EN-TOP} \times 1}{(V_{IN(EN)} - 1)} \quad (12)$$

where, the LT8060x and LT8060xHV remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching does not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8060x and LT8060xHV. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low-dropout (LDO) regulator provides the 1.8V supply that powers the drivers and internal bias circuitry. Bypass $INTV_{CC}$ to GND with a minimum of 2.2µF low-ESR ceramic capacitor. The internal low-dropout linear regulator is powered either from V_{IN} or BIAS/V_{OUT}. During soft-start, $INTV_{CC}$ is powered from V_{IN}. At the end of the programmed soft-start time, if the BIAS/V_{OUT} pin voltage is greater than 2.35V, $INTV_{CC}$ switches to BIAS/V_{OUT}. Powering $INTV_{CC}$ from BIAS/V_{OUT} reduces on-chip dissipation and increases efficiency at higher input voltages. Connect the BIAS/V_{OUT} pin to the converter output-voltage node to achieve output voltages ranging from 2.35V to 25V, improving efficiency. If the BIAS/V_{OUT} pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin.

The LT8060x and LT8060xHV start switching only when the voltage at $INTV_{CC}$ is greater than 1.64V. The device employs an undervoltage lockout circuit that forces the converter off when the $INTV_{CC}$ voltage falls below 1.58V. The 65mV hysteresis prevents chattering during power-up/power-down. Connect the BIAS/V_{OUT} pin to GND when not in use. Do not connect an external load to the $INTV_{CC}$ pin.

Always connect BIAS/V_{OUT} to the converter's output of the when programmed to internal 5V or 3.3V, and the internal feedback is connected to BIAS/V_{OUT}.

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Output Voltage Tracking and Soft-Start

The LT8060x and LT8060xHV allow programming of the output-voltage ramp rate via the TR/SS pin. An internal 5µA pulls up the TR/SS pin to $INTV_{CC}$. Adding an external capacitor on TR/SS enables soft-starting of the output, preventing a current surge on the input supply. During the soft-start ramp, the output voltage proportionally tracks the TR/SS pin voltage. For output-tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.8V, the TR/SS voltage overrides the internal 0.8V reference input to the error amplifier, therby regulating the feedback node voltage to that of the TR/SS pin. When TR/SS is above 0.8V, tracking is disabled, and the feedback node voltage regulates to the internal reference voltage. If the TR/SS voltage is held below 0.78V, regardless of the programmed mode, the device operates in pulse skip mode. During the soft-start operation, if $V_{TR/SS}$ increases above 0.78V, the device transits from pulse skipping mode to programmed mode. Once soft-start is complete, irrespective of the $V_{TR/SS}$ voltage, the device operates in the programmed mode.

The selected output capacitance (C_{OUT_SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 25 \times 10^{-6} \times C_{OUT_SEL} \times V_{OUT} \quad (13)$$

The soft-start time (t_{SS}) is related to the capacitor connected at TR/SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{6.25 \times 10^{-6}} \quad (14)$$

An internal 4Ω MOSFET to GND is connected on the TR/SS pin, which discharges the external soft-start capacitor in the case of fault conditions and restarts the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good and Die Temperature Monitor

The LT8060x and LT8060xHV offer the PG/T_J pin to monitor either the output voltage status or the die temperature. When the LT8060x and LT8060xHV are used for power good functionality, and the output voltage is within the window of the regulation point specified in the *Table 1* (Electrical Characteristics table). The output voltage is considered good, and the open-drain PG/T_J pin is in high-impedance mode and is typically pulled high with an external resistor. Otherwise, the internal pull-down device pulls the PG/T_J pin low. To prevent glitching both the upper and lower thresholds, include 1% of hysteresis.

The PG/T_J pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

To monitor the die temperature, connect a 20kΩ resistor from PG/T_J to GND. The die temperature monitor feature is functional only when the output voltage is good, and the internal open-drain power good MOSFET is in high-impedance mode.

The die temperature (T_J) in °C is calculated as follows:

$$T_J = \frac{(V_{TJ} - 0.595)}{\left(2 \times 10^{-3}\right)} + 25 \quad (15)$$

where, V_{TJ} is the PG/T_J pin voltage in V when the device is loaded.

Note: A minimum of 1V pull-up is needed on PG/T_J for the PGOOD functionality to not interact with the T_J loop at HOT and consume quiescent current.

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Overcurrent Protection (OCP)/Hiccup Mode

The LT8060x and LT8060xHV provide a robust overcurrent protection (OCP) scheme that protects the device under overload and output short-circuit conditions. The OCP scheme protects the device using a hysteretic control of the inductor current that avoids the inductor current runaway condition. In hysteretic control, whenever the inductor peak current exceeds an internal peak current limit ($I_{PEAK-LIMIT}$) of 4.81A for LT80602 and LT80602HV, 5.5A for LT80603 and LT80603HV, or 6.3A for LT80603A and LT80603AHV, the high-side MOSFET is turned off, and the low-side MOSFET is turned on. When the inductor current reduces to 3.9A, the low-side MOSFET is turned off, and the high-side MOSFET is turned on. In addition, if the FB node voltage drops below 91.5% (V_{FB-UV}) and the inductor current is above 3.9A for more than 300ns in each switching cycle after the high side is turned off for 20ms, hiccup mode is activated. This scenario occurs for LT80603A when the part is operated at rated load during dropout conditions, with the FB node voltage below V_{FB-UV}.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 130ms. Once the hiccup timeout period expires, a soft-start is attempted again. Note that when soft start is attempted under overload conditions, if the device operates in current limit, the blanking timer is enabled during soft start. The hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

The device provides a valley current protection scheme that protects itself in FCM mode from large negative currents. Under strong external output bias conditions, when the inductor valley current falls below -2.5A ($I_{VALLEY-LIMIT}$), the device turns off low-side and turns ON high-side until the inductor current reaches zero. Low-side is turned ON again if the output voltage is taken above regulation voltage.

Reversed Input Protection

Reversed Input Protection is found in systems where the inputs to the LT8060x and LT8060xHV are absent, and the output is held high. For example, in battery-charging applications or in battery-backup systems where a battery or another supply is diode-ORed with the LT8060x and LT8060xHV's outputs. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8060x and LT8060xHV's internal circuitry pulls its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded, the SW pin current drops to near 1µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes within the LT8060x and LT8060xHV can pull current from the output through the SW and V_{IN} pins, potentially damaging the device. *Figure 78* shows a connection between the V_{IN} and EN/UV pins that allows the LT8060x and LT8060xHV to run only when the input voltage is present and protects against a shorted or reversed input.

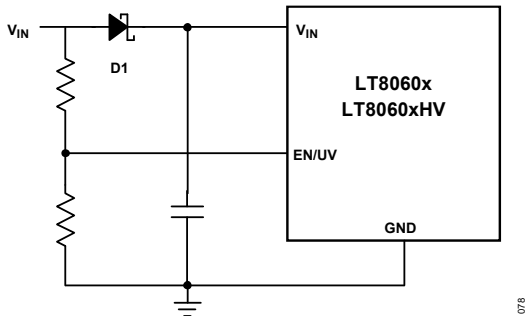


Figure 78. Reverse V_{IN} Protection

In FCM, when diode D1 is used, always ensure that the external applied voltage to the output is less than the regulation set point voltage. Sinking current from the output may result in overvoltage at the input pin and leads to device failure.

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Thermal Considerations and Peak Output Current

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8060x and LT8060xHV. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers spread heat dissipated by the LT8060x and LT8060xHV. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8060x and LT8060xHV can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss.

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - (I_{OUT}^2 \times R_{DCR}) \quad (16)$$

The die temperature (T_J) of the device can be calculated at any given maximum ambient temperature (T_{AMB}) from the following equation when the die temperature monitor (PG/T_J) feature is not used.

$$T_J = T_{AMB} + (\theta_{JA} \times P_{LOSS}) \quad (17)$$

The internal overtemperature protection monitors the junction temperature of the LT8060x and LT8060xHV. If the junction temperature reaches approximately 175°C, the LT8060x and LT8060xHV stop switching and indicate a fault condition until the temperature drops by about 10°C cooler, and then the device restarts with soft-start.

The LT8060x and LT8060xHV experience the greatest temperature rise when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level.

The internal power switches of the LT80602 and LT80602HV can safely deliver up to 2.5A of output current; those of the LT80603 and LT80603HV support up to 3.5A; and the LT80603A and LT80603AHV support up to 4.5A. However, the actual deliverable current in the application must be calculated based on power loss, θ_{JA}, and T_{AMB}.

The top switch current limit is fixed at 4.81A (typ) for the LT80602 and LT80602HV, at 5.5A (typ) for the LT80603 and LT80603HV, and 6.3A (typ) for the LT80603A and LT80603AHV. This also limits the peak output current that the LT8060x and LT8060xHV can deliver for a given application.

Figure 79 and *Figure 80* shows the typical thermal performance of the LT80603 evaluation board.

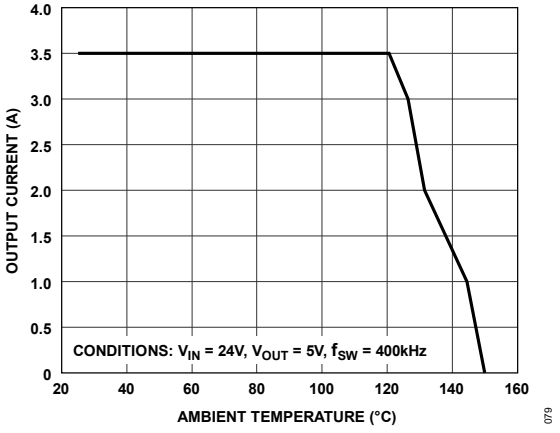


Figure 79. LT80603 5V, 400kHz Thermal Derating

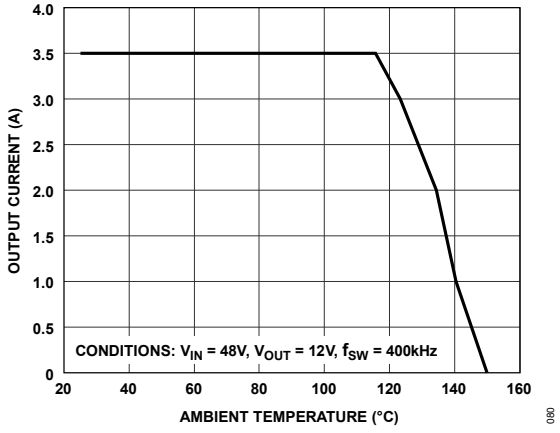


Figure 80. LT80603 12V, 400kHz Thermal Derating

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TYPICAL APPLICATION CIRCUITS

Table 8. V_{OUT} Configuration Table

V_{OUT} (V)	f_{SW} (kHz)	FB/V_{OS}	R_{FB-TOP} (kΩ)	R_{FB-BOT} (kΩ)	C_{FF} (pF)	$R_{FB/Vos}$ (kΩ)
5	400	External FB Divider	1000	191	5.6	Open
5	2100	External FB Divider	1000	191	4.7	Open
3.3	400	External FB Divider	665	216	12	Open
3.3	2100	External FB Divider	665	216	10	Open
5	-	Internal FB Divider	Open	Open	Open	0
3.3	-	Internal FB Divider	Open	Open	Open	Open

Typical Application Circuit 5V/3.5A Output

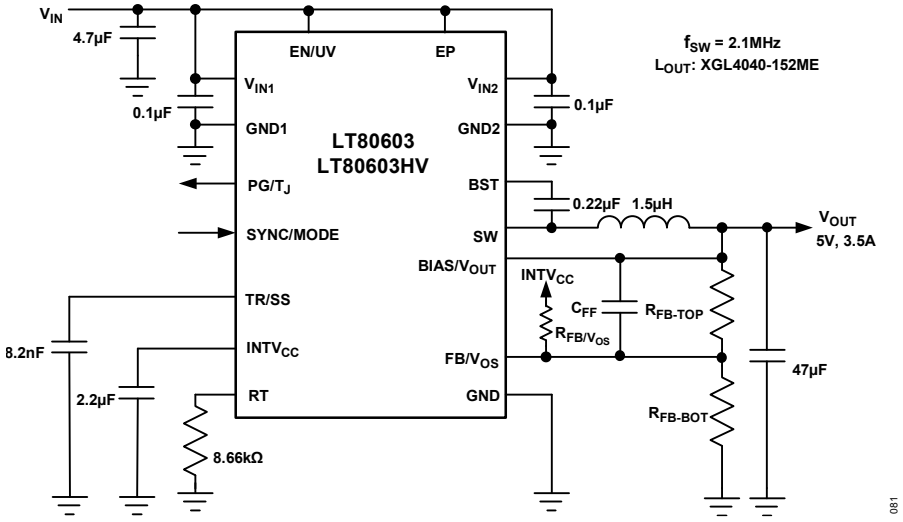


Figure 81. 5V/3.5A Output with 2.1MHz Switching Frequency

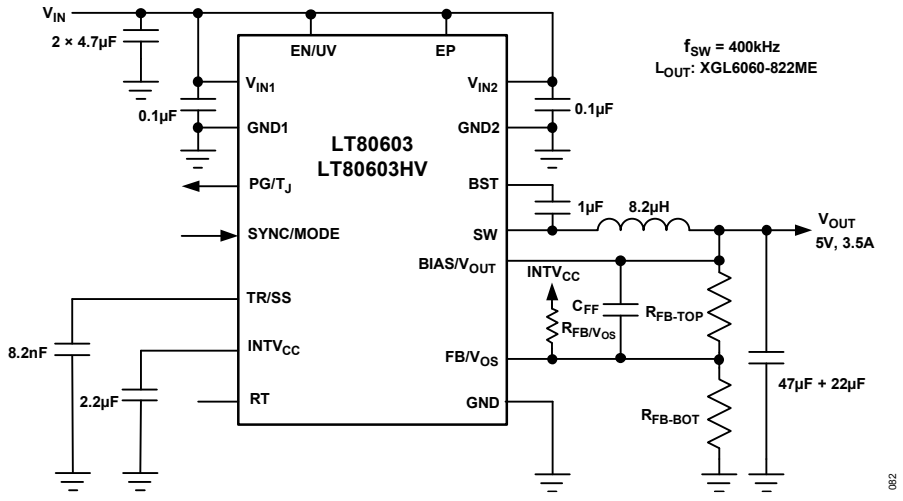


Figure 82. 5V/3.5A Output with 400kHz Switching Frequency

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Typical Application Circuit 12V/3.5A Output

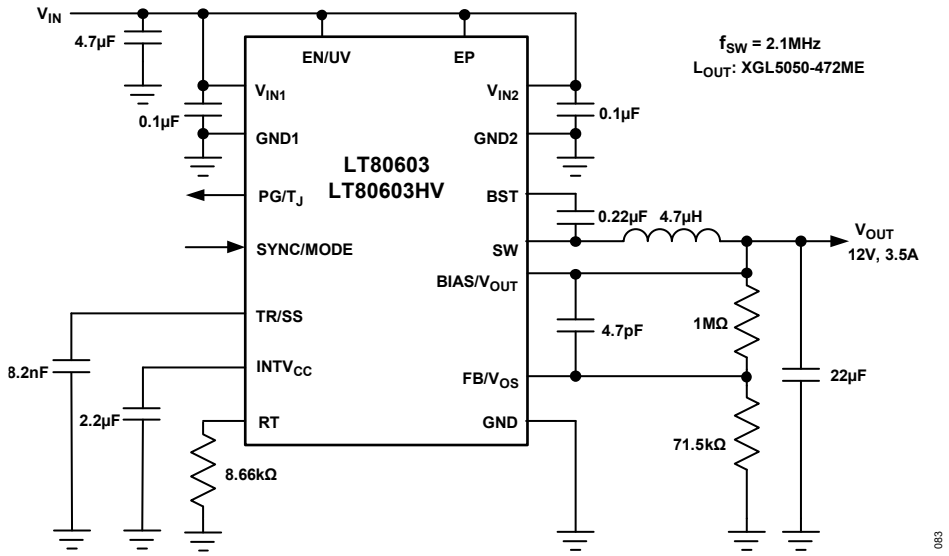


Figure 83. 12V/3.5A Output with 2.1MHz Switching Frequency

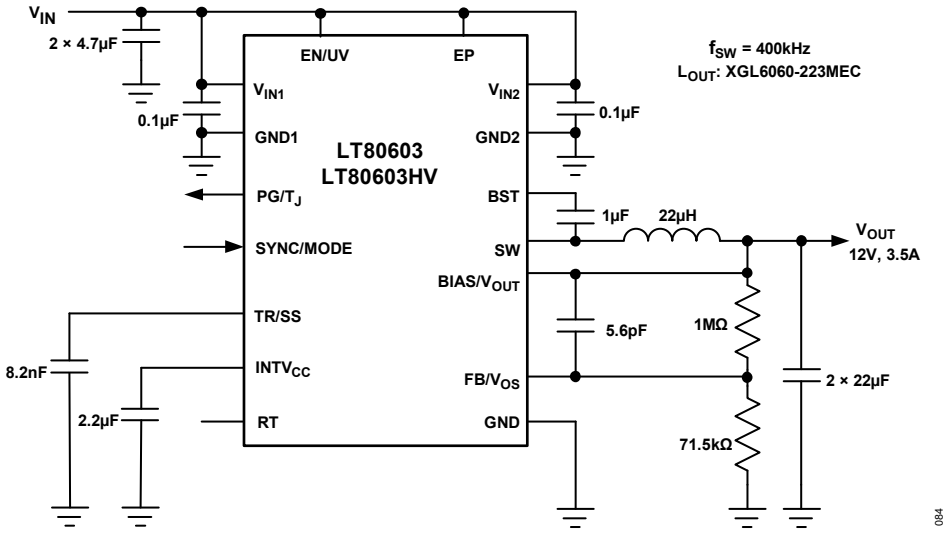


Figure 84. 12V/3.5A Output with 400kHz Switching Frequency

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Typical Application Circuit 3.3V/3.5A Output

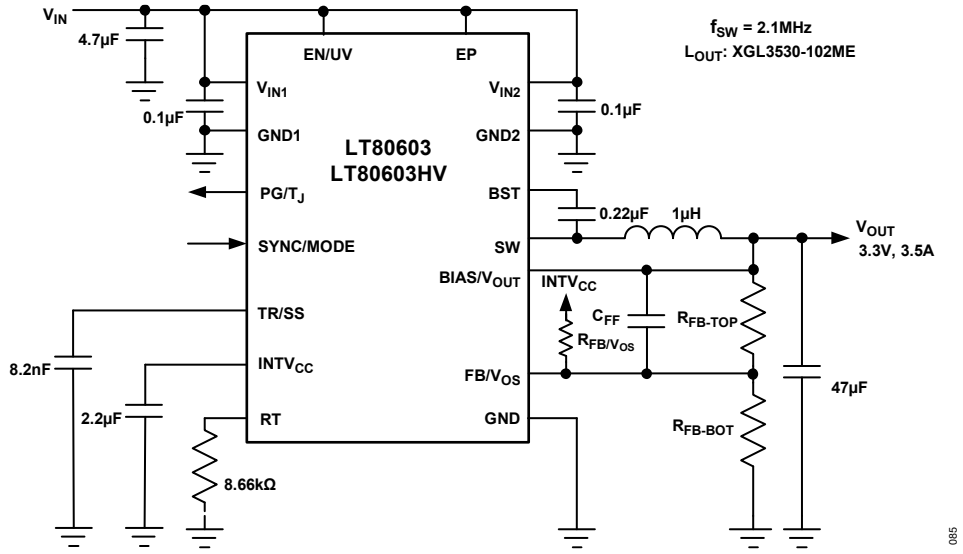


Figure 85. 3.3V/3.5A Output with 2.1MHz Switching Frequency

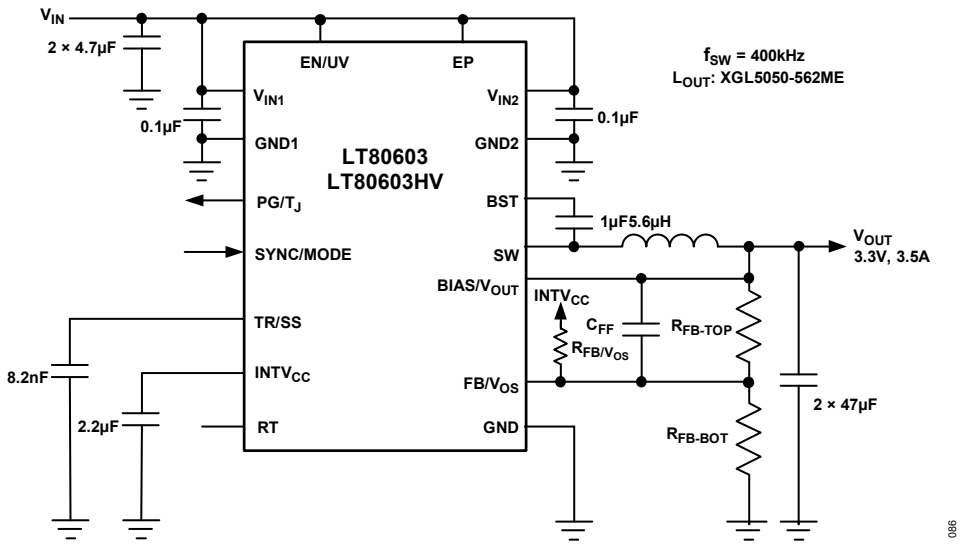


Figure 86. 3.3V/3.5A Output with 400kHz Switching Frequency

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Typical Application Circuit 1.8V/3.5A Output

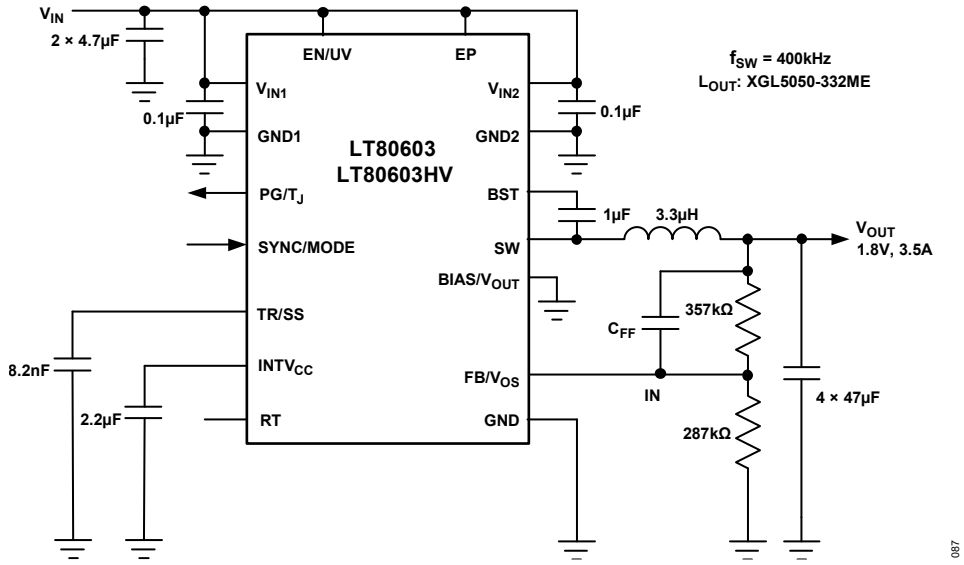


Figure 87. 1.8V/3.5A Output with 400kHz Switching Frequency

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Typical Application Circuit 24V/3.5A Output

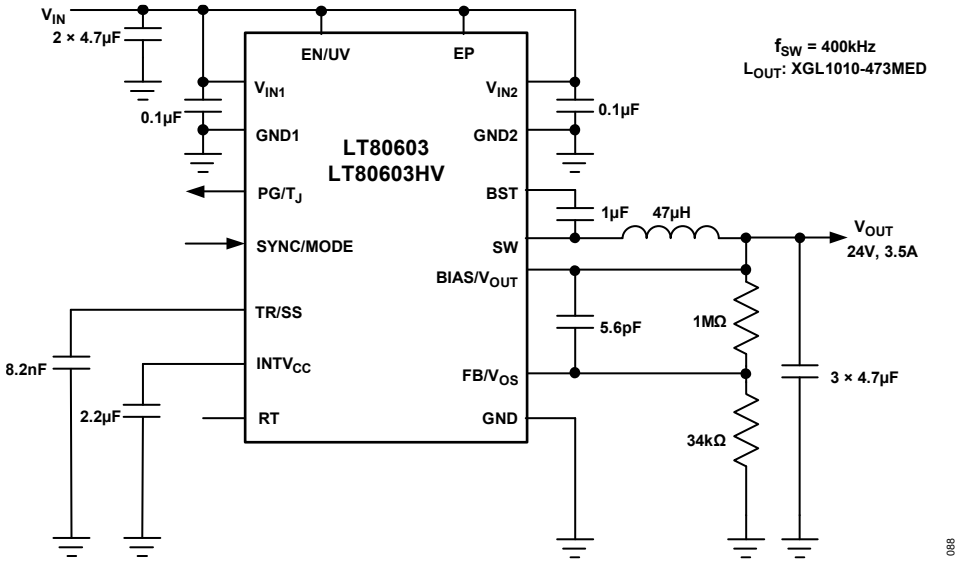


Figure 88. 24V/3.5A Output with 400kHz Switching Frequency

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Typical Application Circuits for Ultralow EMI

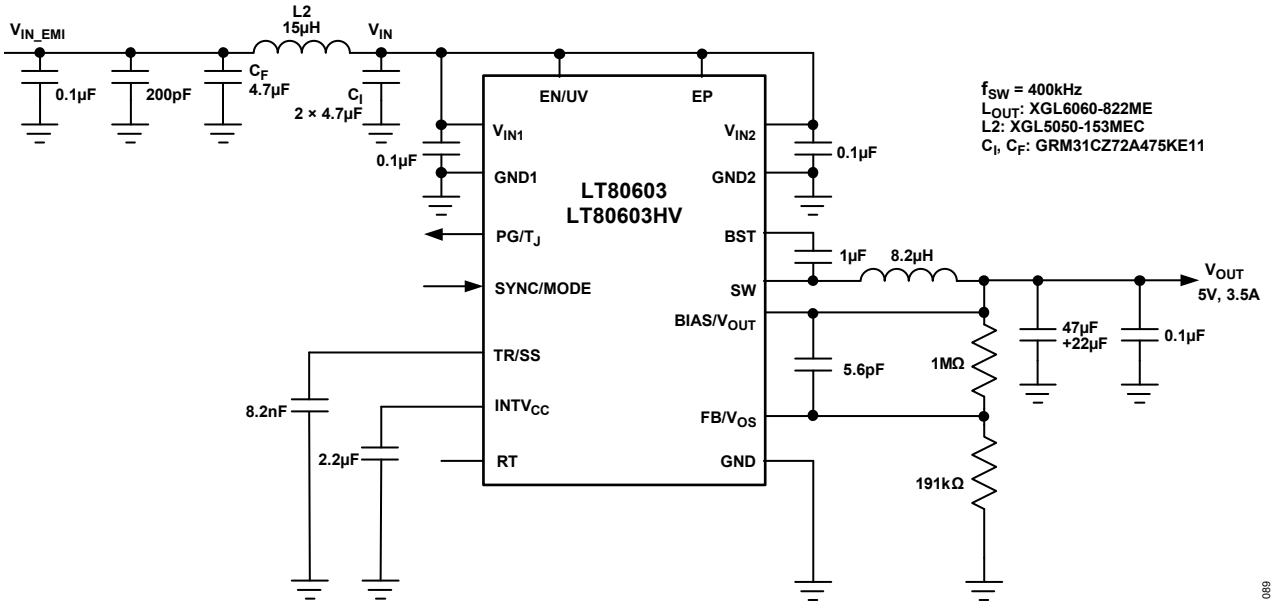


Figure 89. 5V/3.5A Output with 400kHz Switching Frequency for Ultralow EMI

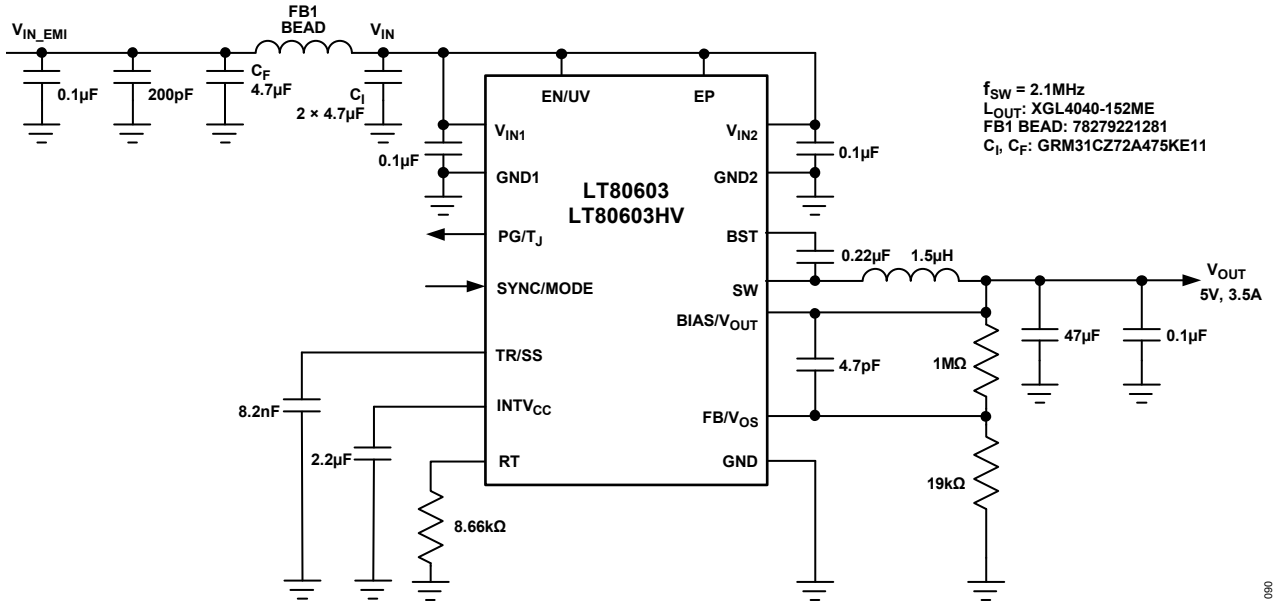


Figure 90. 5V/3.5A Output with 2.1MHz Switching Frequency for Ultralow EMI

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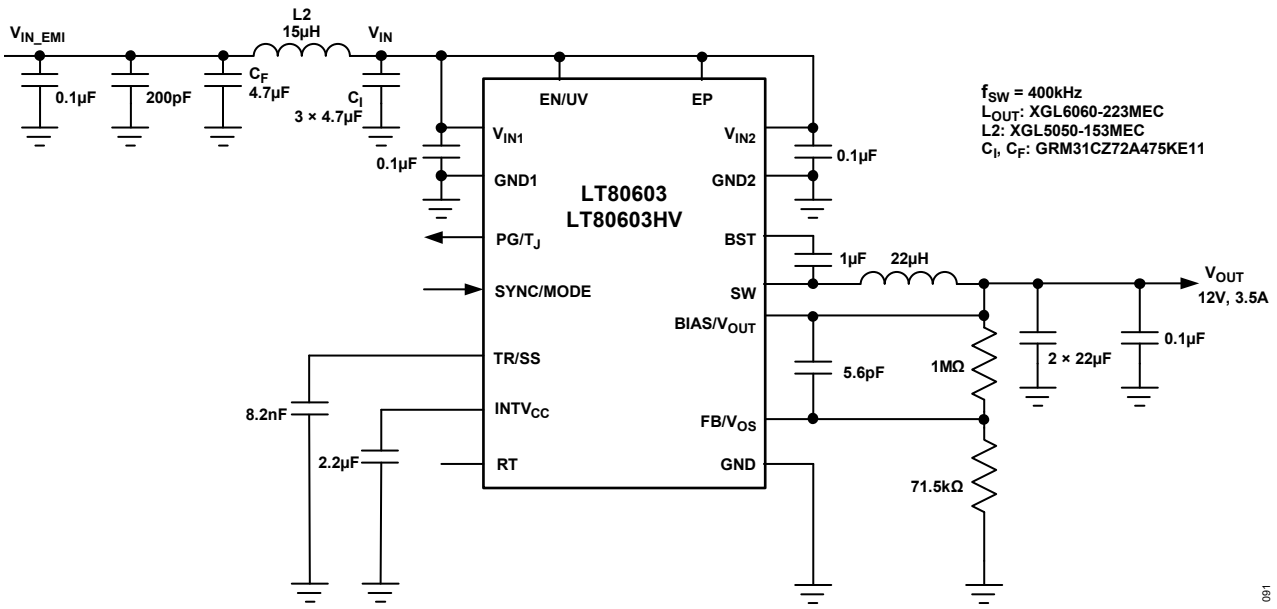


Figure 91. 12V/3.5A Output with 400kHz Switching Frequency for Ultralow EMI

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OUTLINE DIMENSIONS

Table 9. Thermal Resistance of 17L FC2QFN

Thermal Resistance, Four-Layer Board (See Note 1)	
Junction to Ambient (θ_{JA})	31°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	4.4°C/W

Note 1: Package thermal resistances are obtained using the LT80603 evaluation kit with no airflow.

For the latest package outline information and land patterns (footprints), refer to *package index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

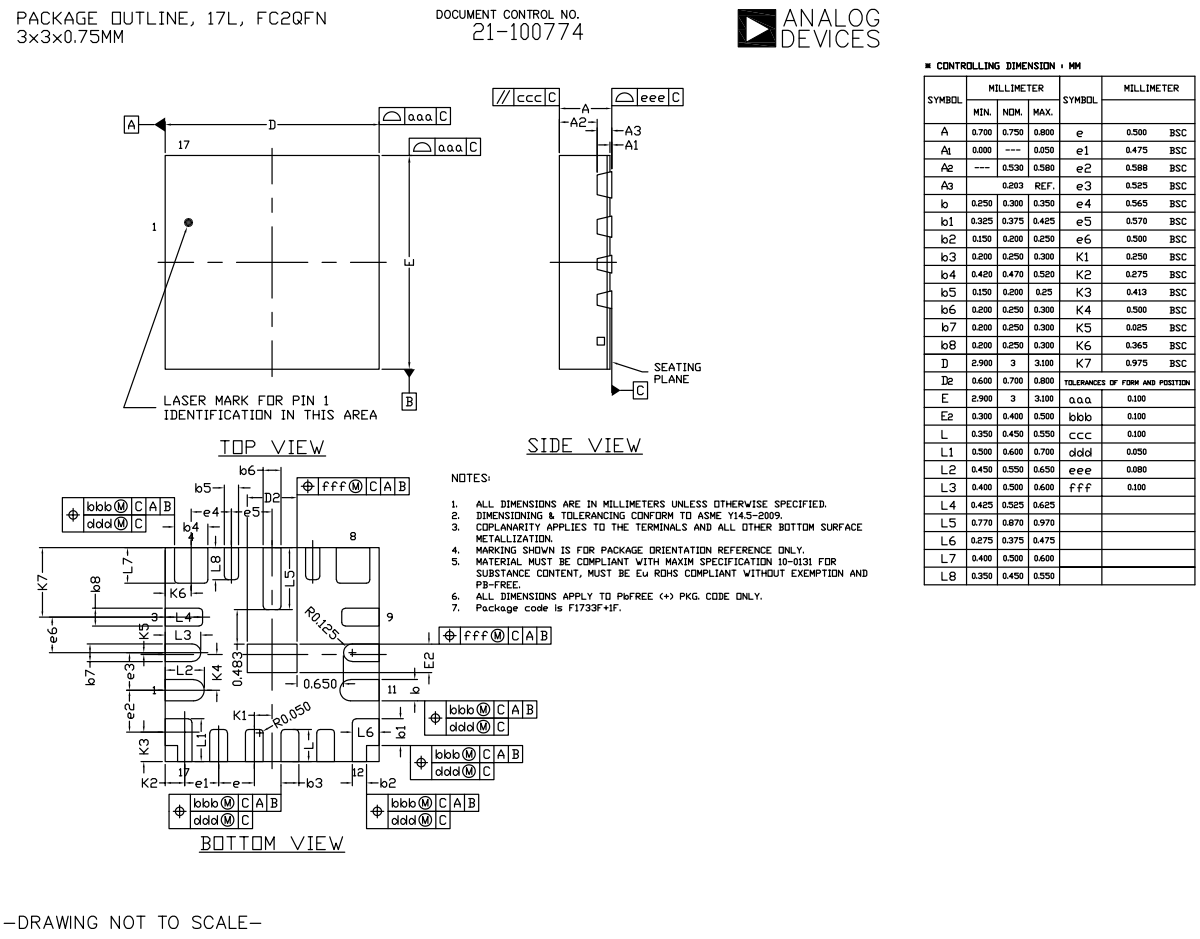
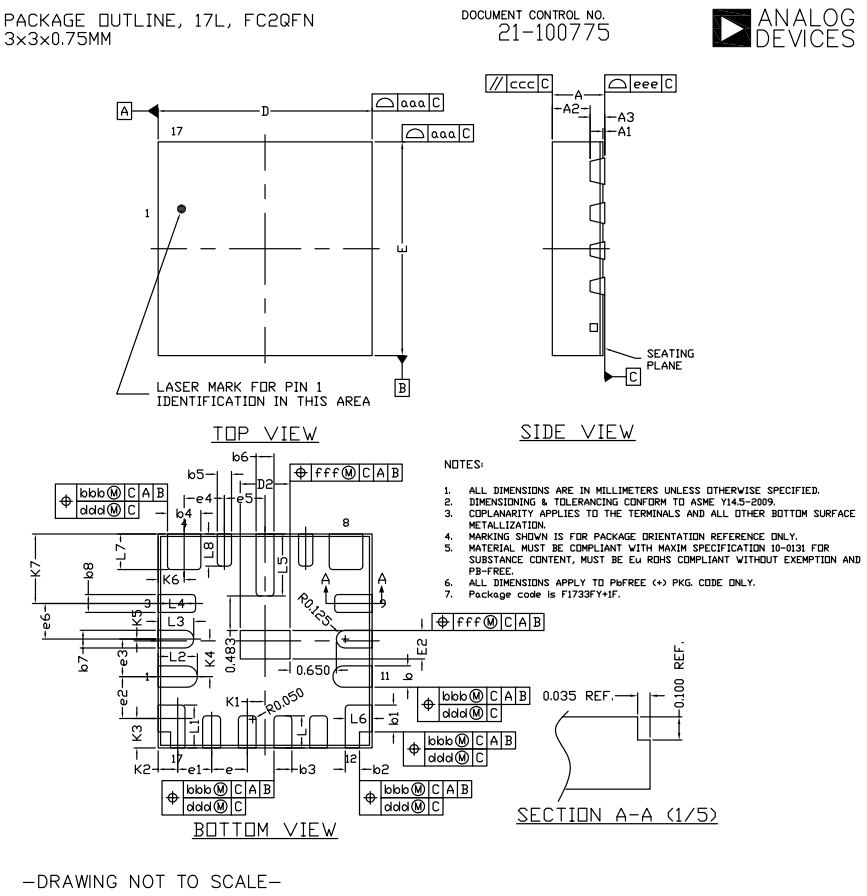


Figure 92. Package Outline for Non-Side Wettable Version

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* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			SYMBOL	MILLIMETER	
	MIN.	NOM.	MAX.			
A	0.700	0.750	0.800	e	0.500	BSC
A1	0.000	---	0.050	e1	0.475	BSC
A2	---	0.530	0.580	e2	0.588	BSC
A3		0.203	REF.	e3	0.525	BSC
b	0.250	0.300	0.350	e4	0.565	BSC
b1	0.325	0.375	0.425	e5	0.570	BSC
b2	0.150	0.200	0.250	e6	0.500	BSC
b3	0.200	0.250	0.300	K1	0.250	BSC
b4	0.420	0.470	0.520	K2	0.275	BSC
b5	0.150	0.200	0.25	K3	0.413	BSC
b6	0.200	0.250	0.300	K4	0.500	BSC
b7	0.200	0.250	0.300	K5	0.025	BSC
b8	0.200	0.250	0.300	K6	0.365	BSC
D	2.900	3	3.100	K7	0.975	BSC
D2	0.600	0.700	0.800	TOLERANCES OF FORM AND POSITION		
E	2.900	3	3.100	aaa	0.100	
E2	0.300	0.400	0.500	bbb	0.100	
L	0.350	0.450	0.550	ccc	0.100	
L1	0.500	0.600	0.700	ddd	0.050	
L2	0.450	0.550	0.650	eee	0.080	
L3	0.400	0.500	0.600	fff	0.100	
L4	0.425	0.525	0.625			
L5	0.770	0.870	0.970			
L6	0.275	0.375	0.475			
L7	0.400	0.500	0.600			
L8	0.350	0.450	0.550			

Figure 93. Package Outline for Side Wettable Version

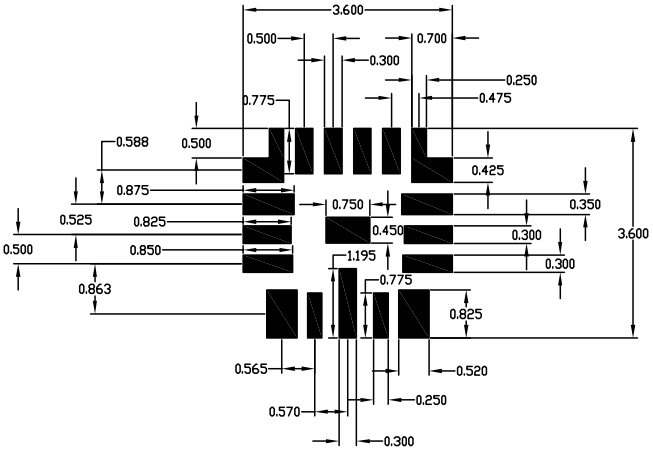
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PACKAGE LAND PATTERN,
[F1733F+1F / F1733FY+1F] FC2QFN

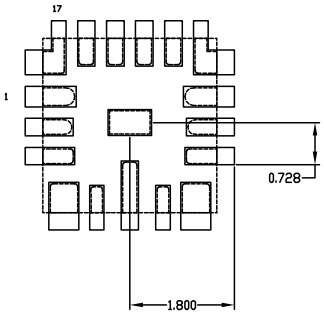
DOCUMENT CONTROL NO. 90-100271 REV. B

ANALOG DEVICES

RECOMMENDED LAND PATTERN



PACKAGE OVERLAY



NOTES:
1. REFERENCE PKG. OUTLINE: 21-100774 / 21-100775
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO LEADED, PbFREE PACKAGES.
5. ALL DIMENSIONS IN MM.

-DRAWING NOT TO SCALE-

This document (including dimensions, notes & specs) is a recommendaton based on typical circuit board manufacturing parameters. Since land pattern design depend on many factors unknown to Analog Devices Inc. (eg. user's board manufacturing specs), user must determine suitability for use. This document is subject to change without notice.
Contact technical support at https://www.analog.com/en/support for further questions.

Figure 94. Package Land Pattern for Side Wettable/Non-Side Wettable Version

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ORDERING GUIDE

Table 10. Ordering Guide

PART NUMBER	PART MARKING	AbsMax V_{IN}	I_{OUT}	SPREAD SPECTRUM	SIDE WETTABLE	AECQ-100	PACKAGE CODE
LT80602AFO+	80602 FO	70V	2.5A	N	N	N	F1733F+1F
LT80602AFO+T	80602 FO	70V		N	N	N	F1733F+1F
LT80602AFOH+	80602 FOH	80V		N	N	N	F1733F+1F
LT80602AFOH+T	80602 FOH	80V		N	N	N	F1733F+1F
LT80602AFOA/VY+T	80602 OA/VY	70V		Y	Y	Y	F1733FY+1F
LT80602AFOAH/VY+T**	80602 AH/VY	80V		Y	Y	Y	F1733FY+1F
LT80603AFO+	80603 FO	70V	3.5A	N	N	N	F1733F+1F
LT80603AFO+T	80603 FO	70V		N	N	N	F1733F+1F
LT80603AFOH+	80603 FOH	80V		N	N	N	F1733F+1F
LT80603AFOH+T	80603 FOH	80V		N	N	N	F1733F+1F
LT80603AFOA/VY+T	80603 OA/VY	70V		Y	Y	Y	F1733FY+1F
LT80603AFOAH/VY+T**	80603 AH/VY	80V		Y	Y	Y	F1733FY+1F
LT80603AAFOA+	80603A AFOA	70V	4.5A	N	N	N	F1733F+1F
LT80603AAFOA+T	80603A AFOA	70V		N	N	N	F1733F+1F
LT80603AAFOAH+	80603A AFOAH	80V		N	N	N	F1733F+1F
LT80603AAFOAH+T	80603A AFOAH	80V		N	N	N	F1733F+1F
LT80603AAFOA/VY+T**	80603A AFOAV	70V		Y	Y	Y	F1733FY+1F
LT80603AAFOAH/VY+T**	80603A AAH/V	80V		Y	Y	Y	F1733FY+1F

+ Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape-and-reel.
*** Potential future product.*
Contact the factory for other sequence options.

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