SLG47003V Demo Board

The SLG47003V Demo Board is designed to demonstrate the basic capabilities of the chip. Three different designs are implemented on the board: an offset and gain tuning, an addressable LED control, and a tunable voltage regulator.

Specifications

The SLG47003V Demo Board R1.0 is optimized for the following operating conditions:

- USB 2.0 specifications for powering the board (from 4.4 V to 5.25 V, max 500 mA)
- Operating System: Windows 7/8.1/10/11, macOS (v10.15 or higher), Ubuntu 22.04/24.04, Debian 12/Testing

Features

- External board power from USB Type-C port
- GreenPAK Serial Debugger support
- GreenPAK Advanced Development Platform support
- Go Configure Software Hub software compatible
- Two Test Points (TS) for output of internal OpAmps
- Encoder for design parameters regulation

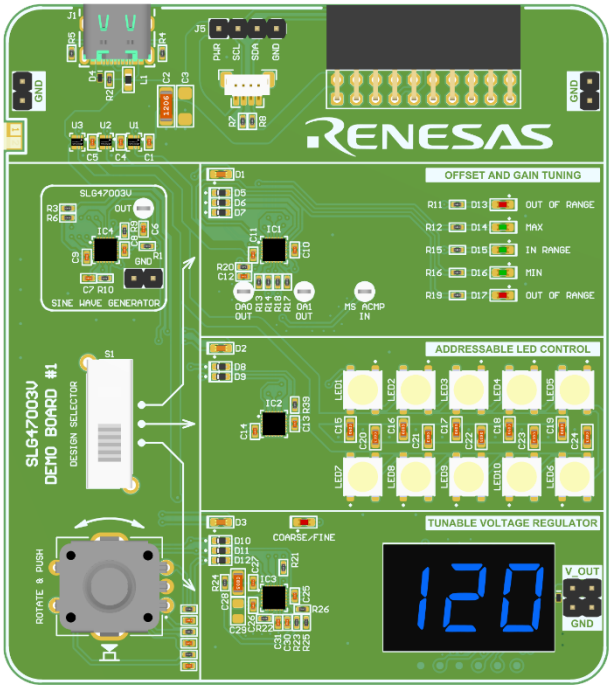


Figure 1. SLG47003V Demo Board, General View

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1. Functional Description

The SLG47003V Demo Board R1.0 implements three different designs on a single board. These designs demonstrate the basic capabilities of the chip and enhance the process of integrating it into a finished device. The designs include:

- an offset and gain tuning,
- an addressable LED control
- a tunable voltage regulator

The main components are shown in Figure 2.

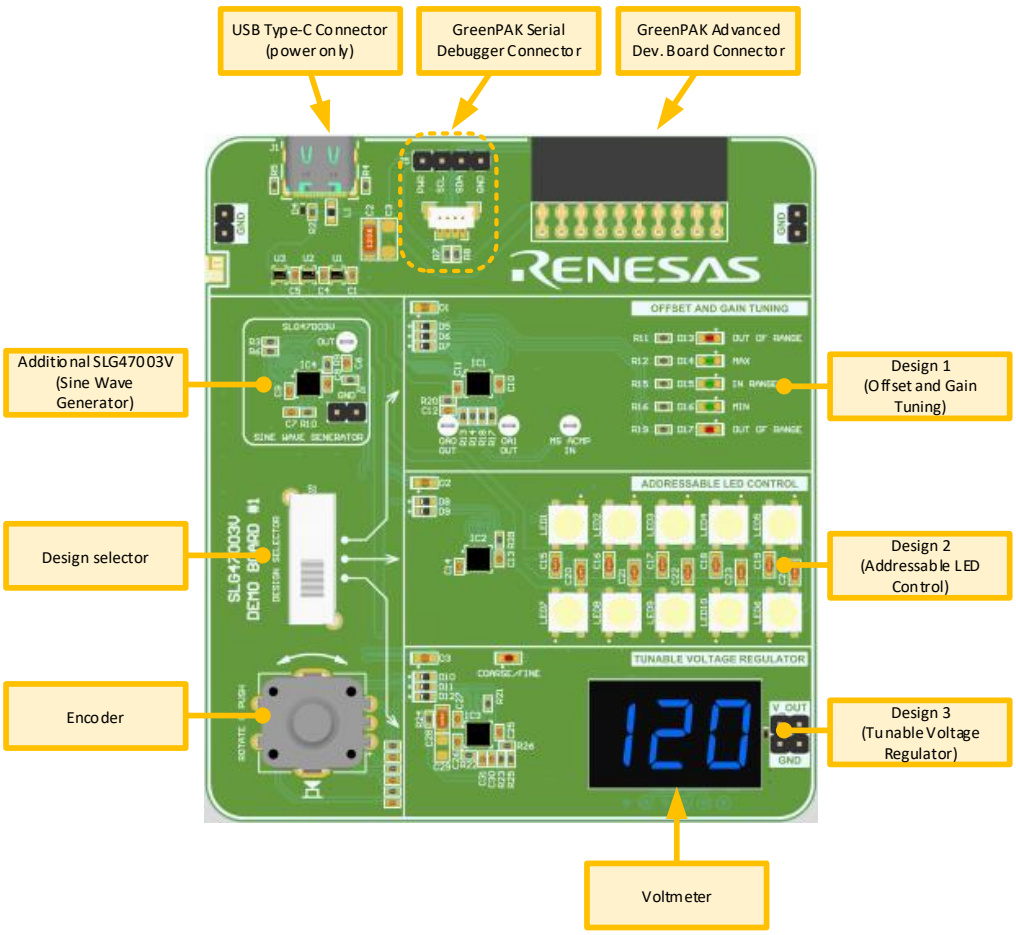


Figure 2. SLG47003V Demo Board Overview

A brief block diagram of the Demo Board is shown in Figure 3.

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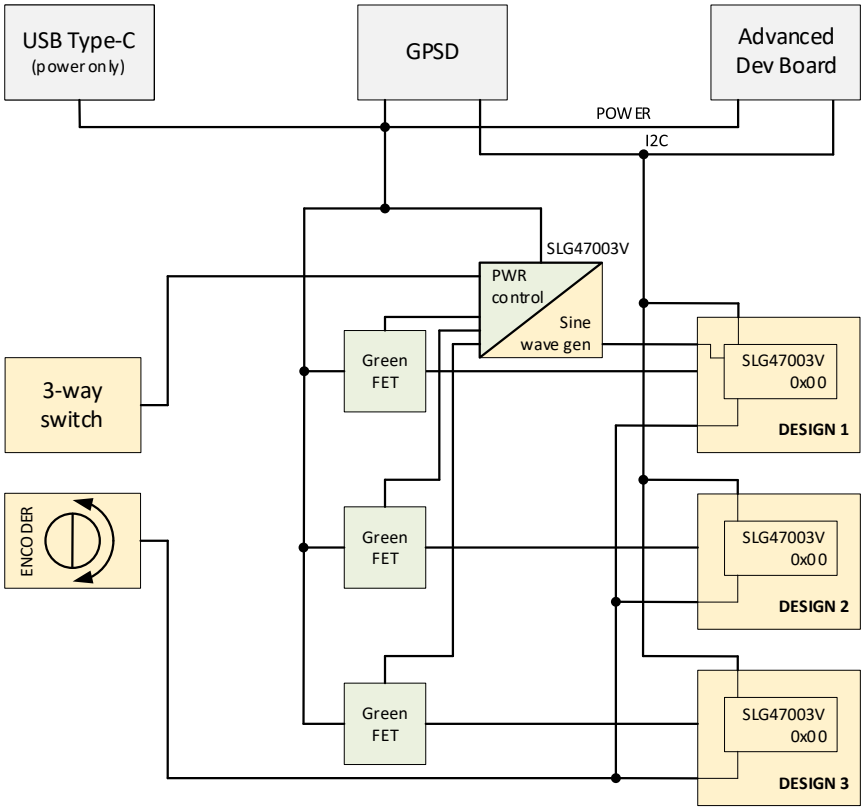


Figure 3. SLG47003V Demo Board Block Diagram

Interaction with the IC on the Demo Board is provided through a USB Type-C port (needed only to power the board), a GreenPAK Serial Debugger, or a GreenPAK Advanced Development Board, along with the Go Configure Software Hub. To emulate the selected design, move the 3-way switch to the appropriate position. By default, the first design is enabled on the board.

2. Board Design

2.1 Offset and Gain Tuning

This design has been developed for a demo board to teach the skills required for working with the SLG47003V and to improve understanding of the operation of the digital and analog blocks in the GreenPAK. It also demonstrates the basic concepts of analog design, such as offset and gain, and their correct application.

The design concept (see Figure 4) involves adjusting the gain and offset of the input sinusoidal signal by changing the resistance of rheostats RH0 and RH1, ensuring it remains within the limits defined by the MS-ACMP. The condition of the output signal is indicated by red and green LEDs (see Figure 5).

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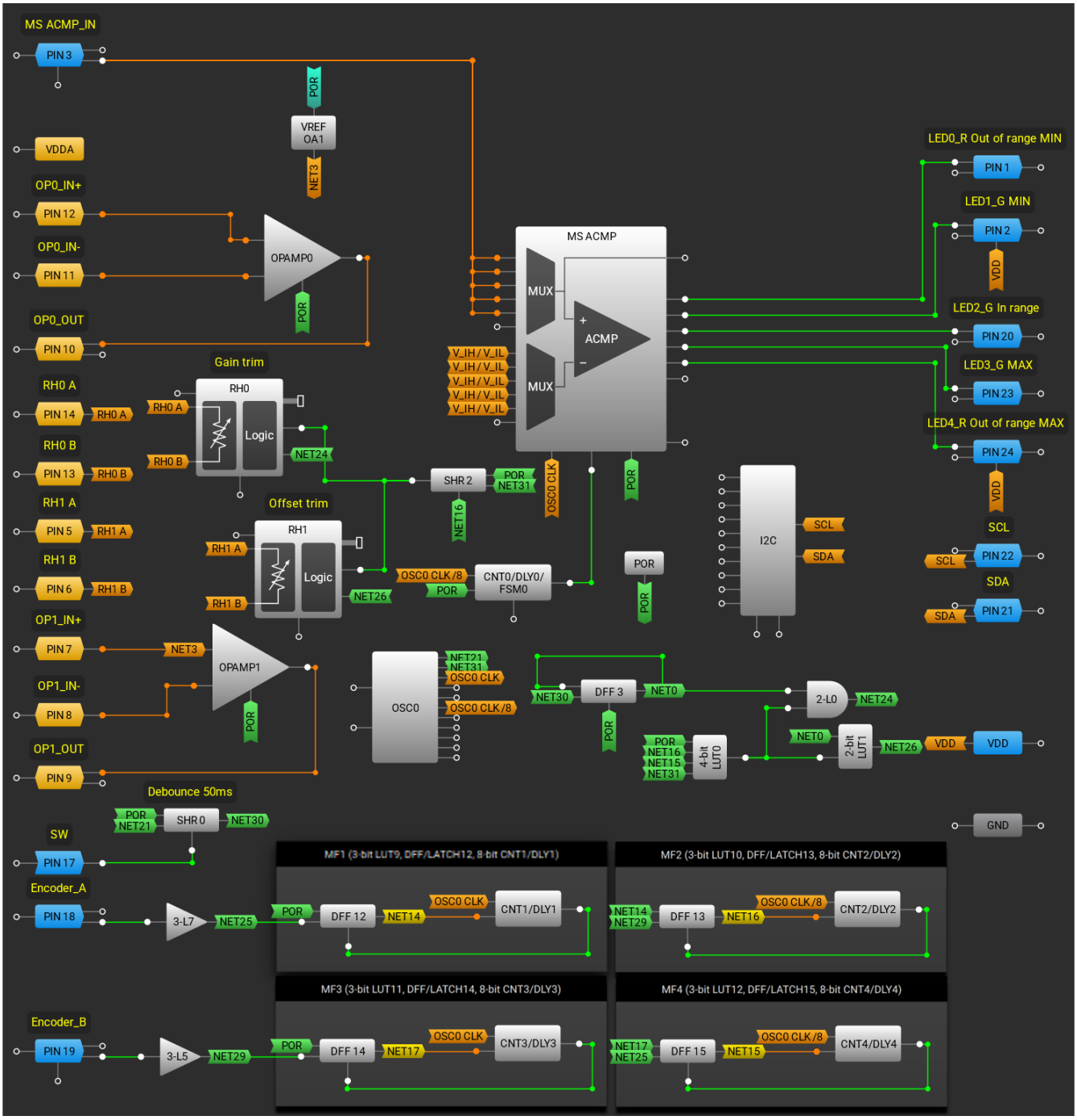


Figure 4. Go Configure Schematic of Offset and Gain Tuning

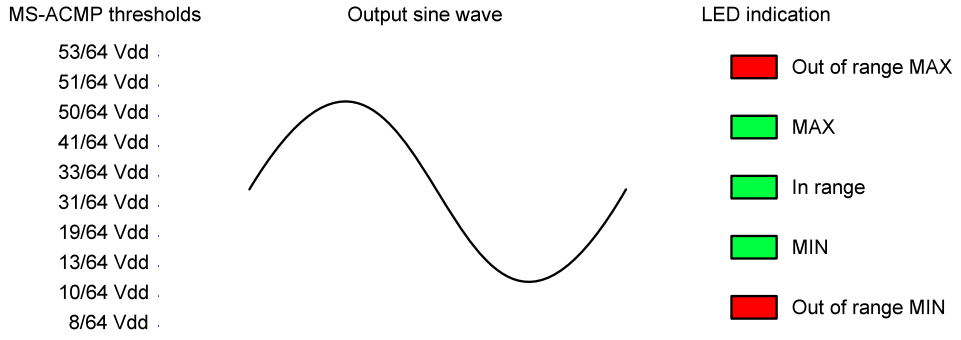


Figure 5. Output Signal Ranges Condition

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This design can be conventionally divided into the following functional parts (see Figure 4 and Figure 6):

- Signal Processing Channel

The signal processing channel includes OpAmp0, whose non-inverting input receives a sinusoidal input signal. Adjusting the resistance of rheostat RH0, connected in the negative feedback loop of OpAmp0, allows for changing the gain of OpAmp0 and adjusting the amplitude of its output sine wave.
Similarly, adjusting the resistance of rheostat RH1 in the negative feedback loop of OpAmp1 enables gain correction and allows for modifying the offset of the sinusoidal voltage at the input of the MS-ACMP.

- Devices and Means for Adjusting Gain and Offset

This part includes an encoder with a button, encoding logic with multifunctional macrocells MF1–MF4, and a set of logic elements for mode switching between gain and offset, as well as trimming gain or offset.

- Visualization Devices

To visualize the gain and offset trimming process, an MS-ACMP is used in multi-channel mode with five threshold voltages. The outputs of the MS-ACMP control the corresponding LEDs on the demo board (see Figure 4, Figure 5 and Figure 6). The encoder's button is used to switch between gain trim and offset trim modes.

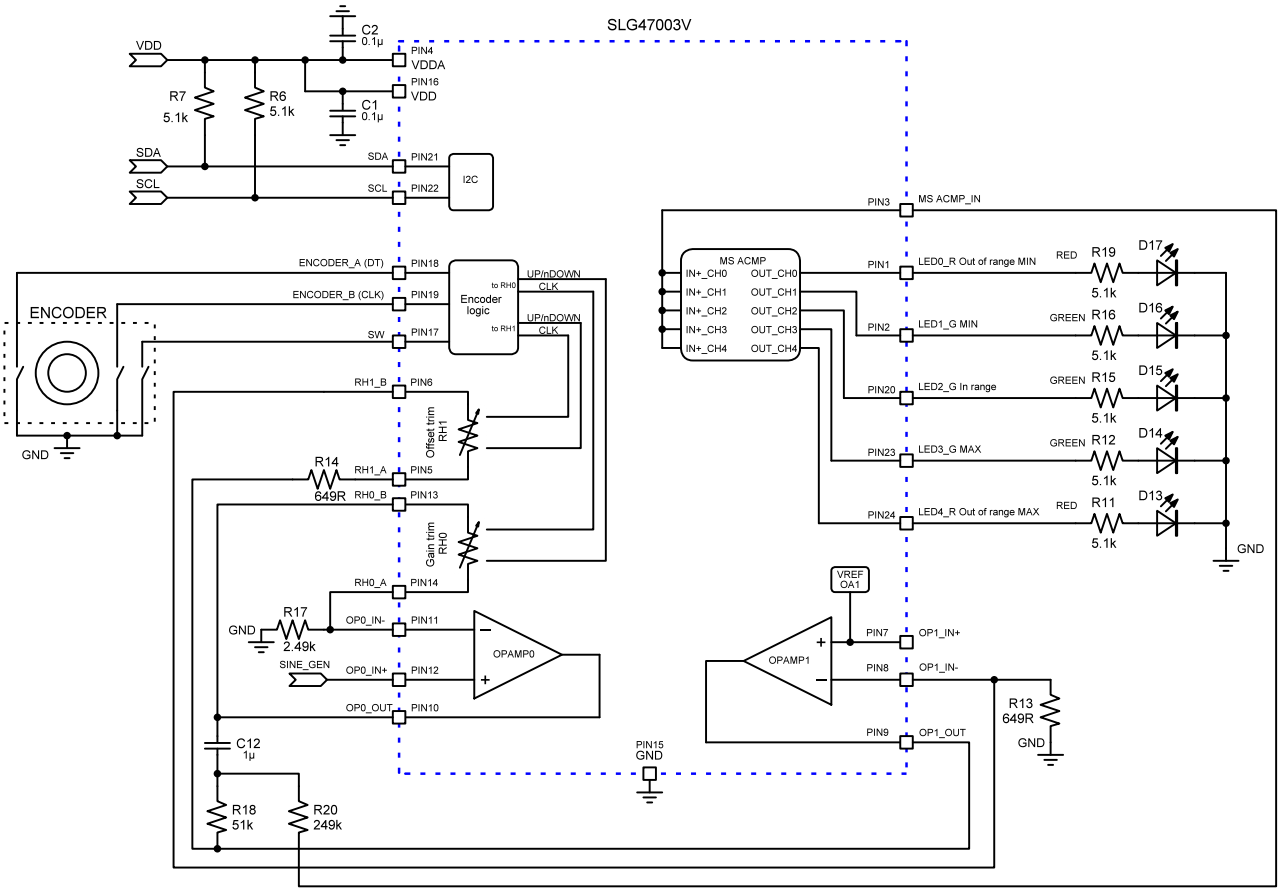


Figure 6. General Schematic of Offset and Gain Tuning

After the encoder is turned left or right, the power is on, and the encoder button is used to switch between gain and offset trim modes. The OpAmp0 output signal should be adjusted until all the green LEDs light up (see Figure 6). This indicates that the output sine wave is within the specified limits, as shown in Figure 5.

2.2 Addressable LED Control

The WS2812B is an addressable RGB LED that combines an RGB LED and an integrated driver in one package, enabling users to independently control the color and brightness of each LED. It also includes signal

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reshaping and amplification circuits, allowing each LED to transmit a signal received from a preceding LED. The WS2812B is controlled using a digital serial protocol and requires only one data line. Figure 7 illustrates the data transmission method.

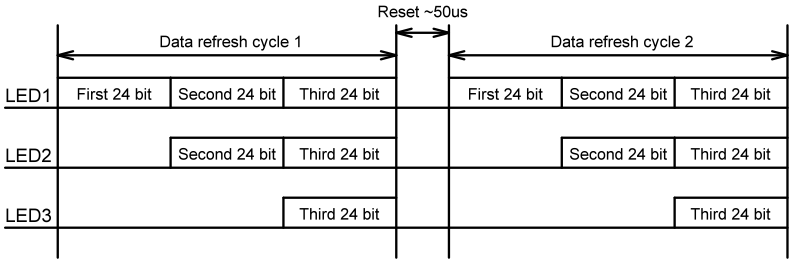


Figure 7. Timing Diagram of Data Transmission Method (Example for Strip of Three LED)

In this design, the SLG47003V is used to implement a visual effect of running 20 rainbow colors along the LED strip. Figure 8 shows a general schematic of the design.

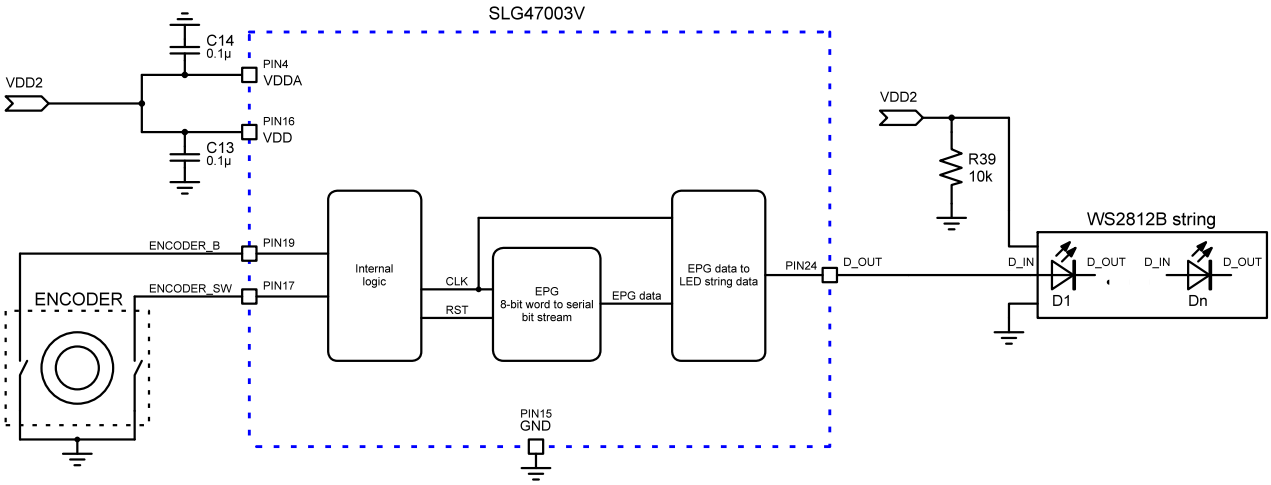


Figure 8. General Schematic of Addressable LED Control

2.2.1. Operating Principle

After the LED power-on reset, the DIN port receives data from GreenPAK SLG47003V. The first pixel collects the initial 24 bits of data and then sends the remaining data to an internal data latch. This data is then processed by the internal signal reshaping and amplification circuit and then sent to the next cascaded pixel through the DOUT port (Figure 9). When the low-level signal is held throughout the period > 50 µs, all the received data is latched and displayed by the LEDs.

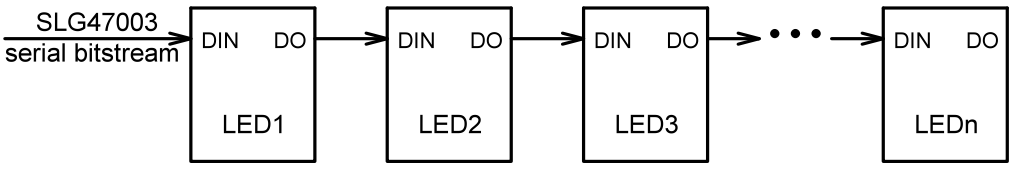


Figure 9. Example of LEDs Connection Cascade Method

To program the LEDs, a serial bitstream of logical 0s and 1s must be transformed into pulse width-modulated voltage levels (see Figure 10). The timings are described in Table 1.

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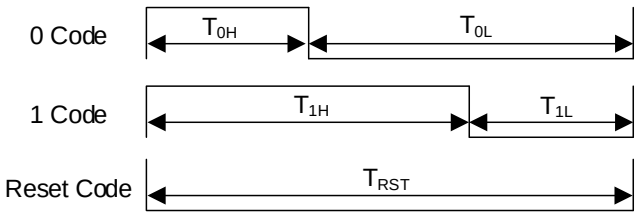


Figure 10. PWM Control Signal

$T_{0H} + T_{0L} = T_{1H} + T_{1L} = 1.25$ µs.

Table 1. Timing Intervals of 0 and 1 Coded Signals

Symbol	Parameter	Typical Value	Margin
T_{0H}	0 code, High Voltage Time	0.4 µs	±150 ns
T_{1H}	1 code, High Voltage Time	0.85 µs	±150 ns
T_{0L}	0 code, Low Voltage Time	0.85 µs	±150 ns
T_{1L}	1 code, Low Voltage Time	0.4 µs	±150 ns
RST	Low Voltage Time	Above 50 µs	--

Please note that the data for LED1 is sent by the SLG47003V, while LED2 and LED3 receive data through the internal reshaping amplification of the LEDs for transmission.
The 24-bit data segment contains information about the brightness of each of the three primary colors (red, green, and blue). Each primary color has 256 brightness levels (8-bit). The composition of the 24-bit data is shown in Figure 11.



Figure 11. Composition of 24-Bit Data

Note: Follow the GRB order when sending data, with the high bit sent first.

2.2.2. GreenPAK Design

An Extended Pattern Generator (EPG) is a key part of the design. The EPG range is 59 bytes, which are stored in the non-volatile memory (NVM). The EPG has a width converter and supports four conversion modes:

- 8-to-8 Mode (8-bit parallel output)
- 8-to-4 Mode (8-bit word to two 4-bit words)
- 8-to-2 Mode (8-bit word to four 2-bit words)
- 8-to-1 Mode (8-bit word to serial bit stream)

The EPG is used in the 8-bit word-to-serial bit stream mode in this design. This EPG mode and the flexible GreenPAK logic part allow for the easily create a serial bit stream of data to control the WS2812B LED strip.

To control the LED strip, it is necessary to generate 24-bit data fragments for each LED in the strip. Considering that the EPG has 59 bytes of dedicated NVM memory and one additional byte for the initial state, a total of 60*8 = 480 bits is available. This allows for storing 480/24 = 20 different colors in the SLG47003V chip. In this design, the EPG is programmed with 20 standard rainbow colors for demonstration (see Figure 13).

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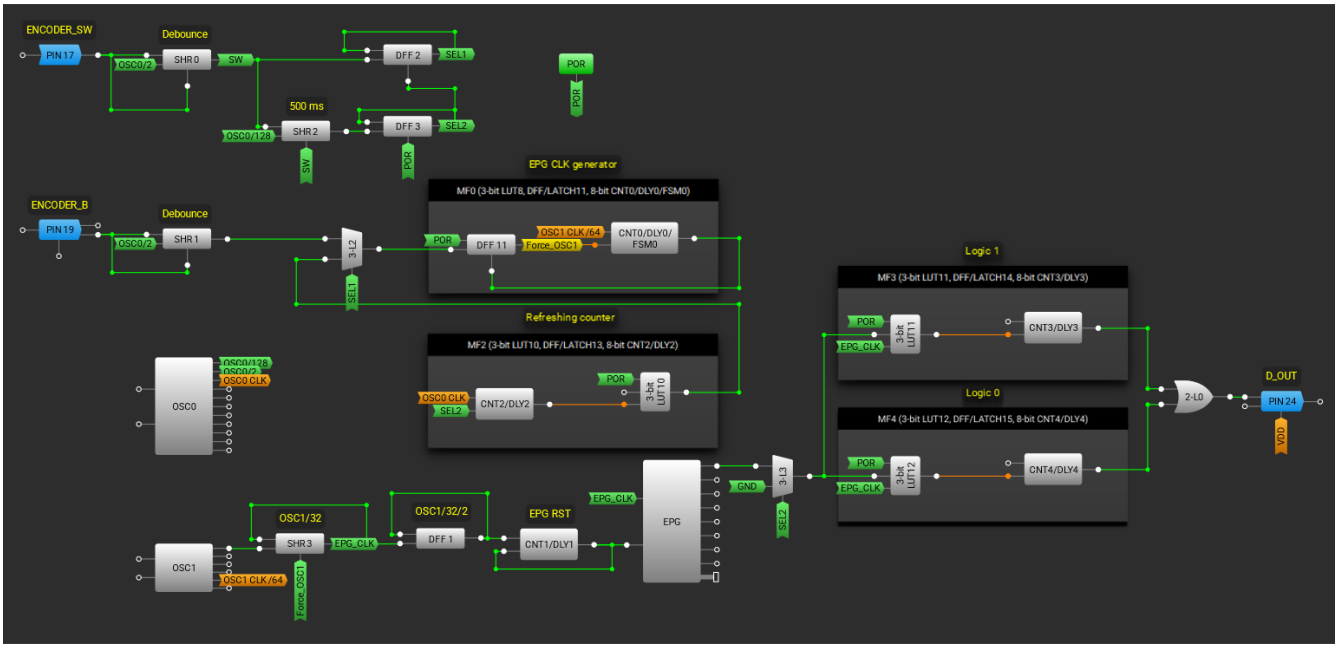


Figure 12. Go Configure Schematic of Addressable LED Control



Figure 13. Standard Rainbow (20 Colors), HEX Codes of Colors

To program the WS2812B LED strip, data from the EPG must be converted into a PWM signal with a fixed high-level time. For logic 1, the high-level lasts 0.85 µs, and for logic 0, it lasts 0.4 µs, with a PWM period of 1.25 µs. The timings are flexible and allow for some deviations.

The PWM converter consists of 3-bit LUT11 and DLY3 for encoding logical 1s, and 3-bit LUT12 and DLY4 for encoding logical 0s. Using the internal dividers of OSC1 and the shift register SHR3 as a divider by 4, an EPG_CLK signal with a frequency of about 780 kHz (1.28 µs period) is generated. This EPG_CLK signal serves as the clock source for both the EPG and the conversion of EPG data to the PWM signal. Each rising edge of the EPG_CLK signal outputs a new bit from the EPG to the input of the PWM converter, and the following falling edge triggers the corresponding One Shot (DLY3 or DLY4) to generate a PWM signal with the appropriate high-level time (logic 1 or 0).

As mentioned, there are 480 bits available for implementing 20 rainbow colors. To write all 20 colors to the LED strip, 480 pulses are needed on the EPG's CLK input. If 480 pulses are sent for each cycle, each LED on the

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strip will display one specific color from the set of 20. To create the effect of running colors, 24 extra pulses are sent during each cycle. The EPG CLK generator, composed of DLY0 and DFF11, provides 504 pulses to the EPG CLK input. Each rising edge from MUX 3-L2 triggers the EPG CLK generator, sending this group of pulses and rewriting the LEDs on the strip.

DLY1 resets the EPG after each 480-bit sequence. This reset is necessary to reuse the initial byte of the EPG during each rewriting cycle, as it's only available after an EPG reset.

The design is controlled by an encoder, with shift registers SHR0 and SHR1 handling the debounce function. The encoder controls a state machine composed of DFF2 and DFF3, which manages MUX 3-L2, MUX 3-L3, and counter CNT2.

A long press on the encoder button (more than 500 ms) turns the LED strip on or off. The 500 ms delay is provided by shift register SHR2. A short press on the encoder button selects the trigger source for the EPG CLK generator between CNT2 and ENCODER_B. When CNT2 is selected, the EPG CLK generator is continuously triggered by each period of CNT2, creating the running color effect. When ENCODER_B is selected, the rewriting cycle of the LED strip can be started manually. In this mode, each pulse from the encoder shifts the LED strip by one color. To turn off the LED strip, MUX 3-L3 writes a zero code to all LEDs.

2.3 Tunable Voltage Regulator

The voltage regulator demonstrates the operation of the SLG47003V as a tunable voltage regulator with voltage control via an encoder (see Figure 14 with the general schematic).

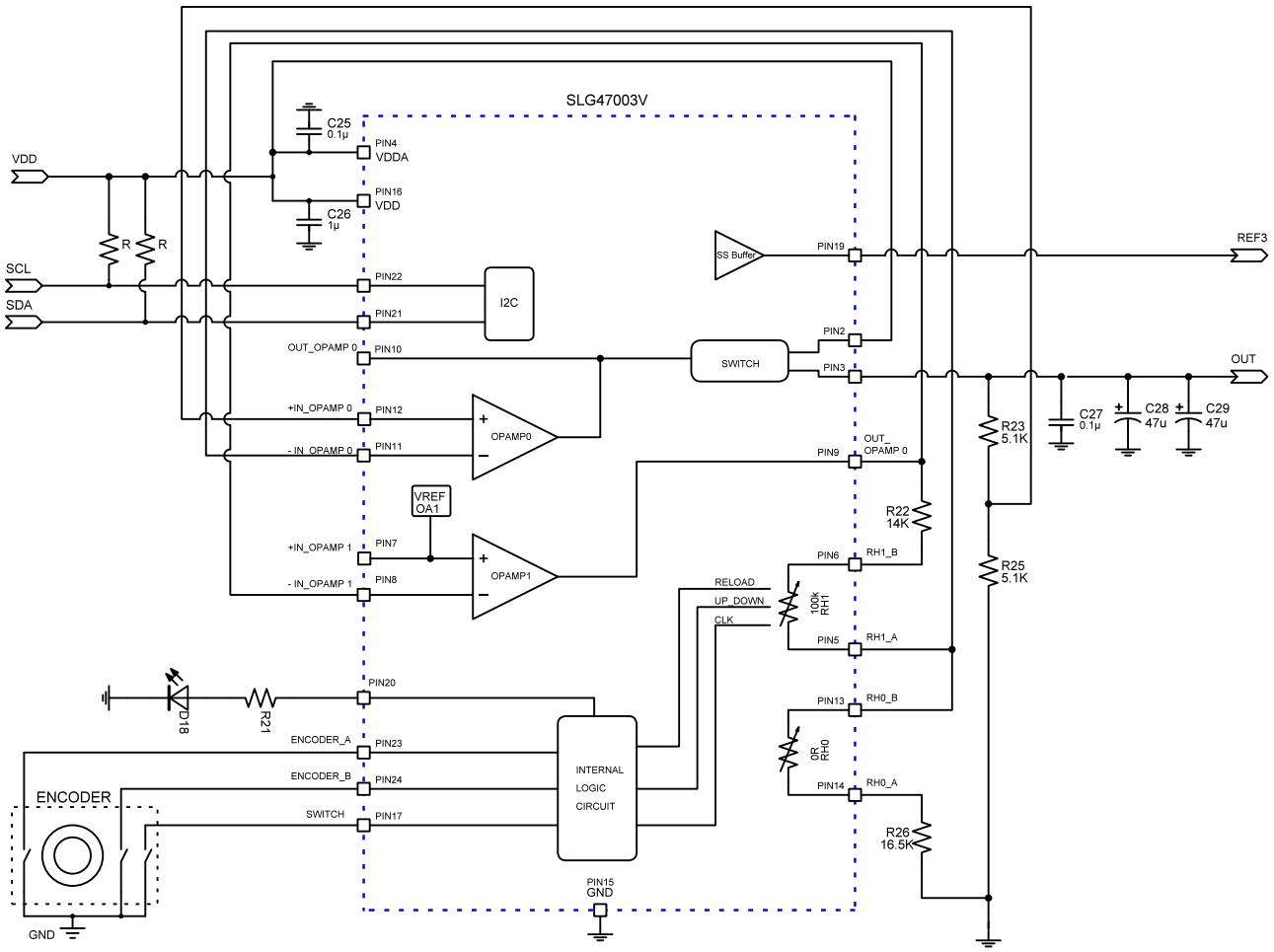


Figure 14. General Schematic of Tunable Voltage Regulator Based on SLG47003V

The design allows adjustment of the output voltage of the voltage regulator within a range from 0.5 V to 3.6 V, with a maximum current of 100 mA supplied to the load. The clockwise rotation of the encoder increases the

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output voltage, while counterclockwise rotation decreases it. A short press of the encoder button changes the voltage adjustment step between 0.006 V and 0.06 V. The D18 LED indicator shows the selected step: when the indicator is ON, the step is 0.06 V; when OFF, the step is 0.006 V. A long press (more than 1 s) of the encoder button reduces the output voltage to the minimum value of 0.5 V.

Figure 15 shows an internal design of the tunable voltage regulator in the Go Configure software.

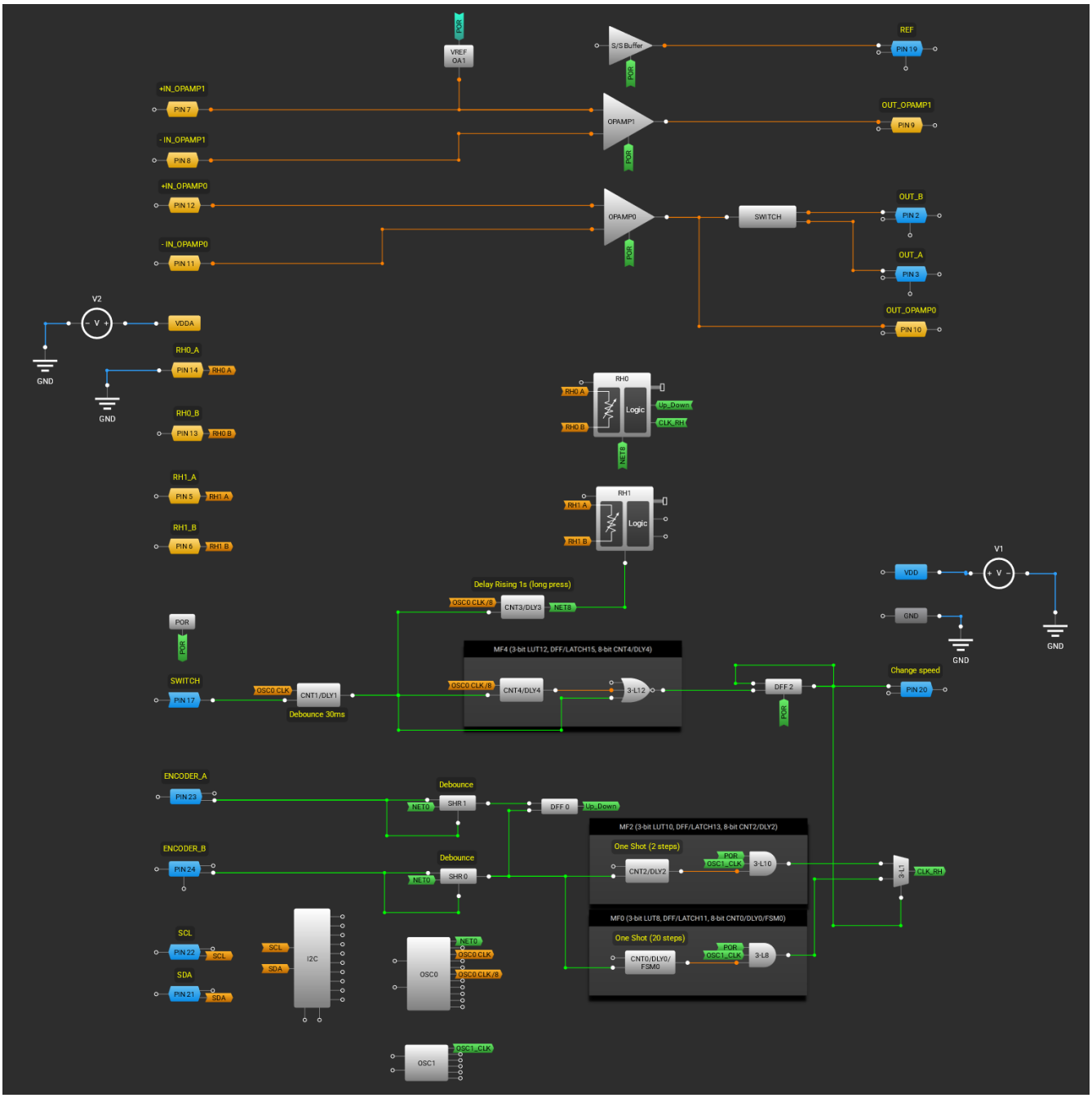


Figure 15. Go Configure Schematic of Tunable Voltage Regulator

The design includes the following basic components:

- Two OpAmps
- Vref
- Sink/Source (S/S) Buffer
- Analog switch
- Two Digital Rheostats

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- Logic elements (LUTs, Delays, DFFs)

The tunable voltage regulator follows a typical OpAmp-based design. In this configuration, the OpAmp0 compares the output voltage, divided by a resistor network consisting of R23 and R25, with a stable reference voltage (Vref) divided by the digital potentiometers RH0, RH1, and controls the analog switch accordingly. By opening or closing the switch based on the output voltage and the current drawn by the load, the circuit maintains a stable output voltage.

Resistors R22 and R26 set the output voltage adjustment range from 0.5 V to 3.6 V. By opening or closing the analog switch depending on the regulator's output voltage and the current drawn by the load, the circuit maintains a stable output voltage.

To adjust the voltage supported by the regulator, change the division ratio of the divider, which includes digital potentiometers RH0 and RH1, and resistors R22 and R26. This adjustment involves altering the resistance of the digital potentiometer.

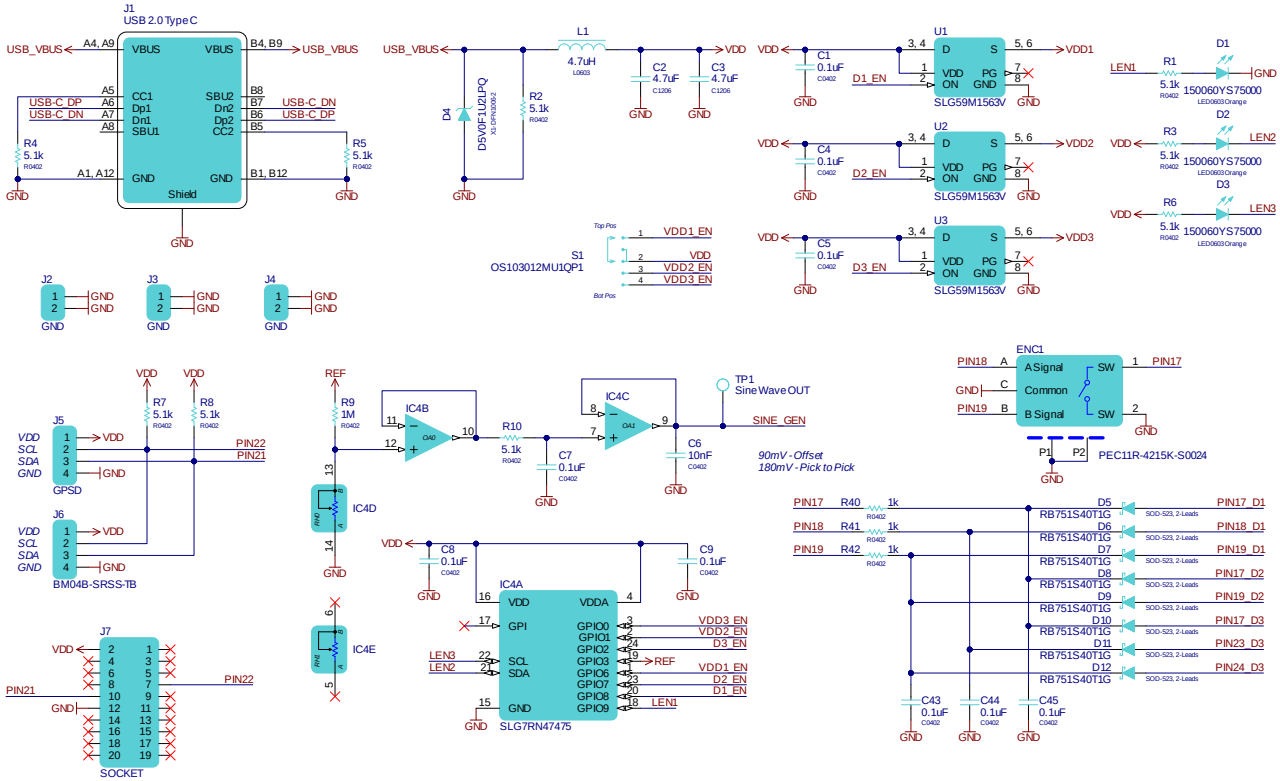
OpAmp1 and Vref OA1 function as a stable voltage source for the voltage regulator. OpAmp1 is configured as a typical voltage follower. The S/S Buffer is used to generate the reference voltage for the built-in voltmeter.

The design offers two ways to control the digital rheostat: through I²C or via an encoder. In I²C mode, the values in the digital rheostat's registers are rewritten using I²C commands.

Control via the encoder is managed by a circuit based on logic elements. CNT1/DLY1 and Shift Registers 0 and 1 handle debounce suppression for both the encoder button and the encoder contacts. The DFF0 element determines the encoder's rotation direction, while a long press of the encoder button is detected by CNT3/DLY3. CNT4/DLY4 and 3-bit LUT12 separate short and long presses. The elements DFF2, CNT2/DLY2, 2-bit LUT1, and 3-bit LUT10 form a circuit that switches the voltage adjustment step at the regulator's output.

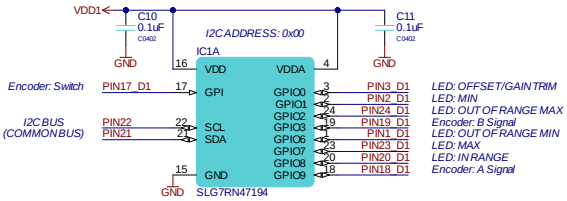
2.4 Schematics

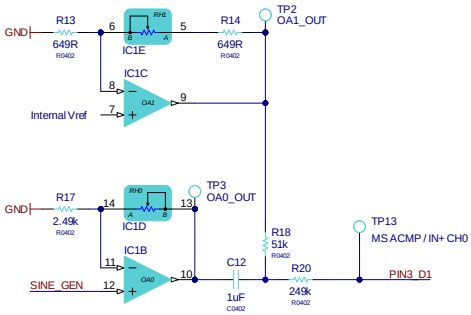
2.4.1. Main

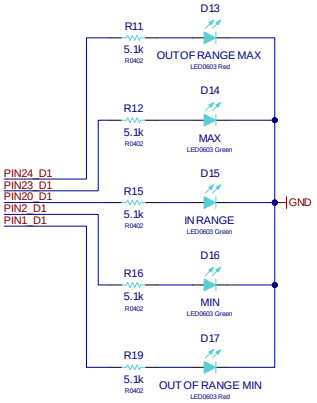


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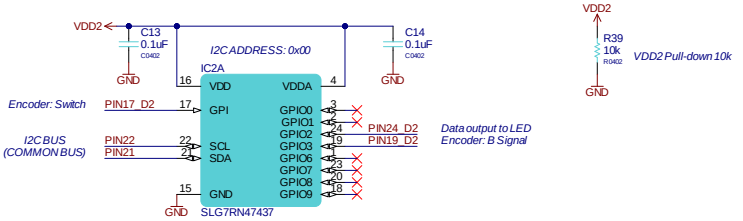
2.4.2. Offset and Gain Tuning

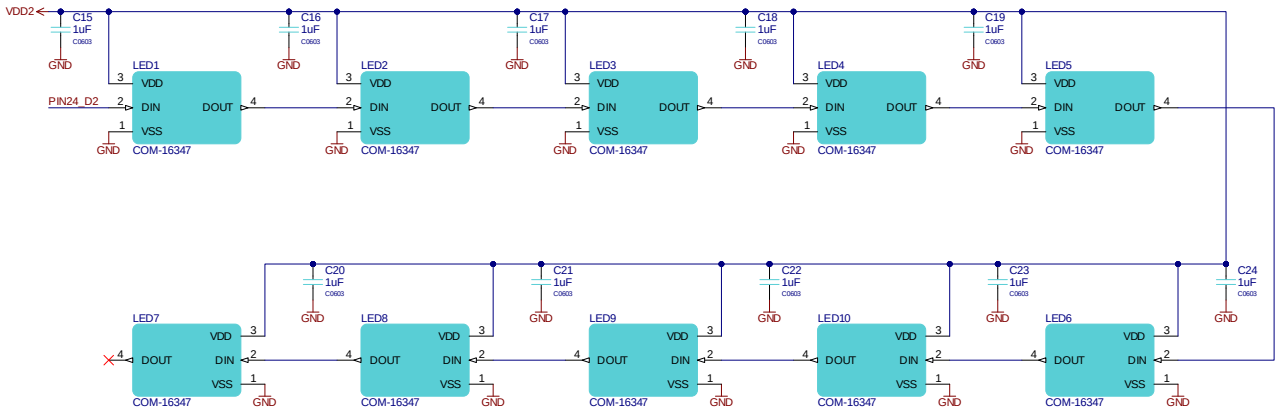






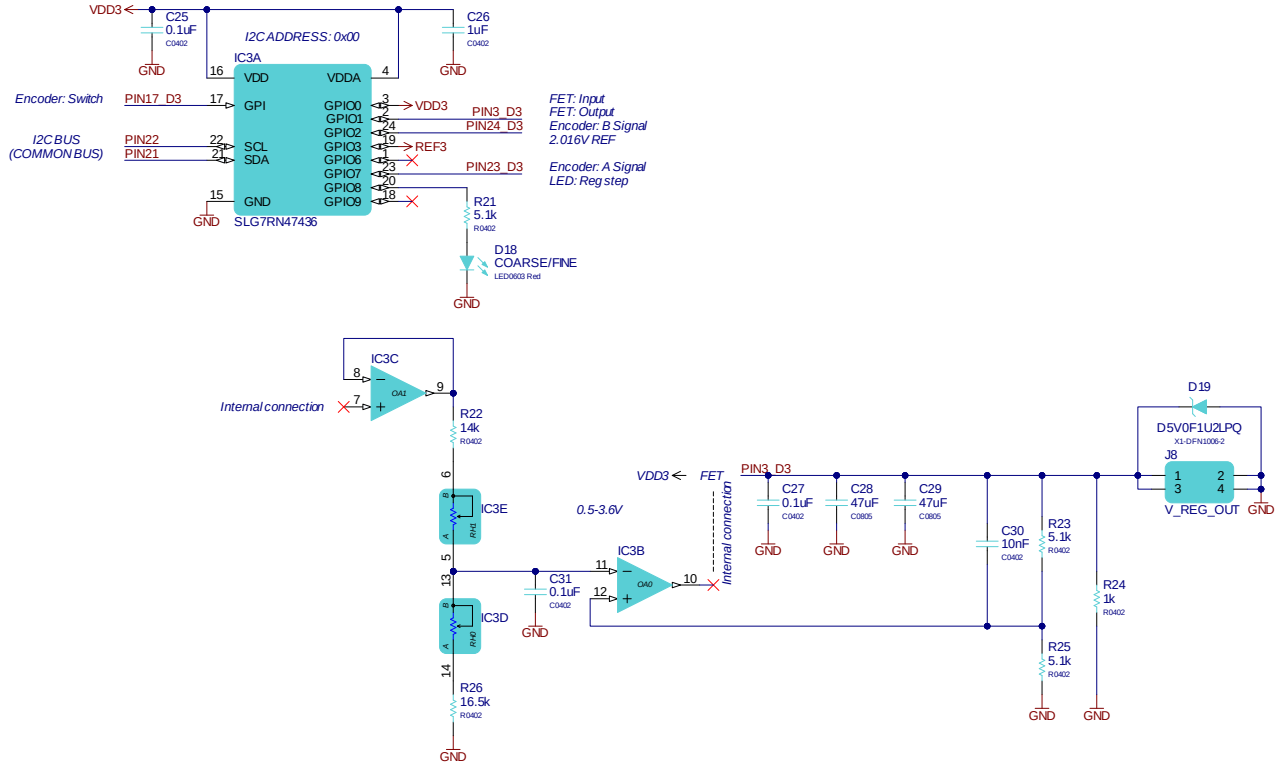
2.4.3. Addressable LED Control



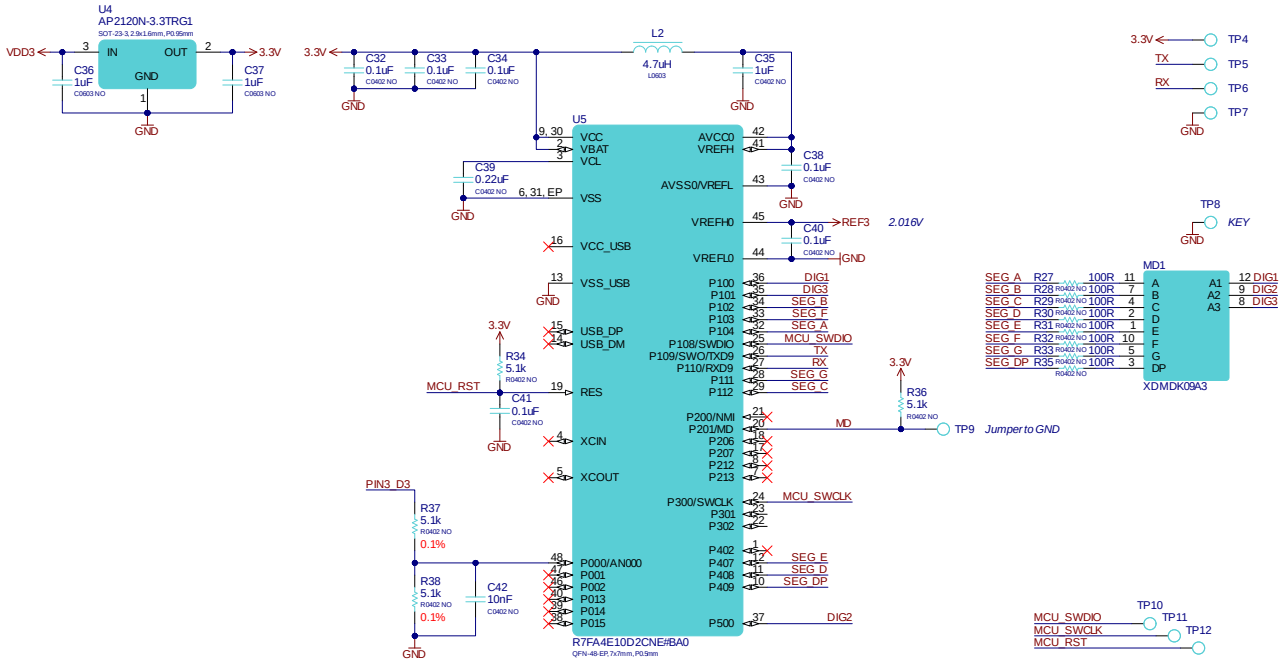


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2.4.4. Tunable Voltage Regulator



2.4.5. Voltmeter



2.5 BOM

#	Designator	Name	Manufacturer Part Number 1	Manufacturer 1	Supplier Part Number 1	Supplier 1	Qty	Footprint
1	BP1, BP2, BP3, BP4	SJ61A6	7010334512	3M	SJ61A6-ND	Digikey	4	Bumper

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#	Designator	Name	Manufacturer Part Number 1	Manufacturer 1	Supplier Part Number 1	Supplier 1	Qty	Footprint
2	C1, C4, C5, C7, C8, C9, C10, C11, C13, C14, C25, C27, C31, C32, C33, C34, C38, C40, C41, C43, C44, C45	0.1 µF 10% 50V X7R 0402	CL05B104KB5NNNC	Samsung	1276-CL05B104KB5NNNCCT-ND	Digikey	22	C040, C0402 NO
3	C2	4.7 µF 10% 16V X7R 1206	CL31B475KOHVPNE	Samsung Electro-Mechanics	1276-6723-1-ND	Digikey	1	C1206
4	C6, C30, C42	10 nF 10% 50V X7R 0402	CL05B103KB5NNNC	Samsung Electro-Mechanics	1276-1028-1-ND	Digikey	3	C040, C0402 NO
5	C12, C26, C35	1 µF 20% 25V X5R 0402	GRM155R61E105MA12D	Murata	490-10018-1-ND	Digikey	3	C040, C0402 NO
6	C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C36, C37	1 µF 20% 16V X7R 0603	CL10B105MO8NNWC	Samsung	1276-6524-1-ND	Digikey	12	C060, C0603 NO
7	C28	47 µF 20% 10V X5R 0805	GRM21BR61A476ME15L	Murata Electronics	490-9961-1-ND	Digikey	1	C0805
8	C39	0.22 µF 10% 10V X5R 0402	CL05A224KP5NNNC	Samsung	1276-1049-1-ND	Digikey	1	C0402 NO
9	D1, D2, D3	150060YS75000	150060YS75000	Wurth Electronics	732-4981-1-ND	Digikey	3	LED0603 Orange
10	D4, D19	D5V0F1U2LPQ-7B	D5V0F1U2LPQ-7B	Diodes	31-D5V0F1U2LPQ-7BCT-ND	Digikey	2	X1-DFN1006-2
11	D5, D6, D7, D8, D9, D10, D11, D12	RB751S40T1G	RB751S40T1G	ON Semiconductor	RB751S40T1GOSCT-ND	Digikey	8	SOD-523, 2-Leads
12	D13, D17, D18	150060RS75000	150060RS75000	Wurth Electronics	732-4978-1-ND	Digikey	3	LED0603 Red
13	D14, D15, D16	150060GS75000	150060GS75000	Würth Elektronik	732-4971-1-ND	Digikey	3	LED0603 Green
14	ENC1	PEC11R-4215K-S0024	PEC11R-4215K-S0024	Bourns	PEC11R-4215K-S0024-ND	Digikey	1	FP-PEC11R-4215K-S0024
15	IC1	SLG7RN47194	SLG7RN47194	Renesas	SLG7RN47194	Renesas	1	SLG47003V
16	IC2	SLG7RN47437	SLG7RN47437	Renesas	SLG7RN47437	Renesas	1	SLG47003V
17	IC3	SLG7RN47436	SLG7RN47436	Renesas	SLG7RN47436	Renesas	1	SLG47003V
18	IC4	SLG7RN47475	SLG7RN47475	Renesas	SLG7RN47475	Renesas	1	SLG47003V
19	J1	USB4105-GF-A	USB4105-GF-A	Global Connector Technology	2073-USB4105-GF-ACT-ND	Digikey	1	USB 2.0, Type C, Horizontal
20	J2, J3, J4	PREC002SAAN-RC	PREC040SAAN-RC	Sullins	S1012EC-02-ND	Digikey	3	CON: M, 2-pin, 1x2, P2.54

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#	Designator	Name	Manufacturer Part Number 1	Manufacturer 1	Supplier Part Number 1	Supplier 1	Qty	Footprint
21	J5	PREC004SAAN-RC	PREC040SAAN-RC	Sullins	S1012EC-04-ND	Digikey	1	CON: M, 4-pin, 1x4, P2.54
22	J6	BM04B-SRSS-TB	BM04B-SRSS-TB	JST	455-BM04B-SRSS-TBCT-ND	Digikey	1	SH SMD Header, V, 4-pins
23	J7	PPPC102LJBN-RC	PPPC102LJBN-RC	Sullins	S5563-ND	Digikey	1	CON: F, 20-pin, 2x10, R, P2.54
24	J8	PREC002DAAN-RC	PREC040DAAN-RC	Sullins	S2012EC-02-ND	Digikey	1	CON: M, 4-pin, 2x2, P2.54
25	L1, L2	4.7uH 620mA	LQM18PN4R7MFRL	Murata	490-12065-1-ND	Digikey	2	L0603
26	LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10	COM-16347	COM-16347	SparkFun	1568-COM-16347CT-ND	Digikey	10	ADA-RGB-1655_V
27	MD1	XDMDK09A3	XDMDK09A3	SunLED	1497-XDMDK09A3-ND	Digikey	1	LED: XDMDK09A3
28	R1, R2, R3, R4, R5, R6, R7, R8, R10, R11, R12, R15, R16, R19, R21, R23, R25, R34, R36	5.1k 1% 0402	RC0402FR-135K1L	Yageo	13-RC0402FR-135K1LCT-ND	Digikey	19	R040, R0402 NO
29	R9	1M 1% 0402	RC0402FR-071ML	Yageo	311-1.00MLRCT-ND	Digikey	1	R0402
30	R13, R14	649R 1% 0402	RC0402FR-07649RL	Yageo	YAG3206CT-ND	Digikey	2	R0402
31	R17	2.49k 1% 0402	RC0402FR-072K49L	Yageo	311-2.49KLRCT-ND	Digikey	1	R0402
32	R18	51k 1% 0402	RC0402FR-0751KL	Yageo	311-51.0KLRCT-ND	Digikey	1	R0402
33	R20	249k 1% 0402	RC0402FR-07249KL	Yageo	311-249KLRCT-ND	Digikey	1	R0402
34	R22	14k 1% 0402	RC0402FR-0714KL	Yageo	311-14.0KLRCT-ND	Digikey	1	R0402
35	R24, R40, R41, R42	1k 1% 0402	RC0603FR-071KL	Yageo	311-1.00KHRCT-ND	Digikey	4	R0402
36	R26	16.5k 1% 0402	RC0402FR-1316K5L	Yageo	13-RC0402FR-1316K5LCT-ND	Digikey	1	R0402
37	R27, R28, R29, R30, R31, R32, R33, R35	100R 1% 0402	RC0402FR-07100RL	Yageo	311-100LRCT-ND	Digikey	8	R0402 NO
38	R37, R38	5.1k 0.1% 0402	RT0402BRE075K1L	Yageo	YAG4404CT-ND	Digikey	2	R0402 NO

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#	Designator	Name	Manufac-turer Part Number 1	Manufac-turer 1	Supplier Part Number 1	Sup-plier 1	Q-ty	Footprint
39	R39	10k 1% 0402	RC0402FR-0710KL	Yageo	311-10.0KLRCT-ND	Digikey	1	R0402
40	S1	OS103012MU1QP1	OS103012MU1QP1	ITT C&K	CKN9552-ND	Digikey	1	SW: Slide 1P3T, OS103012MU1QP1
41	TP1, TP2, TP13	5002	5002	Keystone Electronics	36-5002-ND	Digikey	3	TP: White
42	U1, U2, U3	SLG59M1563V	SLG59M1563V	Renesas	SLG59M1563V	Renesas	3	SLG59M1563V
43	U4	AP2120N-3.3TRG1	AP2120N-3.3TRG1	Diodes	AP2120N-3.3TRG1DICT-ND	Digikey	1	SOT-23-3, 2.9x1.6mm, P0.95mm
44	U5	R7FA4E10D2CNE#BA0	R7FA4E10D2CNE#BA0	Renesas	R7FA4E10D2CNE#BA0	Renesas	1	QFN-48-EP, 7x7mm, P0.5mm

3. Ordering Information

Part Number	Description
SLG47003V-DMO	The SLG47003V Demo Board is designed to demonstrate the basic capabilities of this integrated circuit. Three designs are implemented on the board, namely an offset and gain tuning, an addressable LED control, and a tunable voltage regulator.

4. Revision History

Revision	Date	Description
1.01	Nov 5, 2024	Updated Figures and design description
1.00	Oct 14, 2024	Initial release.

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