SRC0

Smart push-button on/off controller with Smart Reset™ and power-on lockout

Datasheet - production data

TDFN12

Features

- Operating voltage 1.6 V to 5.5 V
- Low standby current of 0.6 µA
- Adjustable Smart Reset™ assertion delay time driven by external C_{SRD}
- Power-up duration determined primarily by push-button press
- Debounced $\overline{PB}$ and $\overline{SR}$ inputs
- $\overline{PB}$ and $\overline{SR}$ ESD inputs withstand voltage up to ±15 kV (air discharge) ±8 kV (contact discharge)
- Active high or active low enable output option ($\overline{EN}$ or EN) provides control of MOSFET, DC-DC converter, regulator, etc.
- Secure startup, interrupt, Smart Reset™ or power-down driven by push-button
- Precise 1.5 V voltage reference with 1% accuracy
- Industrial operating temperature -40 to +85 °C
- Available in TDFN12 2 x 3 mm package

Applications

- Wearable
- Activity tracker
- Smartwatch
- Smartglasses

Table 1. Device summary

Device	$\overline{RST}$	C_{SRD}	$\overline{PB}$ / $\overline{SR}$	EN or $\overline{EN}$	$\overline{INT}$	Startup process
SRC0	open drain(1)	3	3	push-pull	open drain(1)	$\overline{PB}$ must be held low until the PS_{HOLD}(2) confirmation

1. External pull-up resistor needs to be connected to open drain outputs.
2. For a successful startup, the PS_{HOLD} (Power Supply Hold) needs to be pulled high within specific time, t_{ON_BLANK}.

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1 Description

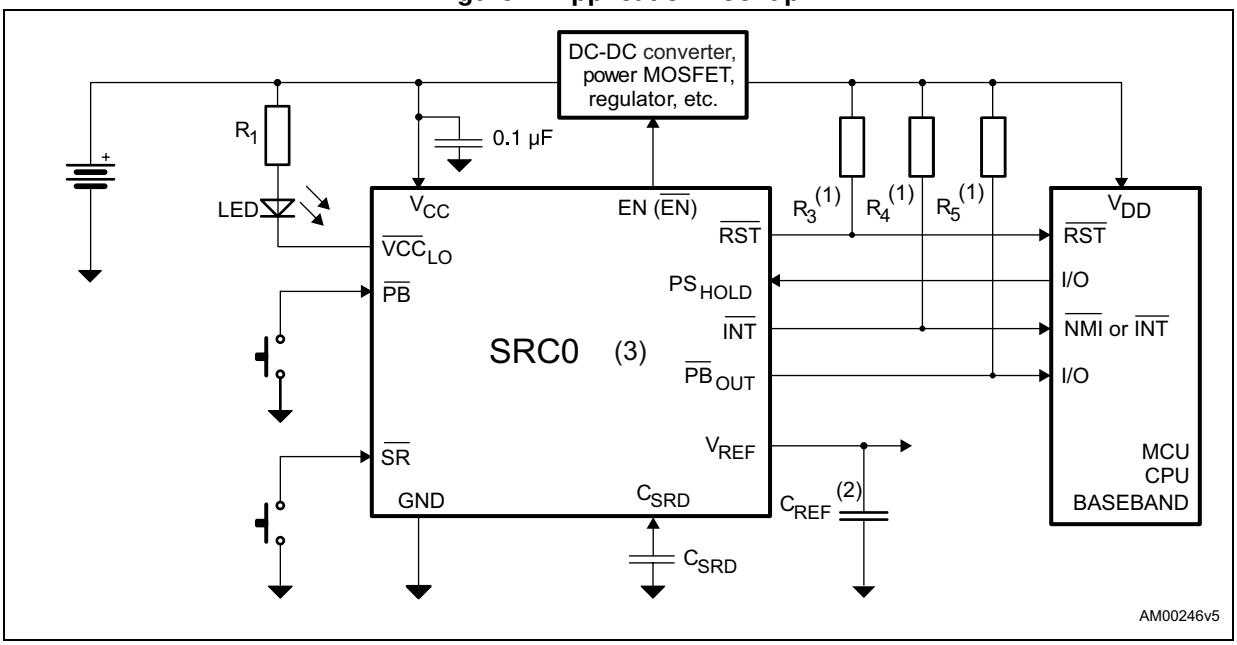
The SRC0 devices monitor the state of connected push-button(s) as well as sufficient supply voltage. An enable output controls power for the application through the MOSFET transistor, DC-DC converter, regulator, etc. If the supply voltage is above a precise voltage threshold, the enable output can be asserted by a simple press of the button. Factory-selectable supply voltage thresholds are determined by highly accurate and temperature-compensated references. An interrupt is asserted by pressing the push-button during normal operation and can be used to request a system power-down. The interrupt is also asserted if undervoltage is detected. By a long push of one button ($\overline{PB}$) or two buttons ($\overline{PB}$ and $\overline{SR}$) either a reset is asserted or power for the application is disabled depending on the option used.

The device also offers additional features such as precise 1.5 V voltage reference with very tight accuracy of 1%, separate output indicating undervoltage detection and separate output for distinguishing between interrupt by push-button or undervoltage.

The device consumes very low current of 6 µA during normal operation and only 0.6 µA current during standby.

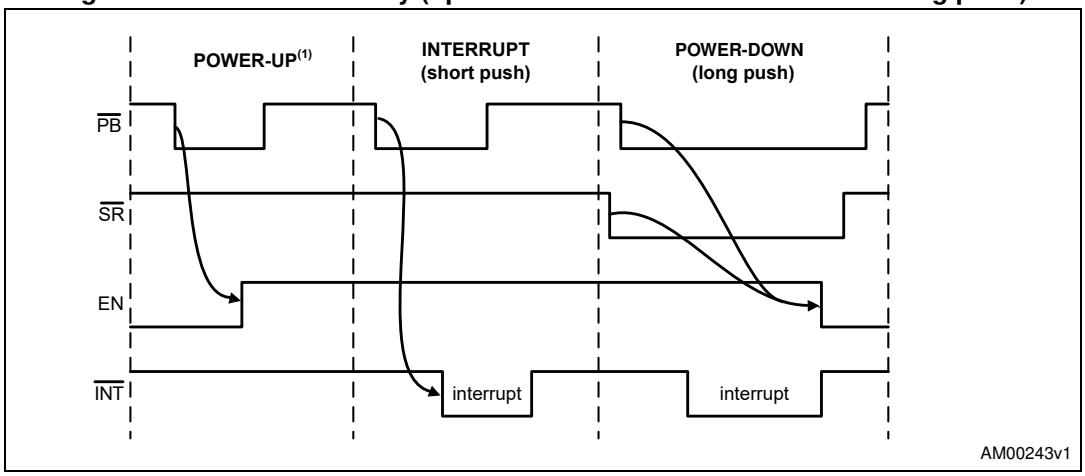
The SRC0 is available in the TDFN12 package and is offered in several options among features such as selectable threshold, hysteresis, timeouts, output types, etc.

Figure 1. Application hookup



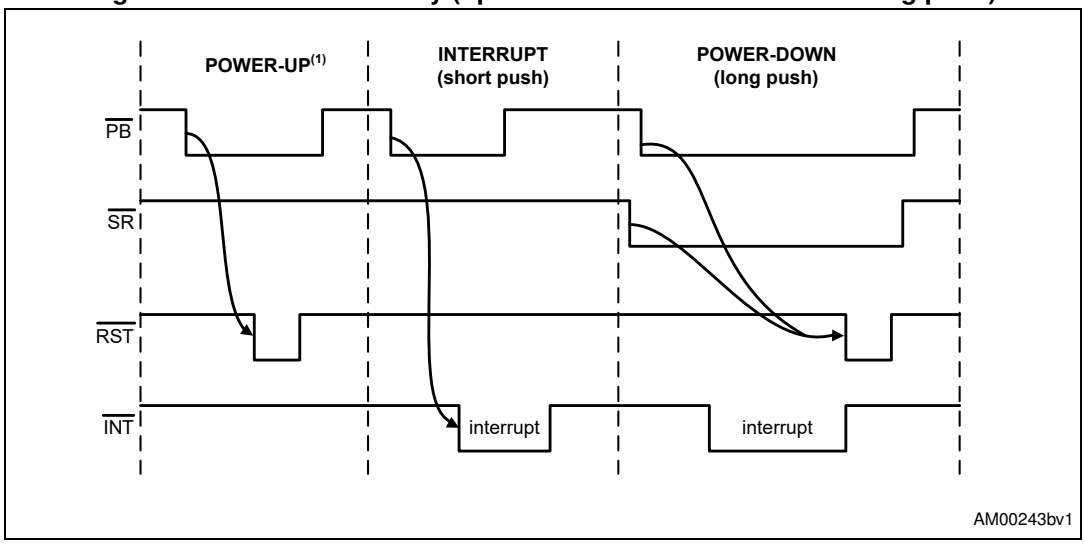
1. A resistor is required for open drain output type only. A 10 kΩ pull-up is sufficient in most applications.
2. Capacitor C_{REF} is mandatory on V_{REF} output (even if V_{REF} is not used). Capacitor value of 1 µF is recommended.
3. For the SRC0 the processor has to confirm the proper power-on during the fixed time period, t_{ON_BLANK}. This failsafe feature prevents the user from turning on the system when there is a faulty power switch or an unresponsive microprocessor.

Figure 2. Basic functionality (option with enable deassertion after long push)



1. For power-up the battery voltage has to be above V_{TH+} threshold.

Figure 3. Basic functionality (option with $\overline{RST}$ assertion after long push)



1. For power-up the battery voltage has to be above V_{TH+} threshold.

Figure 4. Logic diagram

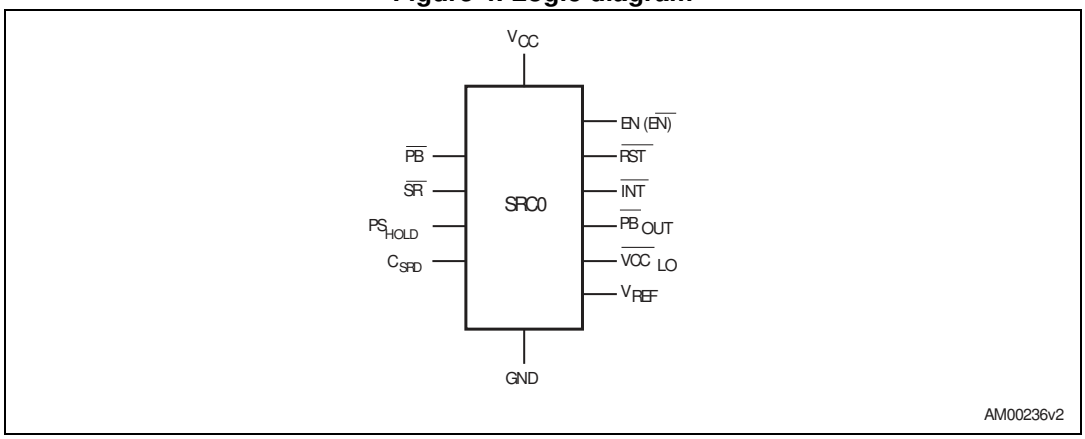


Table 2. Pin descriptions

Pin n°	Symbol	Function
1	V_{CC}	Power supply input
2	$\overline{SR}$	Smart Reset™ button input
3	V_{REF}	Precise 1.5 V voltage reference
4	PS_{HOLD}	PS_{HOLD} input
5	C_{SRD}	Adjustable Smart Reset™ delay time input
6	$\overline{PB}$	Push-button input
7	$\overline{VCC}_{LO}$	Output for high threshold comparator output (V_{TH+})
8	PB_{OUT}	Status of $\overline{PB}$ push-button input
9	EN or $\overline{EN}$	Enable output
10	RST	Reset output
11	INT	Interrupt output
12	GND	Ground

Figure 5. TDFN12 pin connections

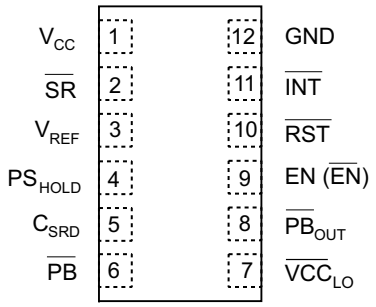
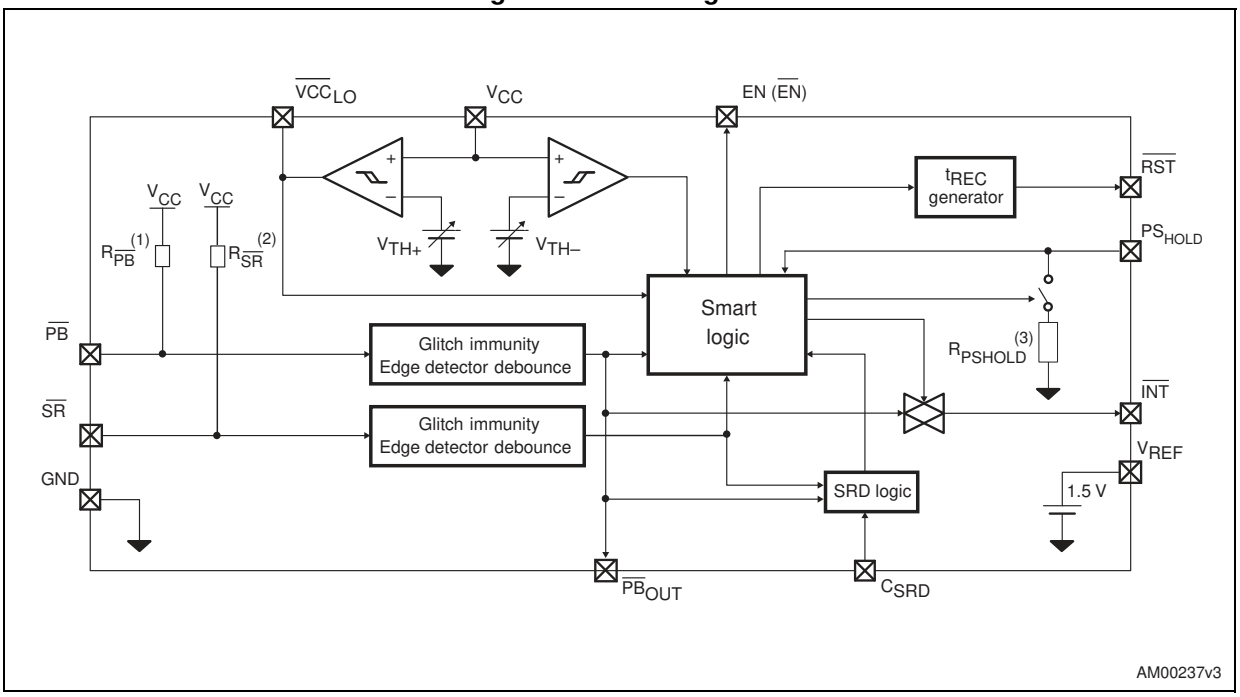


Figure 6. Block diagram



1. Internal pull-up resistor connected to $\overline{PB}$ input (see *Table 5* for precise specifications).
2. Optional internal pull-up resistor connected to $\overline{SR}$ input (see *Table 5* for precise specifications).
3. Internal pull-down resistor is connected to PS_{HOLD} input only during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).

2 Pin descriptions

V_{CC} - power supply input

V_{CC} is monitored during startup and normal operation for sufficient voltage level. Decouple the V_{CC} pin from ground by placing a 0.1 µF capacitor as close to the device as possible.

$\overline{SR}$ - Smart Reset™ button input

This input is equipped with voltage detector with a factory-trimmed threshold and has ±8 kV HBM ESD protection.

Both $\overline{PB}$ and $\overline{SR}$ buttons have to be pressed and held for t_{SRD} period so the long push is recognized and the reset is asserted (or the enable output is deasserted depending on the option) - see *Figure 13*, *14*, and *15*.

Active low $\overline{SR}$ input is usually connected to GND through the momentary push-button (see *Figure 1*) and it has an optional 100 kΩ pull-up resistor. It is also possible to drive this input using an external device with either open drain (recommended) or push-pull output. Open drain output can be connected in parallel with push-button or other open drain outputs, which is not possible with push-pull output. $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently.

V_{REF} - external precise 1.5 V voltage reference

This 1.5 V voltage reference is specified with very tight accuracy of 1% (see *Table 5*). It has proper output voltage as soon as the reset output is deasserted (i.e. after t_{REC} expires) and it is disabled when the device enters standby mode. A mandatory capacitor needs to be connected to V_{REF} output (even if V_{REF} is not used). Capacitor value of 1 µF is recommended.

PS_{HOLD} input

This input is equipped with a voltage detector with a factory-trimmed threshold. It is used to confirm correct power-up of the device (if EN or $\overline{EN}$ is not asserted) or to initiate a shutdown (if EN or $\overline{EN}$ is asserted).

Forcing PS_{HOLD} high during power-up confirms the proper start of the application and keeps enable output asserted. Because most processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS_{HOLD} input during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).

Forcing the PS_{HOLD} signal low during normal operation deasserts the enable output (see *Figure 12*). Input voltage on this pin is compared to an accurate voltage reference.

C_{SRD} - Smart Reset™ delay time input

A capacitor to ground determines the additional time (t_{SRD}) that $\overline{PB}$ with $\overline{SR}$ must be pressed and held before a long push is recognized. The connected C_{SRD} capacitor is charged with I_{SRD} current. Additional Smart Reset™ delay time t_{SRD} ends when voltage on the C_{SRD} capacitor reaches the V_{SRD} voltage threshold. It is recommended to use a low ESR capacitor (e.g. ceramic). If the capacitor is not used, leave the C_{SRD} pin open. If no capacitor is connected, there is no t_{SRD} and a long push is recognized right after $t_{\overline{INT}\_Min}$ expires (see *Figure 18* and *19*).

$\overline{PB}$ - power ON switch

This input is equipped with a voltage detector with a factory-trimmed threshold and has ± 8 kV HBM ESD protection.

When the $\overline{PB}$ button is pressed and held, the battery voltage is detected and EN (or $\overline{EN}$) is asserted if the battery voltage is above the threshold V_{TH+} during the whole $t_{DEBOUNCE}$ period (see *Figure 13*).

A short push of the push-button during normal operation can initiate an interrupt through debounced $\overline{INT}$ output (see *Figure 14*) and a long push of $\overline{PB}$ and $\overline{SR}$ simultaneously can either assert reset output $\overline{RST}$ (see *Figure 18*) or deassert the EN or $\overline{EN}$ output (see *Figure 19*) based on the option used.

Note: A switch to GND must be connected to this input (e.g. mechanical push-button, open drain output of external circuitry, etc.), see Figure 1. This ensures a proper startup signal on $\overline{PB}$ (i.e. a transition from full V_{CC} below specified V_{IL}). $\overline{PB}$ input has an internal 100 kΩ pull-up resistor connected.

$\overline{VCC}_{LO}$ - high threshold detection output

During power-up, $\overline{VCC}_{LO}$ is low when V_{CC} supply voltage is below the V_{TH+} threshold. After successful power-up (i.e. during normal operation) $\overline{VCC}_{LO}$ is low anytime undervoltage is detected (see *Figure 13*).

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{VCC}_{LO}$ is floating when SRC0 is in standby mode.

$\overline{PB}_{OUT}$ - $\overline{PB}$ input state

If the push-button $\overline{PB}$ is pressed, the pin stays low during the $t_{DEBOUNCE}$ time period. If $\overline{PB}$ is asserted for the entire $t_{DEBOUNCE}$ period, $\overline{PB}_{OUT}$ will then stay low for at least $t_{\overline{INT}\_Min}$. If $\overline{PB}$ is asserted after $t_{\overline{INT}\_Min}$ expires, $\overline{PB}_{OUT}$ will return high as soon as $\overline{PB}$ is deasserted (see *Figure 22*). $\overline{PB}_{OUT}$ ignores $\overline{PB}$ assertion during an undervoltage condition. At startup on the SRC0 $\overline{PB}_{OUT}$ will respond only to the first $\overline{PB}$ assertion and any other assertion will be ignored until t_{ON_BLANK} expires. This output is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

EN or $\overline{EN}$ - enable output

This output is intended to enable system power (see *Figure 1*). EN is asserted **high** after a valid turn-on event has been detected and confirmed (i.e. push-button has been pressed and held for $t_{DEBOUNCE}$ or more and $V_{CC} > V_{TH+}$ voltage level has been detected - see *Figure 13*). EN is released **low** if any of the conditions below occur:

a) the push-button is released before PS_{HOLD} is driven high.

b) PS_{HOLD} is driven low during normal operation (see *Figure 14*).

c) an undervoltage condition is detected for more than $t_{SRD} + t_{\overline{INT}\_Min} + t_{DEBOUNCE}$ (see *Figure 21*).

d) a long push of the buttons is detected (only for the device with option “EN deasserted by long push” - see *Figure 19*) or PS_{HOLD} is not driven high during t_{ON_BLANK} after a long push of the buttons (only for the device with option “$\overline{RST}$ asserted by long push” - see *Figure 18*).

Described logic levels are inverted in case of $\overline{EN}$ output. Output type is push-pull by default.

$\overline{RST}$ - reset output

This output pulls low for t_{REC}:

a) during startup. $\overline{PB}$ has been pressed (falling edge on the $\overline{PB}$ detected) and held for at least $t_{DEBOUNCE}$ and $V_{CC} > V_{TH+}$ (see *Figure 7*, *8*, *9*, *10*, *11*, *12* and *13* for more details).

b) after long push detection (valid only for the device with option “$\overline{RST}$ asserted by long push”). $\overline{PB}$ has been pressed (falling edge on the $\overline{PB}$ detected) and held for more than $t_{DEBOUNCE} + t_{SRD}$ (additional Smart Reset™ delay time can be adjusted by the external capacitor C_{SRD}) - see *Figure 18*.

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

$\overline{INT}$ - interrupt output

While the system is under normal operation (PS_{HOLD} is driven high, power for application is asserted), the $\overline{INT}$ is driven **low** if:

a) V_{CC} falls below V_{TH-} threshold (i.e. undervoltage is detected - see *Figure 20* and *21*).

b) the falling edge on the $\overline{PB}$ is detected and the push-button is held for $t_{DEBOUNCE}$ or more. $\overline{INT}$ is driven low after $t_{DEBOUNCE}$ and stays low as long as $\overline{PB}$ is held. The $\overline{INT}$ signal is held high during power-up.

The state of the $\overline{PB}_{OUT}$ output can be used to determine if the interrupt was caused by either the assertion of the $\overline{PB}$ input, or was due to the detection of an undervoltage condition on V_{CC}.

$\overline{INT}$ output is asserted low for at least $t_{\overline{INT}\_Min}$.

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 kΩ is sufficient in most applications.

GND - ground

3 Operation

The SRC0 simplified smart push-button on/off controller with Smart Reset™ and power-on lockout enables and disables power for the application depending on push-button states, signals from the processor, and battery voltage.

Power-on

Because most of the processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS_{HOLD} input during startup (see *Figure 7*, *8*, *9*, *10*, *11*, *12*, *13*, and *18*).
To power up the device the push-button $\overline{PB}$ has to be pressed for at least $t_{DEBOUNCE}$ and V_{CC} has to be above V_{TH+} for the whole $t_{DEBOUNCE}$ period. If the battery voltage drops below V_{TH+} during the $t_{DEBOUNCE}$, the counter is reset and starts to count again when $V_{CC} > V_{TH+}$ (see *Figure 13*). After $t_{DEBOUNCE}$ the enable signal is asserted (EN goes high, $\overline{EN}$ goes low), reset output $\overline{RST}$ is asserted for t_{REC} and then the startup routine is performed by the processor. During initialization, the processor sets the PS_{HOLD} signal high.

On the SRC0 the PS_{HOLD} signal has to be set high prior to push-button release and t_{ON_BLANK} expiration, otherwise the enable signal is deasserted (EN goes low, $\overline{EN}$ goes high) - see *Figure 7*, *8*, *9*, and *10*. The time up to push-button release represents the maximum time allowed for the system to power up and initialize the circuits driving the PS_{HOLD} input. If the PS_{HOLD} signal is low at push-button release, the enable output is deasserted immediately, thus turning off the system power. If t_{ON_BLANK} expires prior to push-button release, the PS_{HOLD} state is checked at its expiration. This safety feature disables the power and prevents discharging the battery if the push-button is stuck or it is held for an unreasonable period of time and the application is not responding (see *Figure 8* and *10*). $\overline{PB}$ status, $\overline{INT}$ status and V_{CC} undervoltage detection are not monitored until power-up is completed.

Push-button interrupt

If the device works under normal operation (i.e. PS_{HOLD} is high) and the push-button $\overline{PB}$ is pressed for more than $t_{DEBOUNCE}$, a negative pulse with minimum $t_{\overline{INT}\_Min}$ width is generated on the $\overline{INT}$ output. By connecting $\overline{INT}$ to the processor interrupt input ($\overline{INT}$ or $\overline{NMI}$) a safeguard routine can be performed and the power can be shut down by setting PS_{HOLD} low - see *Figure 14*.

Forced power-down mode

The PS_{HOLD} output can be forced low anytime during normal operation by the processor and can deassert the enable signal - see *Figure 14*.

Undervoltage detection

If V_{CC} voltage drops below V_{TH-} voltage threshold during normal operation, the $\overline{INT}$ output is driven low (see *Figure 20* and *Figure 21*).

If an undervoltage condition is detected for $t_{DEBOUNCE} + t_{\overline{INT}\_Min} + t_{SRD}$, the enable output is deasserted (see *Figure 21*).

Hardware reset or power-down while system not responding

If the system is not responding and the system hangs, the $\overline{PB}$ and $\overline{SR}$ push-button can be pressed simultaneously longer than $t_{DEBOUNCE} + t_{\overline{INT}\_Min} + t_{SRD}$, and then

a) either the reset output $\overline{RST}$ is asserted for t_{REC} and the processor is reset (valid only for the device with option "$\overline{RST}$ asserted by long push") – see *Figure 18*

b) or the power is disabled by EN or $\overline{EN}$ signal (valid only for the device with option "EN deasserted by long push") – see *Figure 19*

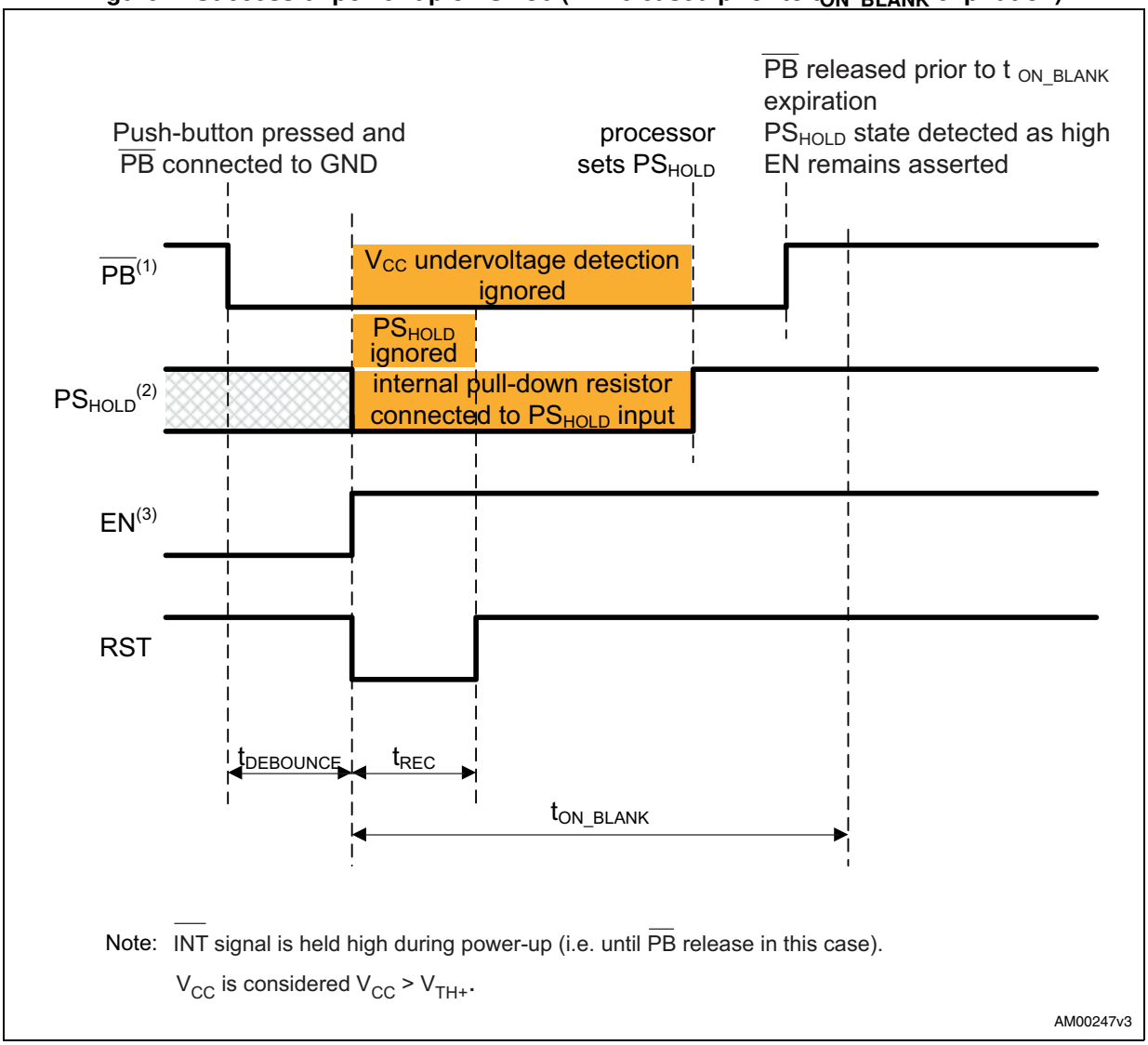
The t_{SRD} is set by the external capacitor connected to the C_{SRD} pin. $\overline{SR}$ input is monitored for falling edge after power-up and must not be grounded permanently.

Standby

If the enable output is deasserted (i.e. EN is low or $\overline{EN}$ is high), the STM660x device enters standby mode with low current consumption (see *Table 5*). In standby mode $\overline{PB}$ input is only monitored for the falling edge. The external 1.5 V voltage reference is also disabled in standby mode.

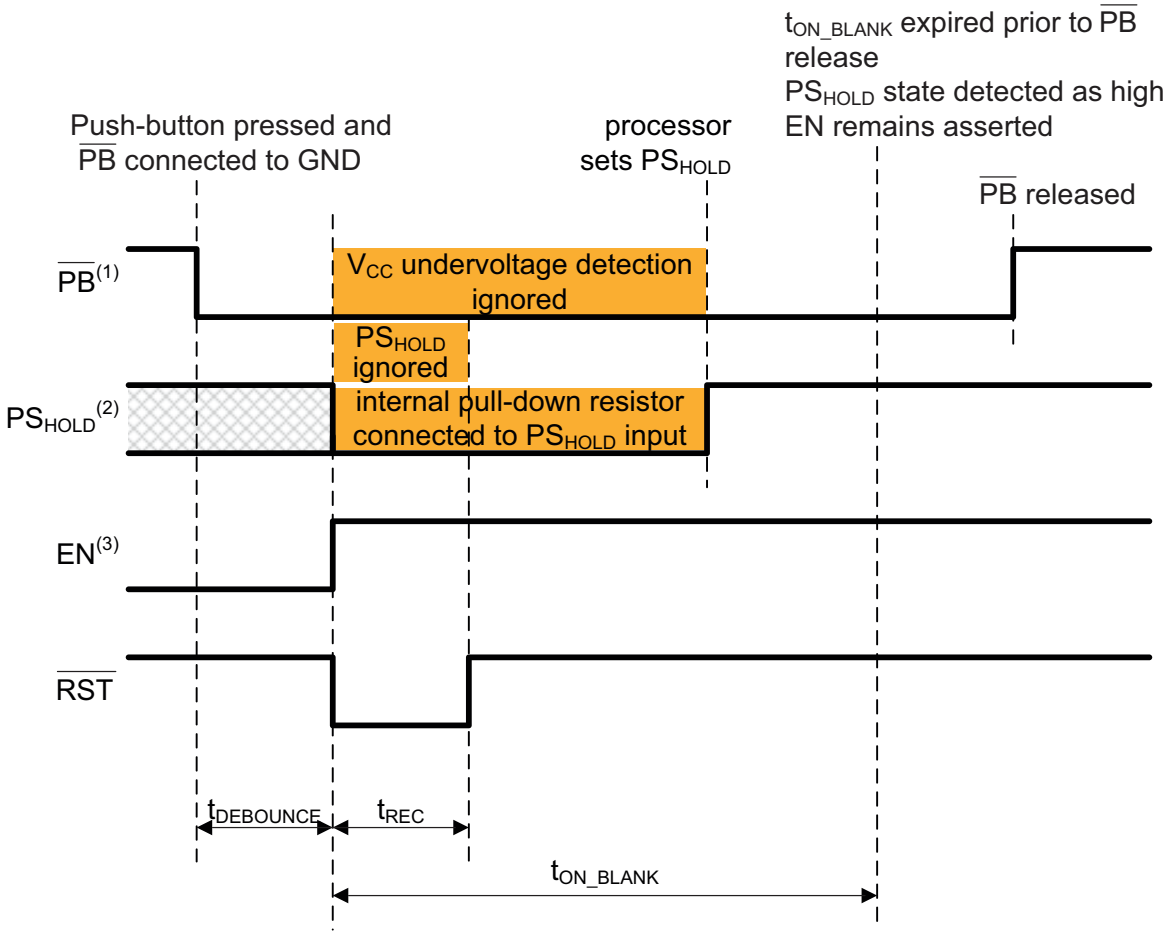
4 Waveforms

Figure 7. Successful power-up on SRC0 ($\overline{PB}$ released prior to t_{ON_BLANK} expiration)



1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. EN signal is high even after $\overline{PB}$ release, because processor sets PS_{HOLD} signal high before $\overline{PB}$ is released.

Figure 8. Successful power-up on SRC0 (t_{ON_BLANK} expires prior to $\overline{PB}$ release)



Note: $\overline{INT}$ signal is held high during power-up (i.e. until t_{ON_BLANK} expires in this case).
V_{CC} is considered $V_{CC} > V_{TH+}$.

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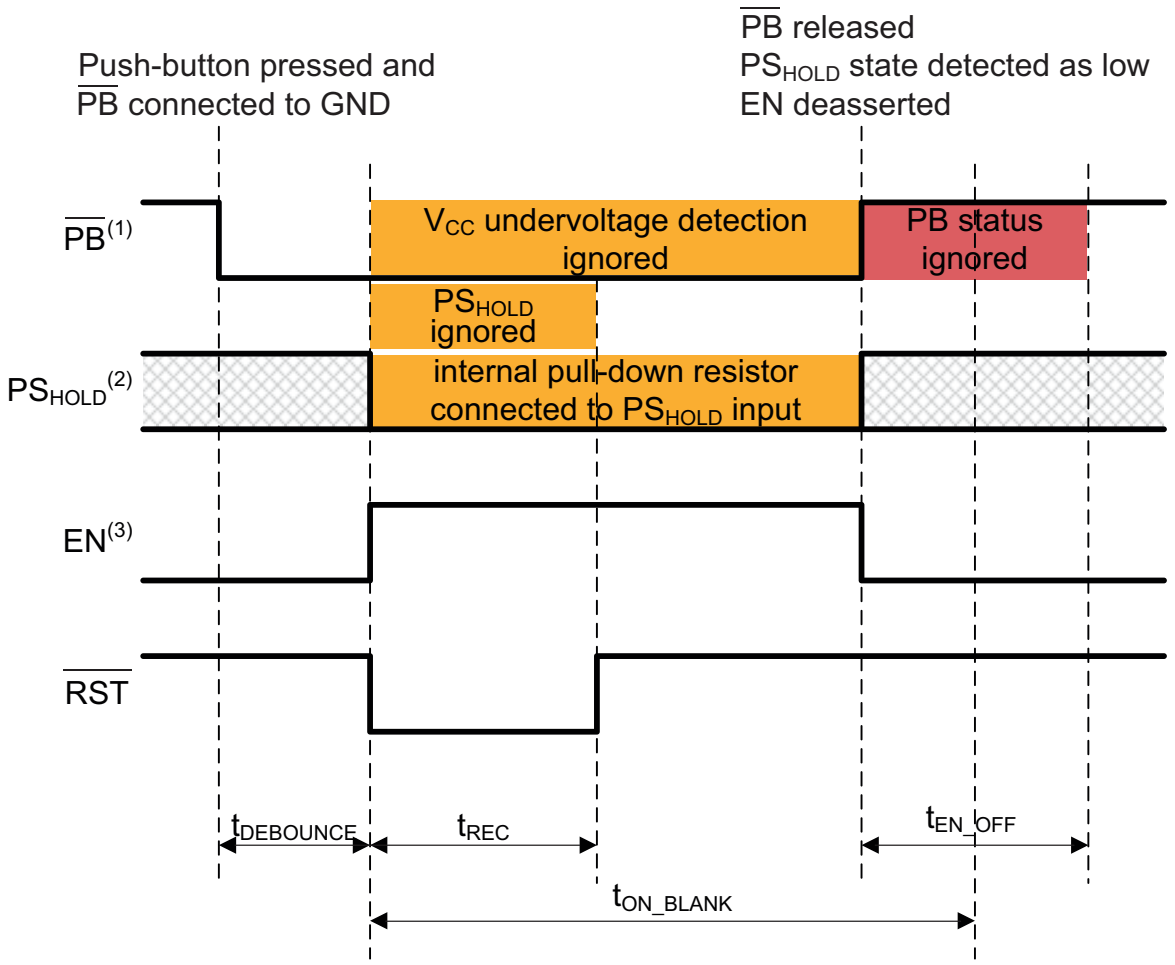
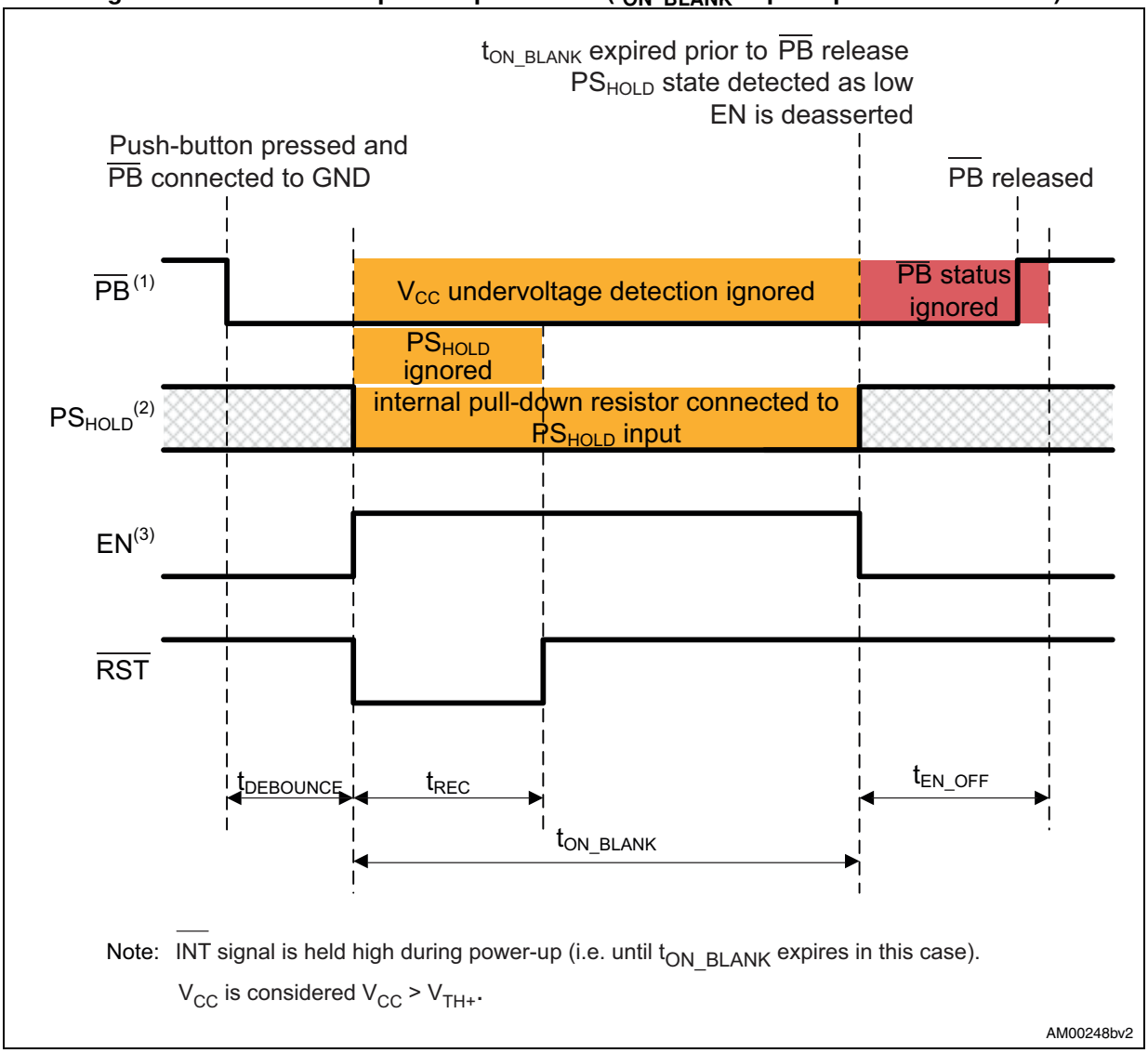
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. t_{ON_BLANK} expires prior to $\overline{PB}$ release so PS_{HOLD} is checked at its expiration.

Figure 9. Unsuccessful power-up on SRC0 ($\overline{PB}$ released prior to t_{ON_BLANK})



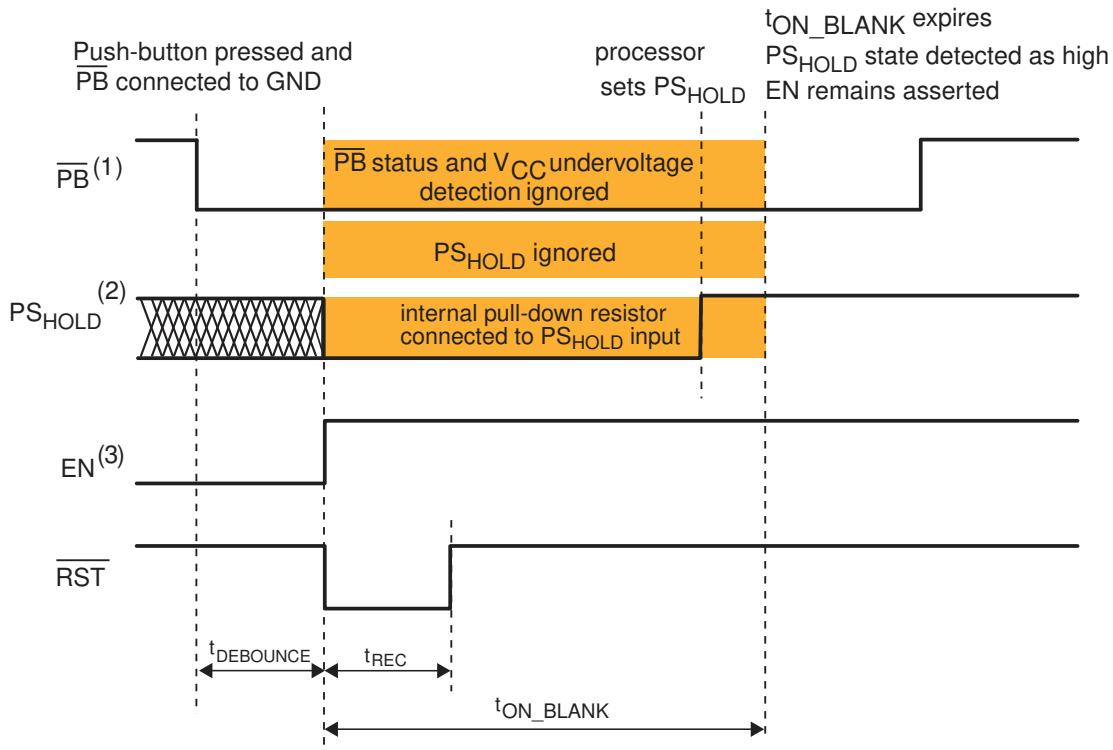
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. EN signal goes low with $\overline{PB}$ release, because processor did not force PS_{HOLD} signal high.

Figure 10. Unsuccessful power-up on SRC0 (t_{ON_BLANK} expires prior to $\overline{PB}$ release)



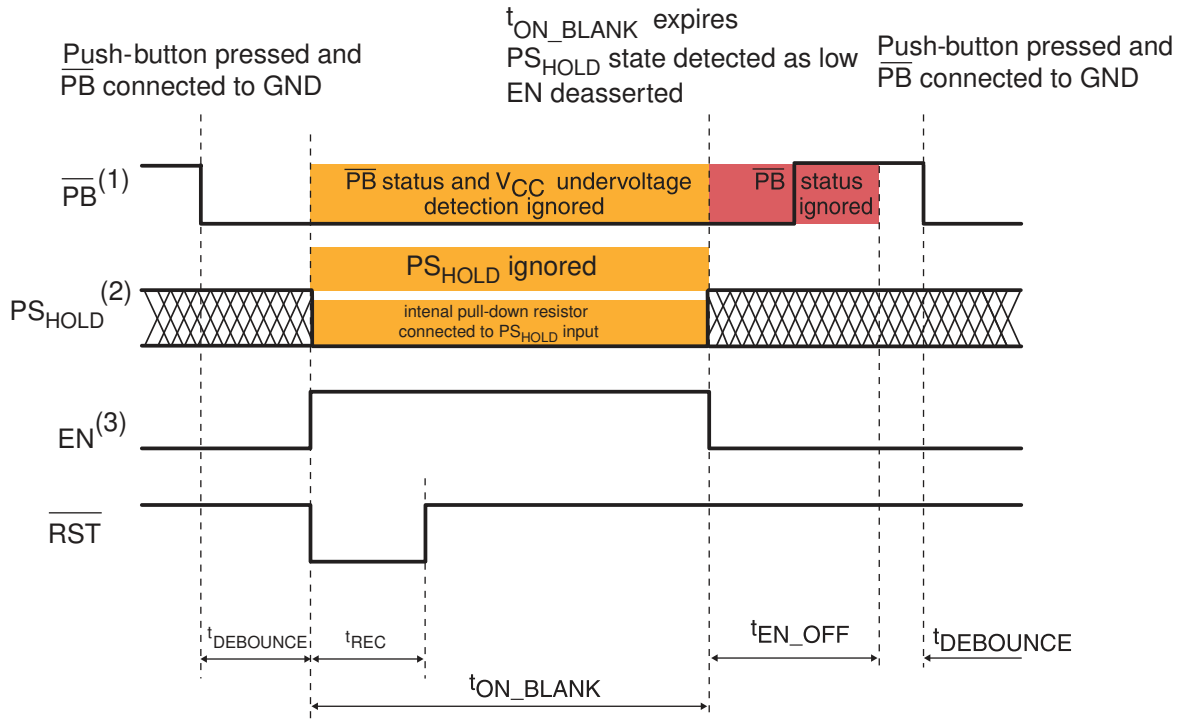
1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. t_{ON_BLANK} expires prior to $\overline{PB}$ release so PS_{HOLD} is checked at its expiration.

Figure 11. Successful power-up on SRC0



1. $\overline{PB}$ detection on falling edge.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. When t_{ON_BLANK} expires, the level of the PS_{HOLD} signal is high therefore the EN signal remains asserted.

Figure 12. Unsuccessful power-up on SRC0



Note: INT signal is held high during power-up (i.e. until t_{ON_BLANK} expires in the case of the STM6601).
V_{CC} is considered $V_{CC} > V_{TH+}$.

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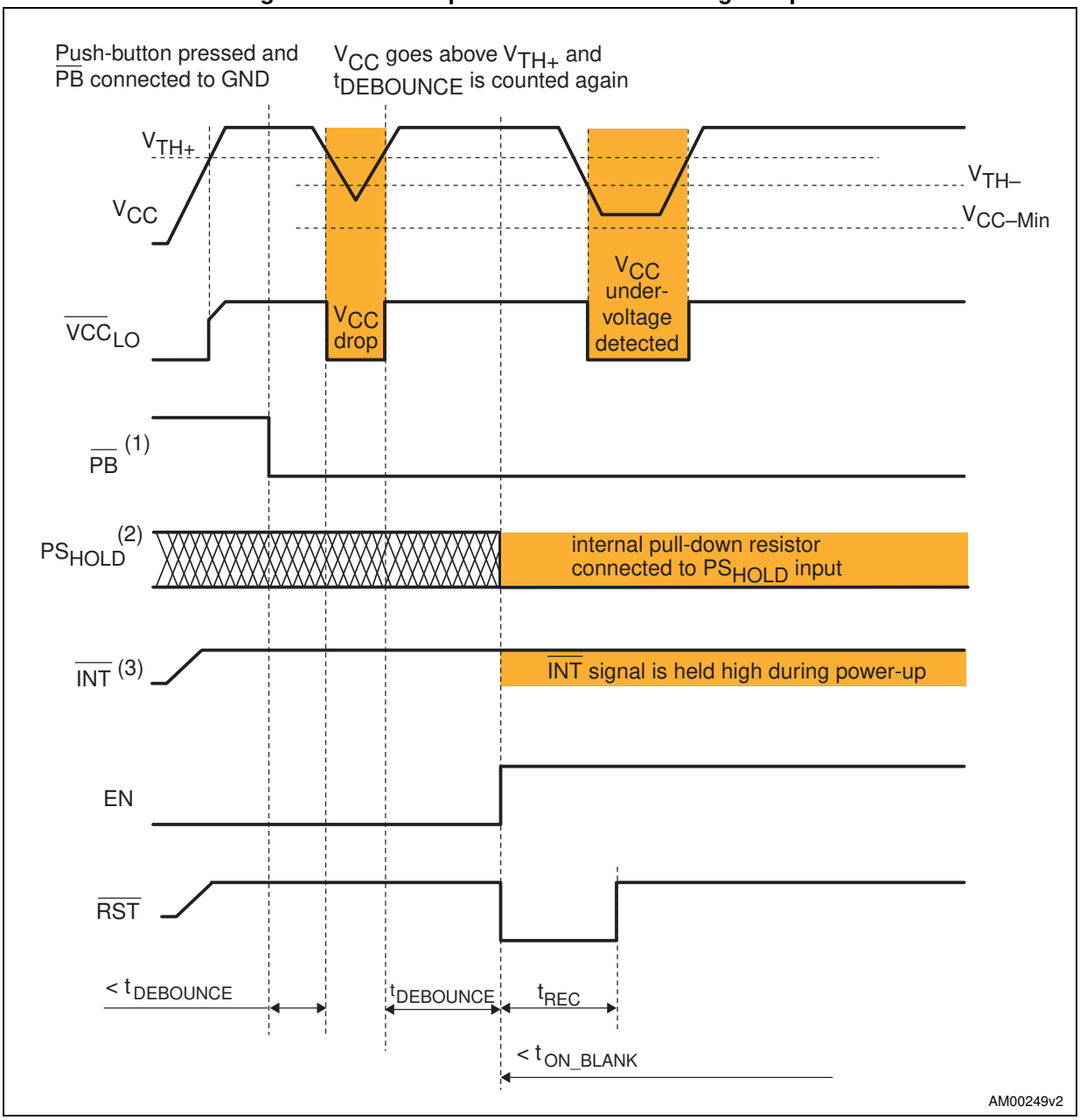
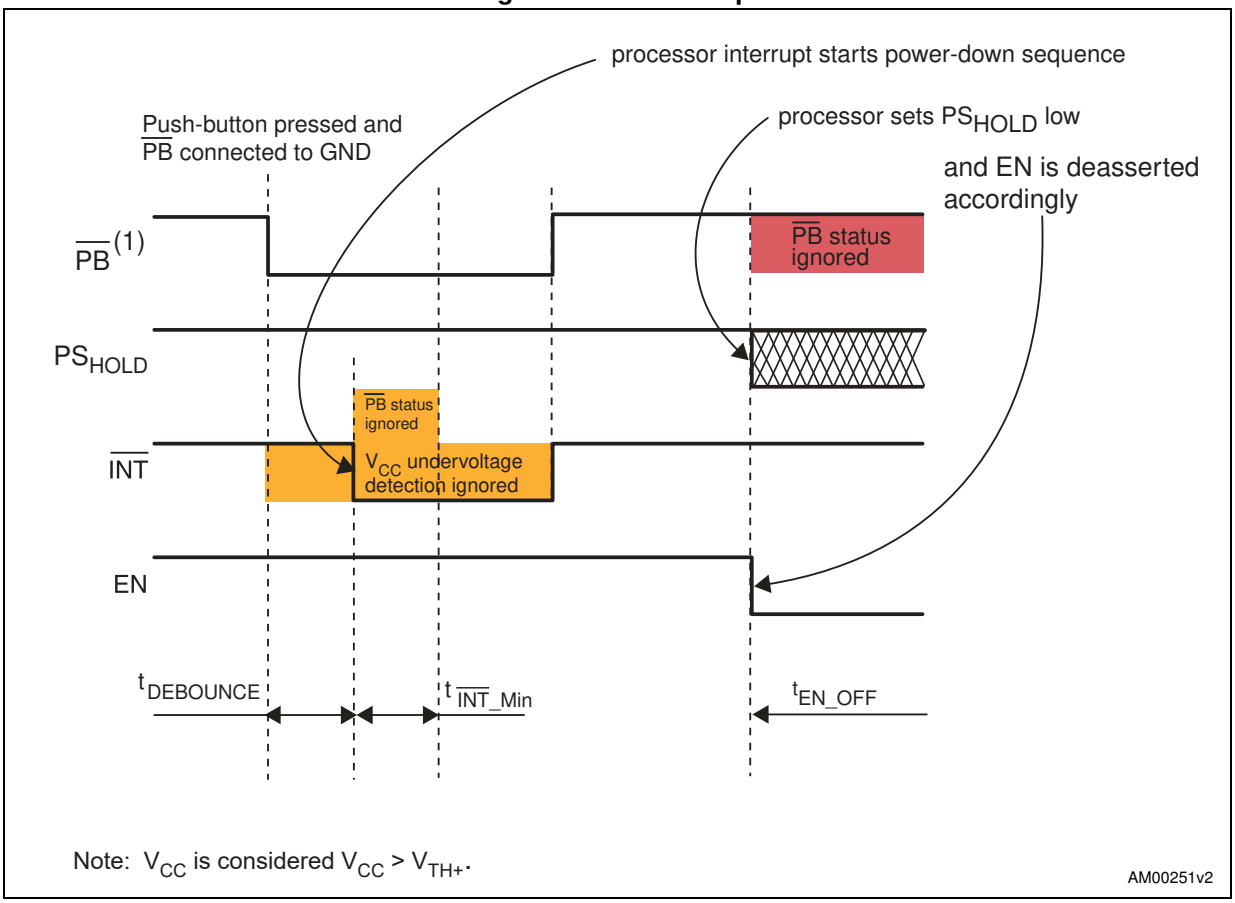
1. PB detection on falling edge.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. When t_{ON_BLANK} expires, the level of the PS_{HOLD} signal is not high therefore the EN signal goes low. Even releasing the PB button after the t_{ON_BLANK} will not prevent this.

Figure 13. Power-up on STM660x with voltage dropout



1. $\overline{PB}$ detection on falling and rising edges.
2. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during power-up.
3. $\overline{INT}$ signal is held high during power-up.

Figure 14. $\overline{PB}$ interrupt



1. $\overline{PB}$ detection on falling edge.

Figure 15. Long push, $\overline{PB}$ pressed first

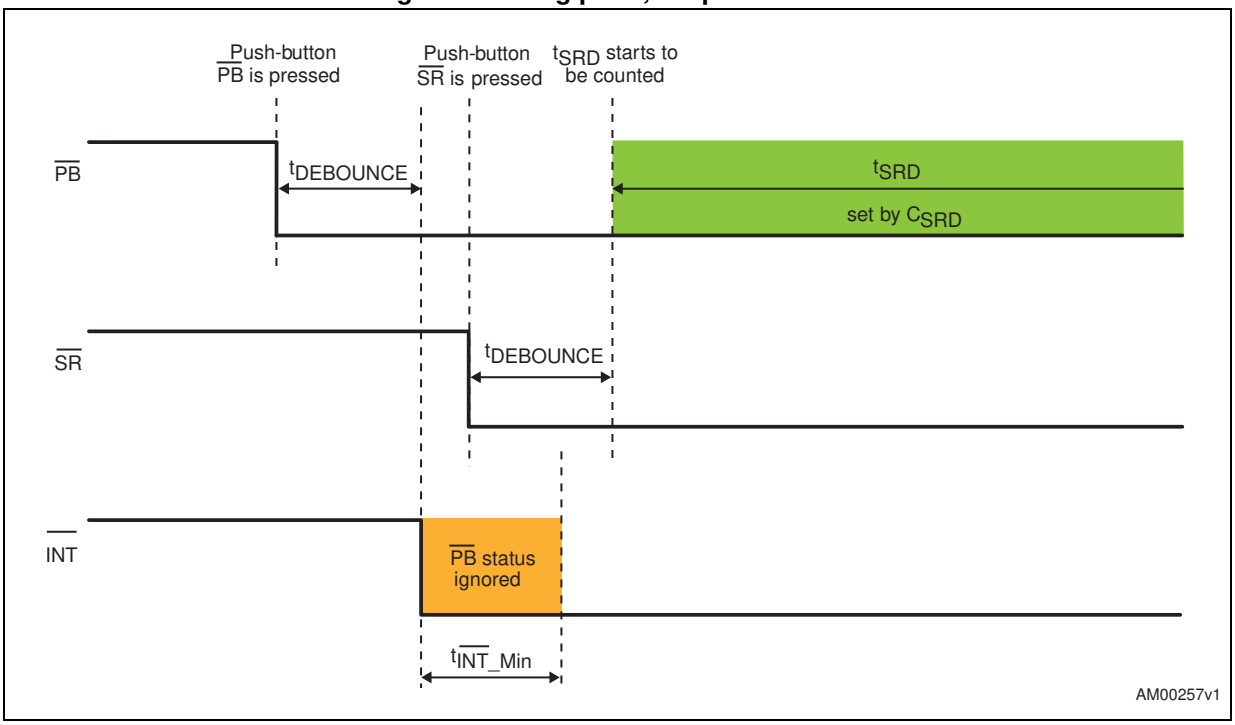


Figure 16. Long push, $\overline{SR}$ pressed first

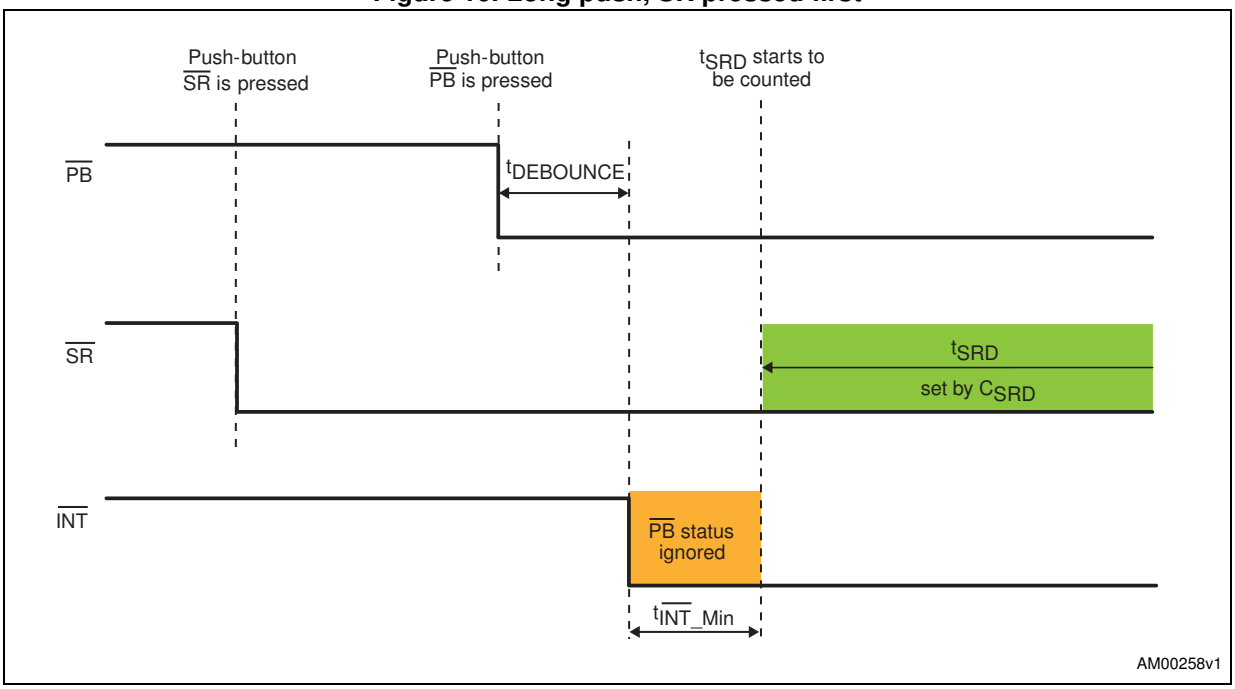


Figure 17. Invalid long push

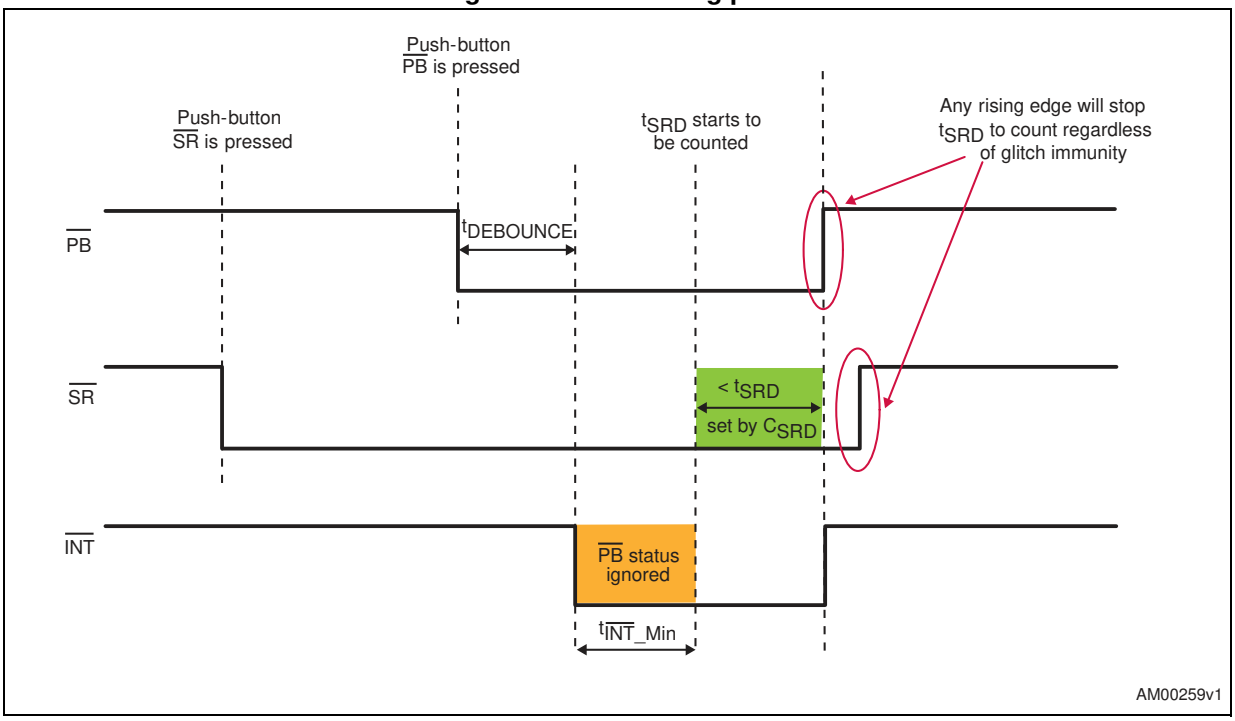
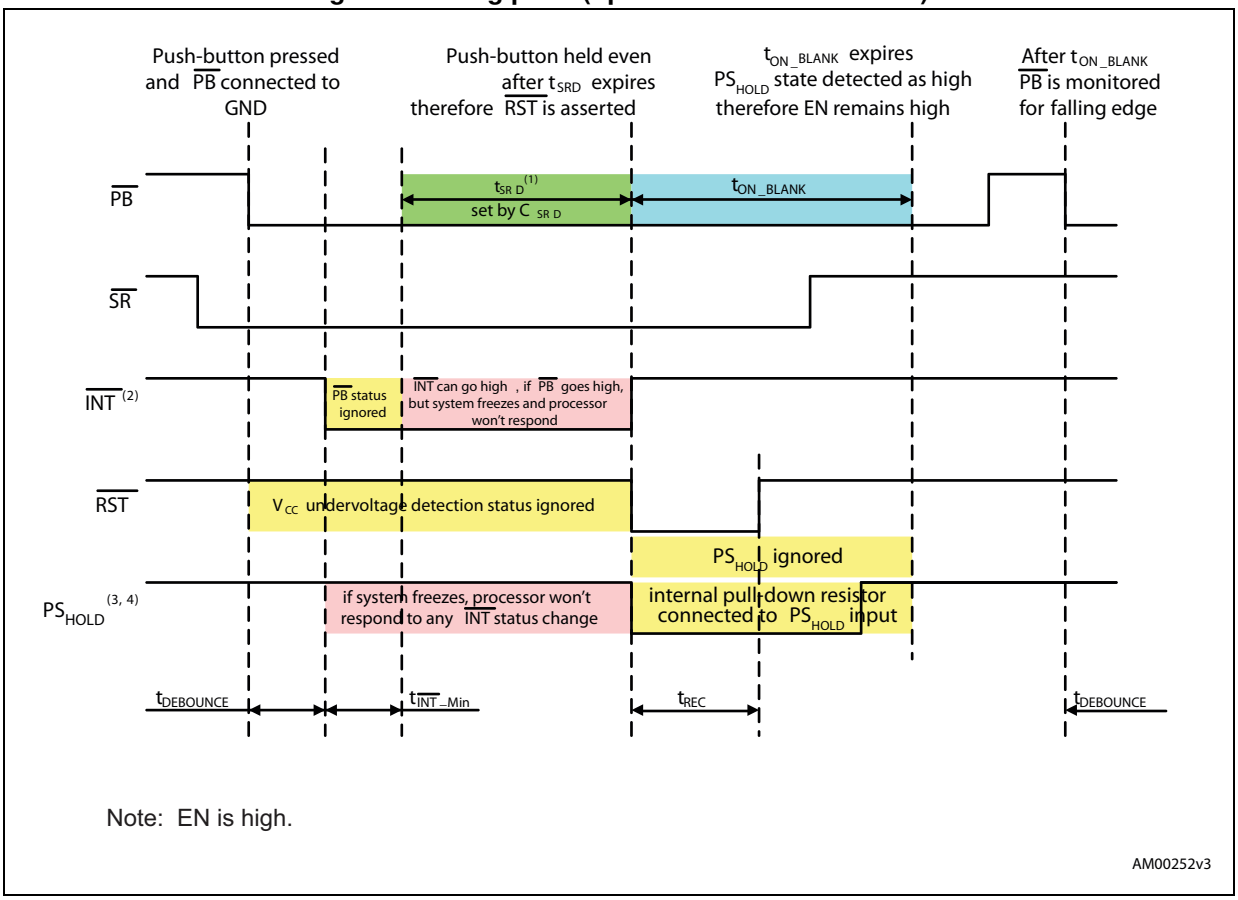
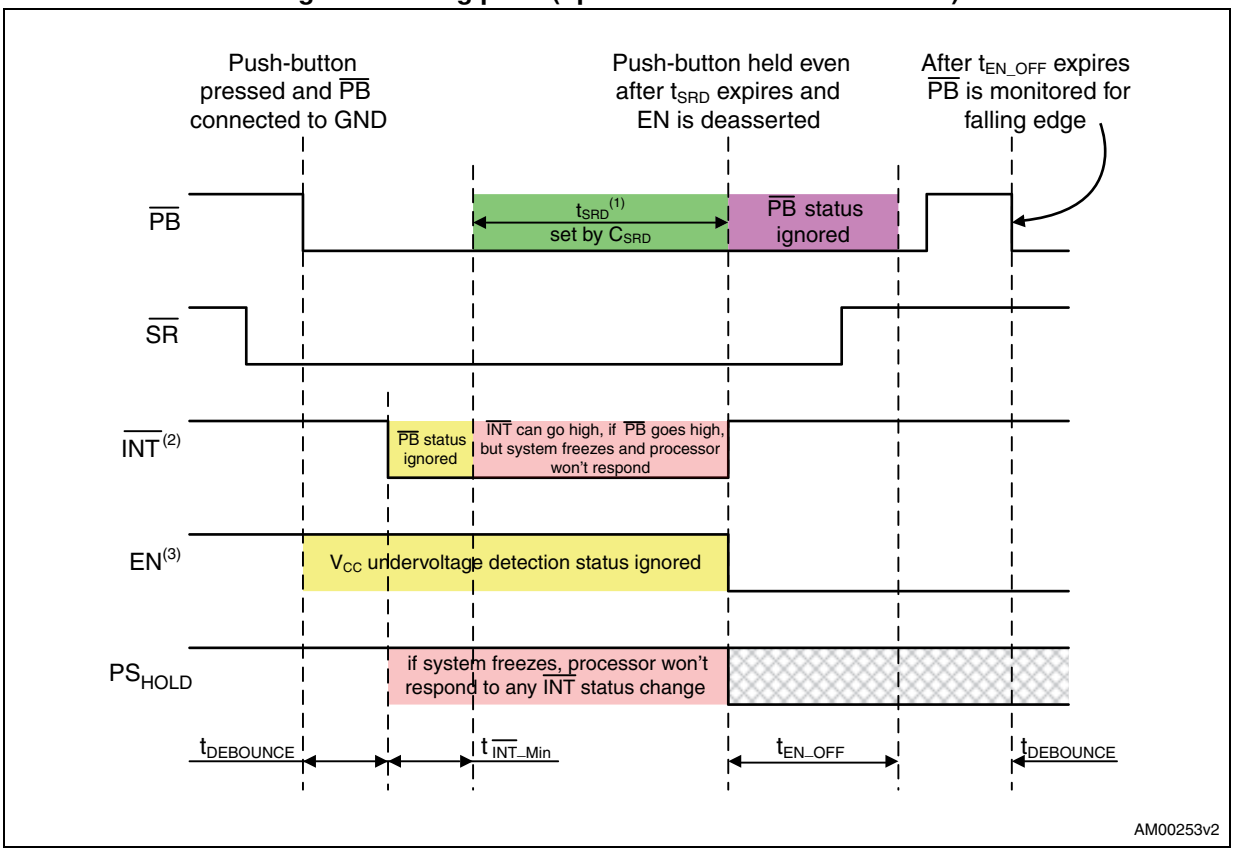


Figure 18. Long push (option with $\overline{RST}$ assertion)



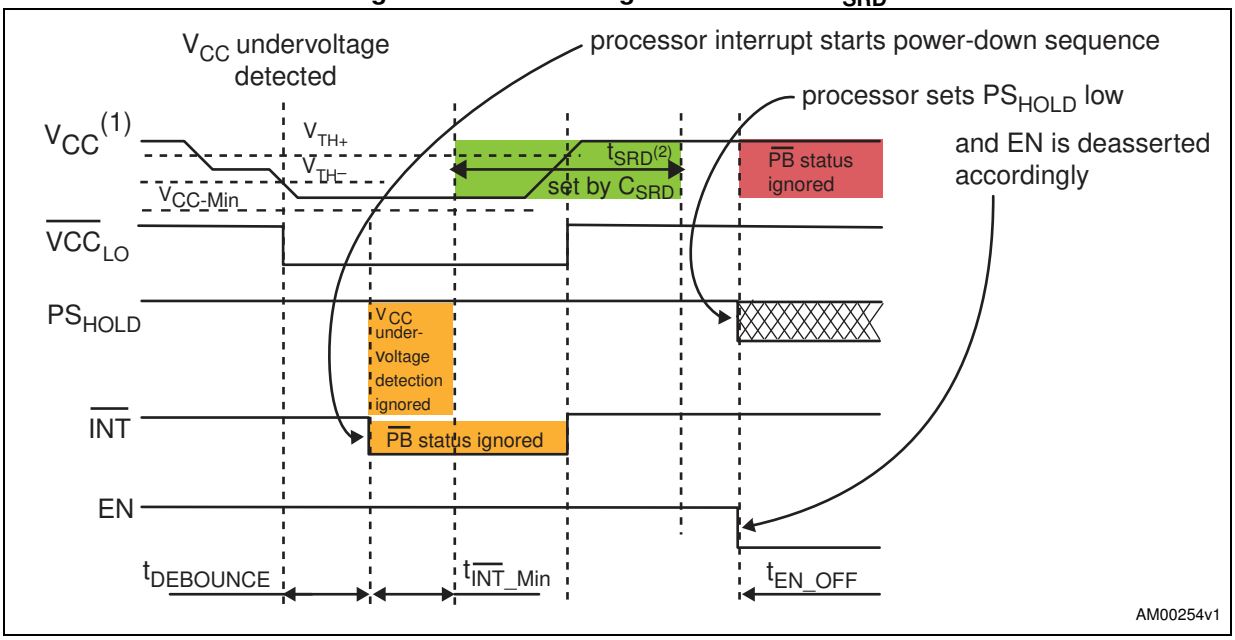
1. t_{SRD} period is set by external capacitor C_{SRD}.
2. $\overline{PB}$ ignored during $t_{\overline{INT}\_Min}$.
3. PS_{HOLD} signal is ignored during t_{ON_BLANK}. Its level is checked after t_{ON_BLANK} expires and if it is high the EN signal remains asserted, otherwise EN goes low.
4. Internal pull-down resistor 300 kΩ is connected to PS_{HOLD} input during startup when device is reset.

Figure 19. Long push (option with enable deassertion)



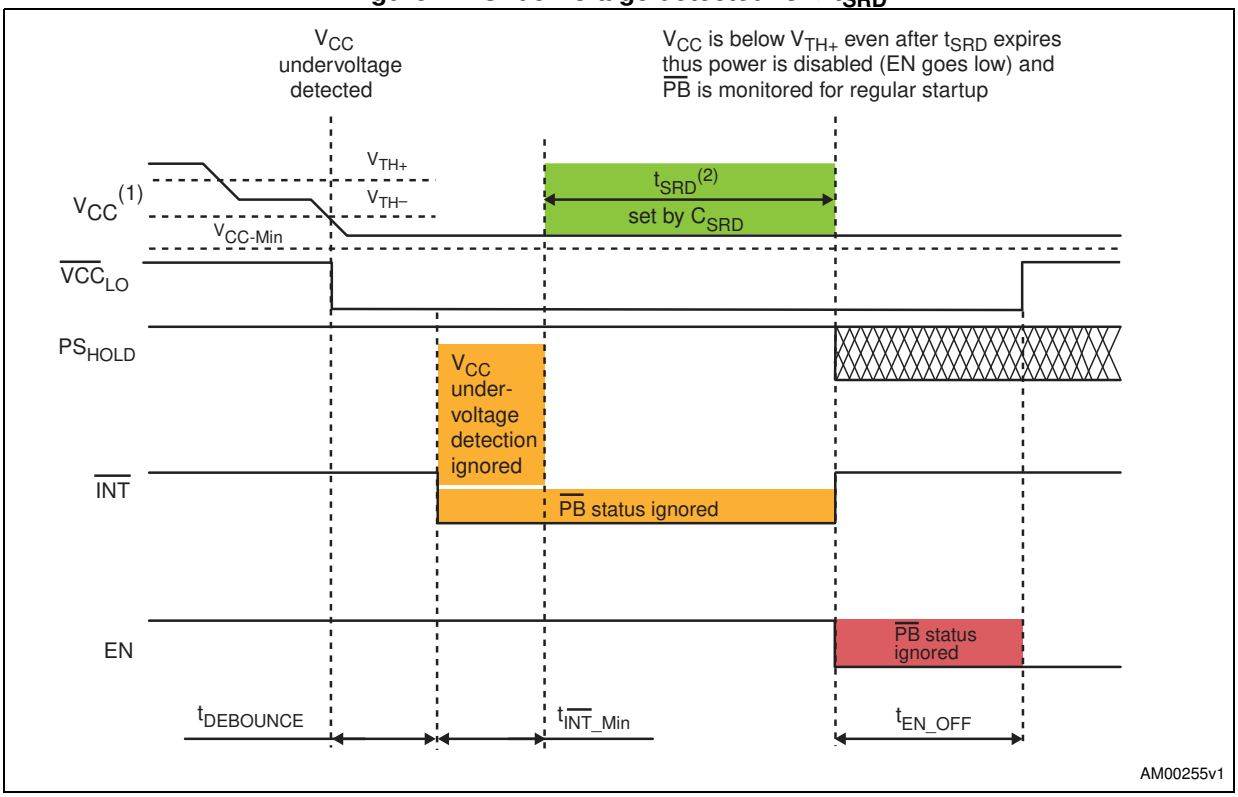
1. t_{SRD} period is set by external capacitor C_{SRD}.
2. $\overline{PB}$ ignored during $t_{\overline{INT}\_Min}$.
3. After t_{SRD} expires EN is forced low.

Figure 20. Undervoltage detected for <t_{SRD}



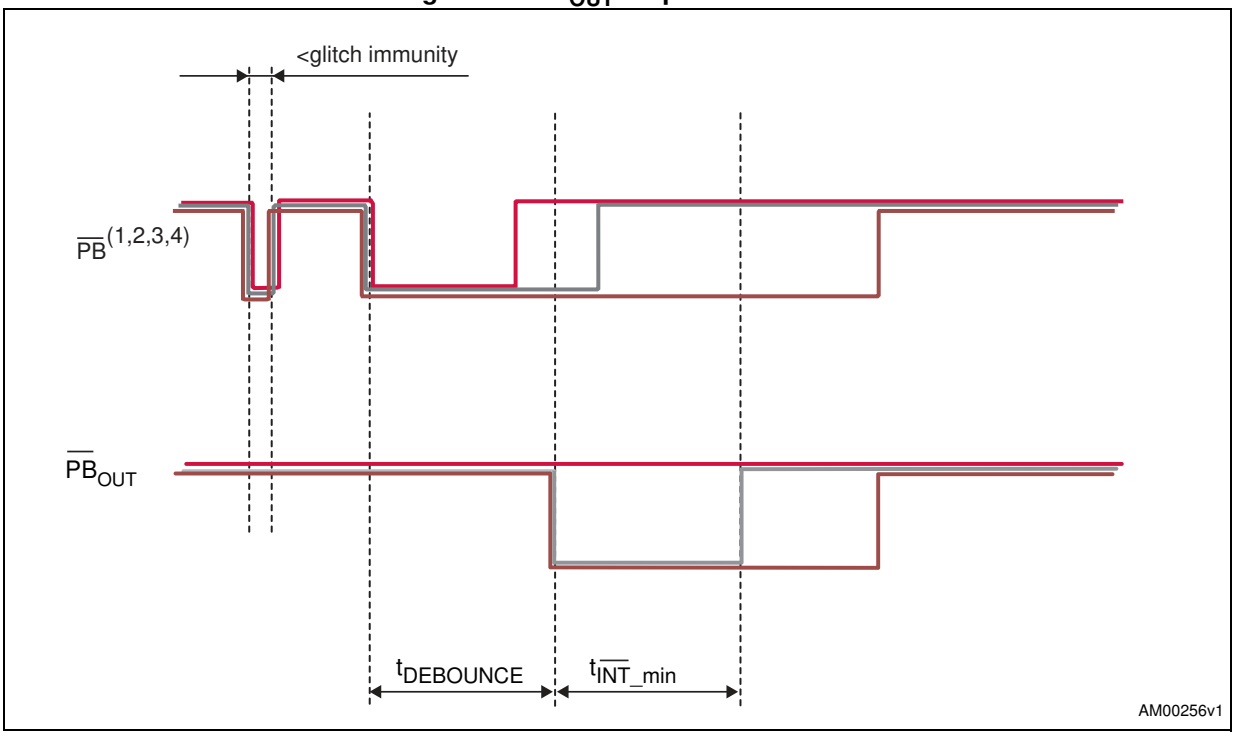
1. V_{CC} goes above V_{TH+} within t_{SRD} thus power is not disabled after t_{SRD} expires.
2. t_{SRD} period is set by external capacitor C_{SRD}.

Figure 21. Undervoltage detected for >t_{SRD}



1. After t_{SRD} expires V_{CC} is still insufficient (below V_{TH+}) thus power is disabled (EN goes low or $\overline{EN}$ goes high).
2. t_{SRD} period is set by external capacitor C_{SRD}.

Figure 22. $\overline{PB}_{OUT}$ output waveform



1. Pulses on $\overline{PB}$ shorter than glitch immunity are ignored.
2. Pulses on $\overline{PB}$ shorter than $t_{DEBOUNCE}$ are not recognized by $\overline{PB}_{OUT}$.
3. Minimum pulse width on $\overline{PB}_{OUT}$ is $t_{\overline{INT}\_Min}$.
4. If push-button is held longer than $t_{DEBOUNCE}$ + $t_{\overline{INT}\_Min}$, $\overline{PB}_{OUT}$ goes high when the push-button is released.

5 Typical operating characteristics

Figure 23. Supply current vs. temperature, normal state

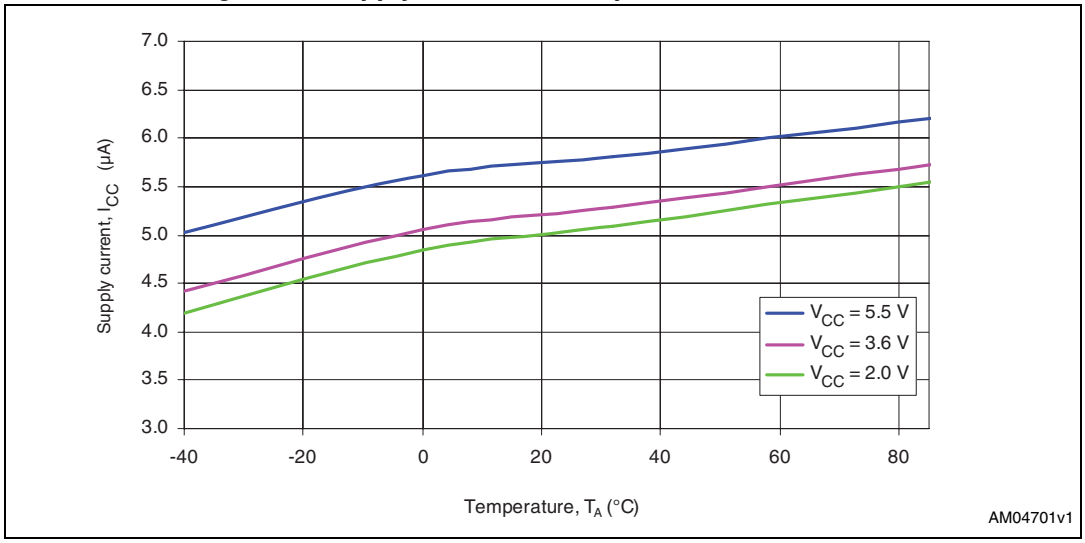


Figure 24. Supply current vs. temperature, standby state

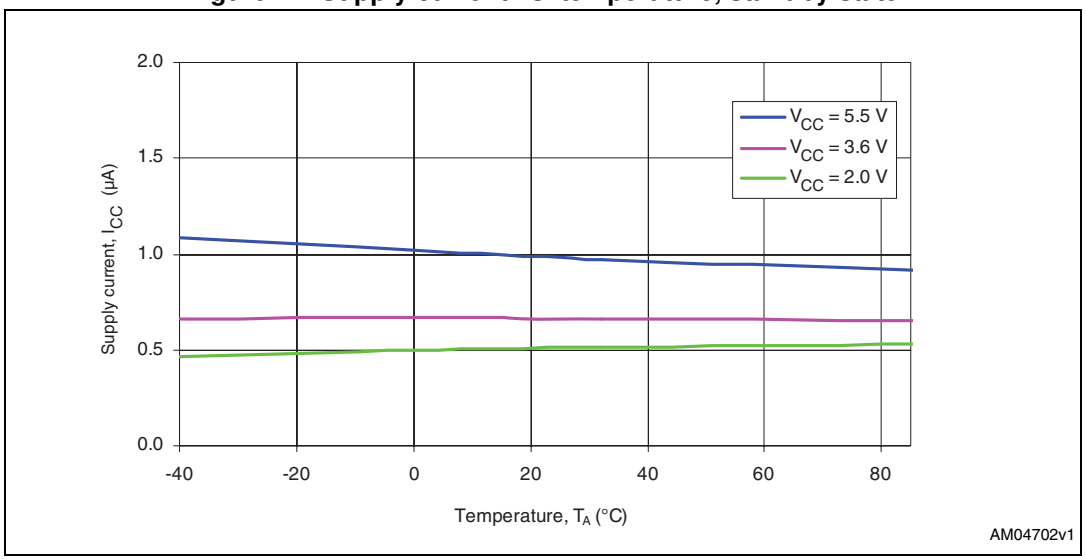


Figure 25. Supply current vs. supply voltage, normal state

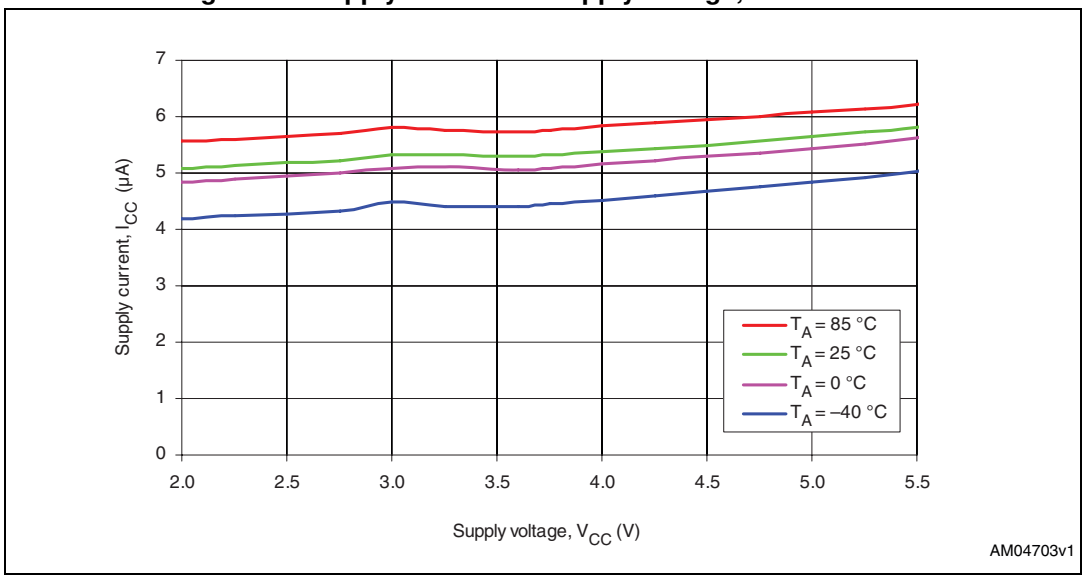


Figure 26. Supply current vs. supply voltage, standby state

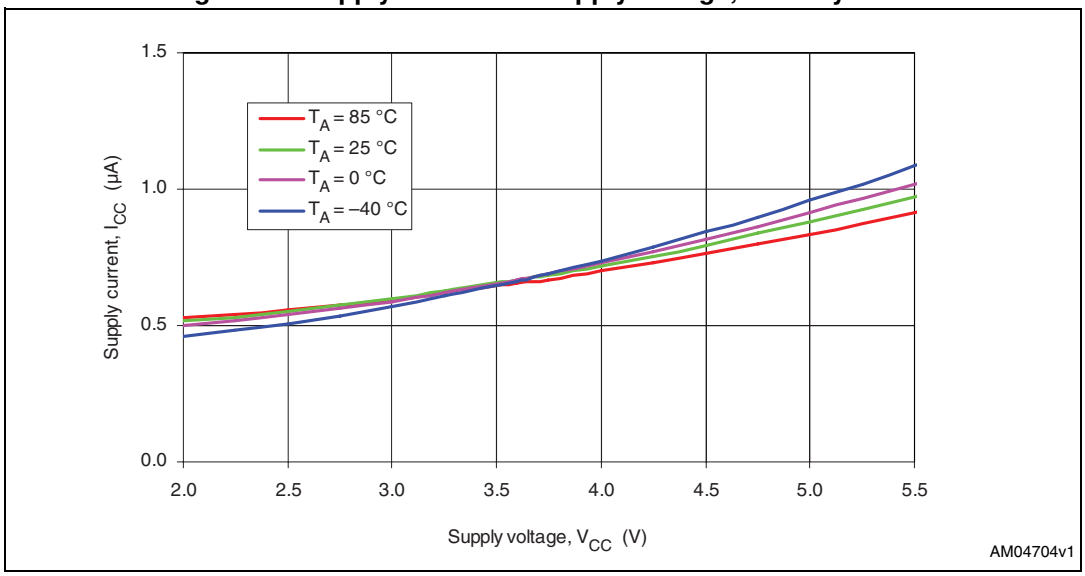


Figure 27. Threshold vs. temperature, V_{TH+} = 3.4 V (typ.)

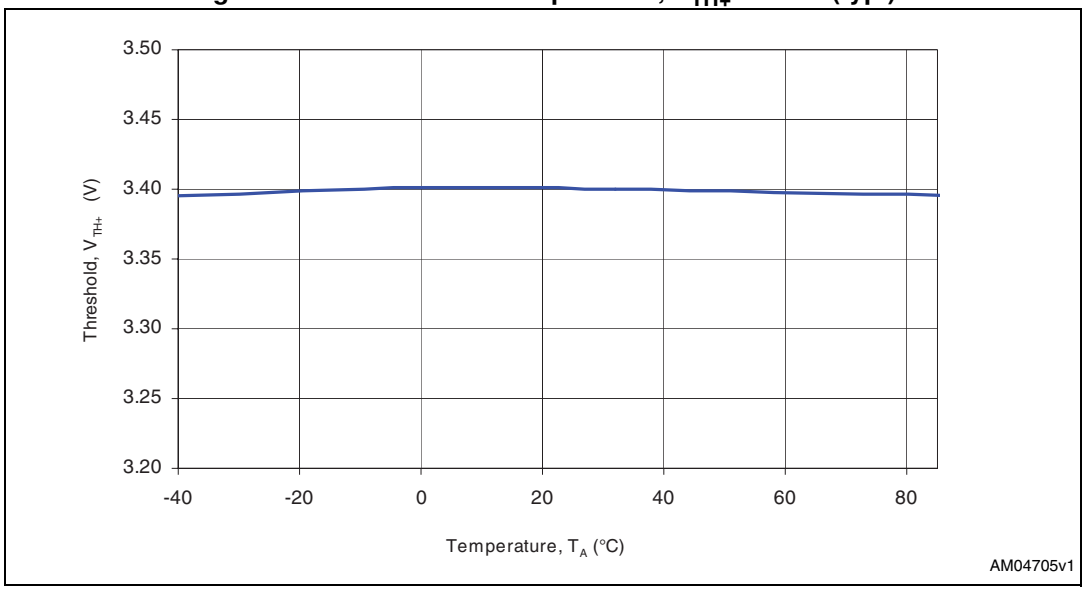


Figure 28. Threshold hysteresis vs. temperature, V_{HYST} = 200 mV (typ.)

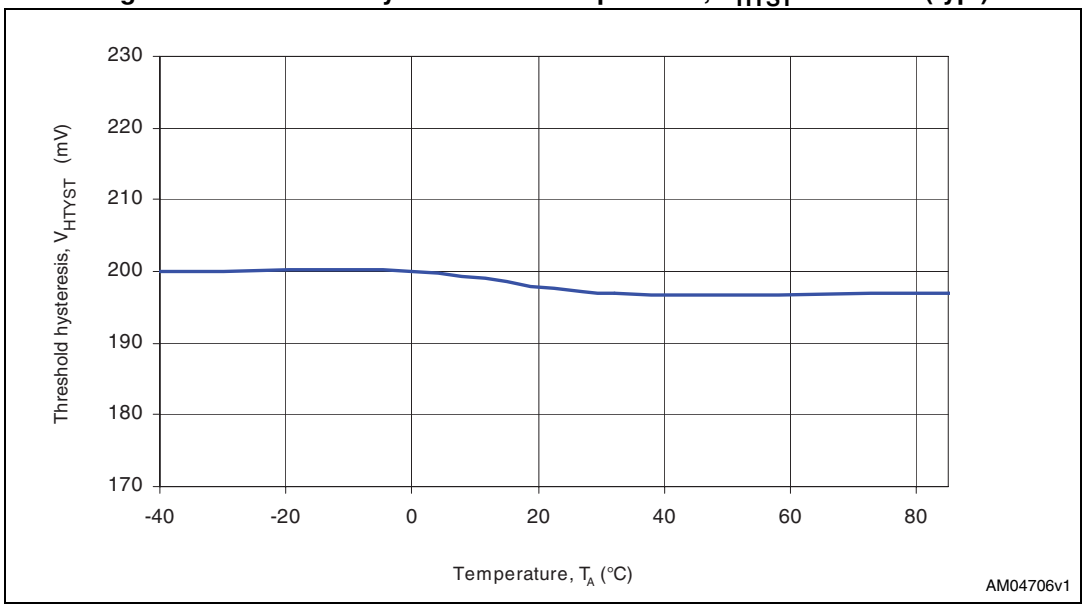


Figure 29. Debounce period vs. supply voltage

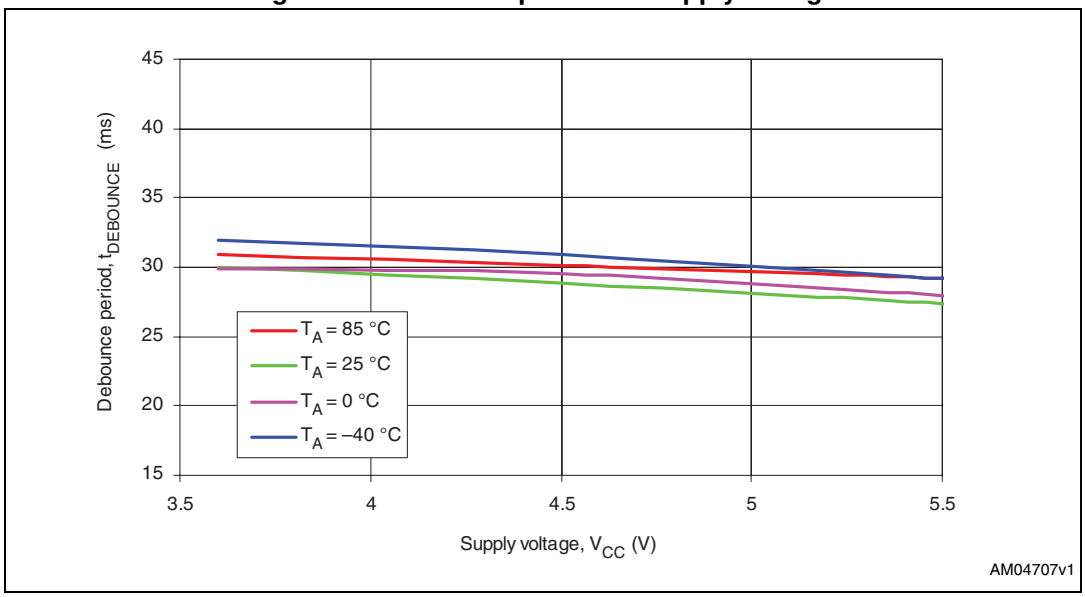


Figure 30. C_{SRD} charging current vs. temperature, V_{CC} = 3.6 V

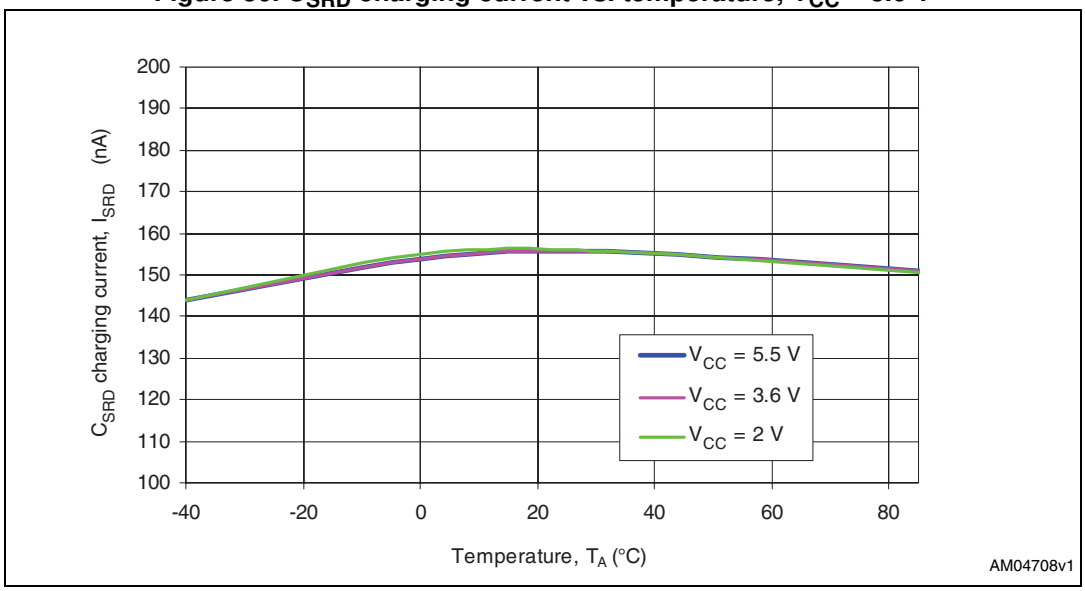
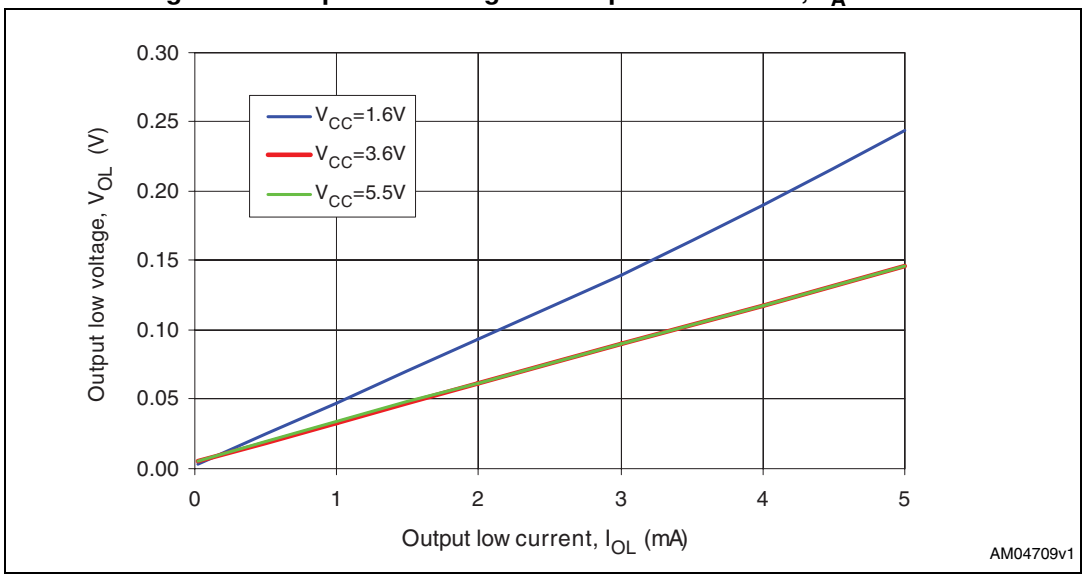
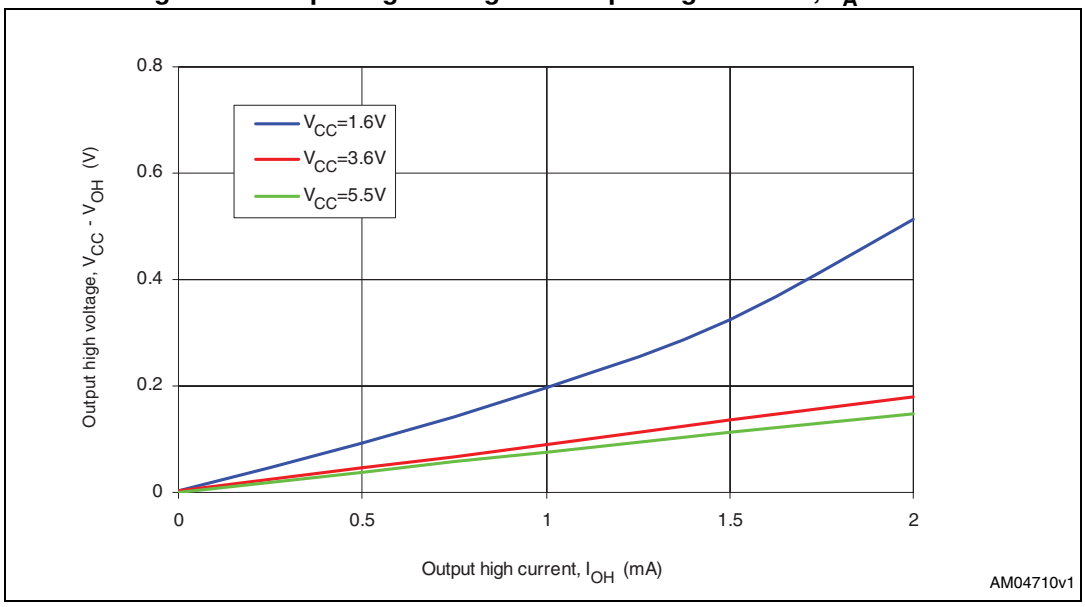


Figure 31. Output low voltage vs. output low current, T_A = 25 °C



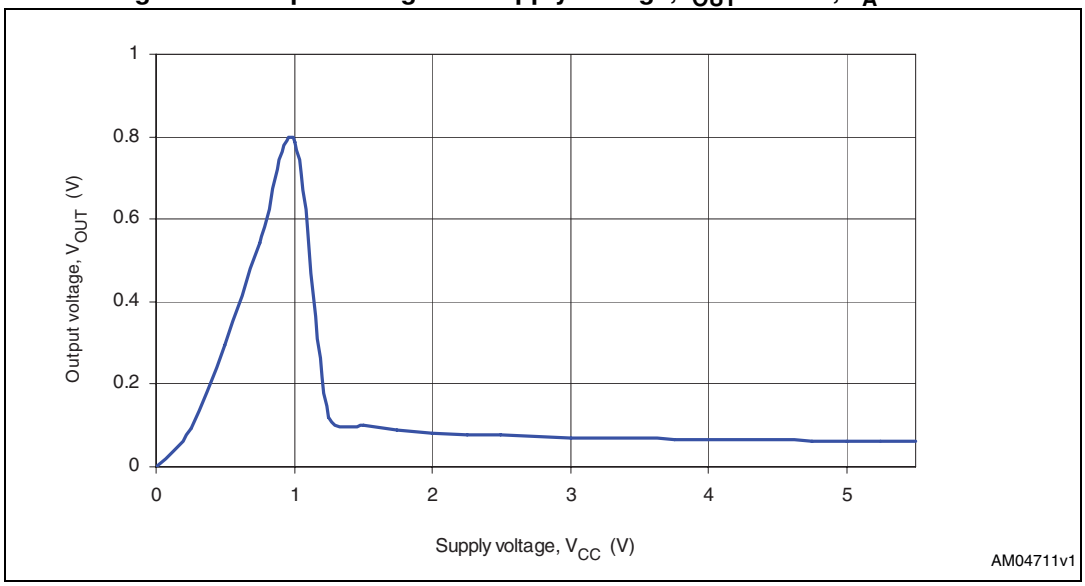
Note: Characteristics valid for all the outputs (EN, $\overline{EN}$, $\overline{RST}$, $\overline{INT}$, $\overline{PB_{OUT}}$ and $\overline{VCC_{LO}}$).

Figure 32. Output high voltage vs. output high current, T_A = 25 °C



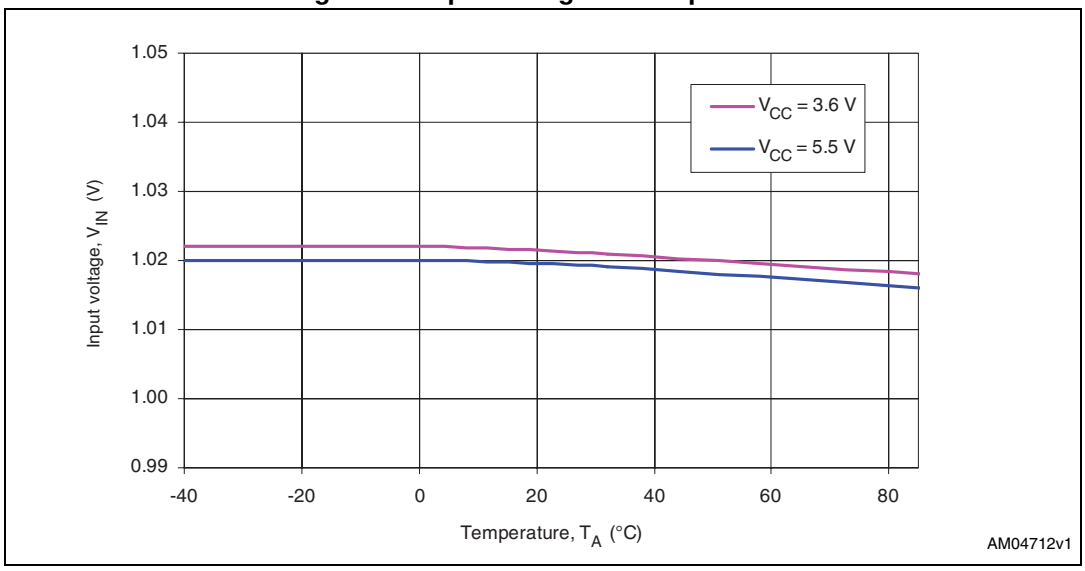
Note: Characteristics valid for EN and $\overline{EN}$ outputs.

Figure 33. Output voltage vs. supply voltage, I_{OUT} = 1 mA, T_A = 25 °C



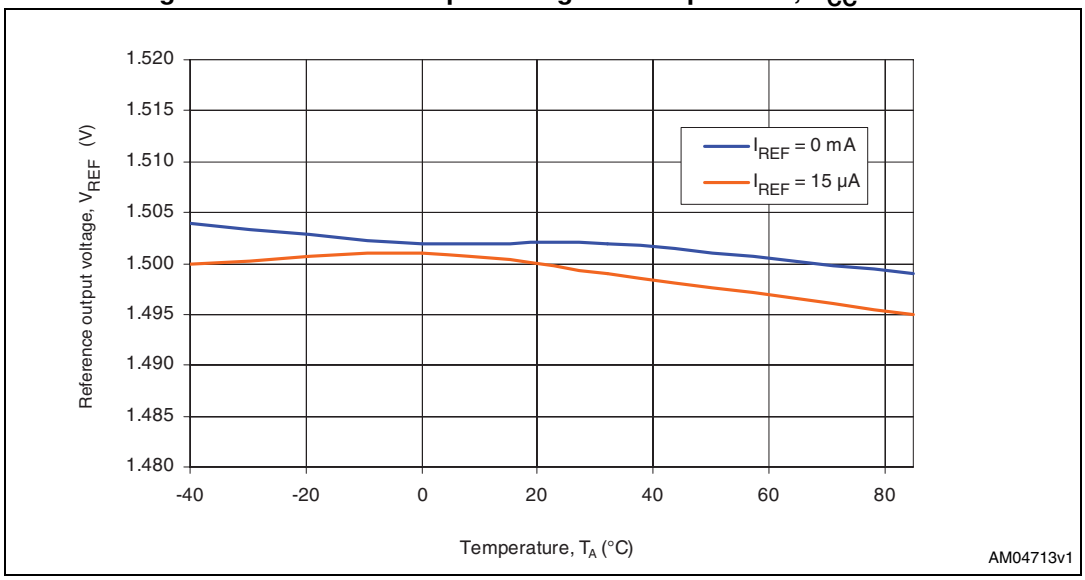
Note: Characteristics valid for all the outputs (EN, $\overline{EN}$, $\overline{RST}$, $\overline{INT}$, $\overline{PB}_{OUT}$ and $\overline{VCC}_{LO}$).

Figure 34. Input voltage vs. temperature



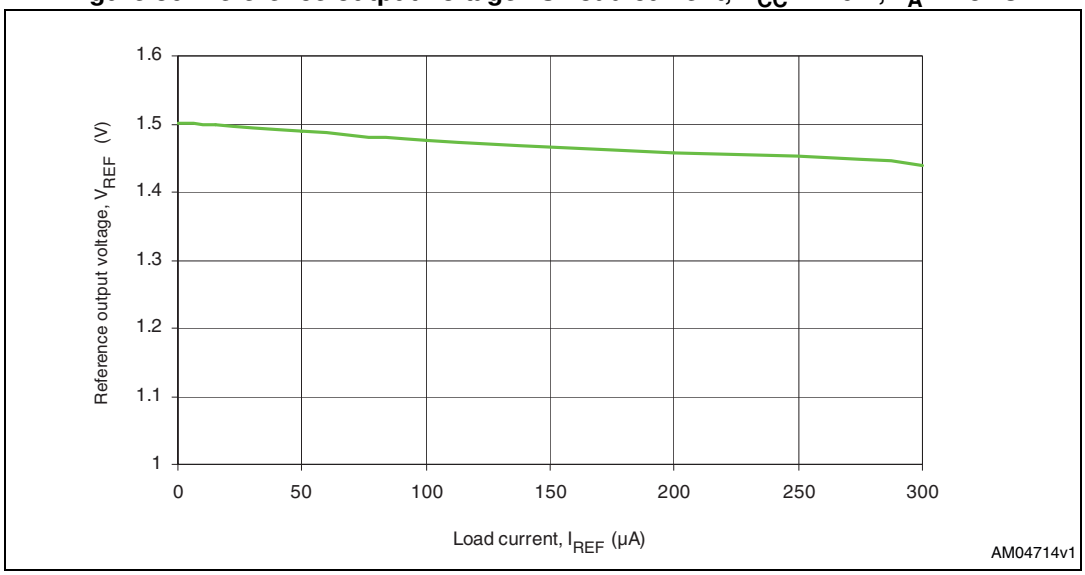
Note: Characteristics valid for $\overline{PB}$, $\overline{SR}$ and PS_{HOLD} inputs.

Figure 35. Reference output voltage vs. temperature, V_{CC} = 2.0 V



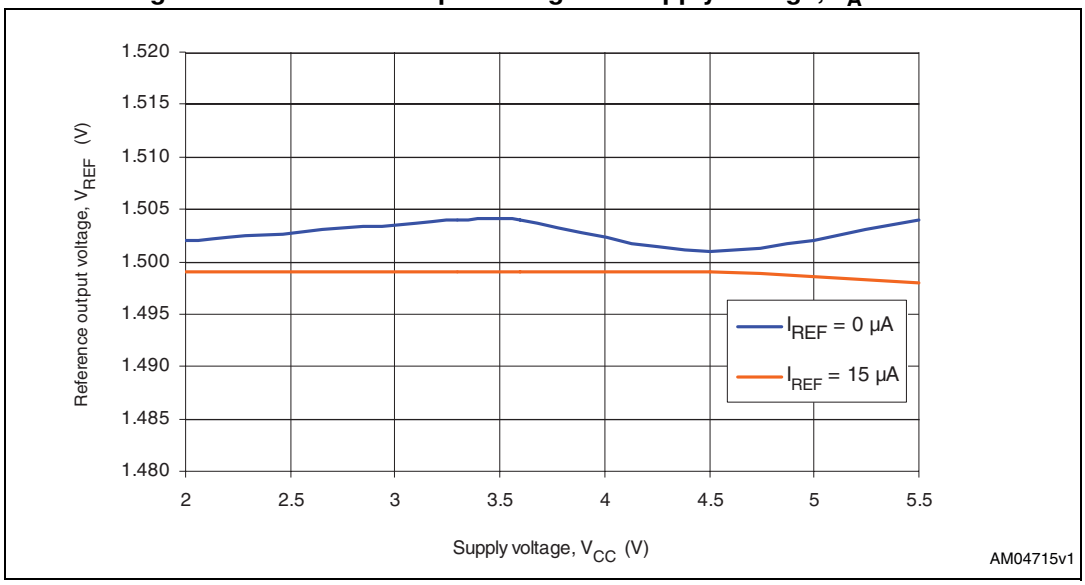
Note: 1 µF capacitor is connected to the V_{REF} pin.

Figure 36. Reference output voltage vs. load current, V_{CC} = 2.0 V, T_A = 25 °C



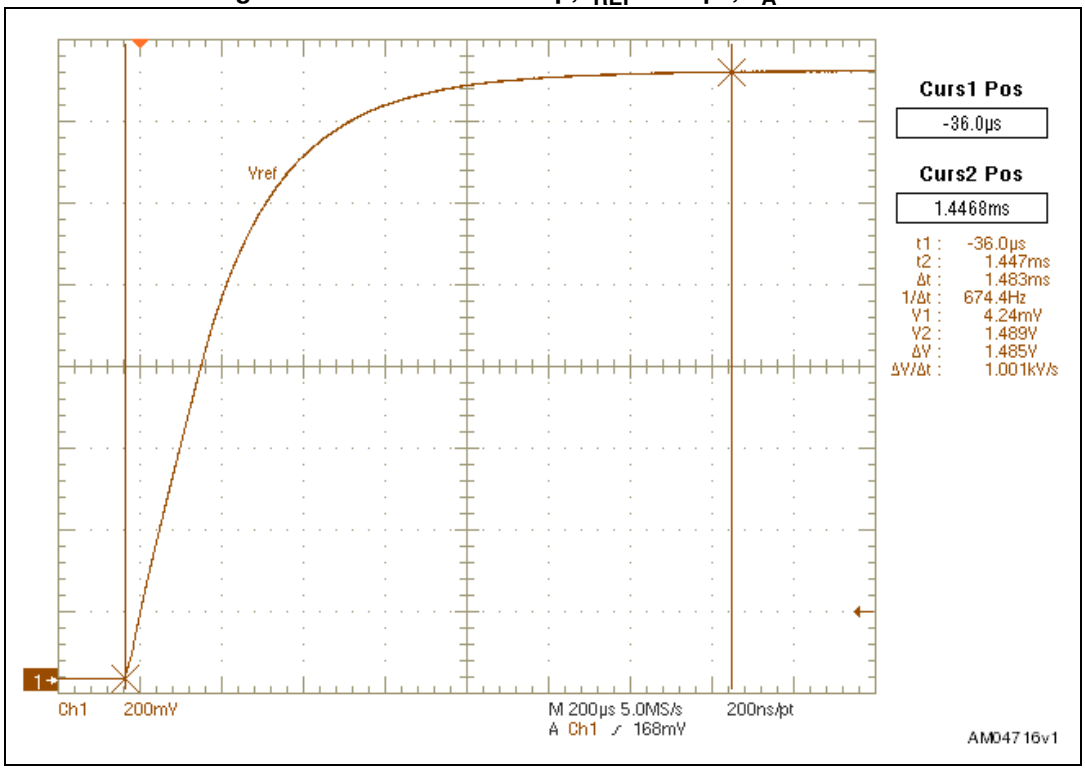
Note: 1 µF capacitor is connected to the V_{REF} pin.

Figure 37. Reference output voltage vs. supply voltage, T_A = 25 °C



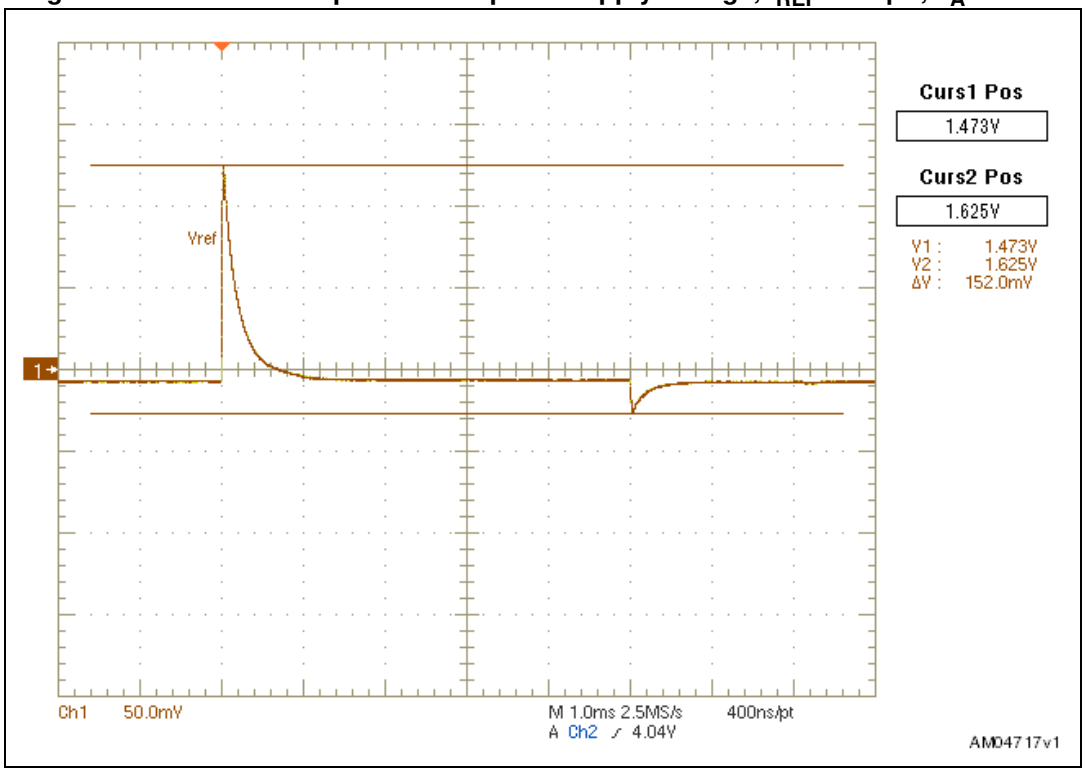
Note: 1 µF capacitor is connected to the V_{REF} pin.

Figure 38. Reference startup, I_{REF} = 15 µF, T_A = 25 °C



Note: 1 µF capacitor is connected to the V_{REF} pin.

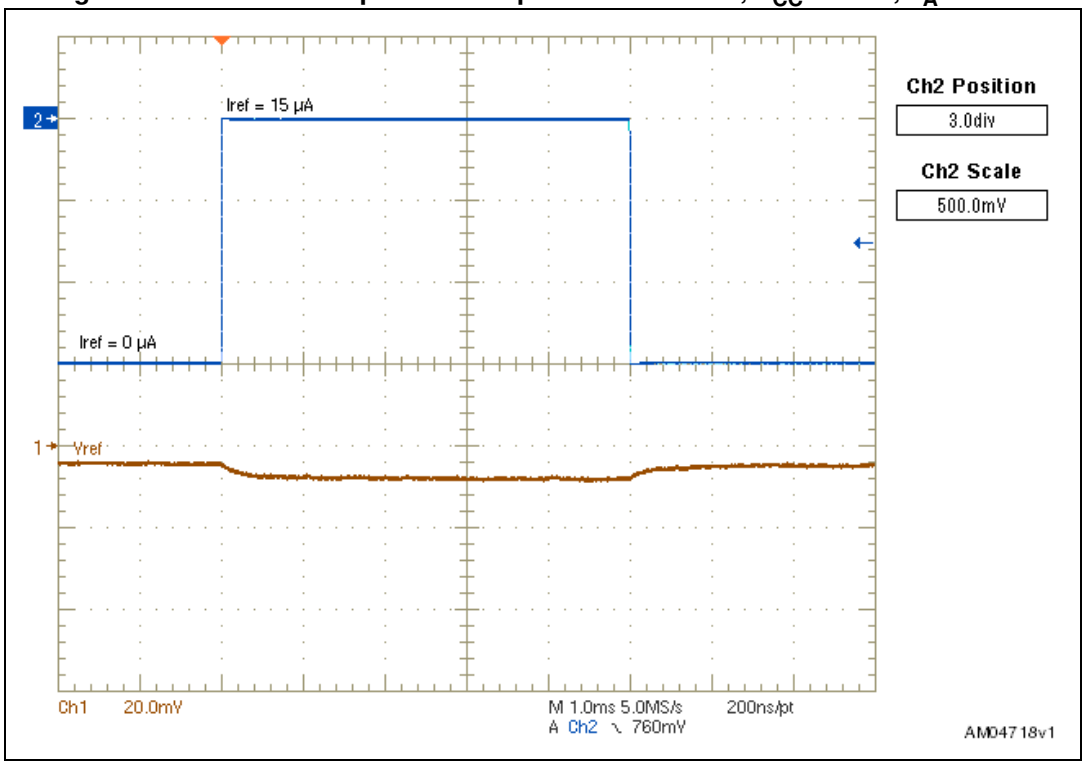
Figure 39. Reference response to steps on supply voltage, I_{REF} = 15 µA, T_A = 25 °C



Note: 1 Supply voltage goes from 3.6 V to 5.5 V and back to 3.6 V, ramp 1 V / 100 ns.

2 1 µF capacitor is connected to the V_{REF} pin.

Figure 40. Reference response to steps in load current, V_{CC} = 3.6 V, T_A = 25 °C



Note: 1 Supply voltage goes from 0 µA to 15 µA and back to 0 µA, ramp 1 µA / 100 ns.

2 1 µF capacitor is connected to the V_{REF} pin.

6 Maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 4* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit	Remarks
V_{CC}	Input supply voltage	–0.3	+7.0	V	
	Input voltages on $\overline{PB}$, $\overline{SR}$, PS_{HOLD} and C_{SRD}	–0.3	V_{CC} + 0.3	V	
	Output voltages on EN ($\overline{EN}$), $\overline{RST}$ and $\overline{INT}$	–0.3	V_{CC} + 0.3	V	
V_{ESD}	Electrostatic protection	–2	+2	kV	Human body model (all pins)
		–8	+8	kV	Human body model ($\overline{PB}$ and $\overline{SR}$)
V_{ESD}	Electrostatic protection	–1000	+1000	V	Charged device model
V_{ESD}	Electrostatic protection	–200	+200	V	Machine model
V_{ESD}	Point discharge on $\overline{PB}$ and $\overline{SR}$ inputs	–8	+8	kV	IEC61000-4-2
V_{ESD}	Air discharge on $\overline{PB}$ and $\overline{SR}$ inputs	–15	+15	kV	IEC61000-4-2
T_A	Operating ambient temperature	–40	+85	°C	
T_{STG}	Storage temperature	–45	+150	°C	
T_{SLD}(1)	Lead solder temperature for 10 seconds		+260	°C	
θ_{JA}	Thermal resistance (junction to ambient)		+132.4	°C/W	

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

7 DC and AC characteristics

This section summarizes the operating measurement conditions and the DC and AC characteristics of the device. The parameters in *Table 5* that follow are derived from tests performed under the measurement conditions summarized in *Table 4*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Condition	Unit
V_{CC} supply voltage	1.6 to 5.5	V
Ambient operating temperature (T_A)	–40 to 85	°C
Input rise and fall times	≤ 5	ns

Table 5. DC and AC characteristics

Symbol	Parameter	Test condition(1)	Min.	Typ.(2)	Max.	Unit
V_{CC}	Supply voltage		1.6		5.5	V
I_{CC}	Supply current	V_{CC} = 3.6 V, no load		6.0	8.0	µA
		Standby mode, enable deasserted, V_{CC} = 3.6 V		0.6	1.0	µA
V_{TH+}	Power-on lockout voltage		3.29	3.40	3.51	V
V_{HYST}	Threshold hysteresis			200		mV
				500		
V_{TH-}	Forced power-off voltage			$V_{TH+} - V_{HYST}$		V
t_{TH-}	Undervoltage detection to $\overline{INT}$ delay	$V_{CC} \geq 2.0$ V	20	32	44	ms
t_{ON_BLANK}	Blanking period (3)		1.4	2.2	3.0	s
			5.6	8.8	12.0	
			11.2	17.6	24.0	
	$\overline{RST}$ assertion to EN ($\overline{EN}$) assertion delay during power-up	V_{CC} = 3.6 V		100		ns
$\overline{PB}$						
V_{IL}	Input low voltage	$V_{CC} \geq 2.0$ V, enable asserted			0.99	V
V_{IH}	Input high voltage	$V_{CC} \geq 2.0$ V, enable asserted	1.05			V
$t_{DEBOUNCE}$	Debounce period	$V_{CC} \geq 2.0$ V	20	32	44	ms
$R_{\overline{PB}}$	Internal pull-up resistor	V_{CC} = 5.5 V, input asserted	65	100	135	kΩ

Table 5. DC and AC characteristics (continued)

Symbol	Parameter	Test condition(1)	Min.	Typ.(2)	Max.	Unit
$\overline{SR}$						
V_{IL}	Input low voltage				0.99	V
V_{IH}	Input high voltage		1.05			V
$t_{DEBOUNCE}$	Debounce period		20	32	44	ms
$R_{\overline{SR}}$(4)	Internal pull-up resistor	V_{CC} = 5.5 V, input asserted	65	100	135	kΩ
$\overline{PB}_{OUT}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{PB}_{OUT}$ asserted			0.3	V
	$\overline{PB}_{OUT}$ leakage current	$V_{\overline{PBOUT}}$ = 3 V, $\overline{PB}_{OUT}$ open drain	–0.1		+0.1	µA
$\overline{VCC}_{LO}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{VCC}_{LO}$ asserted			0.3	V
	$\overline{VCC}_{LO}$ leakage current	$V_{\overline{VCCLO}}$ = 3 V, $\overline{VCC}_{LO}$ open drain	–0.1		+0.1	µA
PS_{HOLD}						
V_{IL}	Input low voltage	$V_{CC} \geq$ 2.0 V			0.99	V
V_{IH}	Input high voltage	$V_{CC} \geq$ 2.0 V	1.05			V
	Glitch immunity		1	80		µs
	PS_{HOLD} leakage current	V_{PSHOLD} = 0.6 V	–0.1		0.1	µA
	PS_{HOLD} to enable propagation delay				30	µs
R_{PSHOLD}	Pull-down resistor connected internally during power-up	V_{PSHOLD} = 5.5 V	195	300	405	kΩ
C_{SRD}						
I_{SRD}	C_{SRD} charging current		100	150	200	nA
V_{SRD}	C_{SRD} voltage threshold	V_{CC} = 3.6 V, load on V_{REF} pin 100 kΩ and mandatory 1 µF capacitor, T_A = 25 °C		1.5		V
t_{SRD}	Additional Smart Reset™ delay time	External C_{SRD} connected		10		s/µF
EN, $\overline{EN}$						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, enable asserted			0.3	V

Table 5. DC and AC characteristics (continued)

Symbol	Parameter	Test condition(1)	Min.	Typ.(2)	Max.	Unit
V_{OH}(5)	Output high voltage	V_{CC} = 2 V, I_{SOURCE} = 1 mA, enable asserted	V_{CC} – 0.3			V
t_{EN_OFF}(6)	enable off to enable on	$V_{CC} \geq 2.0$ V	40	64	88	ms
	EN, $\overline{EN}$ leakage current	V_{EN} = 2 V, enable open drain	–0.1		+0.1	µA
RST						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{RST}$ asserted			0.3	V
t_{REC}	$\overline{RST}$ pulse width	$V_{CC} \geq 2.0$ V	240	360	480	ms
	$\overline{RST}$ leakage current	$V_{\overline{RST}}$ = 3V	–0.1		+0.1	µA
INT						
V_{OL}	Output low voltage	V_{CC} = 2 V, I_{SINK} = 1 mA, $\overline{INT}$ asserted			0.3	V
$t_{\overline{INT}\_Min}$	Minimum $\overline{INT}$ pulse width	$V_{CC} \geq 2.0$ V	20	32	44	ms
	$\overline{INT}$ leakage current	$V_{\overline{INT}}$ = 3 V	–0.1		+0.1	µA
V_{REF}						
V_{REF}	1.5 V voltage reference	V_{CC} = 3.6 V, load on V_{REF} pin 100 kΩ and mandatory 1 µF capacitor, T_A = 25 °C	1.485 –1%	1.5	1.515 +1%	V

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.6 V to 5.5 V (except where noted).
2. Typical values are at T_A = +25 °C.
3. This blanking time allows the processor to start up correctly (see *Figure 7*, *8*, *9*, *10*, *11*, *12*).
4. The internal pull-up resistor connected to the $\overline{SR}$ input is optional.
5. Valid for push-pull only.
6. Minimum delay time between enable deassertion and enable reassertion, allowing the application to complete the power-down properly. PB is ignored during this period.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 41. TDFN12 (2 x 3 mm) package outline

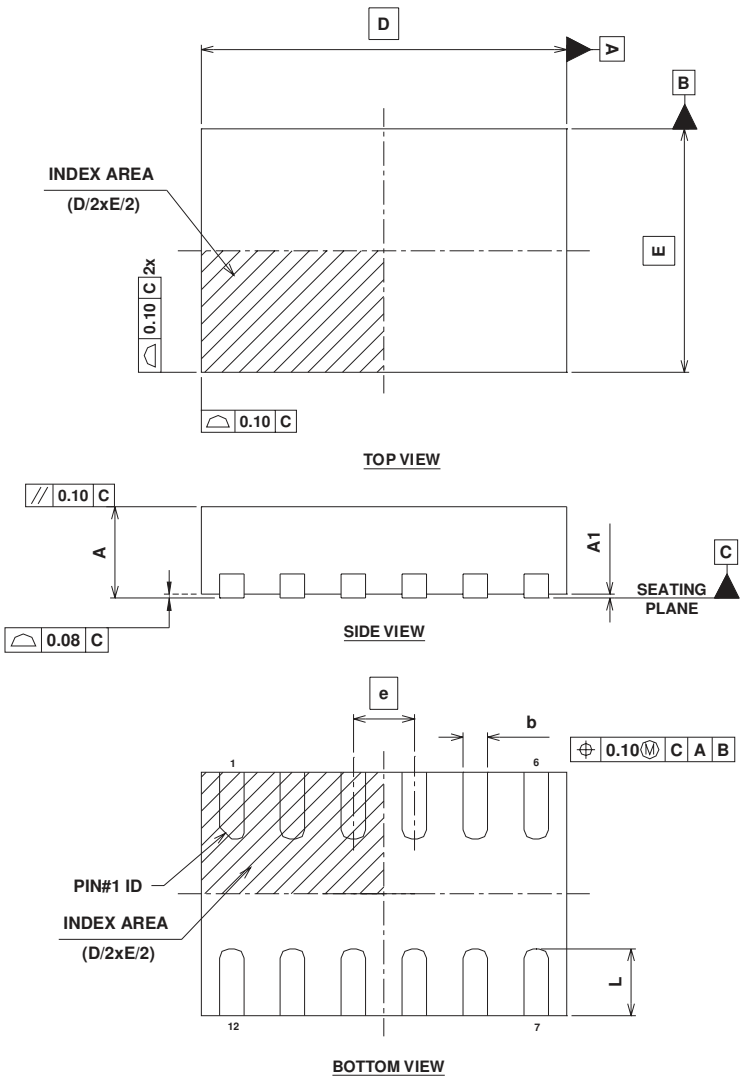
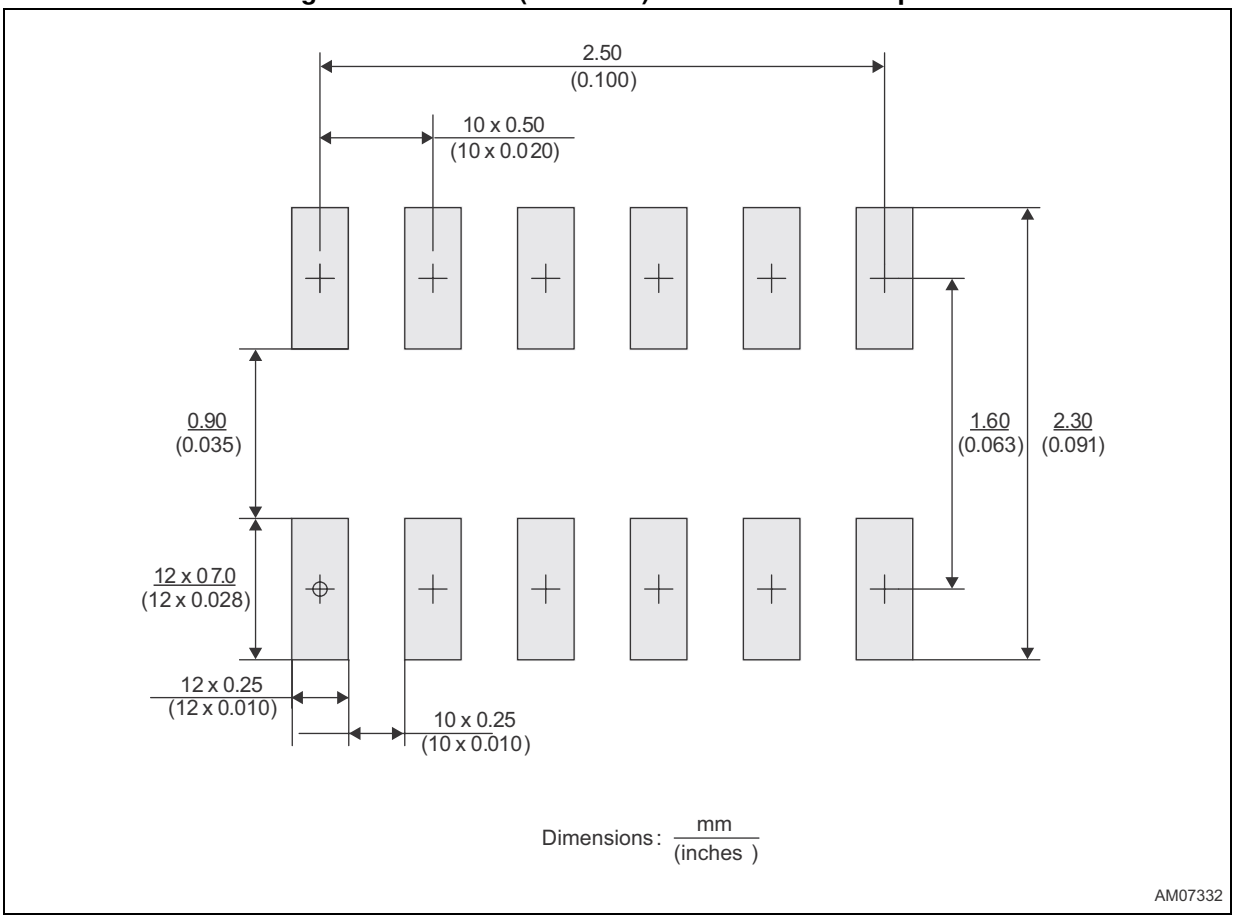


Table 6. TDFN12 (2 x 3 mm) package mechanical data

Symbol	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		3.00 BSC			0.118	
E		2.00 BSC			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

Figure 42. TDFN12 (2 x 3 mm) recommended footprint



Note: Drawing not to scale.

Figure 43. Carrier tape for TDFN12 (2 x 3 mm) package

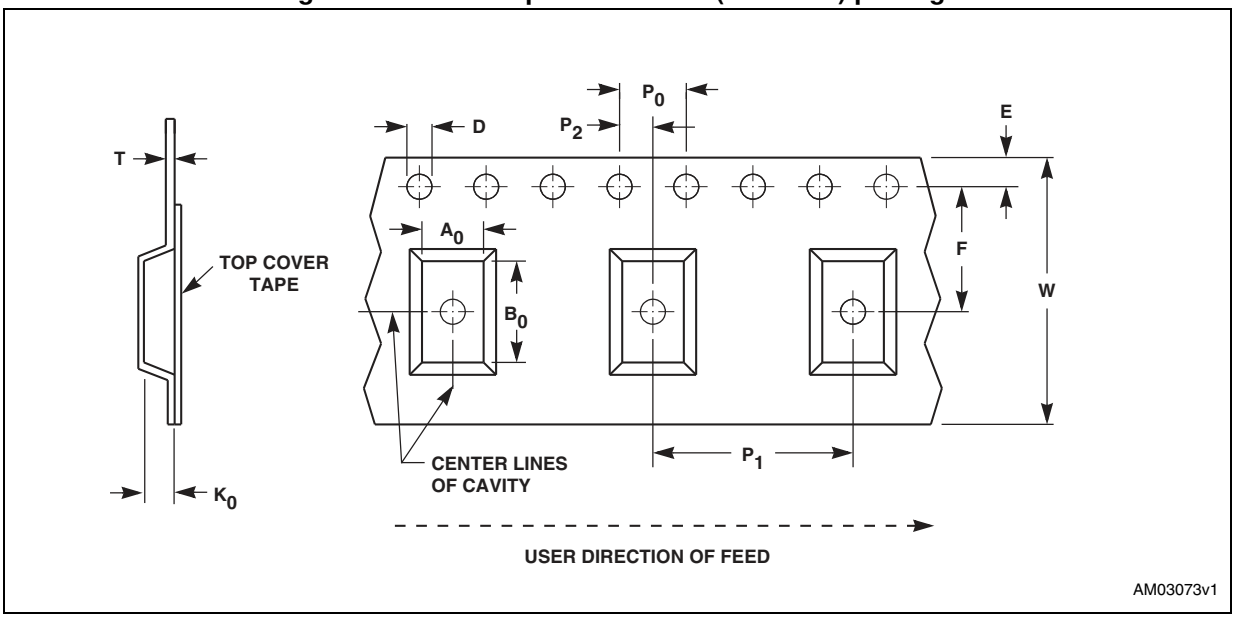


Table 7. Carrier tape dimensions for TDFN12 (2 x 3 mm) package

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk qty.
TDFN12	12.00 ±0.30	1.50 +0.10/ −0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	2.30 ±0.10	3.20 ±0.10	1.10 ±0.01	4.00 ±0.10	0.30 ±0.05	mm	3000

9 Product selector

Table 8. SRC0 product selector

Full part number	EN or $\overline{EN}$[1]	After long push[2]	Internal resistor on $\overline{SR}$ input	Power-on lockout voltage V_{TH+} (V)	Forced power-off voltage V_{TH-} (V)	t_{ON_BLANK} (s) at startup (min.)	Ft_{ON_BLANK} (s) at reset (min.)	Top marking[3]
SRC0CS25D	EN	$\overline{RST}$	pull-up	3.40	3.20	11.2	—	CS25
SRC0GS22D[4]	EN	EN	—	3.40	3.20	1.4	—	GS22

1. EN (or $\overline{EN}$) output is push-pull. $\overline{RST}$, $\overline{INT}$, $\overline{PB}_{OUT}$ and $\overline{VCC}_{LO}$ outputs are open drain.
2. After t_{SRD} expires through long push, either device reset ($\overline{RST}$) will be activated for t_{REC} (240 ms min.) or the EN (or $\overline{EN}$) pin will be deasserted. The additional Smart Reset™ delay time, t_{SRD}, can be adjusted by the user at 10 s/µF (typ.) by connecting the external capacitor to the C_{SRD} pin.
3. Where “p” = assembly plant, “y” = assembly year (0 to 9) and “ww” = assembly work week (01 to 52).
4. Please contact local ST sales office for availability.

10 Revision history

Table 9. Document revision history

Date	Revision	Changes
04-Mar-2014	1	Initial release.
13-May-2014	2	Modified: V_{TH+} values Table 5 on page 39.
16-May-2023	3	Updated *Figure 5*.