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DATA SHEET
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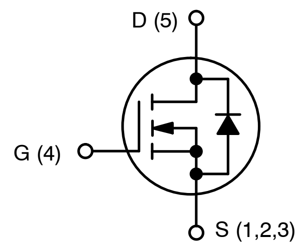
MOSFET – Power, Single N-Channel

100 V, 14 mΩ, 46 A

NVMYS016N10MCL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
100 V	14 mΩ @ 10 V	46 A
	20 mΩ @ 4.5 V	



N−CHANNEL MOSFET

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	46	A
		T_C = 100°C		32	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	64	W
		T_C = 100°C		32	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	10.9	A
		T_A = 100°C		7.7	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.6	W
		T_A = 100°C		1.8	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	264	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	49	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 2.2 A)			E_{AS}	358	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

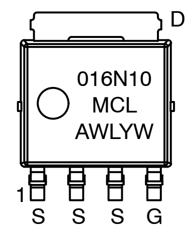
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	2.35	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz. Cu pad.

LFPAK4
CASE 760AB

MARKING DIAGRAM



016N10MCL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

June, 2022 − Rev. 1

Publication Order Number:
NVMYS016N10MCL/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			60		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V	T_J = 25°C			1	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 64 μA		1		3	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 64 μA, ref to 25°C			−5.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 11 A			11.5	14	mΩ
		V_{GS} = 4.5 V, I_D = 9 A			16	20	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 11 A			42		S
Gate−Resistance	R_G	T_A = 25°C			1.2		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V			1250		pF
Output Capacitance	C_{OSS}				460		
Reverse Transfer Capacitance	C_{RSS}				8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 50 V, I_D = 11 A			9.0		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 11 A			19		
Threshold Gate Charge	$Q_{G(TH)}$				2.1		
Gate−to−Source Charge	Q_{GS}				3.7		
Gate−to−Drain Charge	Q_{GD}				2.0		
Plateau Voltage	V_{GP}				2.8		V
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 11 A, R_G = 6 Ω			10		ns
Rise Time	t_r				3.4		
Turn−Off Delay Time	$t_{d(OFF)}$				26		
Fall Time	t_f				4.2		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 11 A	T_J = 25°C		0.84	1.3	V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 6 A			34		ns
Reverse Recovery Charge	Q_{RR}				24		nC
Charge Time	t_a				16		ns
Discharge Time	t_b				17		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

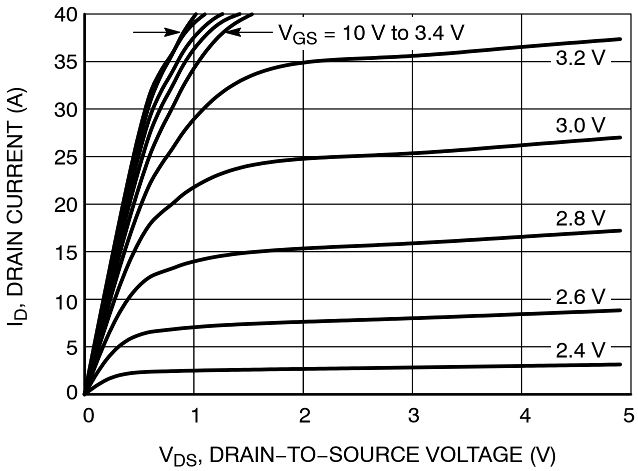


Figure 1. On−Region Characteristics

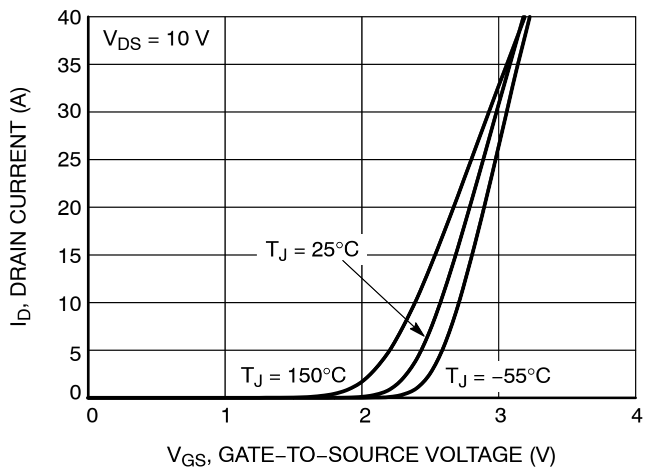


Figure 2. Transfer Characteristics

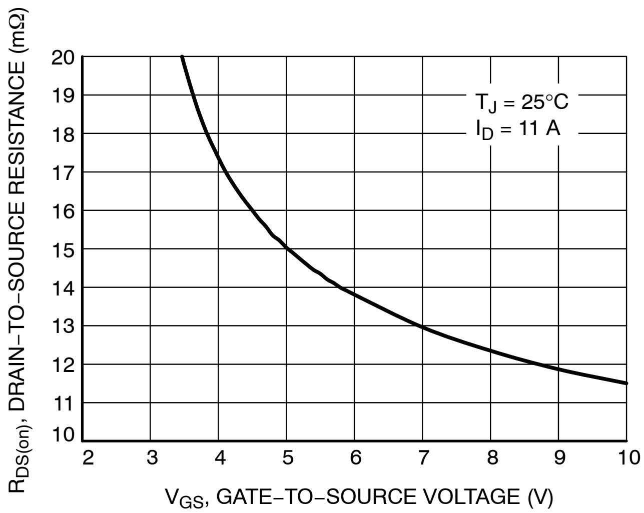


Figure 3. On−Resistance vs. Gate−to−Source Voltage

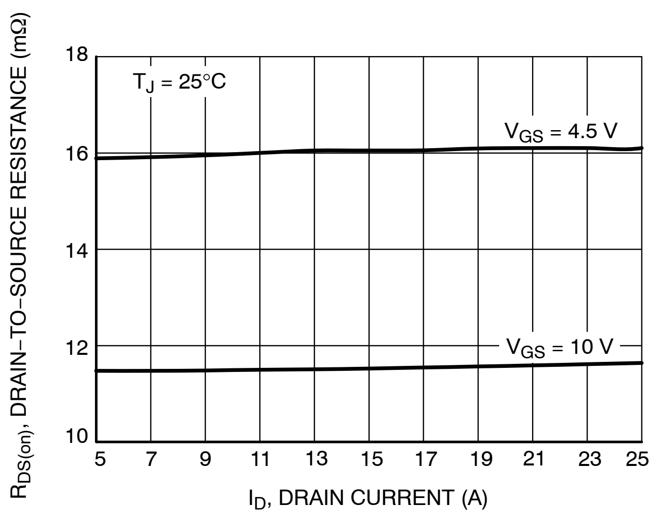


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

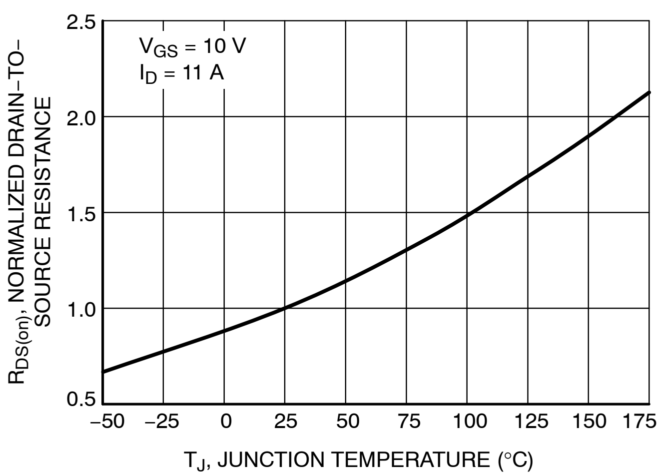


Figure 5. On−Resistance Variation with Temperature

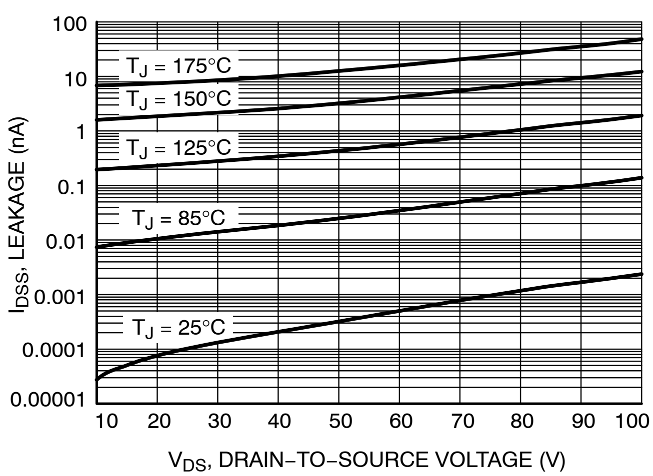


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

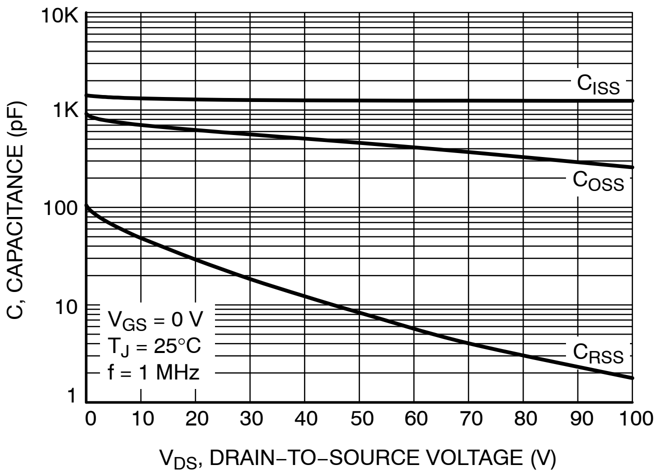


Figure 7. Capacitance Variation

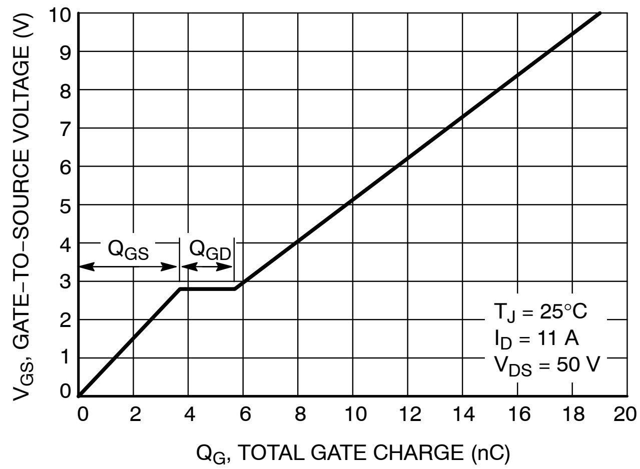


Figure 8. Gate−to−Source Voltage vs. Total Charge

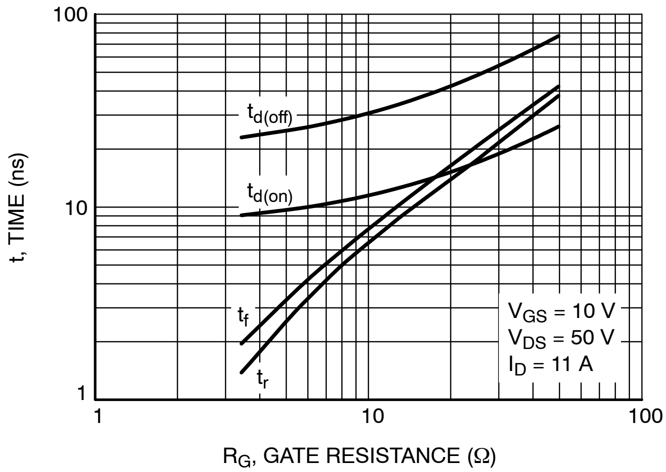


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

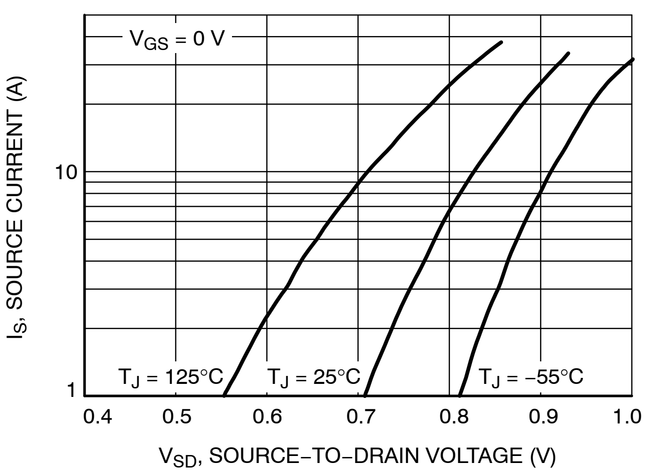


Figure 10. Diode Forward Voltage vs. Current

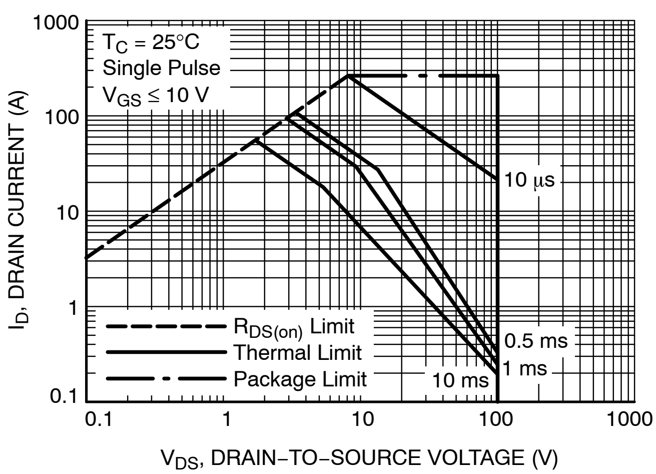


Figure 11. Maximum Rated Forward Biased Safe Operating Area

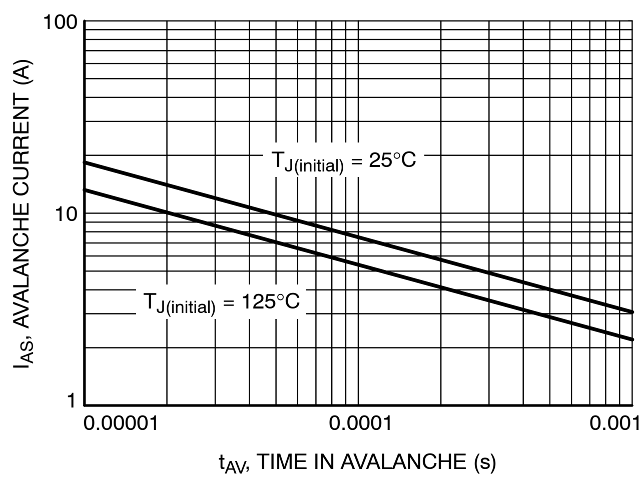


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

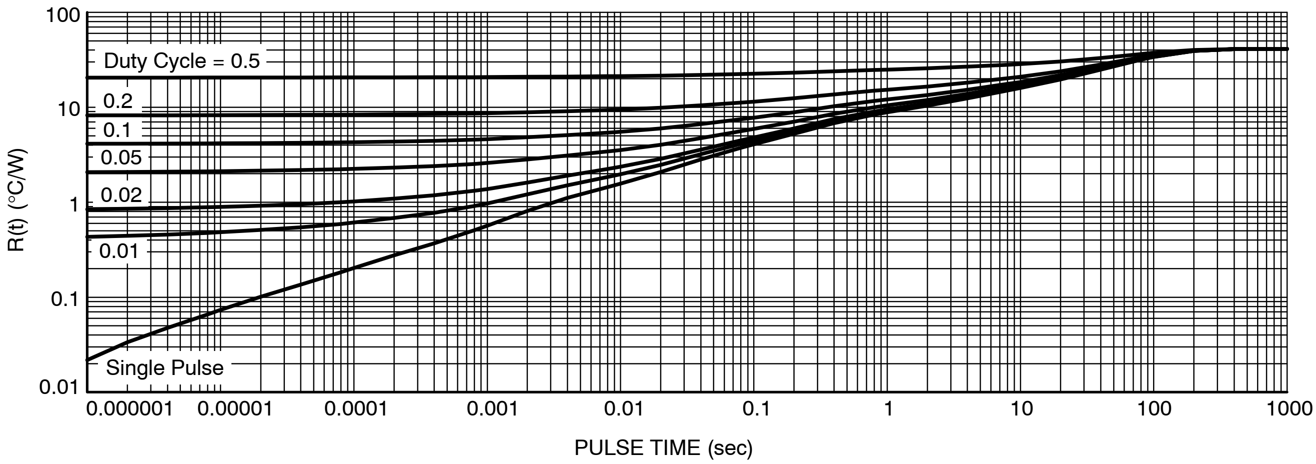


Figure 13. Transient Thermal Impedance

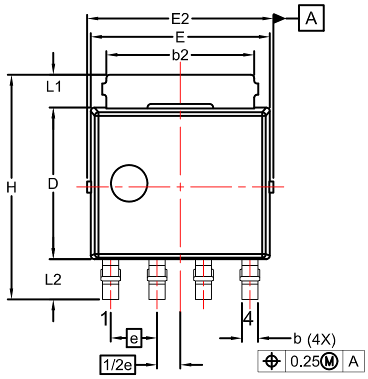
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMYS016N10MCLTWG	016N10MCL	LFPAK4 (Pb−Free)	3000 / Tape & Reel

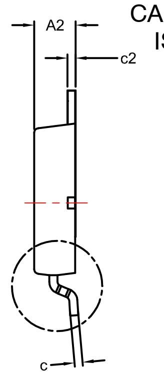
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

LFPAK4 5x6
CASE 760AB
ISSUE C

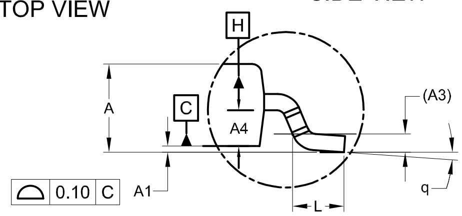


TOP VIEW

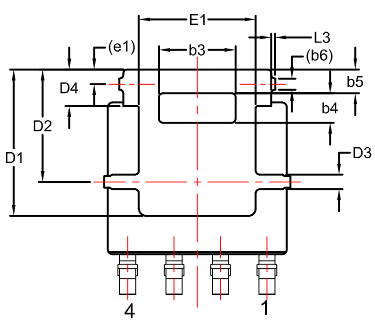


SIDE VIEW

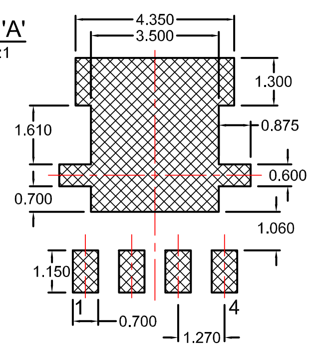
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.



DETAIL 'A'
SCALE: 2:1



BOTTOM VIEW



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3		0.25 REF	
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b3	2.00	2.10	2.20
b4	0.70	0.80	0.90
b5	0.55	0.65	0.75
b6		0.31 REF	
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.05	4.15	4.25
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
E	4.80	4.90	5.00
E1	3.10	3.20	3.30
E2	5.00	5.15	5.30
e		1.27 BSC	
1/2e		0.635 BSC	
e1		0.40 REF	
H	6.00	6.15	6.30
L	0.40	0.65	0.85
L1	0.80	0.90	1.00
L2	0.90	1.10	1.30
L3	0.00	0.10	0.20
q	0°	4°	8°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
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