Description

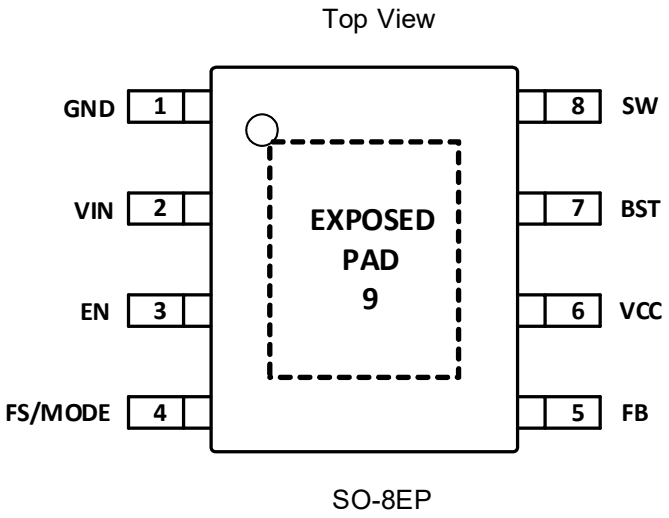
The AP680650Q/AP680651Q and AP681050Q/AP681051Q are adjustable switching frequency, constant-on-time control, DC-DC buck converters. These devices can adjust the switching frequency from 300kHz to 600kHz. The AP680652Q and AP680652Q can program the MODE while operating at fixed 300kHz frequency. The devices fully integrate a 530mΩ high-side and 220mΩ low-side power MOSFETs to provide highly efficient step-down DC-DC conversion.

The AP68065XQ/AP68105XQ enable continuous load current of up to 1A with as high as 92% efficiency. The devices can be easily used by minimizing the external component count due to their adoption of Constant On-Time (COT) control to achieve fast transient response, easy loop stabilization, and low output voltage ripple.

With their high level of integration and minimal need for external components, the AP68065XQ/AP68105XQ simplify board layout and reduce space requirements. This makes them ideal for distributed power architecture.

AP68065XQ/AP68105XQ are available in the standard Green SO-8EP package.

Pin Assignments



Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to +125°C T_A
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C3B
- Functional Safety-Capable ISO26262 – Documentation Available to Aid Functional Safety System Design
- V_{IN} 4.5V to 80V
- V_{OUT} Adjustable from 1.2V to 50V
- 1.2V ±1% Vref
- 0.6A and 1A Continuous Output Current
- Adjustable Switching Frequency Options
- Programmable MODE Options
- Overcurrent Protection (OCP) with Hiccup
- Thermal Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP68065XQ/AP68105XQ are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Applications

- General-purpose point-of-load DC/DC power conversion
- Automotive infotainment
- Battery power applications
- In-dash instrumentation
- Navigation systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit

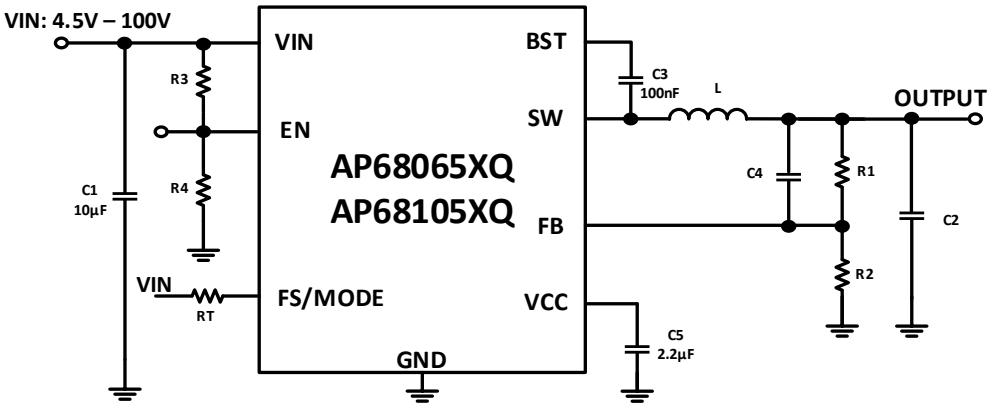


Figure 1. Typical Application Circuit

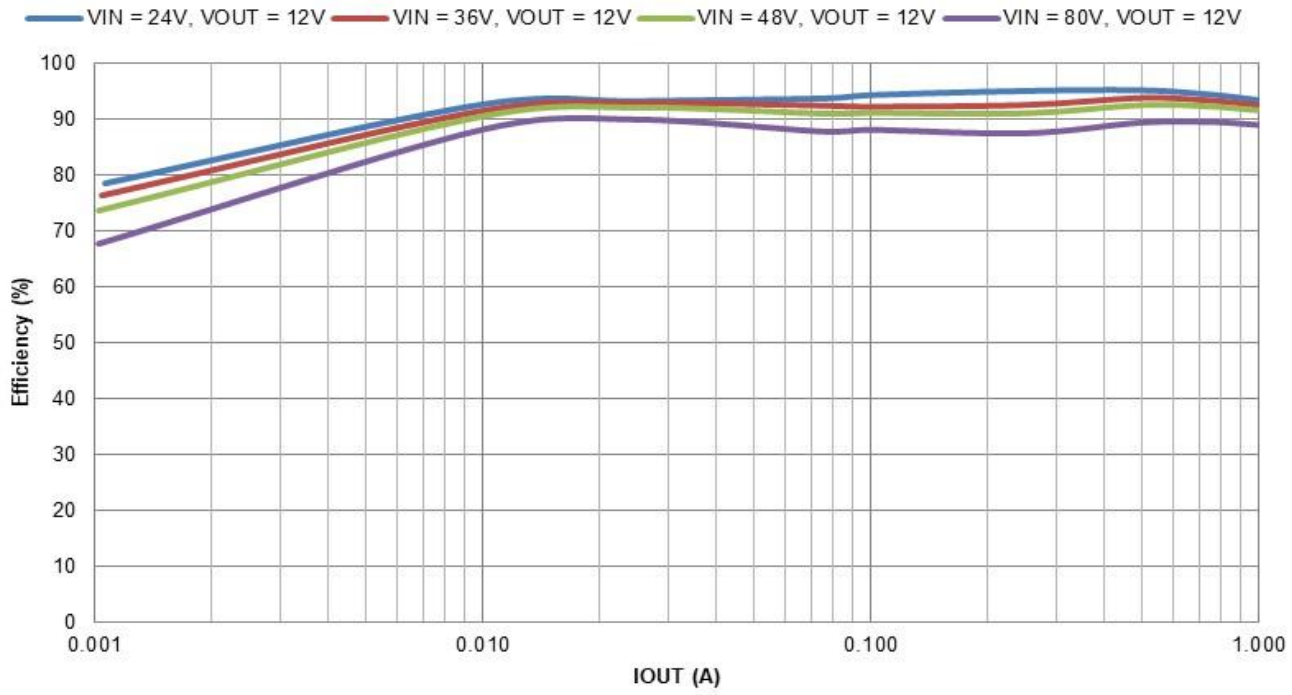


Figure 2. Efficiency vs. Output Current, f_{SW} = 300kHz, L = 68µH

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Pin Descriptions

Pin Name	Pin Number	Function
GND	1	Analog ground that is used for the controller. Single point connection to the EPAD.
VIN	2	Power Input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.5V to 80V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*.
EN	3	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator and low to turn it off. Connect directly to VIN for automatic startup.
FS	4 (AP680650Q/ AP680651Q/ AP681050Q/ AP681051Q)	Set the internal oscillator clock frequency. Connect a resistor from this pin to VIN to set switching frequency.
MODE	4 (AP680652Q/ AP681052Q)	PFM, USM and PWM mode selection. a) Connect the pin to VCC by a resistor (for example 10K) will force the device in Forced Pulse-Width Modulation (PWM mode). b) Ground the pin to operate the device in Pulse-Frequency Modulation (PFM mode) c) Floating the pin to operate the device in Ultrasonic Modulation (USM mode).
FB	5	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive divider connected to it from the output voltage to this pin. The feedback regulation voltage is 1.2V. See *Setting the Output Voltage*.
VCC	6	Output from the Internal High Voltage Regulator. The internal VCC regulator provides bias supply for the gate drivers and other internal circuitry. A larger than 1μF decoupling capacitor is needed, recommended 2.2μF.
BST	7	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side n-channel MOSFET with a 0.1μF or greater capacitor from SW to BST to power the high-side switch.
SW	8	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
EPAD	9	Heat Dissipation Path of Die. Electrical connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

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Functional Block Diagram

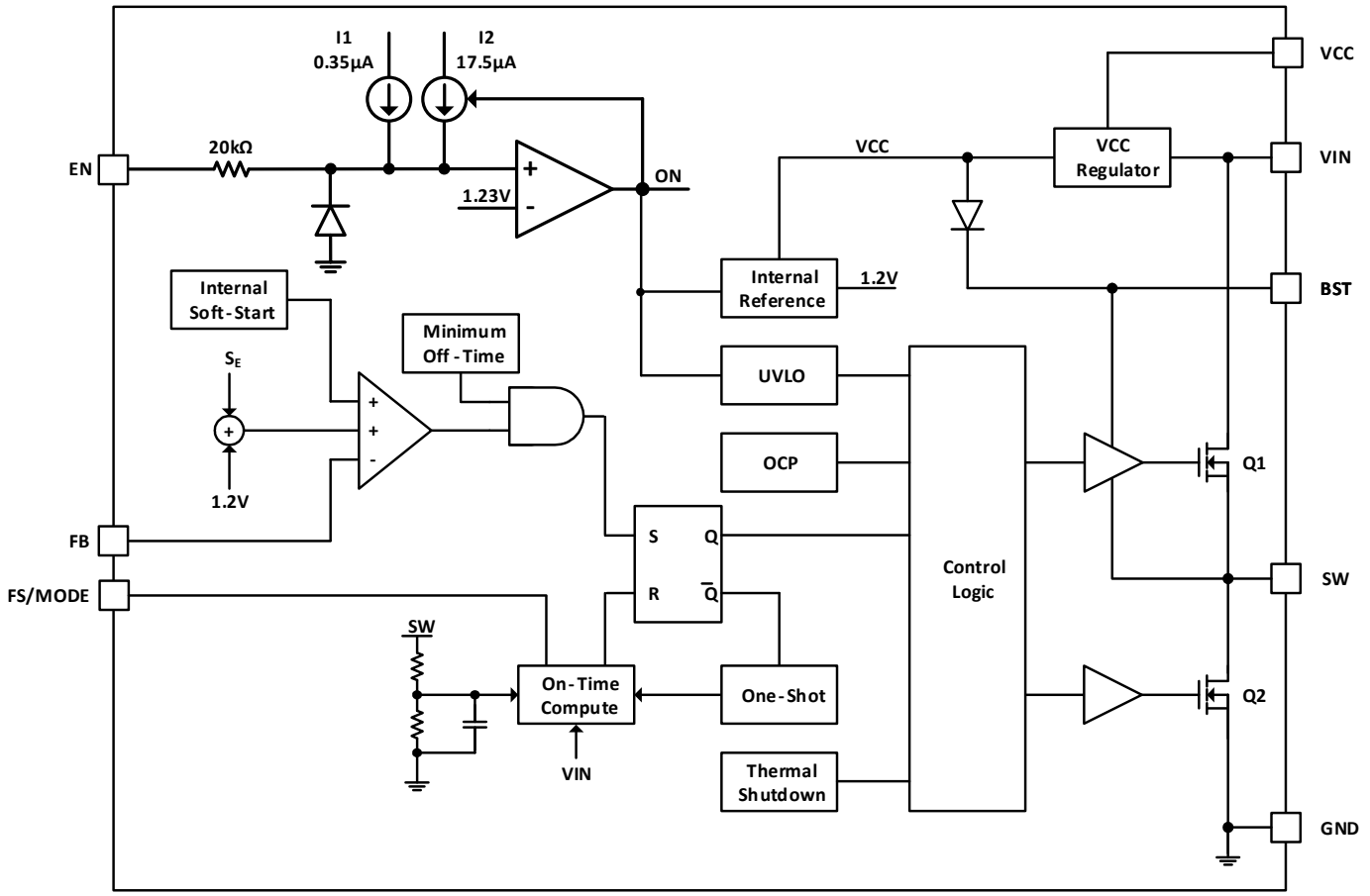


Figure 3. Functional Block Diagram

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Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +105	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} +0.3 (DC)	V
		-2.5 to V_{IN} +5 (ns)	V
V_{EN}	Enable/UVLO Voltage	-0.3V to +105	V
V_{BST}	Bootstrap Voltage	V_{SW} -0.3 to V_{SW} +6.0	V
V_{FB}	Feedback Voltage	-0.3V to +6.0	V
V_{FS}	Frequency Adjust	-0.3V to +6.0	V
V_{CC}	LDO Voltage	-0.3V to +30.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+300	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±1000	V
CDM	Charged Device Model	±1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Information (Note 6)

Symbol	Parameter	Rating		Unit
θ_{JA}	Junction to Ambient	SO-8EP	39	°C/W
$\theta_{JC(TOP)}$	Junction to Case (Top)	SO-8EP	13	°C/W
θ_{JB}	Junction to Board (Bottom)	SO-8EP	13	°C/W
ψ_{JT}	Junction to Top Characterization Parameter	SO-8EP	4.5	°C/W
ψ_{JB}	Junction to Board Characterization Parameter	SO-8EP	12.5	°C/W
$\theta_{JC(BOT)}$	Junction to Case (Bottom)	SO-8EP	3.5	°C/W

Note: 6. Device mounted on FR-4 substrate, JEDEC 4 layer 50mm x 50mm PCB board (2oz copper), with minimum recommended pad layout.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.) (Note 7)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	4.5	80	V
V_{OUT}	Output Voltage	1.2	50	V
T_J	Operating Junction Temperature Range	-40	+150	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

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Electrical Characteristics (T_A = +25°C, V_{IN} = 48V, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +150°C, and input range from 4.5V to 80V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
UVLO	VCC Undervoltage Lockout Threshold	—	—	4.1	4.48	V
	Hysteresis	—	—	220	—	mV
VCC	VCC Regulator Output Voltage	V_{IN} > 9V	—	7.3	—	V
I_{VCC}	VCC Internal LDO Current Limit	—	—	30	—	mA
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0, no load	—	3.0	—	μA
I_Q	Supply Current (Quiescent)	EN floating, no load, non-switching, BOOT-SW = 5V, PFM	—	150	250	μA
$R_{DS(ON)1}$	High-Side Switch On-Resistance	—	—	530	—	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance	—	—	220	—	mΩ
I_{LIMIT}	HS MOSFET Positive Current Limit	AP680650Q/AP680651Q/AP680652Q, from drain to source	—	1.7	—	A
		AP681050Q/AP681051Q/AP681052Q, from drain to source	—	2.5	—	A
I_{LIMIT_LS}	LS MOSFET Current Limit	From source to drain	—	1.3	—	A
I_{LIMIT_LS}	LS MOSFET Current Limit	AP680652Q/AP681052Q, from drain to source	—	3.0	—	A
V_{FB}	Feedback Voltage	—	1.182	1.2	1.218	V
t_{SS}	Soft-Start Period	—	—	4	—	ms
f_{RANGE_RT}	Frequency Range Using RT Mode	AP680650Q/AP680651Q/ AP681051Q/AP681051Q	100	—	600	kHz
f_S	Switching Frequency	AP680652Q/AP681052Q	270	300	330	kHz
t_{ON}	On-Time	V_{IN} = 24V, RT = 100kΩ (1%)	—	420	—	ns
t_{OFF_MIN}	Minimum Off-Time	V_{IN} = 12V	—	200	260	ns
V_{EN_TH}	EN Rising Threshold	—	—	1.23	—	V
	Hysteresis	—	—	10	—	mV
I_{EN_TH}	Enable Pin Pullup Current	EN = 1V	—	0.35	—	μA
		EN = 1.5V	—	17.8	—	μA
V_{MODE_PFM}	PFM Mode Logic Threshold	V_{MODE} = GND, AP680652Q/AP681052Q	—	—	0.5	V
V_{MODE_USM}	Ultrasonic Mode Logic Threshold	V_{MODE} = Floating, AP680652Q/AP681052Q	1.5	2.5	3.4	V
V_{MODE_PWM}	PWM Mode Logic Threshold	V_{MODE} = VCC, AP680652Q/AP681052Q	4.65	—	—	V
V_{OVP}	Feedback Overvoltage with Respect to Reference Voltage	V_{FB} / V_{REF} rising	—	110	—	%
		V_{FB} / V_{REF} falling	—	105	—	%
T_{SHDN}	Thermal Shutdown (Note 8)	—	—	+173	—	°C
T_{HYS}	Thermal Hysteresis (Note 8)	—	—	+25	—	°C

Note: 8. Compliance with the datasheet limits assured by one or more methods: production test, characterization, and/or design.

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Typical Performance Characteristics (AP68065XQ/AP68105XQ @ T_A = +25°C, VIN = 48V, VOUT = 5V, f_{SW} = 300kHz, BOM = Table 1, unless otherwise specified.)

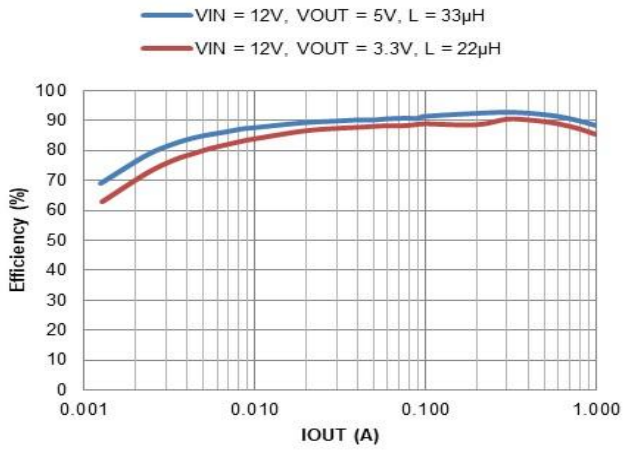


Figure 4. Efficiency vs. Output Current, VIN = 12V

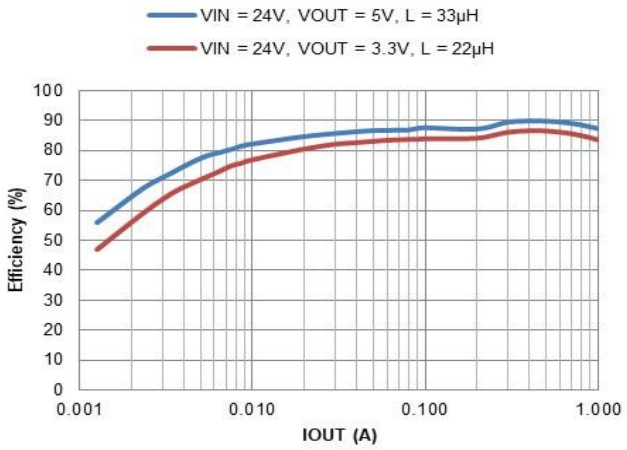


Figure 5. Efficiency vs. Output Current, VIN = 24V

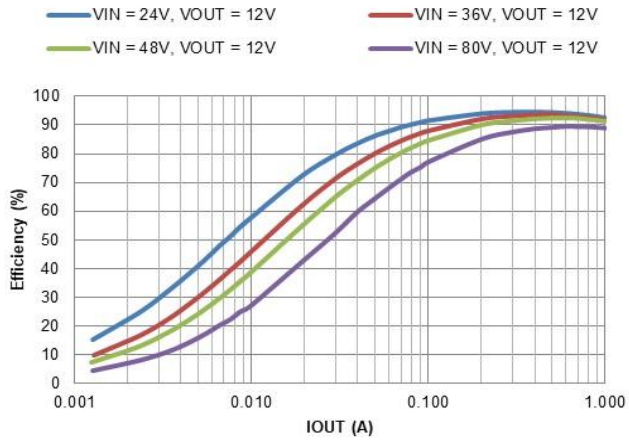


Figure 6. Efficiency PWM Mode, L = 68µH

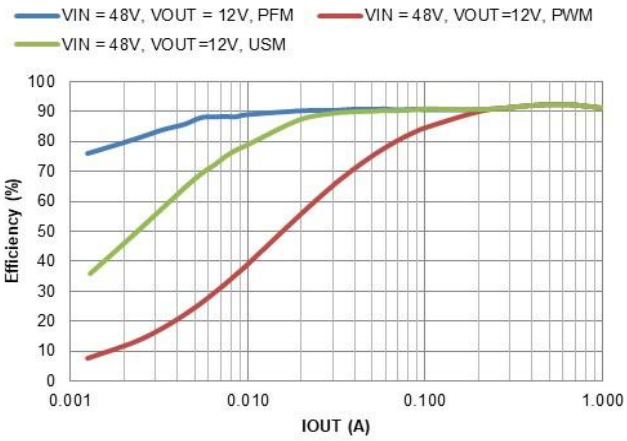


Figure 7. Efficiency PFM, PWM, USM Mode, L = 68µH

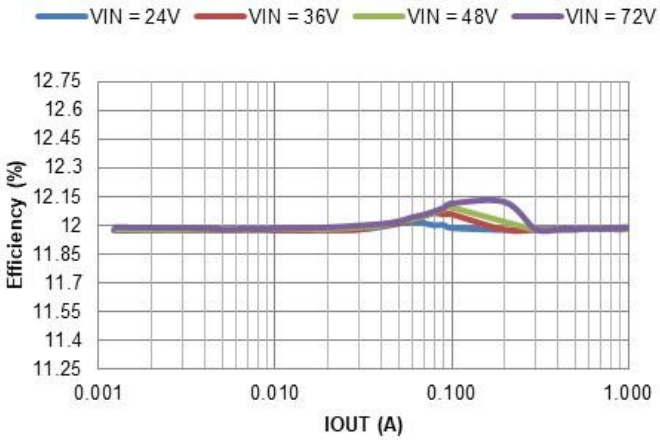


Figure 8. Load Regulation

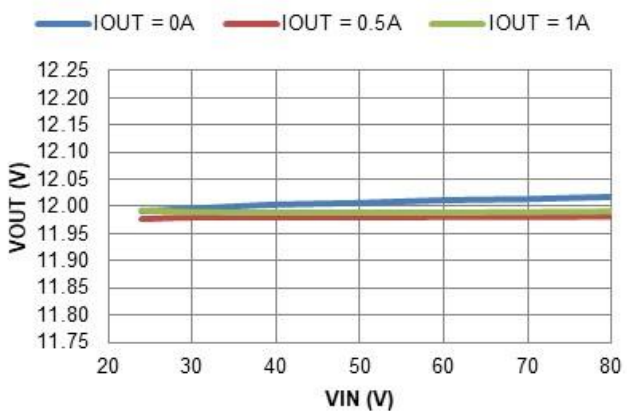


Figure 9. Line Regulation

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Typical Performance Characteristics (AP68065XQ/AP68105XQ @ T_A = +25°C, VIN = 48V, VOUT = 5V, f_{SW} = 300kHz, BOM = Table 1, unless otherwise specified.) (continued)

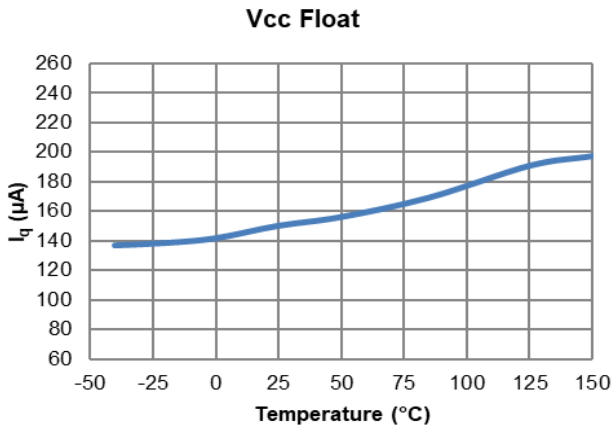


Figure 10. I_Q vs. Temperature, V_{EN} = Float, V_{BST-SW} = 5V, Vcc Float

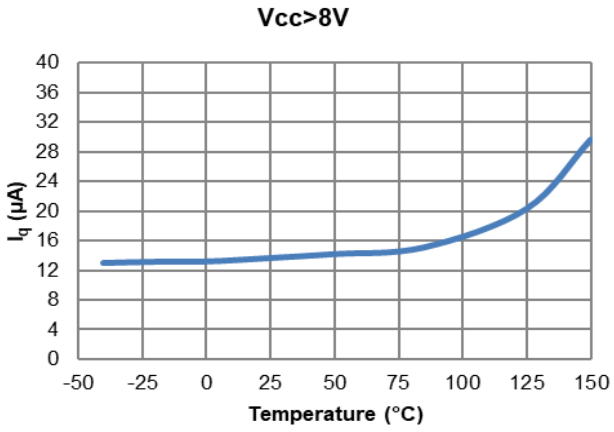


Figure 11. I_Q vs. Temperature, V_{EN} = Float, V_{BST-SW} = 5V, Vcc > 8V

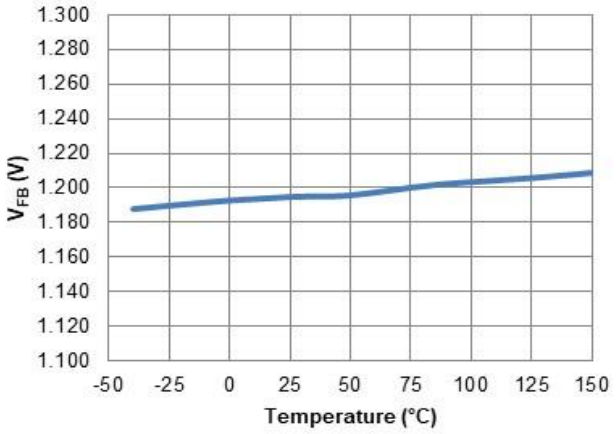


Figure 12. Feedback Voltage vs. Temperature, IOUT = 0

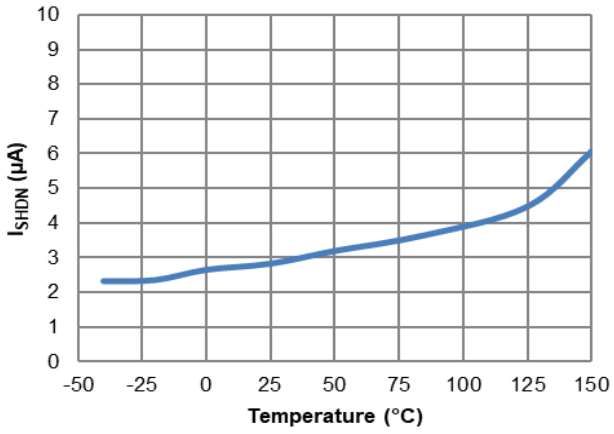


Figure 13. I_{SHDN} vs. Temperature, V_{EN} = 0, IOUT = 0

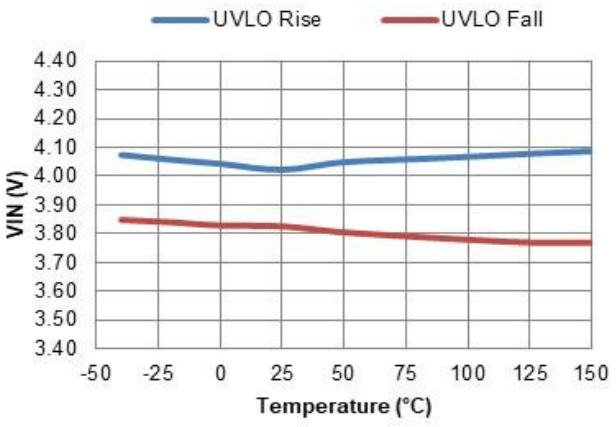


Figure 14. VIN POR and UVLO vs. Temperature

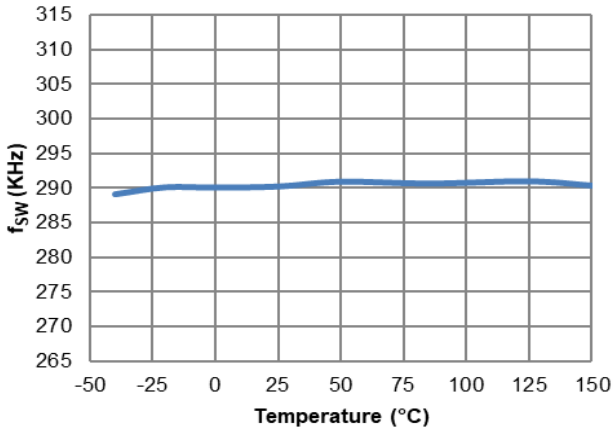


Figure 15. f_{SW} vs. Temperature, FPWM Mode

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Typical Performance Characteristics (AP68065XQ/AP68105XQ @ T_A = +25°C, VIN = 48V, VOUT = 5V, f_{SW} = 300kHz, BOM = Table 1, unless otherwise specified.) (continued)

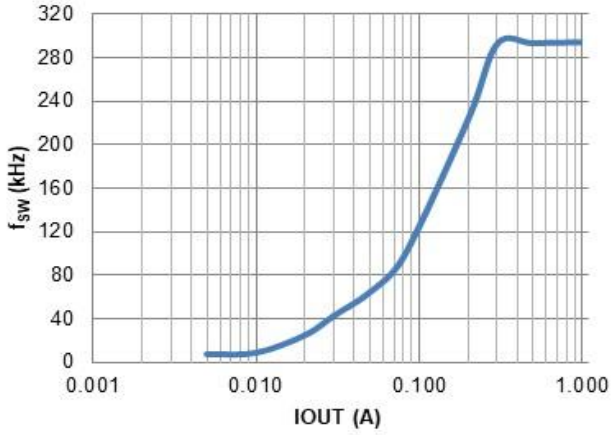


Figure 16. f_{SW} vs. Load

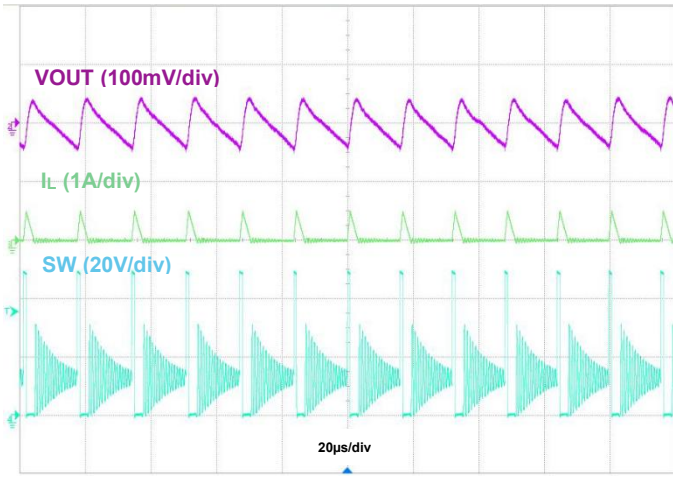


Figure 17. Output Voltage Ripple, IOUT = 50mA

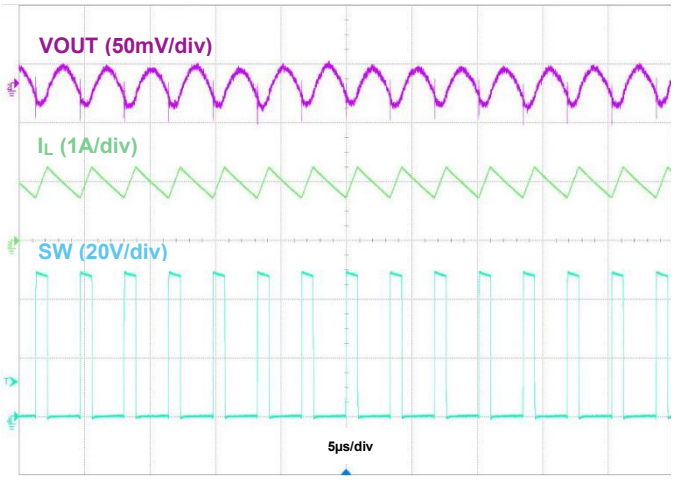


Figure 18. Output Voltage Ripple, IOUT = 1A

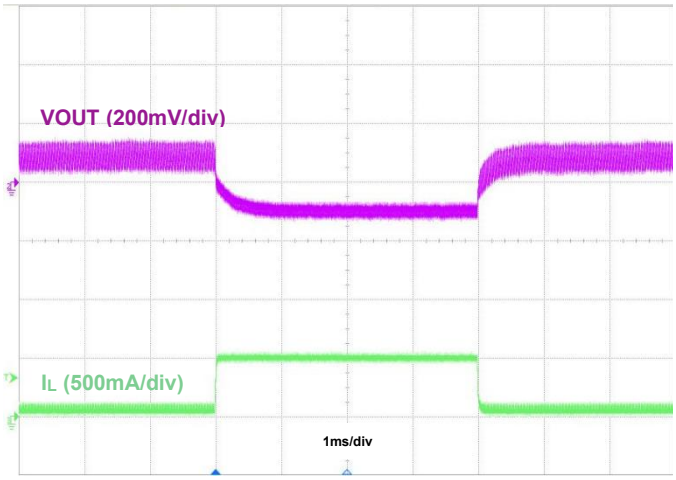


Figure 19. Load Transient, IOUT = 50mA to 500mA to 50mA

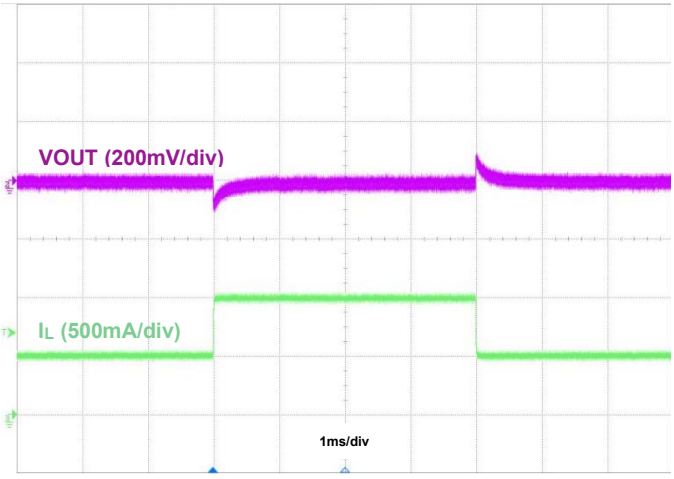


Figure 20. Load Transient, IOUT = 500mA to 1A to 500mA

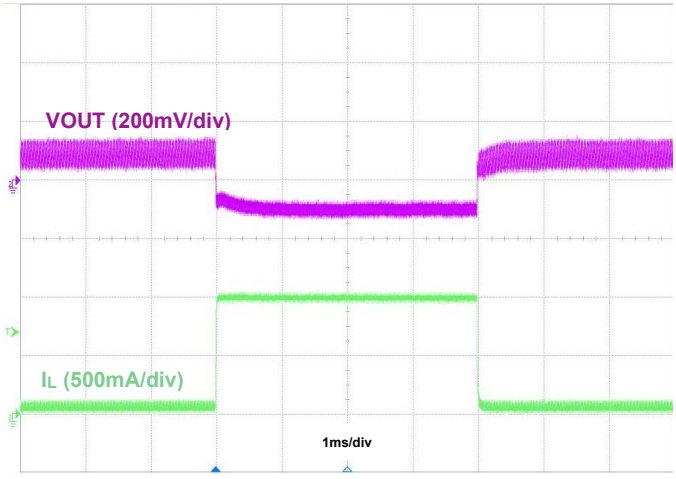


Figure 21. Load Transient, IOUT = 50mA to 1A to 50mA

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Typical Performance Characteristics (AP68065XQ/AP68105XQ @ T_A = +25°C, VIN = 48V, VOUT = 5V, f_{SW} = 300kHz, BOM = Table 1, unless otherwise specified.) (continued)

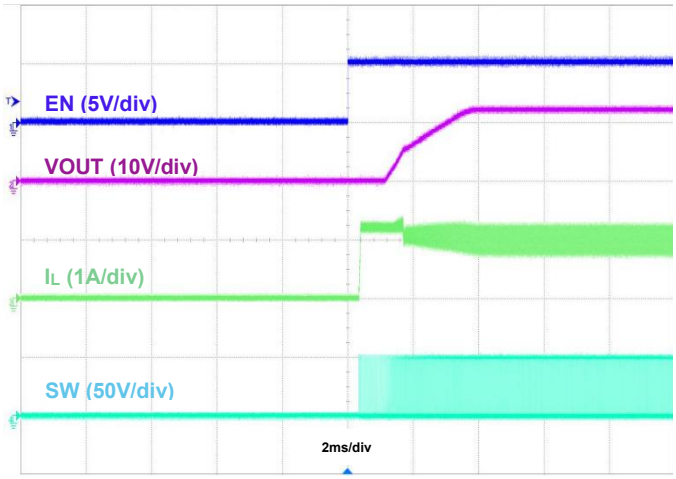


Figure 22. Startup using EN, IOUT = 1A

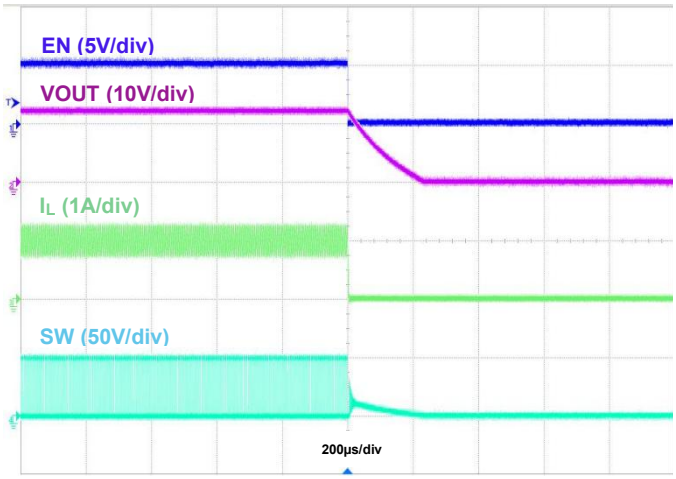


Figure 23. Shutdown using EN, IOUT = 1A

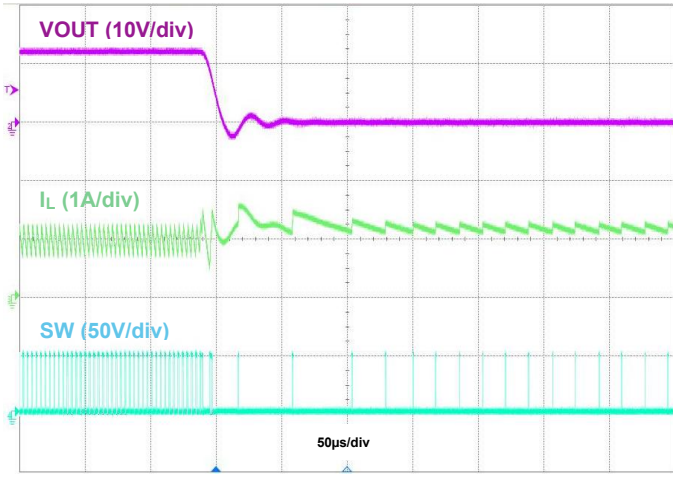


Figure 24. Output Short Protection, IOUT = 1A

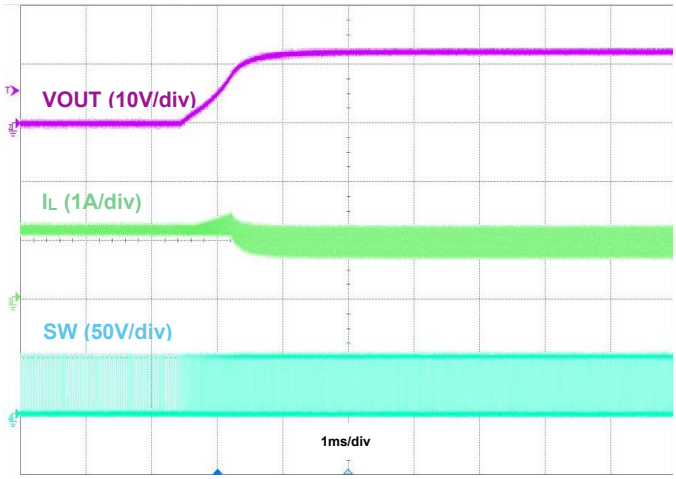


Figure 25. Output Short Recovery, IOUT = 1A

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Application Information

Pulse-Width-Modulation (PWM) Operation

The AP68065XQ/AP68105XQ devices are 4.5V-to-80V input, 0.6A/1A output, EMI friendly, fully integrated synchronous buck converter. Refer to the block diagram in Figure 3. The devices employ constant on-time control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the one-shot pulse turns on the high-side power MOSFET, Q1, for a fixed on-time, t_{ON}. This one-shot on-pulse timing is calculated by the converter's input voltage and output voltage to maintain a pseudo-fixed frequency over the input voltage range. When Q1 is on, the inductor current rises linearly and the device charges the output capacitor. Q1 turns off after the fixed on-time expires, and the low-side power MOSFET, Q2, turns on. Once the output voltage drops below the output regulation, Q2 turns off. The one-shot timer is then reset and Q1 turns on again. The on-time is inversely proportional to the input voltage and directly proportional to the output voltage. It is calculated by the following equation:

$$\mathbf{t_{ON} = \frac{VOUT}{VIN \cdot f_{SW}}} \quad \textbf{Eq. 1}$$

Where:

- VIN is the input voltage.
- VOUT is the output voltage.
- f_{SW} is the switching frequency.

The off-time duration is t_{OFF} and starts after the on-time expires. The off-time expires when the feedback voltage decreases below the reference voltage, which then triggers the on-time duration to start again. The minimum off-time is 200ns typically.

Pulse-Frequency-Modulation (PFM) Operation

The AP680650Q/AP681050Q enter PFM operation at light-load conditions for high efficiency. During light-load conditions, the regulator automatically reduces the switching frequency. As the output current decreases, so does the inductor current. The inductor current, I_L, eventually reaches 0, marking the boundary between Continuous-Conduction Mode (CCM) and Discontinuous-Condition Mode (DCM). During this time, both Q1 and Q2 are off, and the load current is provided only by the output capacitor. When V_{FB} becomes lower than 0.8V, the next cycle begins, and Q1 turns on. Because the AP680650Q/AP681050Q work in PFM during light-load conditions, they can achieve power efficiency of up to 83% at a 5mA load condition.

Likewise, as the output load increases from light load to heavy load, the switching frequency increases to maintain the regulation of the output voltage. The transition point between light and heavy-load conditions can be calculated using the following equation:

$$\mathbf{I_{LOAD} = \left(\frac{VIN - VOUT}{2L}\right) \cdot t_{ON}} \quad \textbf{Eq. 2}$$

Where:

- L is the inductor value.

The quiescent current of AP680650Q and AP681050Q is 100μA typical under a no-load, non-switching condition.

The AP680652Q and AP681052Q enter USM during light-load conditions when the MODE pin is left floating. USM is like PFM Mode but with one key difference. Unlike in PFM Mode, operating in USM limits the switching frequency of the device from going below 22kHz. This prevents the device from switching in the audible frequency range. When the regulator detects that no switching has occurred within the last 35μs, it turns on Q2 for a fixed amount of time to force switching action on SW.

Enable and Disable

The enable (EN) input allows the user to control turning on or off the regulator. Once the voltage on the EN pin is above its threshold, the buck controller powers up and soft starts.

The regulator does not allow the regulator to sink current during the soft-start period. The default time is 4ms.

Overcurrent Protection (OCP)

The inductor current is monitored during high-side MOSFET Q1 on. The AP68065XQ/AP68105XQ implement overcurrent protection with cycle-by-cycle limiting both high-side MOSFET peak and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

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Application Information (continued)

Undervoltage Lockout (UVLO)

Undervoltage lockout is implemented to prevent the IC from insufficient input voltages. The AP68065XQ/AP68105XQ devices have a UVLO comparator that monitors the input voltage and the internal bandgap reference. The AP68065XQ/AP68105XQ are disabled if the input voltage falls below 3.8V or when EN voltage is below 1.05V. In this UVLO event, both the high-side and low-side power MOSFETs turn off.

Some applications may desire higher VIN UVLO threshold voltages than is provided by the default setup. A 3μA hysteresis pullup current source on the EN pin along with an external resistive divider (R3 and R4) configures the VIN UVLO threshold voltages as shown in Figure 26.

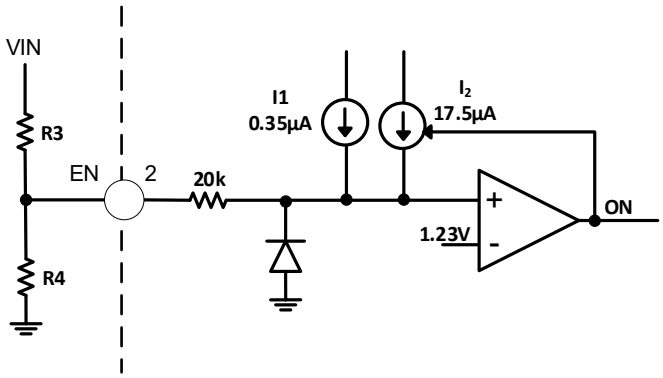


Figure 26. Programming UVLO

The resistive divider resistor values are calculated by:

$$R3 = \frac{0.99V_{ON} - V_{OFF}}{17.5\mu A} \quad \text{Eq. 3}$$

$$R4 = \frac{1.2V \cdot R3}{V_{ON} - 1.2V} \quad \text{Eq. 4}$$

Where:

- V_{ON} is the rising edge VIN voltage to enable the regulator and is greater than 4.5V.
- V_{OFF} is the falling edge VIN voltage to disable the regulator and is greater than 4.2V.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +165°C, the AP68065XQ/AP68105XQ shut down both their high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+145°C typical), the devices initiate a normal power-up cycle with soft-start.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum recommended operating junction temperature, some thermal analysis is required. The regulator's temperature rise is given by:

$$T_{RISE} = PD \cdot (\theta_{JA}) \quad \text{Eq. 5}$$

Where:

- PD is the power dissipated by the regulator.
- θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, given by:

$$T_J = T_A + T_{RISE} \quad \text{Eq. 6}$$

Where:

- T_A is the ambient temperature of the environment.

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Application Information (continued)

For the SO-8EP package, the θ_{JA} is 39°C/W. The actual junction temperature should not exceed the maximum recommended operating junction temperature of +150°C when considering the thermal design. Figure 27 shows a typical derating curve versus ambient temperature.

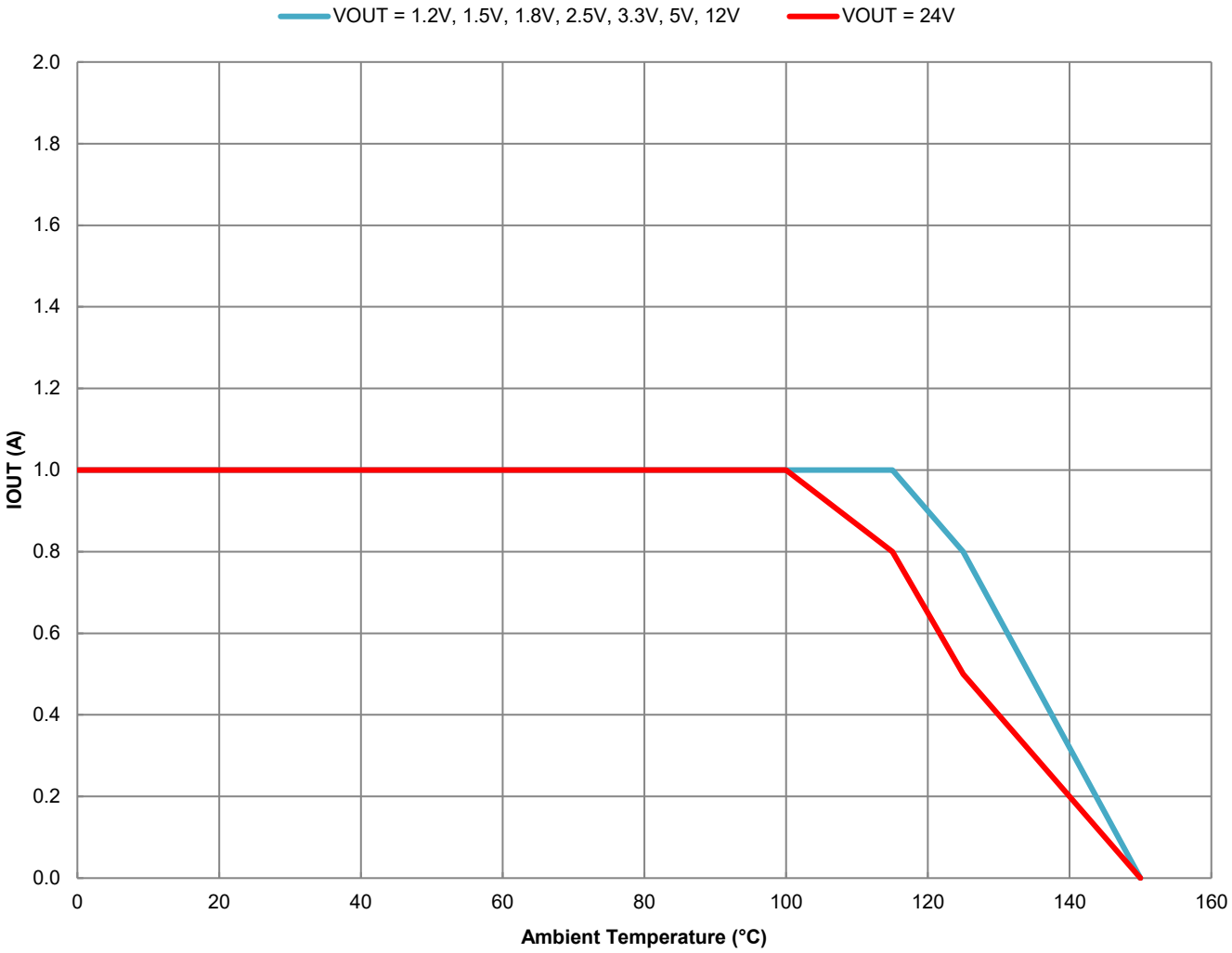


Figure 27. Output Current Derating Curve vs. Ambient Temperature, VIN = 48V

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Application Information (continued)

Setting the Output Voltage

The output voltage can be adjusted from 0.8V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages for 300kHz operation. An optional C4 of 10pF to 470pF can be used to boost the phase margin and improve stability as well as the transient performance. R2 in Figure 28 can be determined by the following equation:

$$R_2 = \frac{1.2V \cdot R_1}{Vout - 1.2V}$$

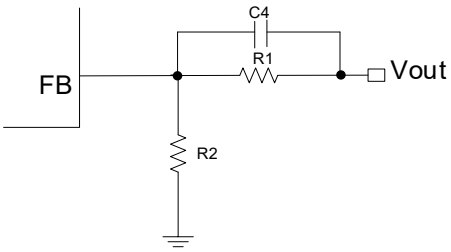


Figure 28. Feedback Divider Network

VOUT (V)	R1 (kΩ)	R2 (kΩ)	C1 (μF)	C2 (μF)	C4 (pF)	L1 (μH)	
						AP68065XQ	AP68105XQ
1.2	100	OPEN	10	2x22	47	20	15
2.5	100	93.1	10	2x22	47	39	22
3.3	100	57.6	10	2x22	47	47	27
5	100	31.6	10	2x22	47	68	39
12	100	11	10	2x22	47	120	82
24	100	5.23	10	2x22	47	150	100

Table 1 Recommended Component Selection

Additional Ripple Network

The A ripple generation network uses an RC filter consisting of R5 and C5 across SW and Vout to produce a triangular ramp that is in phase with the inductor current. This triangular ramp is then AC-coupled into the FB node using C4 as shown in Figure 29. This configuration is suited for applications where low output voltage ripple is crucial.

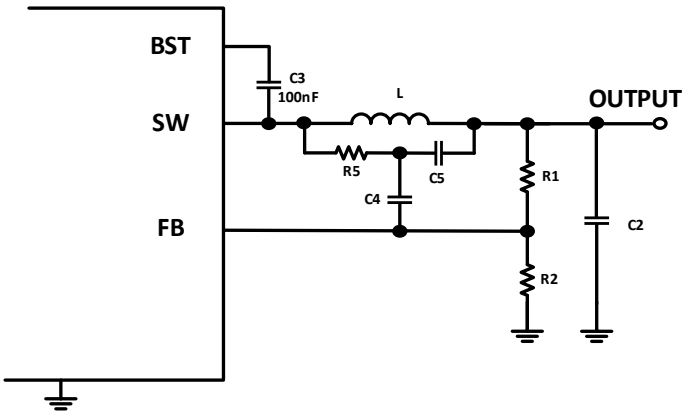


Figure 29. Added Ripple Network

Select C5 between 47nF to 100nF. Then set R5 to match the time constant of the inductor L by the following equation:

$$R_5 = \frac{L}{C_5 \cdot R_{DCR}}$$

Where L is the inductance of the output inductor and the R_{DCR} is the equivalent series resistance of the inductor. R_{DCR} can be found in the typical specification of the inductor. Then set C4 about tenth of C5 or less.

Operating Frequency

Using a resistor from FS to VIN programs the frequency from 100kHz to 600Hz. A minimum on-time of 150ns typical in conjunction with the input and output voltage should be considered when selecting the maximum operating frequency. Use equation below to set the desired switching frequency in PWM:

$$R_T[k\Omega] = \frac{V_{OUT}}{10^{-4} \cdot Fs[KHz]}$$

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Application Information (continued)

Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor must sustain the ripple current produced during the on-time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has RMs rating that is greater than half of the maximum load current.

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 10μF ceramic capacitor is sufficient and 0.1μF parallel capacitor is also recommended for improving the stability. Higher C1 capacitance is recommended for applications where input line is noisy or got wide transient such as during “hot plug” event.

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}}$$

Where ΔI_L is the inductor ripple current and f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% to 40% of the maximum load current. The maximum inductor peak current calculated from:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications.

For highest efficiency, the inductor’s DC resistance should be as low as possible. Use a larger inductance for improved efficiency under light-load conditions.

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

ESR of the output capacitor dominates the output voltage ripple. The amount of ripple can be approximate from the equation below:

$$Vout_{capacitor} = \Delta I_{inductor} * (ESR + \frac{1}{8f_{SW}C_O})$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, a 22μF ceramic capacitor will be sufficient.

$$C_o = \frac{L(I_{out} + \frac{\Delta I_{inductor}}{2})^2}{(\Delta V + V_{out})^2 - {V_{out}}^2}$$

Where ΔV is the maximum output voltage overshoot.

Bootstrap

The internal driver of the HS FET is equipped with a BST undervoltage detection (UV) circuit. If the voltage difference between BST and SW falls below 3V, the UV detection circuit allows the LS FET on for 400ns to recharge the bootstrap capacitor.

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Layout

PCB Layout

1. The AP680650Q/AP680651Q/AP680652Q and AP681050Q/AP681051Q/AP681052Q are high switching frequency converters. Hence, attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short, printed circuit traces. The AP68065XQ/AP68105XQ work up to 1A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 30 for more details.

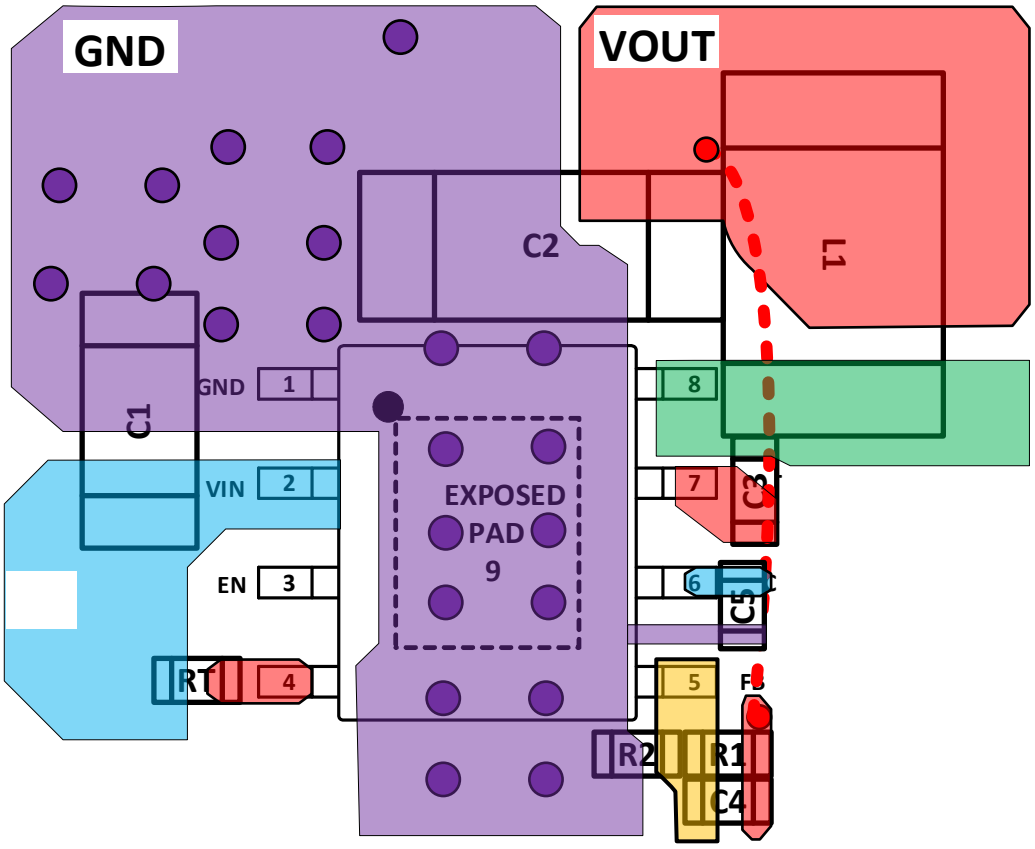
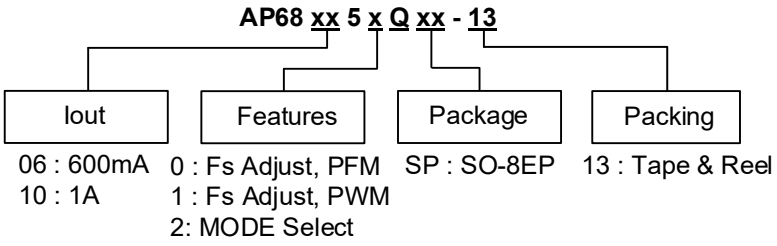


Figure 30. PC Board Layout

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Ordering Information (Note 9)



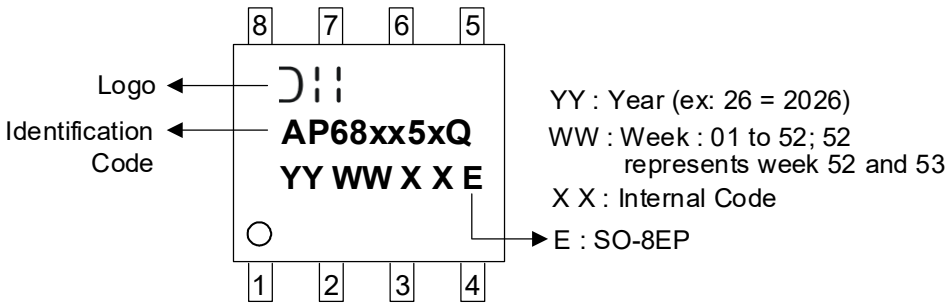
Orderable Part Number	Iout	Frequency	MODE	Package Code	Package	Identification Code	Packing	
							Qty.	Carrier
AP680650QSP-13	600mA	100kHz – 600kHz	PFM	SP	SO-8EP	AP680650Q	4000	Tape & Reel
AP680651QSP-13	600mA	100kHz – 600kHz	PWM	SP	SO-8EP	AP680651Q	4000	Tape & Reel
AP680652QSP-13	600mA	300kHz	PFM/USM/PWM	SP	SO-8EP	AP680652Q	4000	Tape & Reel
AP681050QSP-13	1A	100kHz – 600kHz	PFM	SP	SO-8EP	AP681050Q	4000	Tape & Reel
AP681051QSP-13	1A	100kHz – 600kHz	PWM	SP	SO-8EP	AP681051Q	4000	Tape & Reel
AP681052QSP-13	1A	300kHz	PFM/USM/PWM	SP	SO-8EP	AP681052Q	4000	Tape & Reel

Note: 9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

SO-8EP

(Top View)

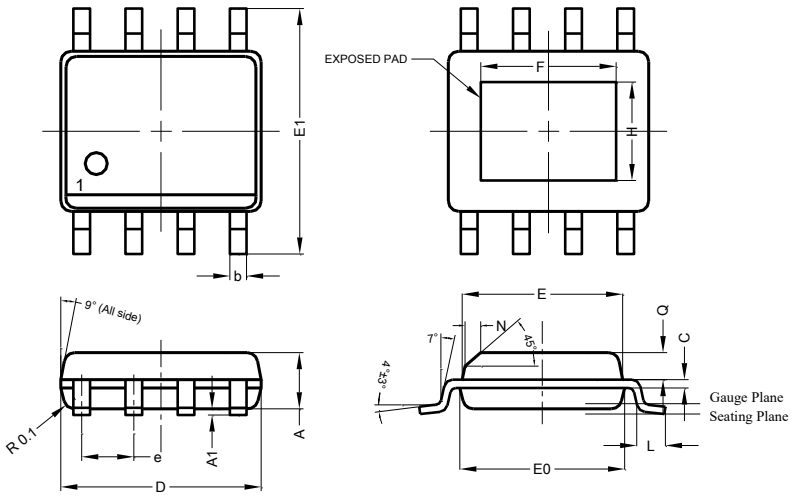


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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP

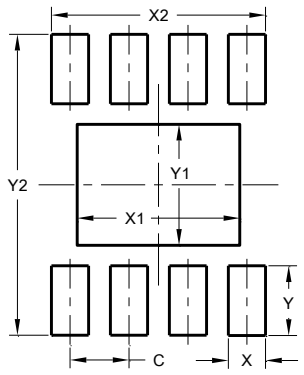


SO-8EP			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.08 grams (Approximate)

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