

Xtrinsic 3-Axis Digital Angular Rate Gyroscope

FXAS21002 is a small, low-power, yaw, pitch, and roll angular rate gyroscope. The full-scale range is adjustable from $\pm 250^\circ/\text{s}$ to $\pm 2000^\circ/\text{s}$. It features both I²C and SPI interfaces.

FXAS21002 is capable of measuring angular rates up to $\pm 2000^\circ/\text{s}$, with output data rates (ODR) from 12.5 to 800 Hz. An integrated Low-Pass Filter (LPF) allows the host application to limit the digital signal bandwidth and noise. The device may be configured to generate an interrupt when a user-programmable angular rate threshold is crossed on any one of the enabled axes.

FXAS21002 is available in a plastic, 24-lead QFN package; the device is guaranteed to operate over the extended temperature range of -40°C to $+85^\circ\text{C}$.

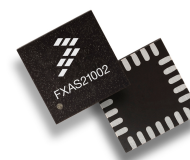
Features

- V_{DD} supply voltage from 1.95 V to 3.6 V; digital interface supply voltage from 1.62 V to 3.6 V
- 16-bit digital output resolution
- $\pm 250/500/1000/2000^\circ/\text{s}$ software-selectable full-scale dynamic ranges
- Noise density of 25 mdps/ $\sqrt{\text{Hz}}$ at 100 Hz bandwidth (200 Hz ODR)
- Current consumption in Active mode is $\leq 3\text{ mA}$
- Time to transition from Standby to Active mode is $\leq 50\text{ ms}$
- Interfaces:
 - I²C Normal-mode (100 kHz)
 - I²C Fast-mode (400 kHz)
 - I²C Fast-mode Plus (1 MHz)
 - SPI 3-wire (up to 2 MHz)
 - SPI 4-wire (up to 2 MHz)
- FIFO buffer is 192 bytes deep (32 X/Y/Z samples) with stop, circular and triggered operating modes
- Output data rates (ODR) from 12.5 to 800 Hz; programmable low-pass filter to further limit digital output data bandwidth
- Angular rate sensitivity of $0.061^\circ/\text{s}$ in $\pm 2000^\circ/\text{s}$ FSR mode
- Low power standby mode
- Power mode transition control via external pin for accelerometer-based power management (motion interrupt)
- Rate threshold interrupt
- Integrated self-test function
- No external charge-pump capacitor needed
- 8-bit temperature sensor
- MSL 3 compliant package

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice. © 2014 Freescale Semiconductor, Inc. All rights reserved.

Preliminary
Non-Disclosure Agreement required

FXAS21002



24 QFN
4 mm x 4 mm x 1 mm
Case 2209-01

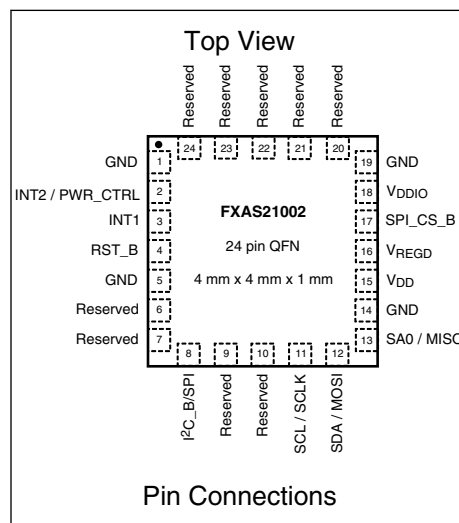


Table of Contents

1 Typical Applications.....	3	2.3.1 Typical Application Circuit—I2C Mode.....	5
2 General Description.....	3	2.3.2 Typical Application Circuit—SPI Mode.....	6
2.1 Block Diagram.....	3	2.4 Sensing Direction.....	7
2.2 Pinout.....	3	3 Package Description.....	8
2.3 System Connections.....	5	4 Revision History.....	9

1 Typical Applications

- Game controller
- Gyro stabilized electronic compass
- Orientation determination
- Gesture-based user interfaces
- Indoor navigation
- Human machine interface
- Mobile phones
- Toy helicopter
- Virtual and augmented reality devices (including glasses)

2 General Description

2.1 Block Diagram

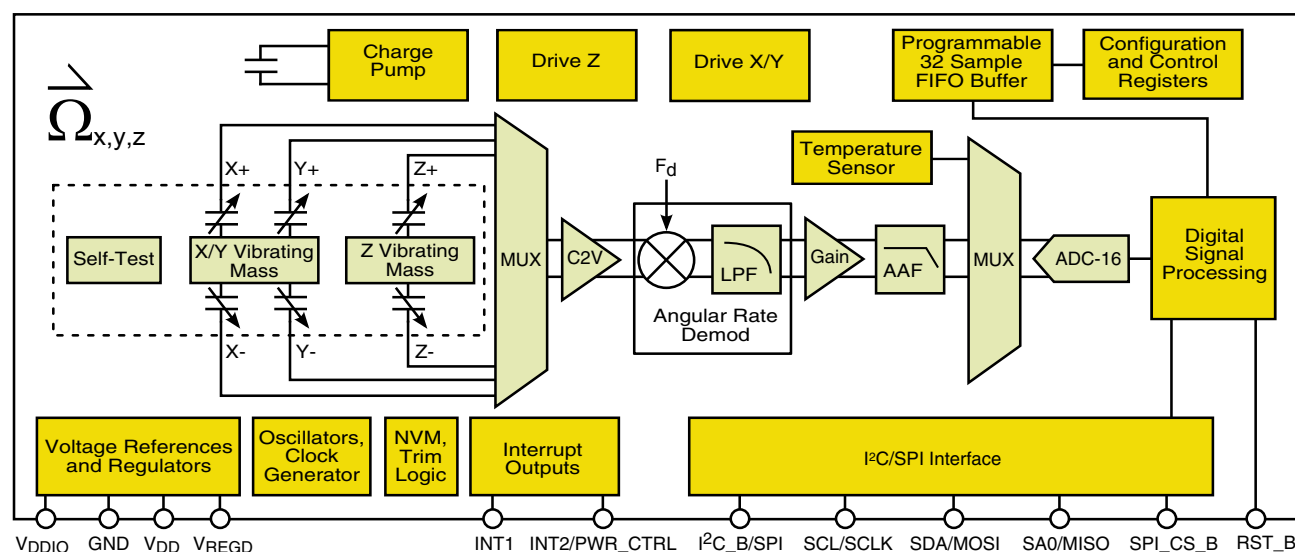


Figure 1. Block Diagram

2.2 Pinout

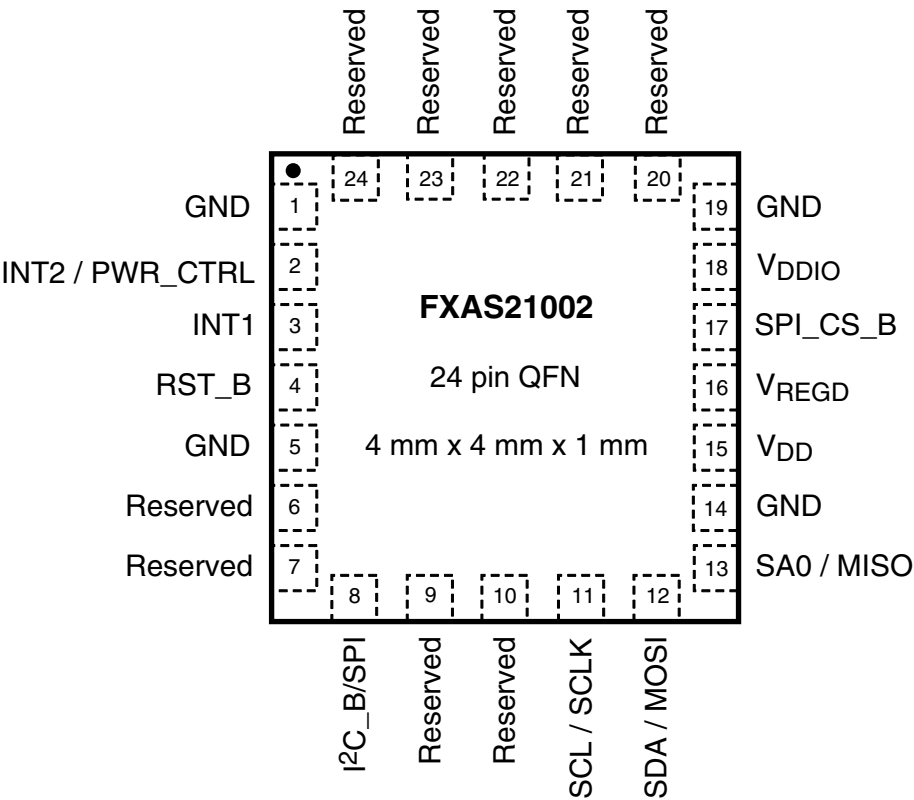


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin	Name	Function
1	GND	Ground
2	INT2/PWR_CTRL	Interrupt Output 2 / Power state transition control input
3	INT1	Interrupt Output 1
4	RST_B	Reset input (active low, connect to V _{DDIO} if unused)
5	GND	Ground
6	Reserved	Reserved - Must be tied to ground
7	Reserved	Reserved - Must be tied to ground
8	I ² C_B/SPI	Digital interface selection pin – must be tied either high or low to select either SPI or I ² C interface mode, respectively
9	Reserved	Reserved - Must be tied to ground
10	Reserved	Reserved - Must be tied to ground
11	SCL/SCLK	I ² C / SPI clock
12	SDA/MOSI/SPI_DIO	I ² C data / SPI 4-wire Master Out Slave In / SPI 3-wire data In/Out ¹
13	SA0/MISO	I ² C address bit0 / SPI 4-wire Master In Slave Out
14	GND	Ground

Table continues on the next page...

Table 1. Pin functions (continued)

Pin	Name	Function
15	V _{DD}	Supply voltage
16	V _{REGD}	Digital regulator output. Please connect a 0.1 uF capacitor between this pin and GND
17	SPI_CS_B	SPI chip select input, active low. This pin must be held logic high when operating in I ² C interface mode (I ² C/SPI_CS_B set high) to ensure correct operation.
18	V _{DDIO}	Interface supply voltage
19	GND	Ground
20	Reserved	Reserved - Must be tied to ground
21	Reserved	Reserved - Must be tied to ground
22	Reserved	Reserved - Must be tied to ground
23	Reserved	Reserved - Must be tied to ground
24	Reserved	Reserved - Must be tied to ground

1. MOSI becomes a bidirectional data pin when FXAS21002 is operated in 3-wire SPI mode with CTRL_REG0[SPIW]=1.

2.3 System Connections

The FXAS21002 offers the choice of connecting to a host processor through either I²C or SPI interfaces. [Figure 3](#) and [Figure 4](#) show the recommended circuit connections for implementing both options.

2.3.1 Typical Application Circuit—I²C Mode

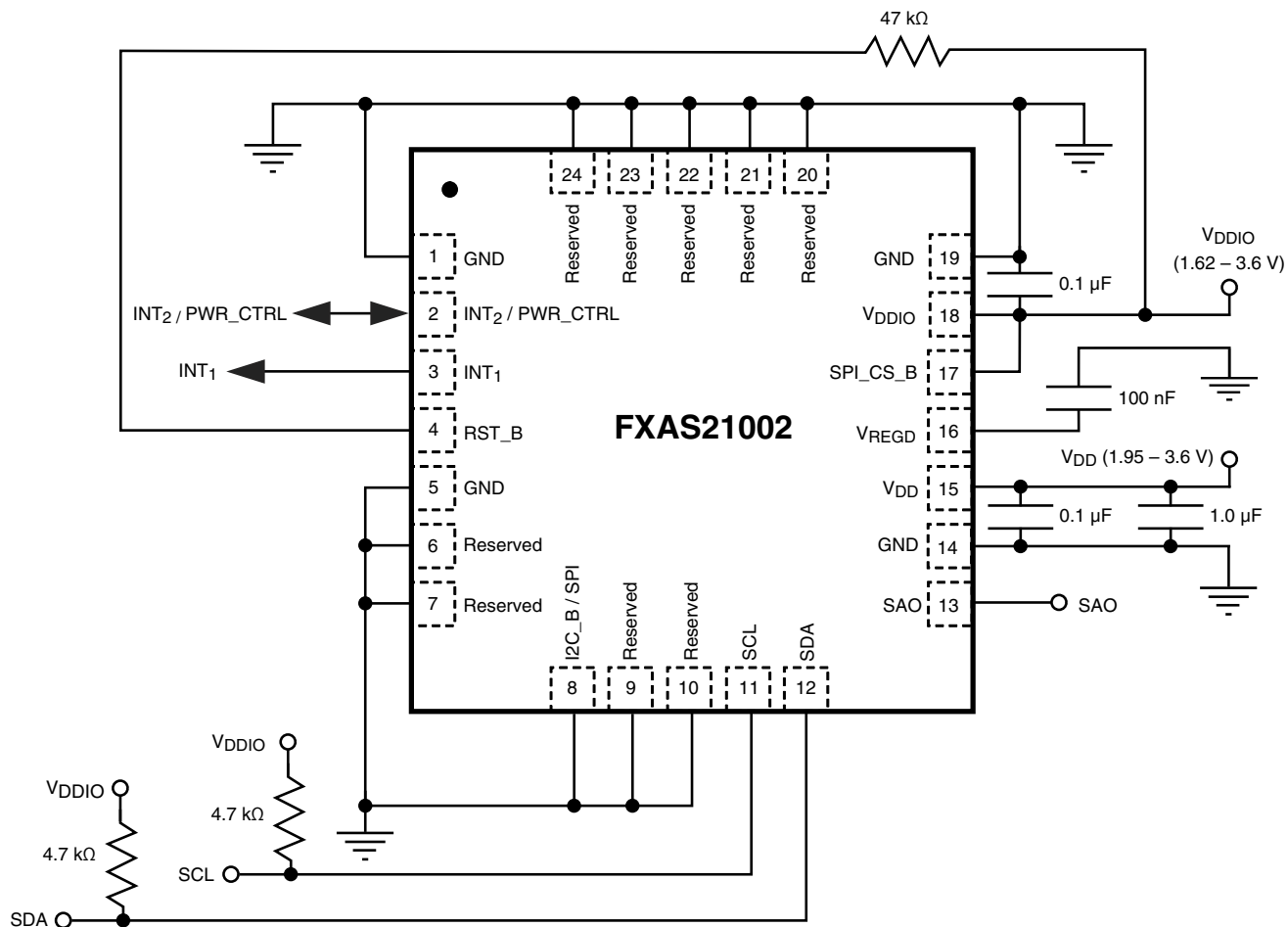


Figure 3. I²C mode electrical connections

2.3.2 Typical Application Circuit—SPI Mode

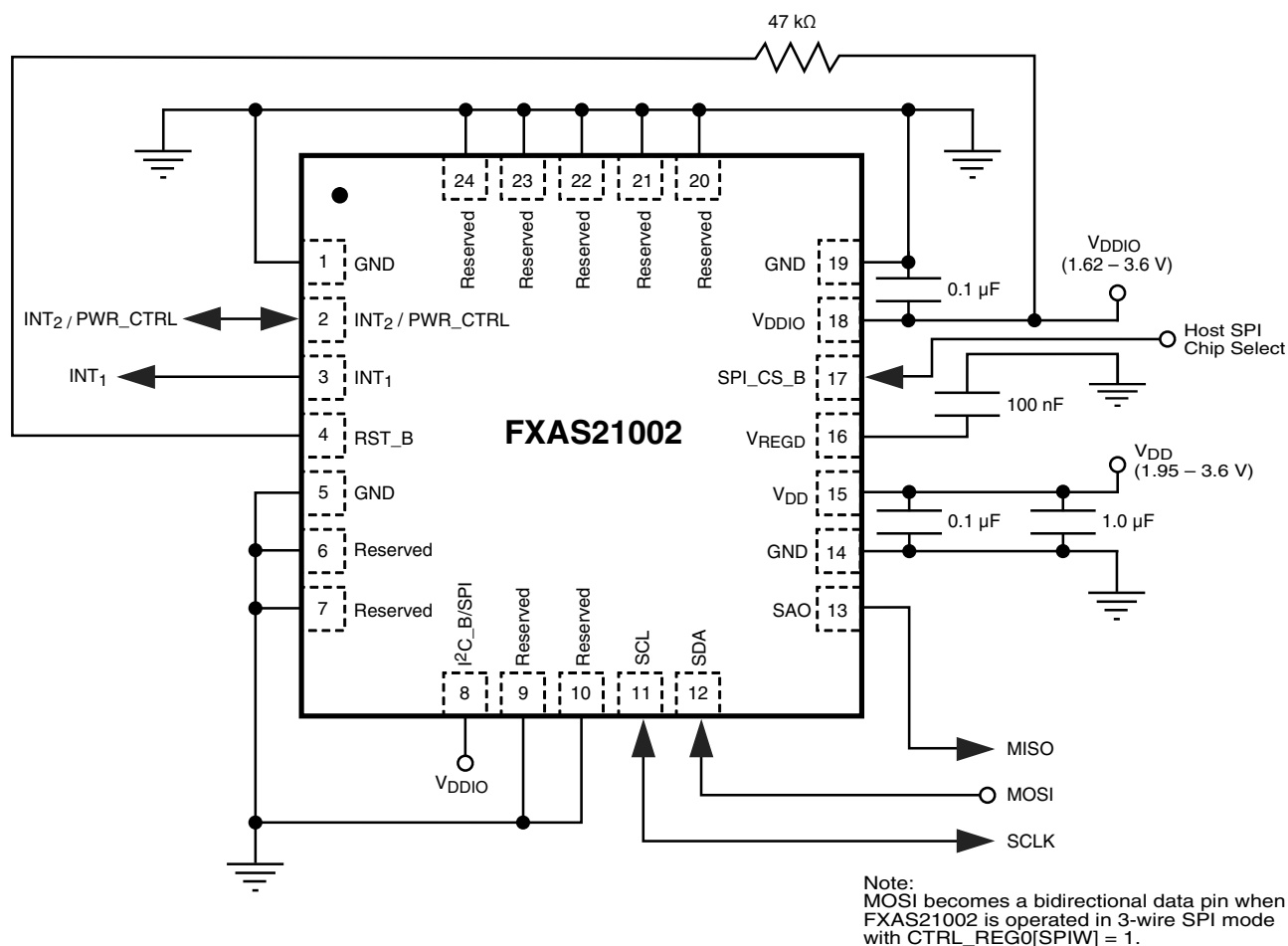


Figure 4. SPI mode electrical connections

2.4 Sensing Direction

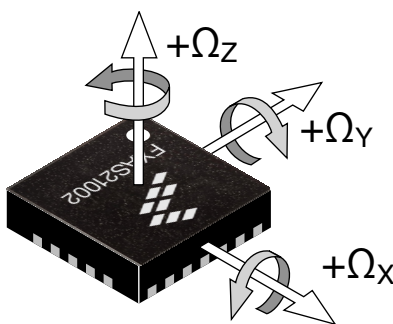
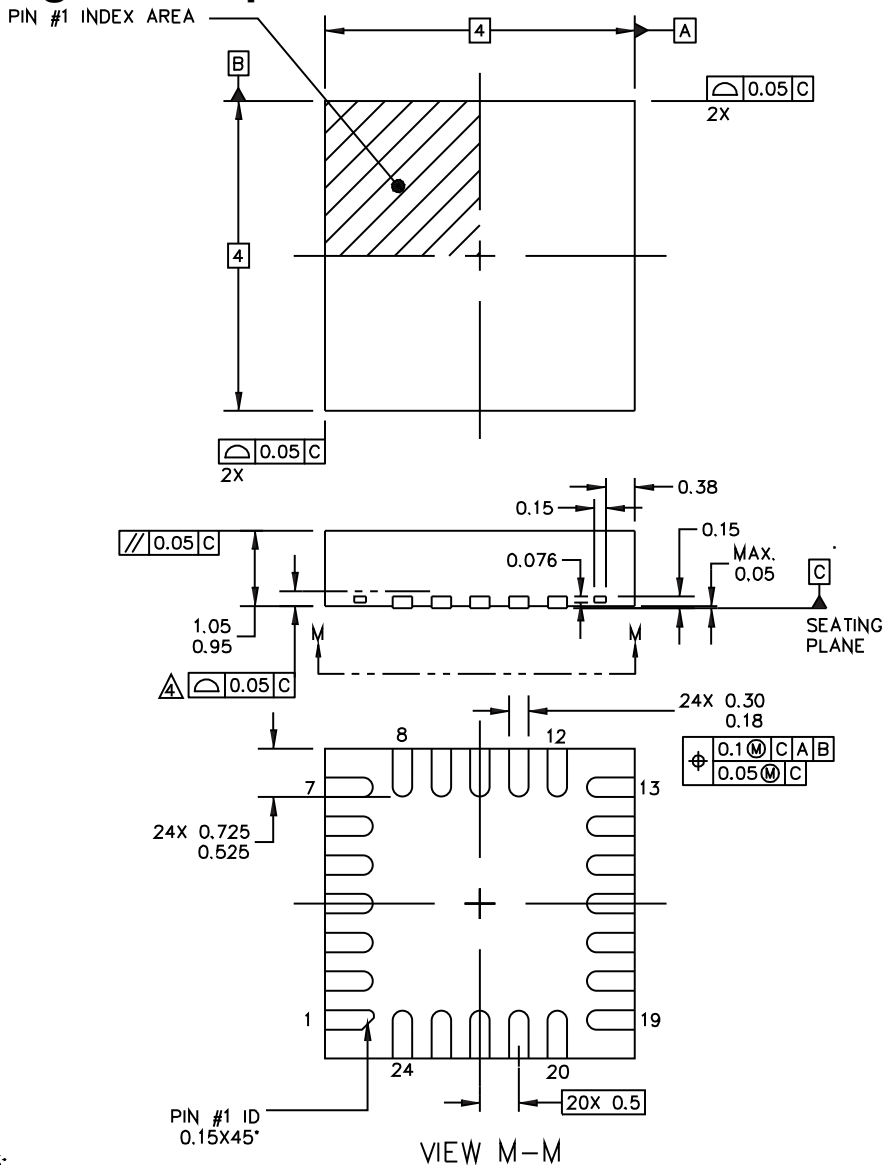


Figure 5. Reference frame for rotational measurement

3 Package Description



- NOTES:
- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 - 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - 3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
 - 4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
 - 5. MIN. METAL GAP SHOULD BE 0.2 MM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: QFN, CHIP ON LEAD (COL), 4 X 4 X 1, 0.5 PITCH, 24 TERMINAL		DOCUMENT NO: 98ASA00356D	REV: 0
		CASE NUMBER: 2209-01	15 DEC 2011
		STANDARD: NON-JEDEC	

This drawing is located at freescale.com.

4 Revision History

Revision number	Revision date	Description
0.3	3/2014	Initial release of document



How to Reach Us:

Home Page:

freescale.com

Web Support:

freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale, the Freescale logo, and the Energy Efficient Solutions logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Xtrinsic is a trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

Document Number FXAS21002
Revision 0.3, 3/2014

