

1 Description

- Qualified for automotive applications requiring AEC-Q100 Rev H Grade 1 Compliance
- High frequency, low profile DC-DC converters

The TLF12501 integrated power-stage contains a low quiescent current synchronous buck gate-driver IC which is co-packed with control and synchronous MOSFETs. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing when layout guidelines are followed. The paired gate driver and MOSFET combination enables higher efficiency at lower output voltages required by cutting edge CPU, GPU, and DDR memory designs.

The internal MOSFET sensing achieves superior current sense accuracy vs. best-in-class controller-based Inductor DCR sense methods.

Protection includes IC temperature reporting and over temperature protection feature (OTP with thermal shutdown), cycle-by-cycle over-current protection (OCP), control MOSFET short detection (HSS - High side short detection), VDRV and bootstrap under-voltage protection. The TLF12501 also features "refreshing" of bootstrap capacitor to prevent the bootstrap capacitor from over-discharging.

Operation of up to 2 MHz switching frequency enables high performance transient response, allowing miniaturization of output inductors, as well as input and output capacitors while maintaining industry leading efficiency.

Features

- Integrated driver, control MOSFET Q1 and synchronous MOSFET Q2
- On-chip MOSFET Current sensing and reporting at 5uA/A.
- Input voltage (VIN) range of 4.25 V to 16 V
- VCC and VDRV supply of 4.25 V to 5.5 V
- Output voltage range from 0.225 V up to 5.5 V at VIN = 12 V
- Output current capability of 60 A
- Operation up to 2 MHz
- VDRV under-voltage lockout (UVLO)
- Bootstrap under-voltage protection
- 8mV / °C temperature analog output
- Over-temperature protection and thermal shutdown
- Cycle-by-cycle over current Protection (OCP) and flag
- Control MOSFET short (HSS) detection and flag
- Auto-replenishment on bootstrap capacitor
- Compatible with 3.3 V tri-state PWM Input
- Auto SLEEP mode after 20 µs of PWM Tri-state (1.6 mA typ.)
- DEEP SLEEP mode for power saving via EN= low (32 µA typ.)
- Small 5 mm x 6 mm x 0.9 mm PQFN package
- Lead free RoHS compliant package
- Compliant to automotive AEC-Q100 Rev H Grade 1 requirements

Table 1 Product Identification			
Part Number	Temp Range	Package	Marking
TLF12501	-40 to 125°C	PQFN 5 mm x 6 mm	TLF12501

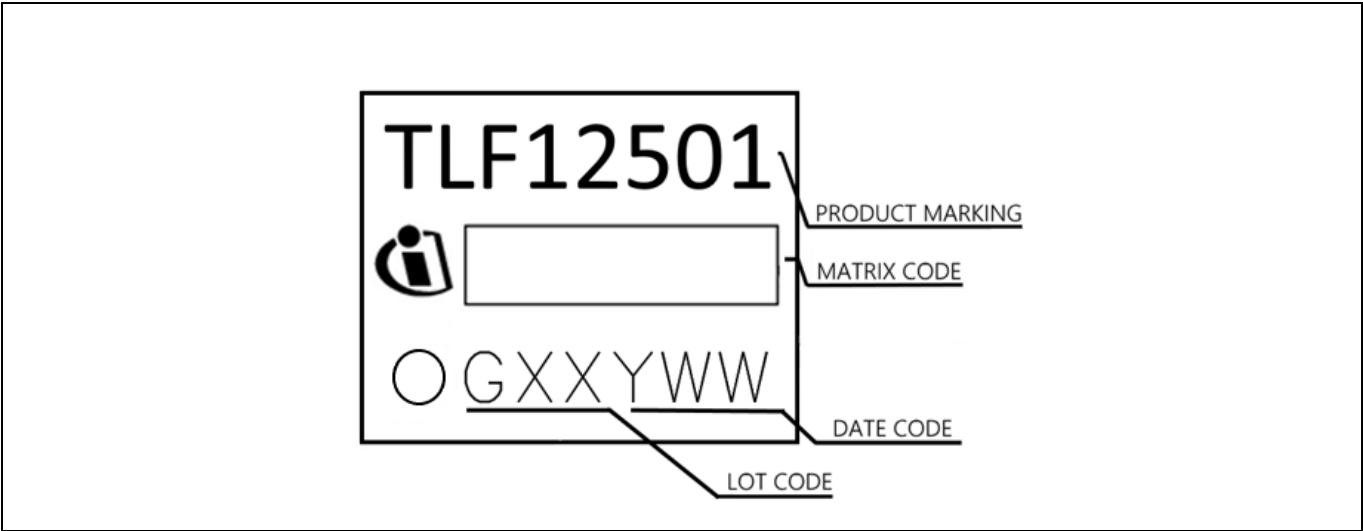


Figure 1 Picture of the Product

1.1 Pinout

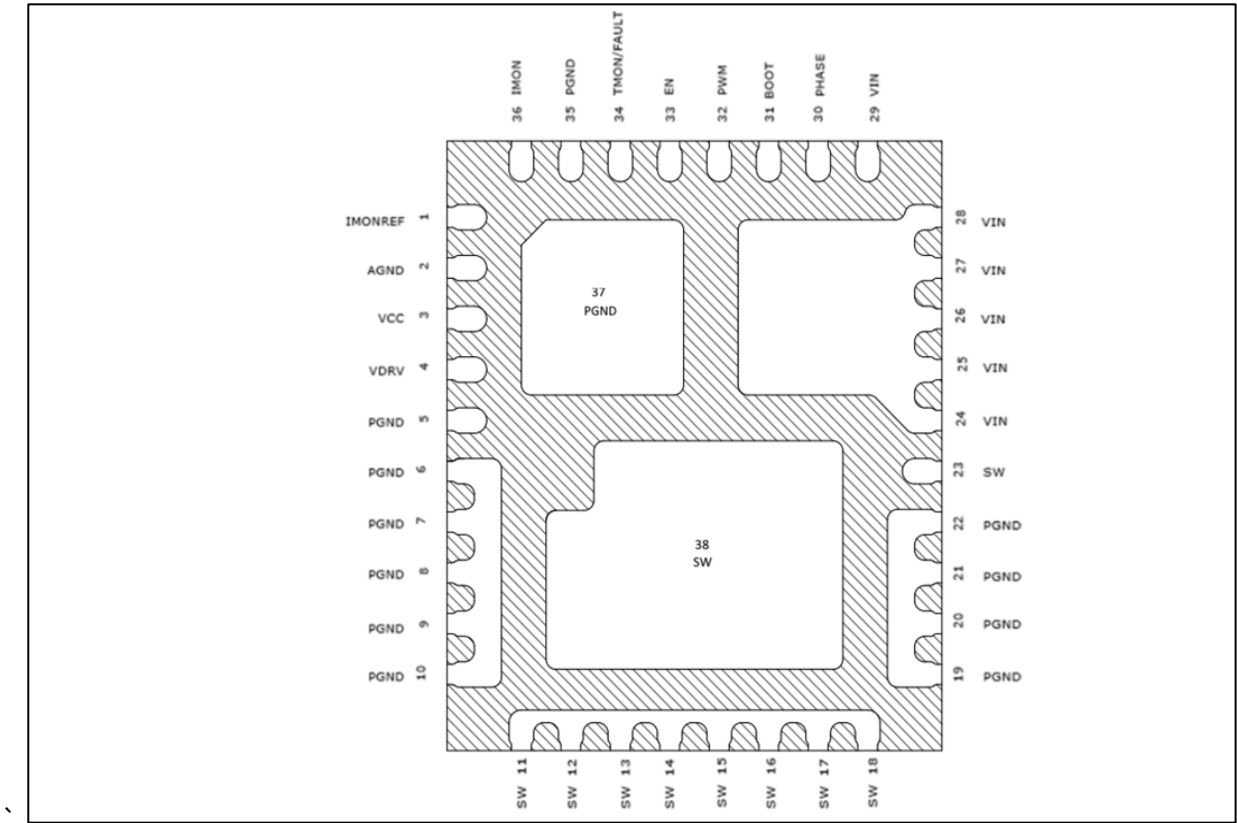


Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

2 Pinout, Numbering and Name of Pins (transparent top view)

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	IMONREF	I/O	Analog	This pin provides a common-mode voltage reference for the IMON information. This pin may be tied to a fixed voltage such as bias rails of a PWM controller or left floating.
11-18, 23, 38	SW	O	Analog	Switching node of synchronous buck converter.
30	PHASE	I	Analog	Switching node. For Bootstrap capacitor connection only.
31	BOOT	I	Analog	Bootstrap capacitor connection. Connect an X7R ceramic capacitor with value between 0.22 μ F to 0.56 μ F from BOOT to PHASE pin. Recommended value is 0.47 μ F. The bootstrap capacitor provides the charge to turn on the control MOSFET. For VIN > 13.2 V, a 2- Ω bootstrap resistor in series with the capacitor is required to help reduce SW ringing and EMI.
32	PWM	I/O	+3.3 V logic	3.3 V logic level PWM input. PWM input: "High" turns control MOSFET on; "Tri-state" turns both MOSFETs off; "Low" turns the synchronous MOSFET on.
33	EN	I	+3.3 V logic	Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a pull-down is embedded to keep the driver off if the pin is floating. Pin is VCC tolerant.
34	TMON / FAULT	O	Analog	The voltage at this pin is defined by the equation $8\text{mV} \cdot (\text{Celsius Temperature}) + 0.6 \text{ V}$. This pin will be pulled up to 3.3 V under severe over-temperature, over-current, HSS or bootstrap under-voltage condition.
36	IMON	O	Analog	Sensed current output signal referenced to the IMONREF pin through external resistor. V (IMON – IMONREF) voltage across that resistor represents current information.

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
3	VCC	POWER	–	Bias voltage for control logic. Connect a 1 μ F cap between VCC and AGND. VCC should be connected to +5 V power supply.
4	VDRV	POWER	–	The supply of gate driver. Connect a 1 μ F cap between VDRV and PGND. VDRV should be connected to +5 V power supply.
24-29	VIN	POWER	–	4.25 V to 16 V high current input voltage connection.

Table 4 **Ground Pins**

Pin No.	Name	Pin Type	Buffer Type	Function
2	AGND	GND	–	Signal ground. All interface signals are referenced to this pin.
5-10, 37	PGND	GND	–	Power ground. It is also the power ground of the synchronous MOSFET.
19-22	PGND	GND	–	Power ground. It is also the power ground of the synchronous MOSFET.
35	PGND	GND	–	Power ground. It is also the power ground of the synchronous MOSFET.

3

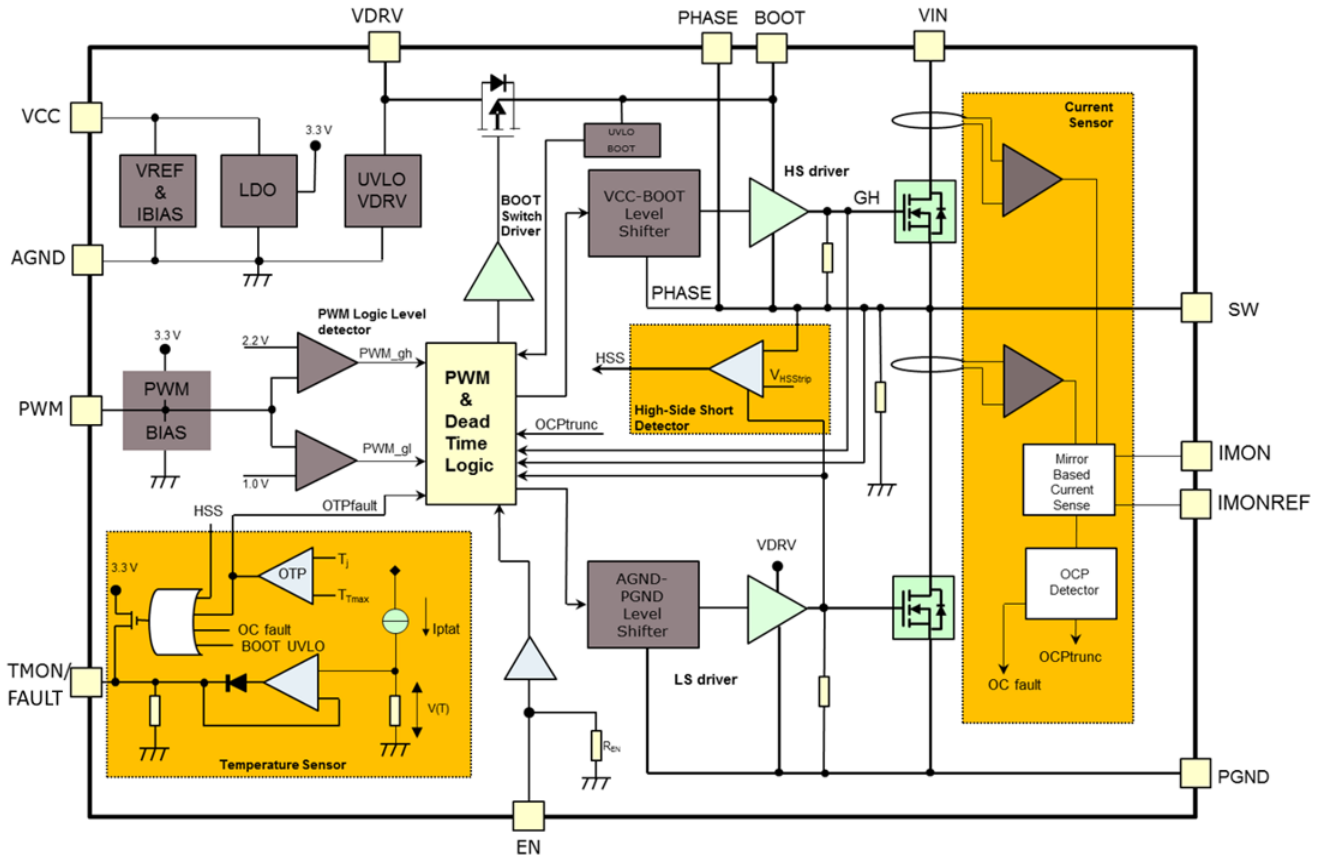


Figure 3 Simplified Block Diagram

4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: $T_A = 25\text{ }^{\circ}\text{C}$

Stresses above those listed in Table 5 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	0.1	–	2	MHz	
Maximum average load current	I_{OUT}	–	–	60	A	
Input Voltage	V_{IN}	-0.30	–	25	V	Pin VIN
Logic supply voltage	V_{CC}	-0.3	–	6.5	V	Pin VCC
High and low-side driver voltage	V_{DRV}	-0.3	–	6.5	V	Pin VDRV
Switch node voltage	V_{SW} (DC)	-1	–	25	V	Pin SW
	V_{SW} (AC)	-8 for 10ns	–	32 for 2ns		
PHASE voltage	V_{PHASE} (DC)	-1	–	25	V	Pin PHASE
	V_{PHASE} (AC)	-8 for 10ns	–	32 for 2ns		
VIN-PHASE Voltage	$V_{VIN-PHASE}(DC)$	-1	–	25	V	
	$V_{VIN-PHASE}(AC)$	Below -5V for 5ns	–	32 for 1ns		
BOOT voltage	V_{BOOT} (DC)	-0.3	–	29	V	Pin BOOT
	V_{BOOT} (AC)		--	30 for 10ns		
	$V_{BOOT-PHASE}$	-0.3	–	6.5V (DC), 7.5V for 3ns		–
EN voltage	V_{EN}	-0.3	–	6.5	V	Pin EN
PWM voltage	V_{PWM}	-0.3	–	3.6	V	Pin PWM
TMON voltage	V_{TMON}	-0.3	–	3.6	V	Pin TMON / FAULT
IMON voltage	V_{IMON}	-0.3	–	3.6	V	Pin IMON
IMONREF voltage	$V_{IMONREF}$	-0.3	–	3.6	V	Pin IMONREF
Junction temperature	T_{Jmax}	-40	–	150	$^{\circ}\text{C}$	
Storage temperature	T_{STG}	-55	–	150	$^{\circ}\text{C}$	–

Note: All rated voltages are relative to voltages on the AGND and PGND pins unless otherwise specified.

4.2 Thermal Characteristics

Table 6 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance-Junction to PCB	θ_{JC_PCB}	–	1.5	–	K/W	
Thermal resistance-Junction to top of package	θ_{JC_Top}	–	17.8	–		–
Thermal resistance to ambient	θ_{JA}^{Note}	–	28.4	–		–

Note: Thermal Resistance (θ_{JA}) is measured with the component mounted on a high effective thermal conductivity test board in free air.

4.3 Recommended Operating Conditions

Table 7 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	4.25	–	16	V	–
MOSFET driver voltage	V_{DRV}	4.25	–	5.5		–
Logic supply voltage	V_{CC}	4.25	–	5.5		–
Frequency of the PWM	f_{SW}	100	–	2000	kHz	–
EN voltage	V_{EN}	–	–	5.5	V	Pin EN
PWM voltage	V_{PWM}	–	–	3.6	V	Pin PWM
Current Sense reference voltage	V_{IMON_CM}	1.1	–	1.9	V	
Junction temperature	T_{JOP}	–40	–	+125	°C	

4.4 Electrical Characteristics

Note: $V_{DRV} = V_{CC} = 5\text{ V}$, $T_J = 25\text{ °C}$, $V_{IMONREF} = 1.2\text{ V}$

Table 8 Voltage Supply, Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO VDRV rising	V_{UVLO_R}	3.9	4.05	4.2	V	
UVLO VDRV falling	V_{UVLO_F}	3.7	3.85	4.0		
Bootstrap Under-voltage rising threshold	V_{UVBOOT_R}	3.7	3.85	4.0		
Bootstrap Under-voltage falling threshold	V_{UVBOOT_F}	3.65	3.82	4.0		
Driver current	I_{VDRV}	–	29	–	mA	EN = H, $f_{SW} = 600\text{ kHz}$, D=15%
		1.4	2.5	4.2	μA	EN = L
Supply Current	I_{VCC}	3.5	8	9.5	mA	EN = H, $f_{SW} = 600\text{ kHz}$, D=15%
		18	30	42	μA	EN = L
VIN Current	I_{VIN}	–	–	5	μA	No switching

Table 9 Current Sense

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
IMON	IMON Voltage range	V_{IMON}	0.8	–	2.35	V	DC + AC components
	IMON/IMONREF reference voltage range	V_{IMON_CM}	1.1	–	1.9	V	Reference Voltage connected externally for the current sense signal
	Current sense gain	A_{CS}	–	5	–	$\mu A/A$	
	IMON Gain resistor range	R_{IMON}	–	1	–	k Ω	Resistor to be connected between IMON and IMONREF. For 5mV/A, recommended 1k Ω R_{IMON}
	Leakage Current	I_{Leak}	–2	0	2	μA	$I_{OUT} = 0A$, $V_{IMON} = 1.2V$ PWM in tri-state
	Zero current offset	I_{offset}	–3	0	3	μA	Corresponds to 3 mV at 5 mV/A. ($R_{IMON} = 1 k\Omega$), device in regulation
	Accuracy at $T_J = -5$ to $125^\circ C$ $V_{CC} = V_{DRV} = 5 V \pm 10 \%$		–3.0	–	3.0	%	for $25A < I_{OUT} < I_{OCP_TH}$ ^{Note 1}
			–0.5	–	0.5	A	for $-25A < I_{OUT} < 25A$ ^{Note 1}

Table 10 Temperature Sense and Fault Communication

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TMON / FAULT	Temperature Sense Slope	$A_{TMPGAIN}$	7.84	8.0	8.16	mV/ $^\circ C$	$25^\circ C \leq T_J \leq 125^\circ C$, ^{Note 1}
	Temperature Sense Offset Voltage	$V_{TMPOFFSET}$	784	800	816	mV	$T_J = 25^\circ C$, $0.6 V + 8 mV/^\circ C * T_J$
	TMON / FAULT Source Current	$I_{TMONSRC}$	400	500	650	μA	TMON / FAULT pulled low
	TMON / FAULT Sink Current	$I_{TMONSNK}$	26	32	40	μA	TMON / FAULT pulled high
	Fault mode Active High	$V_{TFLTHIGH}$	2.6	3.3	3.6	V	$I_{TMON/FAULT} = 5 mA$ and under Over-Temperature, Over-Current, bootstrap under-voltage or HSS Fault
	TMON / FAULT Low ^{Note 1}	$V_{TFLTLOW}$	–	–	0.35	V	No Fault, $V_{DRV} < V_{UVLO1_R}$
	TMON / FAULT pull down resistance	R_{PULLDN_TMON}	–	150	–	k Ω	No Fault, $V_{DRV} < V_{UVLO1_R}$

Table 11 Other Logic Functions, Inputs/Outputs And Thresholds

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN	Enable Power-on Delay	$t_{EN_ondelay}$	–	27	35	μs	PWM=0. Measured from EN rising edge to $V_{SW} > 1 V$.
	Enable Power-off Delay	$t_{EN_offdelay}$	–	–	1	μs	PWM=0. Measured from EN falling edge to $V_{SW} < 0.9 \cdot V_{IN}$.
	Internal Pull down Resistance	R_{PULLDN_EN}	–	280	–	$k\Omega$	When EN is floating
	Input High Voltage	V_{EN_H}	2.0	–	–	V	
	Input Low Voltage	V_{EN_L}	–	–	0.8	V	
PWM	PWM Input High Threshold	V_{IH}	2.4	–	–	V	PWM Low or Tri-state to High
	PWM Input Low Threshold	V_{IL}	–	–	0.8	V	PWM High or Tri-state to Low
	PWM Hysteresis	I_{PWM_HYS}	–	40	–	mV	Active to Tri-state or Tri-state to Active
	PWM Input Tri-State Floating Voltage	V_{PWM_TRI}	1.4	1.6	1.8	V	PWM Input Floating
	Tri-state Window	V_{PWM_S}	1.2	–	2.0	V	
	PWM Input Equivalent Pull-up Resistance	R_{PWM_PU}	–	20	–	$k\Omega$	$V_{PWM} = 0 V$
	PWM Input Equivalent Pull-down Resistance	R_{PWM_PD}	–	50	–	$k\Omega$	$V_{PWM} = 3.3 V$
Bootstrap Diode	Forward Voltage	V_{FWD}	–	620	–	mV	$I(BOOT) = 5mA$
SW Bleeding Resistor	SW Floating Voltage	V_{SW_FLOAT}	–	–	200	mV	$V_{PWM} = 1.6 V$ or Tri-state, $V_{CC} = V_{DRV} = 5V$
	SW Pull Down Resistance	$R_{SW_PULL_DOWN}$	0.85	1.125	1.5	$k\Omega$	

Table 12 Protection

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
OTP	Over Temp Rising Threshold	T_{RISE}	–	155	–	°C	TMON/FAULT pulled up high ^{Note 1}
	Over Temp Falling Threshold	T_{FALL}	–	143	–	°C	TMON/FAULT released ^{Note 1}
HSS FAULT	High-side MOSFET Short Threshold	V_{HSS_TH}	–	560	–	mV	$V_{SW} - V_{PGND}$
	TMON/FAULT Delay	T_{HSS_DEL}	–	150	–	ns	After V_{HSS_TH} is detected and TMON/FAULT is pulled high
OCP	Over-Current Threshold	I_{OCP_TH}	80	90	100	A	
	Over-Current Delay	T_{OCP_DEL}	10	–	–	Cycle	PWM High-Low Cycles to TMON/FAULT is pulled high

Table 13 Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM High Propagation Delay	$t_{PWM_HI_DELAY}$	–	48	–	ns	Measured from PWM rising edge to V_{SW} starts to rise
PWM Low Propagation Delay	$t_{PWM_LO_DELAY}$	–	45	–	ns	Measured from PWM falling edge to V_{SW} starts to fall
Tri-State to High Propagation Delay	$t_{TRI_HI_DELAY}$	–	53	–	ns	PWM Tri-state to High transition to $V_{SW} > 1\text{ V}$
Tri-State Hold Off Time	$t_{TriHold}$	40	56	76	ns	PWM Low to Tri-state transition to SW starts to fall ^{Note 1}
			75			PWM High to Tri-state transition to SW starts to fall ^{Note 1}
Minimum Recognized PWM Pulse Width ^{Note 1}	t_{MinPWM}	–	17	–	ns	
Minimum output pulse width	$t_{OnSWmin}$	–	18	–	ns	Positive load current. PWM pulses shorter than $t_{OnSWmin}$ will be extended to $t_{OnSWmin}$. ^{Note 1}

Notes

1. Guaranteed by design but not tested in production

5 Typical operating conditions

Single Phase Circuit of Figure 18, $V_{IN} = 12\text{ V}$, $V_{OUT} = 0.8\text{ V}$, $f_{SW} = 500\text{ KHz}$, $L = 100\text{ nH}$, $V_{CC} = V_{DRV} = 5\text{ V}$, $T_{AMBIENT} = 25\text{ }^{\circ}\text{C}$, $R_{IMON} = 1\text{ k}\Omega$ 0.1%, no heat sink, no air flow, 8-layer PCB board of 3.7" (L) x 2.6" (W), no PWM controller loss, no inductor loss, unless specified otherwise.

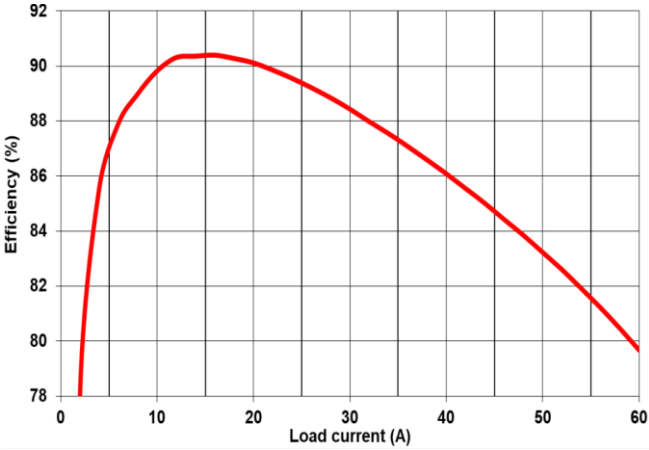


Figure 4 Power stage Efficiency

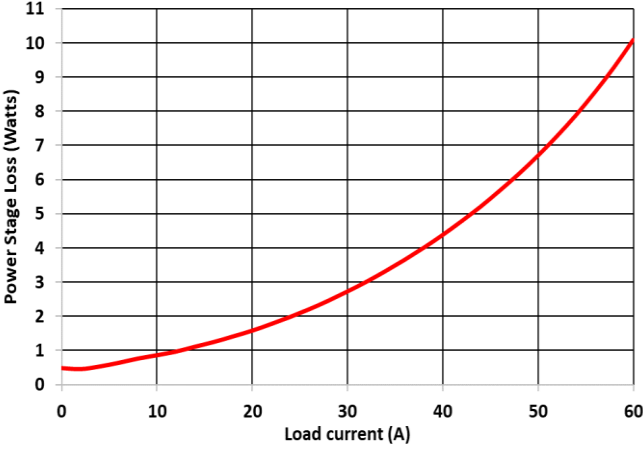


Figure 5 Power stage Loss

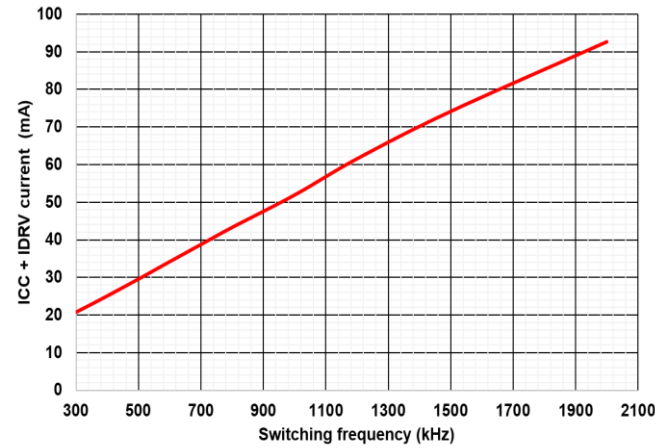


Figure 6 VCC / VDRV current vs Frequency

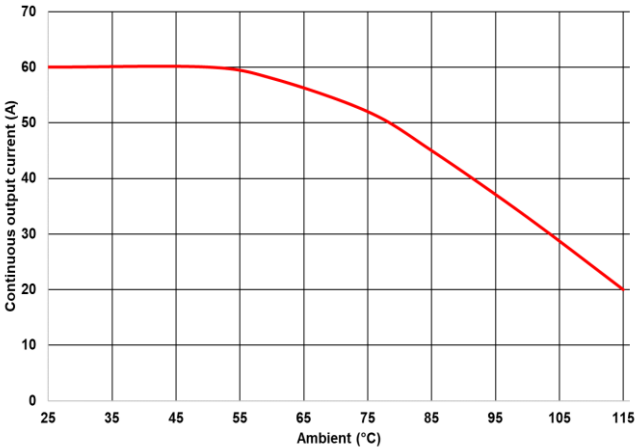


Figure 7 Thermal derating

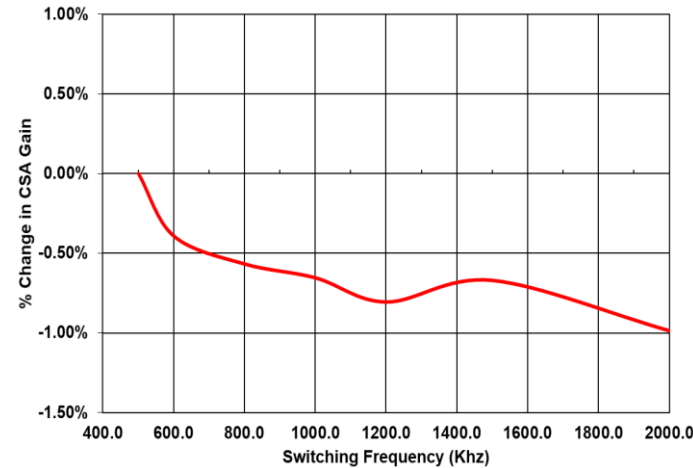


Figure 8 Current sense gain variation vs Frequency

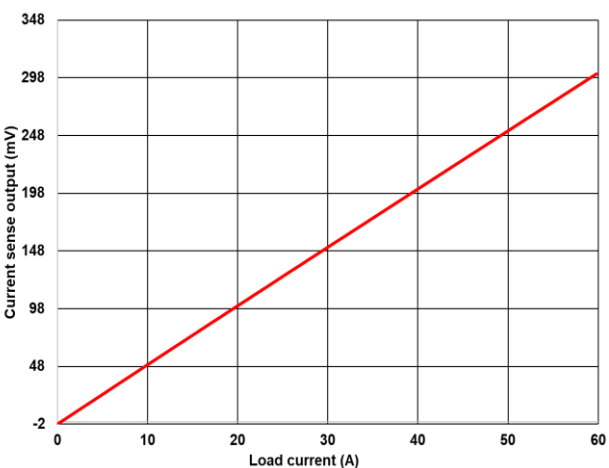


Figure 9 Current sense output

Single Phase Circuit of Figure 18, $V_{IN} = 12\text{ V}$, $V_{OUT} = 0.8\text{ V}$, $f_{SW} = 500\text{ KHz}$, $L = 100\text{ nH}$, $V_{CC} = V_{DRV} = 5\text{ V}$, $T_{AMBIENT} = 25\text{ }^{\circ}\text{C}$, $R_{IMON} = 1\text{ k}\Omega$ 0.1%, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

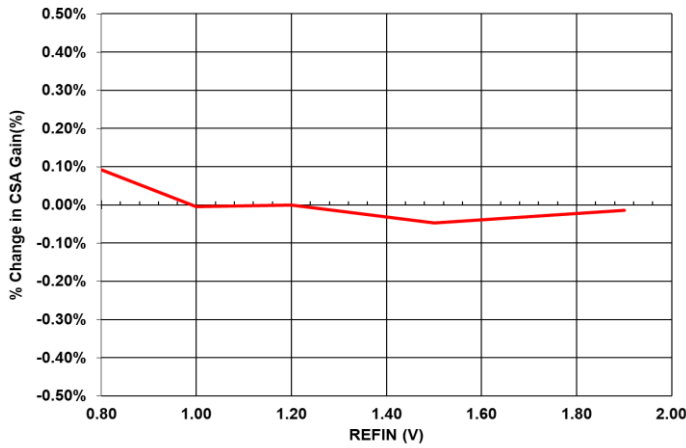


Figure 10 Current sense gain vs Reference Voltage

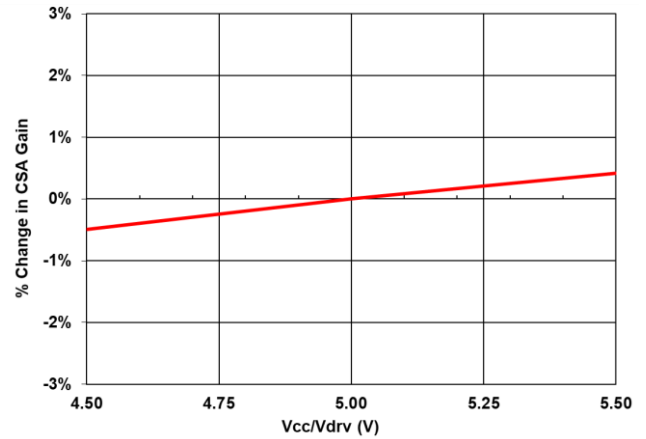


Figure 11 Current sense gain variation vs VCC/VDRV

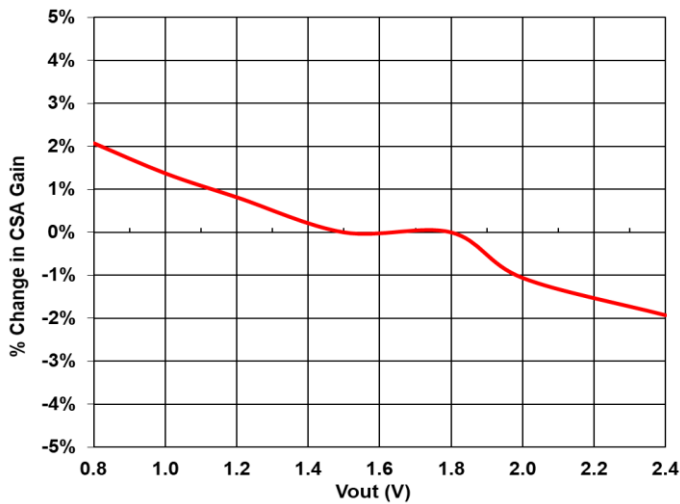


Figure 12 Current sense gain variation vs Vout

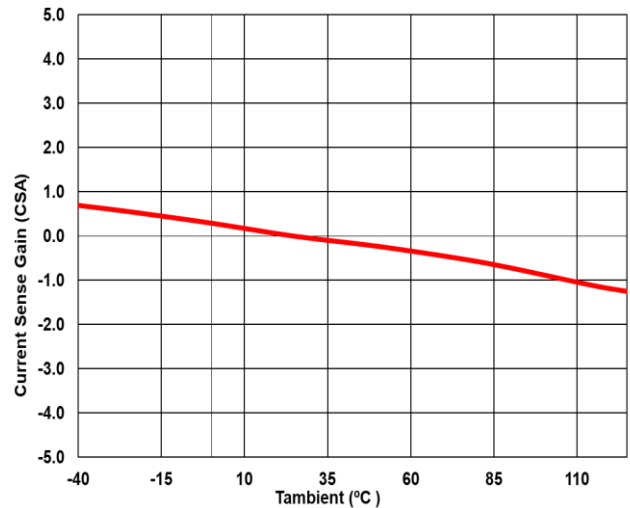


Figure 13 Current sense gain variation vs Temperature

6 Theory of Operation

6.1 Description

The TLF12501 contains an improved high speed MOSFET driver optimized to drive a pair of co-packaged high-side and low-side Optimos MOSFETs at frequency up to 2 MHz. DC-DC controllers using traditional current sense methods like DCR sensing and $R_{ds(on)}$ sensing typically have limitations. DCR current sensing is sensitive to temperature changes of the inductor and needs temperature compensation either implemented externally using a thermo-couple or inside the power stage. $R_{ds(on)}$ current sensing, on the other hand, is not dependent on the inductor but there is a temperature co-efficient associated with the MOSFET $r_{ds(on)}$. Besides, it is difficult to implement $r_{ds(on)}$ current sensing for high-side MOSFET which is therefore replaced by emulated current while the low-side current is sensed across the MOSFET. With the advanced current-mirror sensing in TLF12501, all these limitations are eliminated while achieving superior accuracy. Current on both high-side as well as low-side MOSFET is mirrored on a sense MOSFET which is a part of the main MOSFET device, and hence comes with an inherent temperature compensation without the need for an additional circuitry. Real current-sensing on both MOSFET ensures that the system is always monitoring the real output current and can immediately react to any critical events like load step or over-current fault.

The TLF12501 reports accurate temperature with the gain of 8 mV / °C, which helps the system to actively monitor the temperature in real time. Temperature outputs from multiple power stages can be connected together to report the highest temperature to Infineon's digital PWM controller.

The TLF12501 PWM input is compatible with industry standard 3.3V PWM input with tri-state.

The TLF12501 can enable Body-Braking mode by responding to PWM tri-state signals sent from the controller, quickly disabling both MOSFETs in the power stage in order to enhance transient performance or provide a high impedance output.

The TLF12501 supports diode emulation mode through the PWM tri-state signal. Controlled by Infineon's digital PWM controller, the PWM tri-state signal will force the low-side FET to be off when the inductor current is about to go negative. The light-load efficiency then can be increased by preventing conduction loss caused by negative inductor current.

The TLF12501 also supports deep-sleep power saving mode. When in deep-sleep mode, the driver will disable most of the function circuitry to greatly reduce power consumption.

The TLF12501 features a full-range of protection, including VCC/VDRV Under-Voltage-Lockout (UVLO), thermal shutdown against an internal over-temperature condition, phase fault detection of a shorted high-side MOSFET, and cycle-by-cycle over-current protection due to an overload condition or saturated output inductor.

The TLF12501 also features internal protection circuitry to automatically replenish the voltage across the bootstrap capacitor. It avoids the gradual depletion of capacitor energy when the power stage sits in tri-state for a long period of time.

6.2 Sleep Modes

When EN is pulled low, the power stage enters deep-sleep mode. The gate driver circuitry will be turned off immediately and most of the logic circuitry will be shut down to reduce the bias current to less than 32 μ A. The IMON output will be shorted to IMONREF in deep sleep mode.

When EN toggles from low to high, the power stage will be active and able to accept PWM signals after a delay of 17 μ s.

6.3 Current Sensing and Reporting

The TLF12501 features a very accurate current mirror architecture on both high-side as well as low-side MOSFET, thus reporting the real time current information. The current information is reported using the IMON pin. The reported current is in the form of current output with the gain of 5 μ A/A from the IMON pin. In order to convert this into voltage, a 1k Ω , 0.1% resistor is recommended at the IMON pin and placed close to the PWM controller. A differential voltage signal from this resistor is connected to the controller as the reported current information. Note that for accurate current reporting, it is important that the other end of the resistor cannot be left floating. The converted voltage signal at the controller side has an effective gain of 5mV/A i.e. for every 1 A load, the controller will read 5mV from the power stage. The current-output differential signal from the power stage provides excellent noise immunity to the reported current information.

6.4 Advanced Fault reporting

TLF12501 uses TMON / FAULT pin for reporting all types of faults detected. Since typical multiphase applications connect the TMON / FAULT signal from all the phases in a particular loop into a wired OR connection, the system cannot distinguish the faulty phase and the type of fault occurred. This is resolved by using advanced fault reporting in TLF12501 which uses a combination of TMON / FAULT and IMON signals to identify the fault. Since the IMON is separately connected from each phase to the controller, it provides phase-specific information in the event of a fault. Appropriate IMON response to each fault is explained in the corresponding fault sub-sections further. A summary of fault reporting is given in the Table 14 at the end of Section 6.

6.5 VDRV Under-voltage Lock-out (UVLO)

TLF12501 features a VDRV under-voltage lock-out fault circuitry that monitors the VDRV voltage actively. As shown in Table 15, this is a non-catastrophic fault and the TMON/FAULT pin is pulled low with a weak pull down as long

as the VDRV voltage is below the UVLO threshold. If the power stage has not started up, the power stage PWM pin is also pulled down to 0V with a weak pull down. This can be monitored by the PWM controller as a signal from the power stage indicating that it is not ready yet for power up. As soon as VDRV voltage is above the UVLO threshold, the PWM pin is at tri state instead of 0V, this indicating the controller that it is OK to send the PWM signals.

Once the powerstage is in normal operation, if then it encounters a VDRV UVLO condition, the power stage stops switching, and both TMON and IMON pins are pulled down to 0V. If there are multiple phases connected in the same loop, the TMON pin voltage, being connected to other power stage TMON pins, will continue reporting the highest power stage temperature. But the controller can still detect IMON pin voltage to be 0V ($IMON - IMONREF = -IMONREF$, as seen by the controller), and thus identify this faulty phase. Since TMON pin is not pulled high, but continues reporting the temperature, this can be distinguished from a BOOT UVLO condition as shown in Table 14.

6.6 Temperature Reporting and Over-temperature protection

An internal temperature-sense circuit monitors the temperature of the TLF12501. The sensed temperature is reported at the TMON/FAULT pin with a linear voltage slope of 8mV/°C and a 0.6V offset at 0°C, as shown in equation (1).

$$V_{TMON/FAULT}(V) = 0.6V + 0.008V/^{\circ}C \times T_j(^{\circ}C) \dots\dots\dots (1)$$

The TMON/FAULT pin also serves as a FAULT pin that is pulled to 3.3V in case of any catastrophic faults and is pulled down to 0V in case of any non-catastrophic faults. When there is no fault, it continues reporting temperature as long as the VCC supply is connected to a voltage in the recommended operating range. For a junction temperature below -25°C, the TMON voltage is clamped to 0.4V to avoid false triggering of VDRV under-voltage.

Once the temperature rises above the OTP rising threshold (155 °C), the TMON/FAULT output will be pulled high immediately, the driver will stop switching and stop responding to the PWM signal input from the controller. Both high-side and low-side MOSFET are turned off. The TMON/FAULT will remain high until temperature falls below the falling threshold (143 °C). As soon as TMON is pulled high during OTP, the IMON is internally shorted to IMONREF, thus identifying the faulty phase and occurrence of OTP to the system.

6.7 Over-current Protection and Flag

This feature protects the power stage from self-destruction from repetitive high current events such as saturated inductors due to poor component selection or by incorrectly optimized control loops. These high current events could eventually lead to a shorted high-side MOSFET failure.

With cycle-by-cycle self-preservation, the current is monitored every cycle. If the over-current threshold (default 90 A) has been exceeded, the PWM high pulse will be truncated so that the inductor current is allowed to relax. When TLF12501 detects 10 consecutive PWM cycle over-current events, the TMON/FAULT pin is flagged high to indicate the controller of the fault. The TMON/FAULT flagged “high” along with IMON information crossing the over-current threshold helps the controller identify the faulty phase that caused OC. Note the PWM pulse “on-time” should be at least 50ns for accurate functioning over-current protection.

6.8 Bootstrap Capacitor Under-Voltage

TLF12501 features a bootstrap capacitor under-voltage circuitry that detects a missing bootstrap capacitor before powering up or a damaged bootstrap capacitor during normal operation. Once bootstrap capacitor under-voltage is determined, the TMON/FAULT pin will be pulled high to report a catastrophic fault to the PWM controller. At the same time, IMON pin is pulled to 0V or GND voltage, thus effectively indicating a negative IMONREF voltage differential between IMON and IMONREF pins at the controller.

Table 14 Advanced Fault Reporting

Fault Severity Level	Type of Fault	Power stage PWM Response	Power stage IMON Response	Powerstage TMON Response	Recommended Controller Identification Criteria
Non-Catastrophic	VDRV UVLO (power-up)	Weak pull down to 0V (PWM pin voltage can be driven by controller, no switching on powerstage)	= IMONREF	Weak pull down to 0V (or V_{TMON} from other power stages in same loop)	$TMON < 2V$, $PWM < 0.8V$
	VDRV UVLO (normal operation)	Weak pull down to 0V (PWM pin voltage can be driven by controller, no switching on powerstage)	= 0V	Weak pull down to 0V (or V_{TMON} from other power stages in same loop)	$TMON < 2V$, $IMON < 0.4V$
Catastrophic	OTP	Power stage stops switching until OTP clears	=IMONREF	= 3.3V	$TMON > 2.6V$, $IMON=IMONREF$, $1V < IMON < 2V$
	OCP (10 events without 3 consecutive good cycles)	Power stage continues responding to PWM signal from controller. Truncates high side pulse until powerstage is in OCP.	Continues reporting current	= 3.3V	$TMON > 2.6V$, $IMON-IMONREF > CTRL_OCP$, $IMON < 2.6V$
	HSS (1 st event)	Power stage continues responding to PWM signal from controller.	= 3.3V (latched)	= 3.3V	$TMON > 2.6V$, $IMON > 2.6V$
	BOOT UVLO (10 events without 3 consecutive good cycles)	Power stage continues responding to PWM signal from controller.	= 0V (latched)	= 3.3V	$TMON > 2.6V$, $IMON < 0.4V$

7 Application Diagram

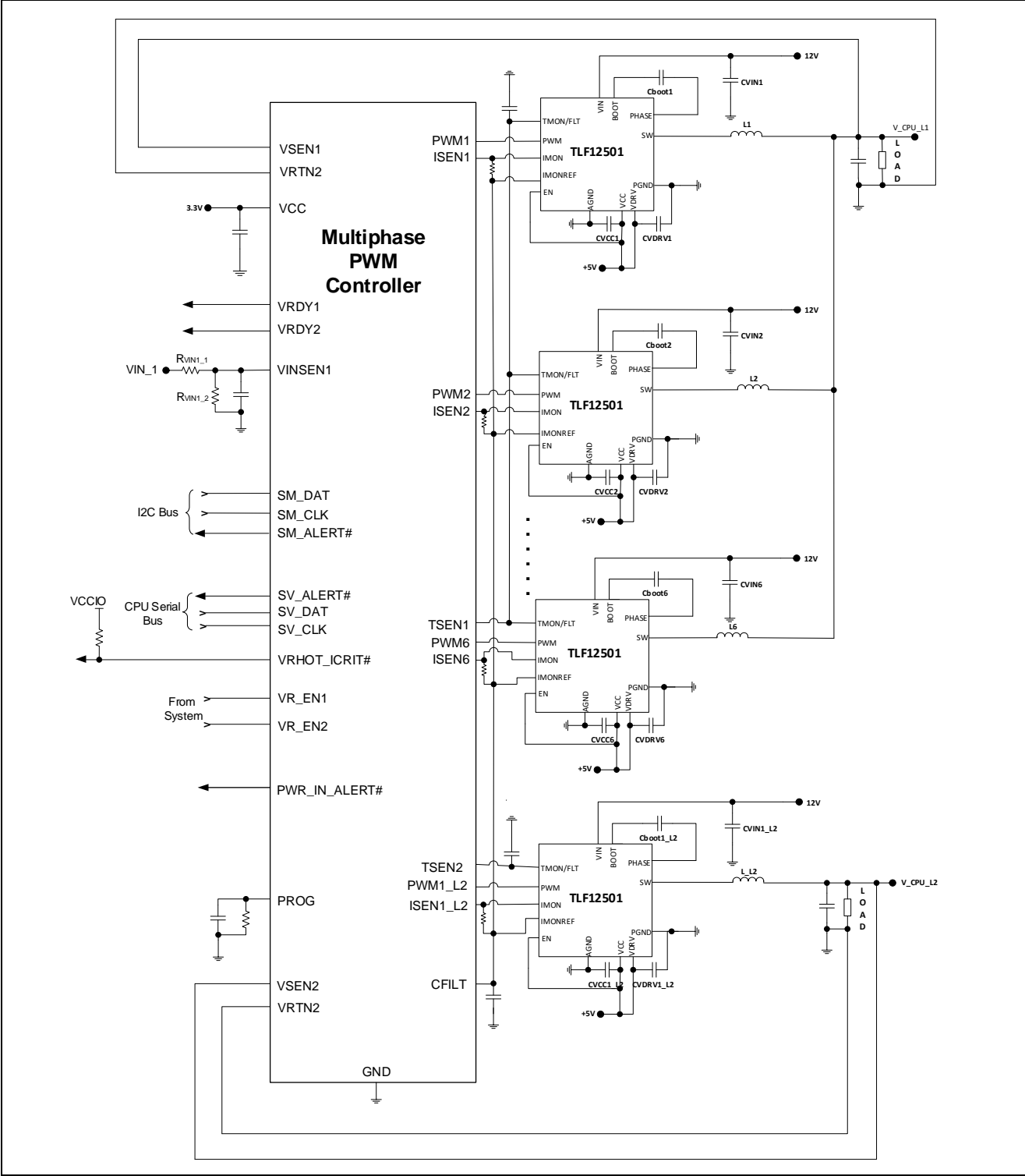


Figure 14 6+1 - Phase Voltage Regulator - Typical Application (simplified schematic)

8 Mechanical Dimensions (Top View and Side View) PQFN

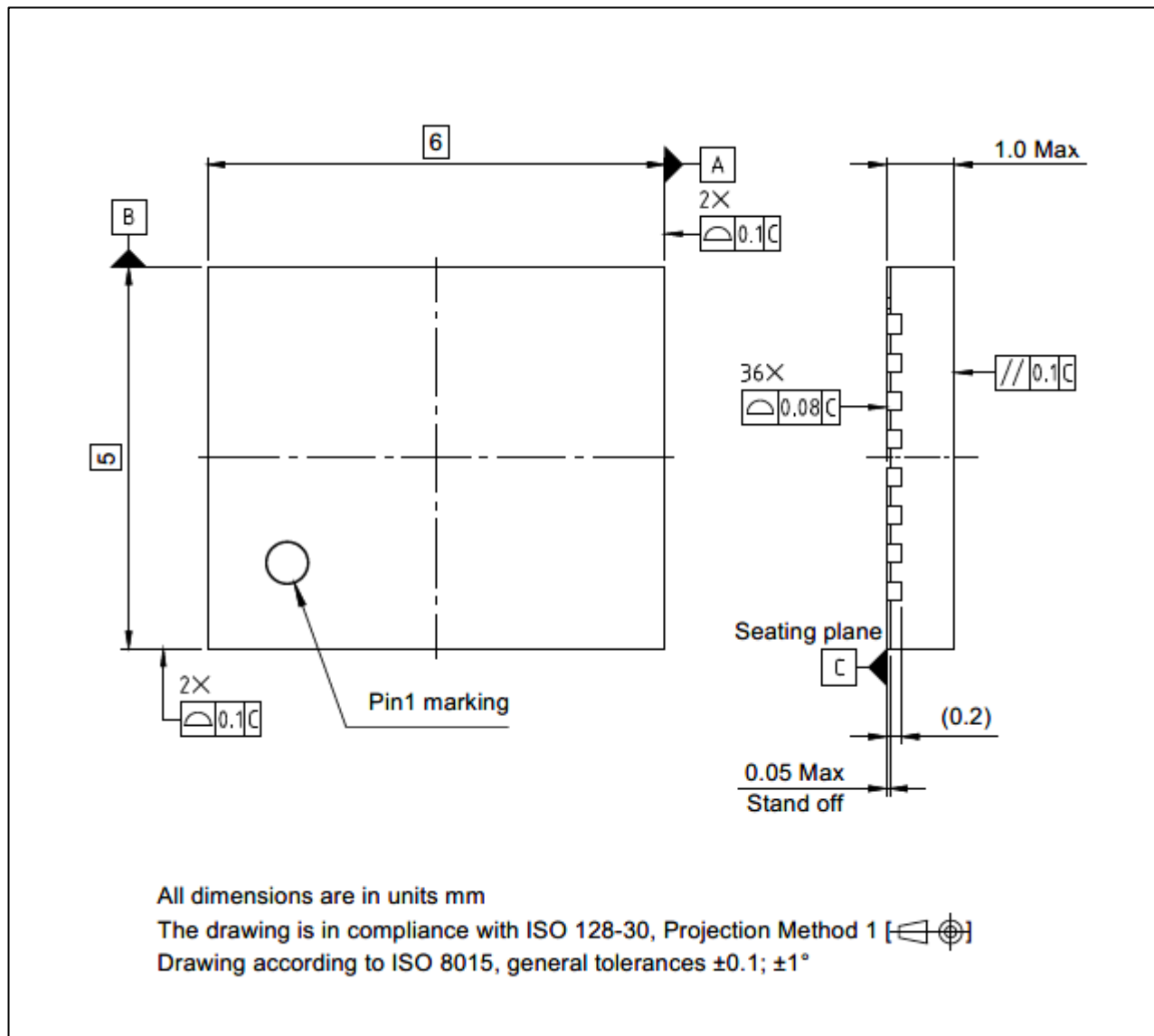


Figure 15 Mechanical Dimensions of Package (Top View and Side View) in mm

9 Mechanical Dimensions of Package in mm

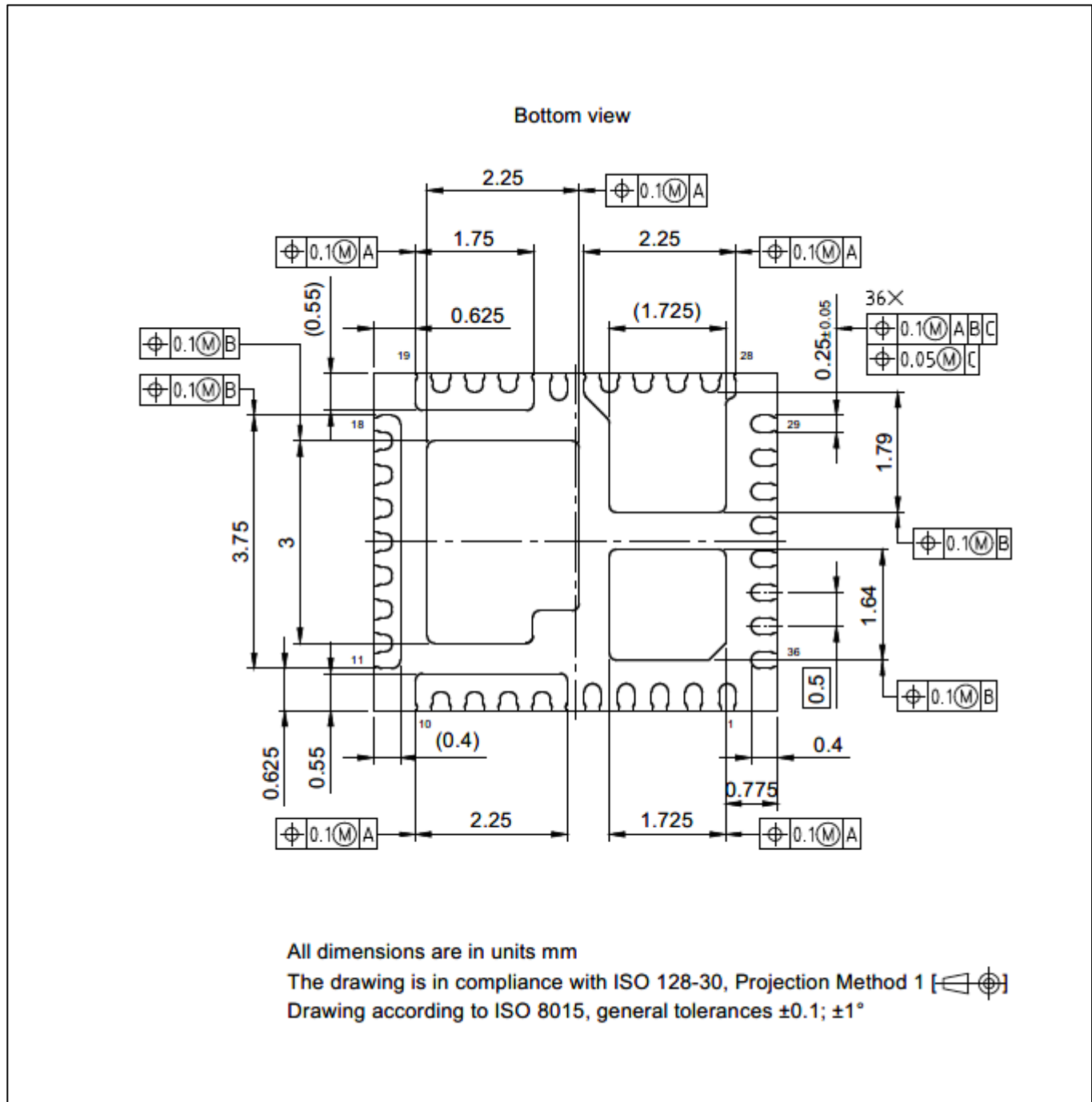


Figure 16 Mechanical Dimensions of Package (Bottom View) in mm

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