

Description

The LSF0106/0108 is 6/8-CH bi-directional multi-voltage level translator for open-drain and push-pull applications. This device is a universal level translator with A port operating from 0.65V to 4.5V (Vref_A) and B port 1.5V to 5.5V (Vref_B). This range allows for bi-directional voltage translations between 0.65V and 5.0V. Meanwhile, Vref_B is recommended to be at 1V higher than Vref_A for best signal integrity.

The EN pin is used to activate the device. When EN is HIGH, the translator switch is on. Otherwise, EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input must be connected to Vref_B and both pins pulled to HIGH through a pullup resistor (typically 200kΩ). EN must be LOW to ensure the high-impedance state during power-up or power-down.

Be aware that external Rpu (pullup resistor) is required on each signal in both A and B ports for push-pull application because a pull-high state can avoid misoperation during power-up or power-down. As same as open-drain application, the smaller Rpu results in the larger driving current. For bi-directional signal flows, there is no need for a direction pin to minimize system effort. This device supports 5V tolerant I/O pins in a variety of applications which require different voltage translation levels.

Features

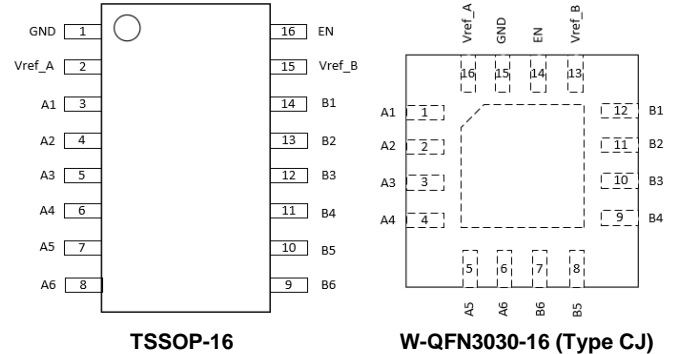
- Bi-directional level shifter for both push-pull and open-drain
- Maximum data rate is dominated by the system capacitance and pullup resistors
 - $\leq 100\text{MHz}$; $C_L = 15\text{pF}, 30\text{pF}$, $R_{pu} \leq 300\Omega$
 - $\leq 50\text{MHz}$; $C_L = 50\text{pF}$, $R_{pu} \leq 300\Omega$
- Bi-directional voltage level translation between:
 - 0.65V and 1.5V, 1.8V, 2.5V, 3.3V and 5.0V
 - 1.2V and 1.8V, 2.5V, 3.3V and 5.0V
 - 1.8V and 2.5V, 3.3V and 5.0V
 - 2.5V and 3.3V and 5.0V
 - 3.3V and 5.0V
- ESD protection exceeds JESD 22
 - 3500V HBM (A114)
 - 1500V CDM (C101)
- Latchup exceeds 100mA per JESD 17
- 5V tolerant I/O pins to support TTL
- Specified from -40°C to $+125^\circ\text{C}$
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.**

<https://www.diodes.com/quality/product-definitions/>

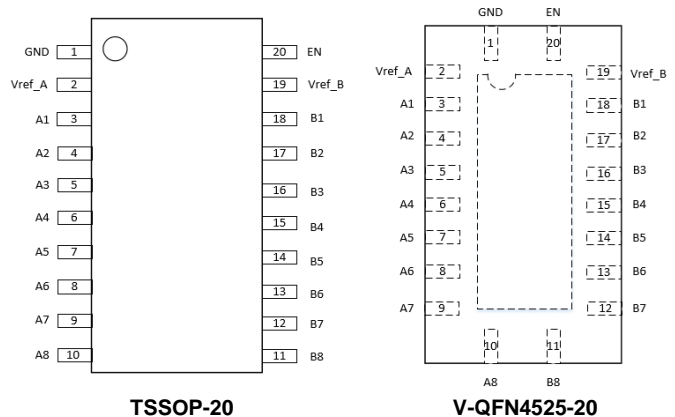
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain $<900\text{ppm}$ bromine, $<900\text{ppm}$ chlorine ($<1500\text{ppm}$ total Br + Cl) and $<1000\text{ppm}$ antimony compounds.

Pin Assignments

LSF0106 Packages



LSF0108 Packages



Applications

- GPIO, MDIO, SDIO, SVID, UART
- PMBus, SMBus, I2C, and other interfaces
- Telecom infrastructures
- Industrials
- High-performance computing
- Wide array of products such as:
 - PCs, networking, notebooks
 - Smart phones
 - Tablets

Pin Descriptions

LSF0106 Pin Descriptions

Pin Name	Pin Number		Function
	TSSOP-16	W-QFN3030-16 (Type C-J)	
GND	1	15	Ground
Vref_A	2	16	Reference supply voltage; A port
A1	3	1	Input/output 1
A2	4	2	Input/output 2
A3	5	3	Input/output 3
A4	6	4	Input/output 4
A5	7	5	Input/output 5
A6	8	6	Input/output 6
B6	9	7	Output/input 6
B5	10	8	Output/input 5
B4	11	9	Output/input 4
B3	12	10	Output/input 3
B2	13	11	Output/input 2
B1	14	12	Output/input 1
Vref_B	15	13	Reference supply voltage; B port
EN	16	14	Enable input (Active HIGH)

LSF0108 Pin Descriptions

Pin Name	Pin Number		Function
	TSSOP-20	V-QFN4525-20	
GND	1	1	Ground
Vref_A	2	2	Reference supply voltage; A port
A1	3	3	Input/output 1
A2	4	4	Input/output 2
A3	5	5	Input/output 3
A4	6	6	Input/output 4
A5	7	7	Input/output 5
A6	8	8	Input/output 6
A7	9	9	Input/output 7
A8	10	10	Input/output 8
B8	11	11	Output/input 8
B7	12	12	Output/input 7
B6	13	13	Output/input 6
B5	14	14	Output/input 5
B4	15	15	Output/input 4
B3	16	16	Output/input 3
B2	17	17	Output/input 2
B1	18	18	Output/input 1
Vref_B	19	19	Reference supply voltage; B port
EN	20	20	Enable input (Active HIGH)

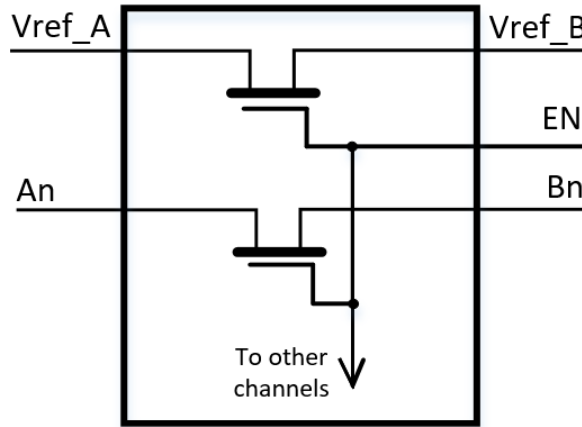
Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	±3.5	kV
ESD CDM	Charged Device Model ESD Protection	±1.5	kV
VREF	Supply Reference Voltage Range	-0.5 to +7.0	V
V _{I/O}	Input-Output Voltage Range	-0.5 to +7.0	V
I _{CH}	Continuous Channel Current	128	mA
I _{IK}	Input Clamp Current, V _I < 0	-50	mA
T _J	Junction Temperature	+150	°C
T _{STG}	Storage Temperature	-65 to +150	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Functional Diagram

NOTE:
See Load Circuit
Suggest to connect EN to Vref_B and both pins pulled to HIGH through a pullup resistor (typically 200kΩ)



Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vref_A	Reference Voltage, A Port	0.65	4.5	V
Vref_B	Reference Voltage, B Port, when Vref_A ≥ 1V	Vref_A + 0.6	5.5	V
	Reference Voltage, B Port, when Vref_A < 1V	Vref_A + 0.8	5.5	V
V _{I/O}	Input/Output Voltage	0	5.5	V
V _{EN}	Enable Voltage when Vref_A ≥ 1V	Vref_A + 0.6	5.5	V
	Enable Voltage when Vref_A < 1V	Vref_A + 0.8	5.5	V
I _{PASS}	Pass Transistor Current	—	64	mA
T _A	Operating Free-Air Temperature	-40	+125	°C

Electrical Characteristics (Over operating free-air temperature range, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ (Note 5)	Max	Unit	
Vref_A	A port supply voltage	What if config to be low voltage side	0.65	—	4.5	V	
Vref_B	B port supply voltage	What if config to be high voltage side	1.5	—	5.5	V	
V _{IK}	Input clamping voltage	I _I = -18mA, V _{EN} = 0	-1.2	—	0	V	
I _L	Leakage current	Pins An, Bn, Vref_A, Vref_B and EN; V _I = GND to 5.0V	0.001	0.1	3	μA	
I _{CC}	Supply current	Vref_B = EN = 5.5V, Vref_A = 4.5V, I _o = 0, V _I = 0V or V _{CC}	—	0.05	5	μA	
C _i (Vref_A/B/EN)		V _I = 3V or 0	—	10	—	pF	
C _{IO(off)}		V _O = 3V or 0, EN = 0	—	5	6	pF	
C _{IO(on)}		V _O = 3V or 0, EN = 3 V	—	10	13	pF	
R _{on} (Note 6)	V _I = 0, I _o = 64mA	Vref_A = 3.3V; Vref_B = EN = 5V	—	3	—	Ω	
		Vref_A = 2.5V; Vref_B = EN = 5V	—	3	—		
		Vref_A = 1.8V; Vref_B = EN = 5V	—	4	—		
		Vref_A = 1.0V; Vref_B = EN = 5V	—	5	—		
	V _I = 0, I _o = 32mA	Vref_A = 3.3V; Vref_B = EN = 5V	—	3	—		
		Vref_A = 2.5V; Vref_B = EN = 5V	—	3	—		
		Vref_A = 1.8V; Vref_B = EN = 5V	—	4	—		
		Vref_A = 1.0V; Vref_B = EN = 5V	—	5	—		
	V _I = 0, I _o = 20mA		Vref_A = 0.65V; Vref_B = EN = 5V	—	15		—
	V _I = 1.8V, I _o = 15mA, Vref_A = 3.3V; Vref_B = EN = 5V			—	4		—
	V _I = 1.0V, I _o = 10mA, Vref_A = 1.8V; Vref_B = EN = 3.3V			—	7		—
	V _I = 0V, I _o = 10mA	Vref_A = 1.0V; Vref_B = EN = 3.3V	—	5	—		
		Vref_A = 0.65V; Vref_B = EN = 3.3V	—	15	—		
		Vref_A = 1.0V; Vref_B = EN = 1.8V	—	6	—		
Vref_A = 0.65V; Vref_B = EN = 1.8V		—	15	—			

Notes: 5. All typical values are measured at T_A = +25°C.
6. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

Translating Down Switching Characteristics (Note 7, $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Translating Down, 5.0V to 1.8V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.5	0.3	0.2	ns
t_{PHL}			0.9	0.7	0.5	ns

Test conditions: $V_{ref_A} = 1.8\text{V}$, $V_{PU} = V_{IH} = 5.0\text{V}$, $V_M = 0.9\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Translating Down, 3.3V to 1.8V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.4	0.2	0.1	ns
t_{PHL}			1.0	0.7	0.4	ns

Test conditions: $V_{ref_A} = 1.8\text{V}$, $V_{PU} = V_{IH} = 3.3\text{V}$, $V_M = 0.9\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Translating Down, 3.3V to 1.2V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.6	0.4	0.2	ns
t_{PHL}			1.1	0.8	0.6	ns

Test conditions: $V_{ref_A} = 1.2\text{V}$, $V_{PU} = V_{IH} = 3.3\text{V}$, $V_M = 0.6\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Translating Down, 1.8V to 1.2V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.5	0.3	0.1	ns
t_{PHL}			1.8	1.4	1.1	ns

Test conditions: $V_{ref_A} = 1.2\text{V}$, $V_{PU} = V_{IH} = 1.8\text{V}$, $V_M = 0.6\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Translating Down, 1.8V to 0.8V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.7	0.4	0.2	ns
t_{PHL}			1.5	1.2	0.9	ns

Test conditions: $V_{ref_A} = 0.8\text{V}$, $V_{PU} = V_{IH} = 1.8\text{V}$, $V_M = 0.4\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Translating Down, 1.8V to 0.65V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	0.8	0.5	0.3	ns
t_{PHL}			1.6	1.2	1.0	ns

Test conditions: $V_{ref_A} = 0.65\text{V}$, $V_{PU} = V_{IH} = 1.5\text{V}$, $V_M = 0.32\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Translating Down, 1.5V to 0.65V

Parameter	From (Input)	To (Output)	$C_L = 50\text{pF}$	$C_L = 30\text{pF}$	$C_L = 15\text{pF}$	Unit
			Typ	Typ	Typ	
t_{PLH}	B	A	1.0	0.6	0.4	ns
t_{PHL}			1.9	1.5	1.1	ns

Test conditions: $V_{ref_A} = 0.65\text{V}$, $V_{PU} = V_{IH} = 1.5\text{V}$, $V_M = 0.4\text{V}$, $PRR = 10\text{MHz}$ (unless otherwise noted, see load circuit)

Note: 7. All typical values are measured at $T_A = +25^\circ\text{C}$. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{MHz}$; $Z_O = 50\Omega$. Definitions test circuit: $C_L = \text{Load capacitance including jig and probe capacitance}$; $R_L = \text{Load resistance} = 300\Omega$; $R_{pu} = \text{ext. pullup resistance} = 200\text{k}\Omega$.

Translating Up Switching Characteristics (Note 7, T_A = 25°C, unless otherwise specified.)

Translating Up, 1.8V to 5.0V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.4	0.3	0.3	ns
t _{PHL}			2.3	1.7	1.0	ns

Test conditions: V_{IH} = V_{ref_A} = 1.8V, V_{EXT} = V_{PU} = 5.0V, R_L = 300Ω, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)

Translating Up, 1.8V to 3.3V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.4	0.3	0.3	ns
t _{PHL}			1.7	1.2	0.6	ns

Test conditions: V_{IH} = V_{ref_A} = 1.8V, V_{EXT} = V_{PU} = 3.3V, R_L = 300Ω, V_M = 0.9V, PRR = 10MHz (unless otherwise noted, see load circuit)

Translating Up, 1.2V to 3.3V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.4	0.3	0.2	ns
t _{PHL}			2.9	2.2	1.6	ns

Test conditions: V_{IH} = V_{ref_A} = 1.2V, V_{EXT} = V_{PU} = 3.3V, R_L = 300Ω, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)

Translating Up, 1.2V to 1.8V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.6	0.3	0.2	ns
t _{PHL}			2.8	2.3	1.8	ns

Test conditions: V_{IH} = V_{ref_A} = 1.2V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.6V, PRR = 10MHz (unless otherwise noted, see load circuit)

Translating Up, 0.8V to 1.8V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.6	0.3	0.2	ns
t _{PHL}			3.7	2.9	2.1	ns

Test conditions: V_{IH} = V_{ref_A} = 0.8V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.4V, PRR = 10MHz (unless otherwise noted, see load circuit)

Translating Up, 0.65V to 1.8V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.7	0.3	0.2	ns
t _{PHL}			5.0	3.8	2.7	ns

Test conditions: V_{IH} = V_{ref_A} = 0.65V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.32V, PRR = 10MHz (unless otherwise noted, see load circuit)

Translating Up, 0.65V to 1.5V

Parameter	From (Input)	To (Output)	C _L = 50pF	C _L = 30pF	C _L = 15pF	Unit
			Typ	Typ	Typ	
t _{PLH}	A	B	0.7	0.3	0.2	ns
t _{PHL}			5.0	3.8	2.7	ns

Test conditions: V_{IH} = V_{ref_A} = 0.65V, V_{EXT} = V_{PU} = 1.8V, R_L = 300Ω, V_M = 0.32V, PRR = 10MHz (unless otherwise noted, see load circuit)

Note: 7. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; Z_O = 50Ω. Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance = 300Ω; R_{pu} = ext. pullup resistance = 200kΩ.

Parameter Measurement Information

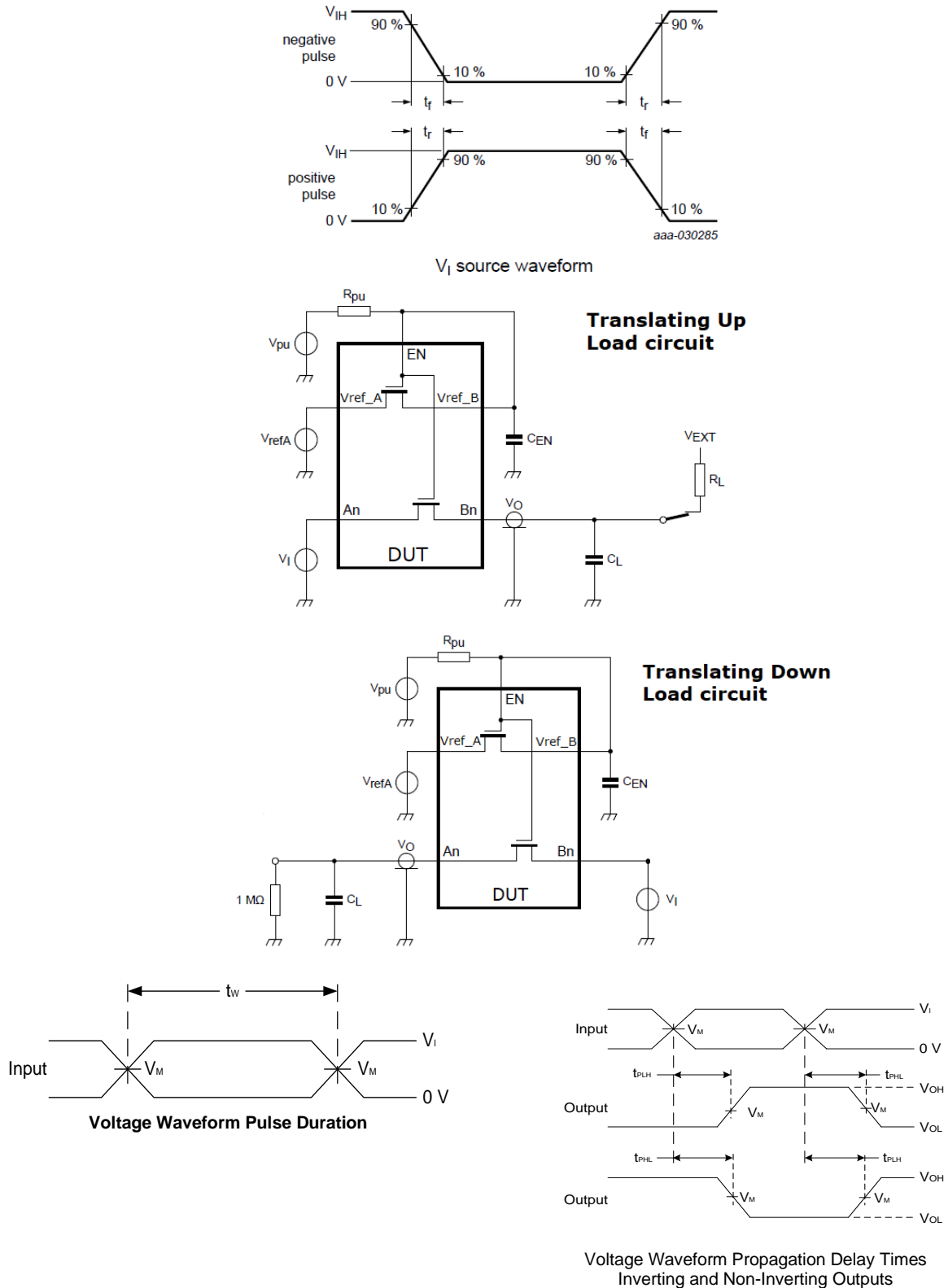


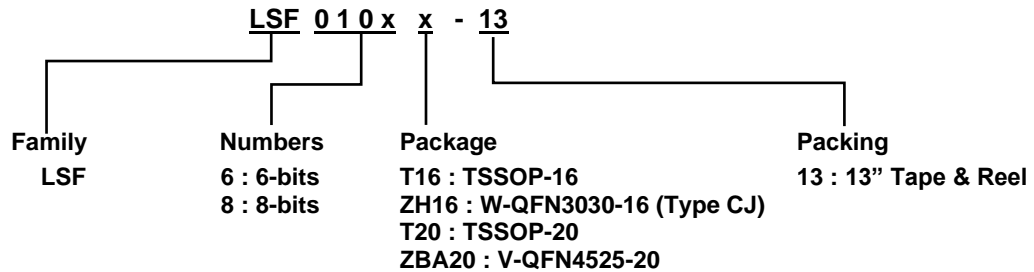
Figure 1. Load Circuit and Voltage Waveforms, $R_{pu} = 200k\Omega$, $C_{EN} = 0.1\mu F$, $R_L = 300\Omega$, $C_L = 15pF, 30pF, 50pF$

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	TSSOP-16	Note 8	—	136	—	°C/W
		W-QFN3030-16 (Type CJ)		—	89	—	
		TSSOP-20		—	95	—	
		V-QFN4525-20		—	59	—	
θ_{JC}	Thermal Resistance Junction-to-Case	TSSOP-16	Note 8	—	57	—	
		W-QFN3030-16 (Type CJ)		—	26	—	
		TSSOP-20		—	22	—	
		V-QFN4525-20		—	22	—	

Note: 8. Test condition for each of the 3 package types: device mounted on JEDEC standard PCB per JESD51, with minimum recommended pad layout.

Ordering Information



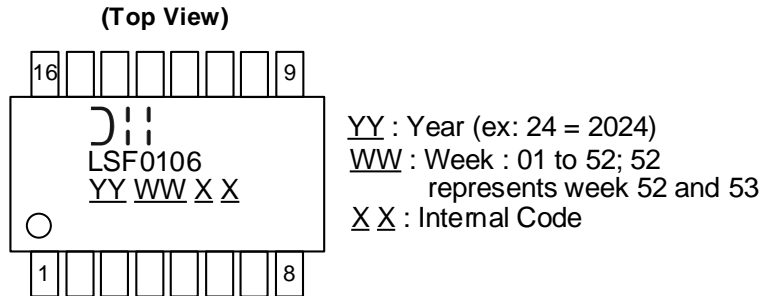
Orderable Part Number	Part Number Suffix	Package Code	Package	Packing (Note 9)	
				Qty.	Carrier
LSF0106T16-13	-13	T16	TSSOP-16	2500	13" Tape and Reel
LSF0106ZH16-13	-13	ZH16	W-QFN3030-16 (Type CJ)	5000	13" Tape and Reel
LSF0108T20-13	-13	T20	TSSOP-20	4000	13" Tape and Reel
LSF0108ZBA20-13	-13	ZBA20	V-QFN4525-20	2500	13" Tape and Reel

Notes: 9. The taping orientation is located on our website at <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf>
 10. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.
 11. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at <http://www.diodes.com/package-outlines.html>.

Marking Information

For LSF0106

(1) TSSOP-16

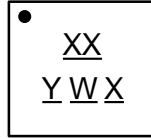


Orderable Part Number	Package	Identification Code
LSF0106T16-13	TSSOP-16	LSF0106

Marking Information (continued)

(2) W-QFN3030-16 (Type CJ)

(Top View)



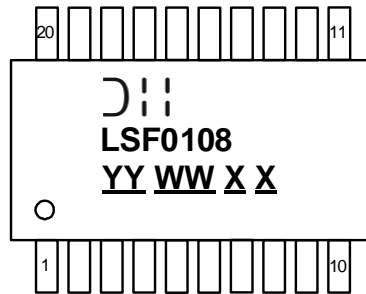
XX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
LSF0106ZH16-13	W-QFN3030-16 (Type CJ)	JG

For LSF0108

(1) TSSOP-20

(Top View)

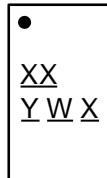


YY : Year (ex: 24 = 2024)
WW : Week : 01 to 52; 52 represents week 52 and 53
XX : Internal Code

Orderable Part Number	Package	Identification Code
LSF0108T20-13	TSSOP-20	LSF0108

(2) V-QFN4525-20

(Top View)



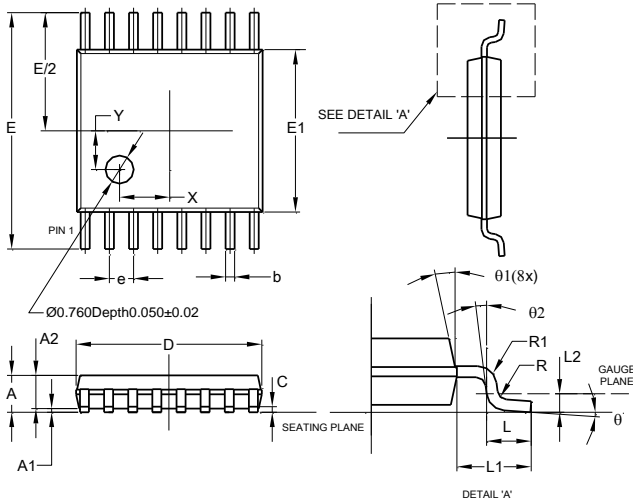
XX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
LSF0108ZBA20-13	V-QFN4525-20	JH

Package Outline Dimensions (LSF0106)

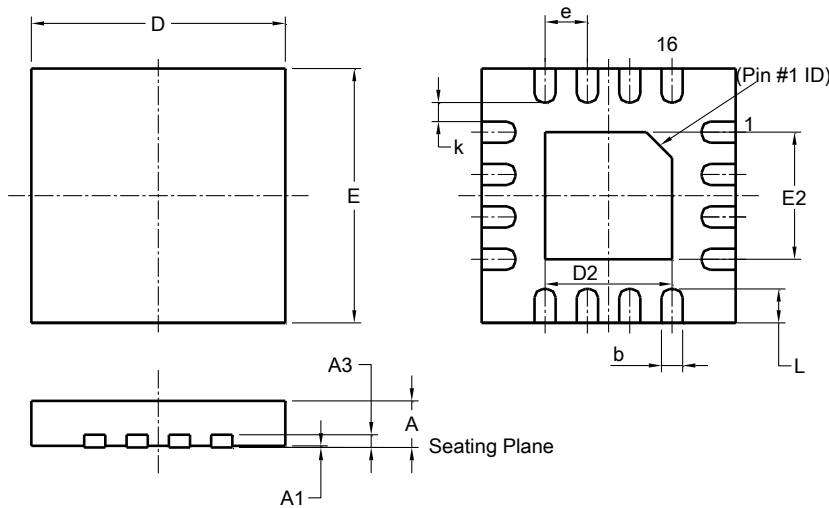
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

TSSOP-16



TSSOP-16			
Dim	Min	Max	Typ
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ_1	5°	15°	-
θ_2	0°	-	-
All Dimensions in mm			

W-QFN3030-16 (Type CJ)

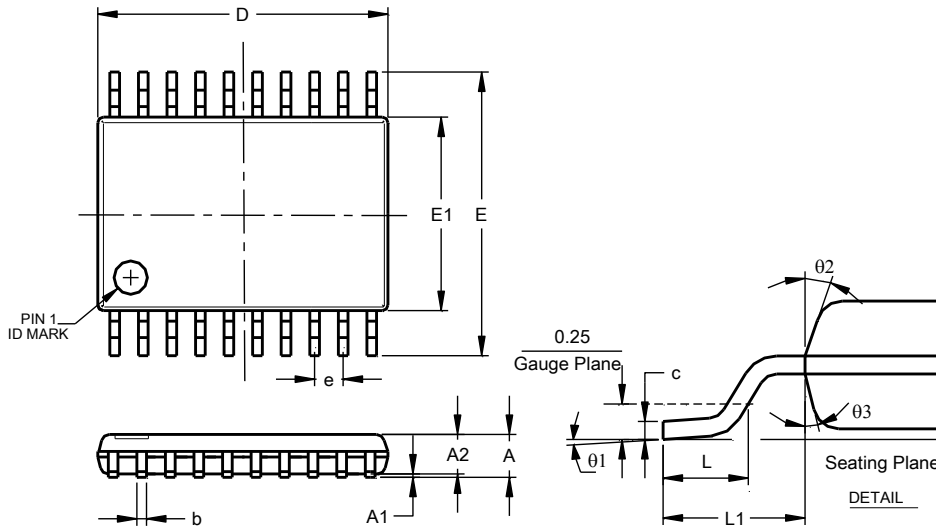


W-QFN3030-16 (Type CJ)			
Dim	Min	Max	Typ
A	0.700	0.800	--
A1	0.000	0.050	--
A3	0.203 REF		
b	0.180	0.300	--
D	3.00 BSC		
D2	1.600	1.800	--
E	3.00 BSC		
E2	1.600	1.800	--
e	0.500 TYP		
k	0.200 MIN		
L	0.300	0.500	--
All Dimensions in mm			

Package Outline Dimensions (LSF0108)

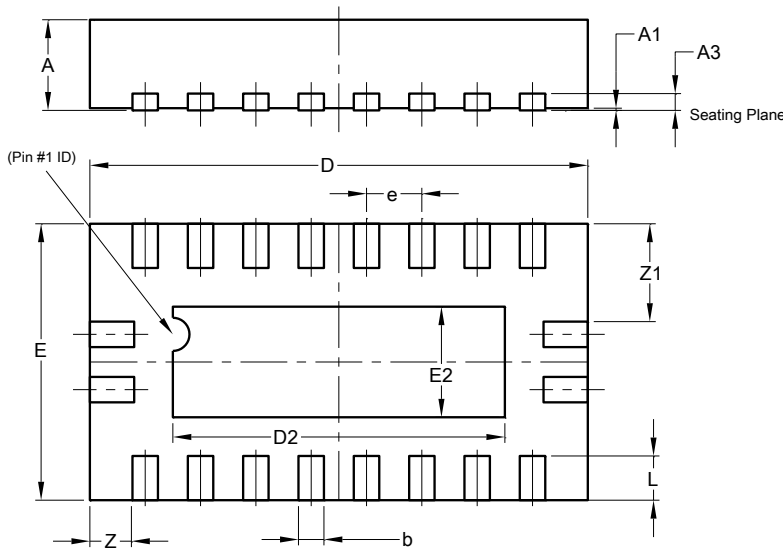
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

TSSOP-20



TSSOP-20			
Dim	Min	Max	Typ
A	-	1.20	-
A1	0.05	0.15	-
A2	0.80	1.05	-
b	0.19	0.30	-
c	0.09	0.20	-
D	6.40	6.60	6.50
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
theta1	0°	8°	-
theta2	10°	14°	12°
theta3	10°	14°	12°
All Dimensions in mm			

V-QFN4525-20

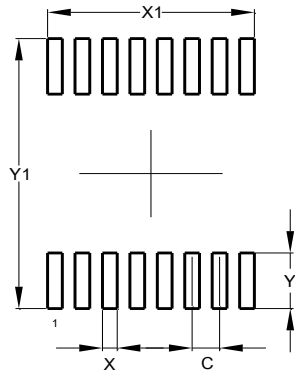


V-QFN4525-20			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.18	0.30	0.23
D	4.45	4.55	4.50
D2	2.85	3.15	3.00
E	2.45	2.55	2.50
E2	0.85	1.15	1.00
e	0.50BSC		
L	0.30	0.50	0.40
Z	-	-	0.385
Z1	-	-	0.885
All Dimensions in mm			

Suggested Pad Layout (LSF0106)

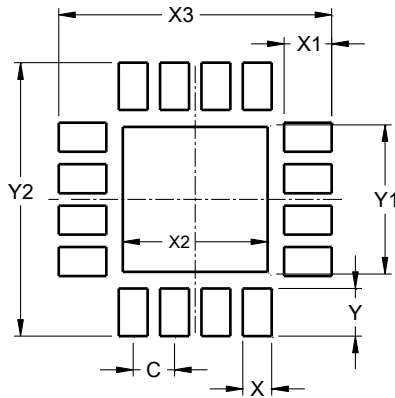
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

TSSOP-16



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	4.900
Y	1.400
Y1	6.800

W-QFN3030-16 (Type CJ)

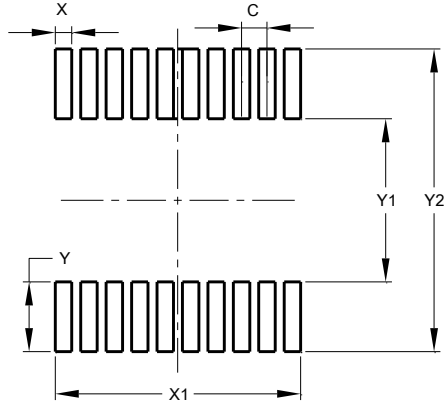


Dimensions	Value (in mm)
C	0.500
X	0.350
X1	0.570
X2	1.800
X3	3.300
Y	0.570
Y1	1.800
Y2	3.300

Suggested Pad Layout (LSF0108)

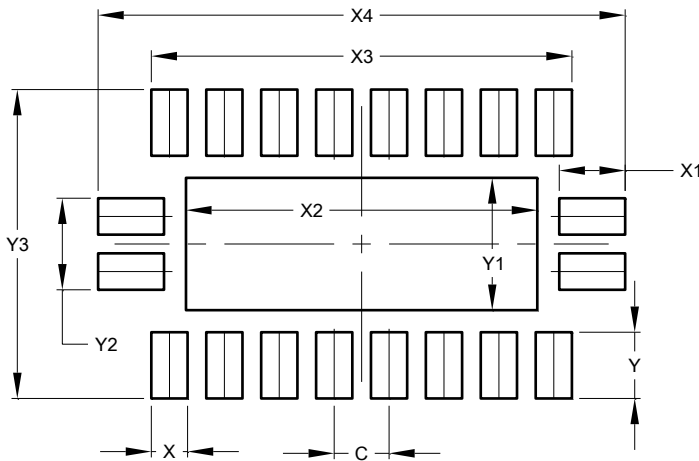
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

TSSOP-20



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	6.270
Y	1.780
Y1	4.160
Y2	7.720

V-QFN4525-20



Dimensions	Value (in mm)
C	0.500
X	0.330
X1	0.600
X2	3.200
X3	3.830
X4	4.800
Y	0.600
Y1	1.200
Y2	0.830
Y3	2.800

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ③
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020
- Weight:
 - TSSOP-16: 0.054811 grams (Approximate)
 - W-QFN3030-16 (Type CJ): 0.035 grams (Approximate)
 - TSSOP-20: 0.071 grams (Approximate)
 - V-QFN4525-20: 0.024 grams (Approximate)

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).
2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.
3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.
4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.
5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.
7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.
8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.
9. This Notice may be periodically updated with the most recent version available at <https://www.diodes.com/about/company/terms-and-conditions/important-notice>

The Diodes logo is a registered trademark of Diodes Incorporated in the United States and other countries.
All other trademarks are the property of their respective owners.
© 2024 Diodes Incorporated. All Rights Reserved.

www.diodes.com