Data Sheet

ADL8120

30 kHz to 20 GHz, Ultra-Wideband, Low Noise Amplifier

FEATURES

- Single positive supply (self biased)
- Resistor programmable bias setting
- Wideband operation: 30 kHz to 20 GHz
- Extended operating temperature range: −55°C to +125°C
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Telecommunications
- Instrumentation
- Radar
- Electronic warfare

GENERAL DESCRIPTION

The ADL8120 is an ultra-wideband low noise amplifier (LNA) that operates from 30 kHz to 20 GHz. Typical gain and noise figure are 14 dB and 1.9 dB, respectively, from 30 kHz to 14 GHz. Output power for 1 dB compression (OP1dB), output third-order intercept (OIP3), and output second-order intercept (OIP2) are 16 dBm, 29.5 dBm and 33 dBm, respectively, from 30 kHz to 14 GHz. The nominal quiescent current (I_{DQ}), which can be adjusted, is 55 mA from a 3.3 V supply voltage (V_{DD}). The internally matched, DC-coupled RF input and output pins require external AC coupling capacitors along with a bias inductor on RFOUT. In addition, the RF input is biased through an external inductor connected between the VBIAS pin and the RFIN pin.

The ADL8120 is fabricated on a pseudomorphic high electron mobility transistor (pHEMT) process. It is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP and is specified for operation from −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

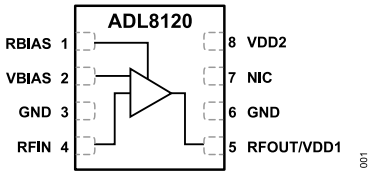

Figure 1. Functional Block Diagram

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REVISION HISTORY

4/2024—Revision 0: Initial Version

SPECIFICATIONS

30 KHz TO 14 GHz FREQUENCY RANGE

V_{DD} = 3.3 V, I_{DQ} = 55 mA, bias resistance (R_{BIAS}) = 542 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 30 kHz to 14 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.00003		14	GHz	Refer to the Low Frequency Bias Tee section for the parameter coverage and operation down to 30 kHz range
GAIN	12	14		dB	
Gain Variation over Temperature		0.0213		dB/°C	
NOISE FIGURE		1.9		dB	
RETURN LOSS					
Input (S11)		14		dB	
Output (S22)		15		dB	
OUTPUT					
OP1dB	13.5	16		dBm	
P_{SAT}		17.5		dBm	
OIP3		29.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 0 dBm
OIP2		33		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
POWER ADDED EFFICIENCY (PAE)		20.5		%	Measured at P_{SAT}

14 GHz TO 20 GHz FREQUENCY RANGE

V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 14 GHz to 20 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	14		20	GHz	
GAIN	13	15		dB	
Gain Variation over Temperature		0.022		dB/°C	
NOISE FIGURE		2.3		dB	
RETURN LOSS					
S11		8		dB	
S22		15		dB	
OUTPUT					
OP1dB	11	13.5		dBm	
P_{SAT}		16		dBm	
OIP3		26.5		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		33		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		16		%	Measured at P_{SAT}

SPECIFICATIONS

DC SPECIFICATIONS

Table 3. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		55		mA
Amplifier Current (I_{DQ_AMP})		51		mA
RBIAS Current (I_{RBIAS})		4		mA
SUPPLY VOLTAGE				
V_{DD}	3	3.3	3.6	V

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	5.5 V
RF Input Power (RFIN)	28 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 10 mW/°C Above 85°C)	0.9 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 3.3 V, I_{DQ} = 55 mA, Input Power (P_{IN}) = Off)	103.15°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance.

Table 5. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	98	°C/W
Worst Case[2], T_{CASE} = 85°C	100	°C/W

1 Thermal resistance varies with operating conditions.

2 Across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8120

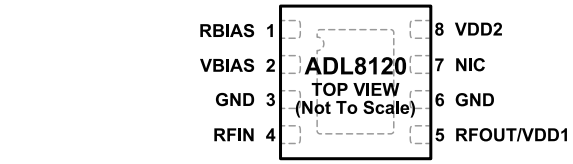
Table 6. ADL8120, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±300	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. THE NIC PIN IS NOT CONNECTED INTERNALLY. FOR NORMAL OPERATION, CONNECT THIS PIN TO GROUND.
2. GROUND PADDLE. CONNECT THE GROUND PADDLE TO A GROUND PLANE THAT HAS LOW ELECTRICAL AND THERMAL IMPEDANCE.

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDDx to set I_{DQ}. See Figure 109 and Table 8 for more details. See Figure 3 for the interface schematic.
2	VBIAS	Bias Setting Voltage Output. VBIAS sets the bias voltage for the RFIN pin. Connect VBIAS to RFIN using an inductor or ferrite bead as shown in Figure 109. See Figure 4 for the interface schematic.
3, 6	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 5 for the interface schematic.
4	RFIN	RF Input. The RFIN pin is DC-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
5	RFOUT/VDD1	RF Output and Drain Bias Voltage. The RF output is DC-coupled and also serves as the drain biasing node. For the drain bias voltage, connect a DC bias network to provide the drain current and AC-couple the RF output path. See Figure 7 for the interface schematic.
7	NIC	No Internal Connection. The NIC pin is not connected internally. For normal operation, connect this pin to ground.
8	VDD2	Drain Bias. Connect the VDD2 pin to a common supply with VDD1. See Figure 8 for the interface schematic.
	GROUND PADDLE	Ground Paddle. Connect the ground paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

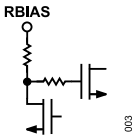


Figure 3. RBIAS Interface Schematic

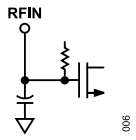


Figure 6. RFIN Interface Schematic

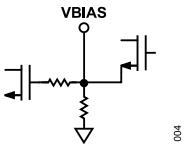


Figure 4. VBIAS Interface Schematic

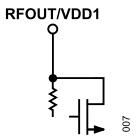


Figure 7. RFOUT/VDD1 Interface Schematic

Figure 5. GND Interface Schematic

Figure 8. VDD2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

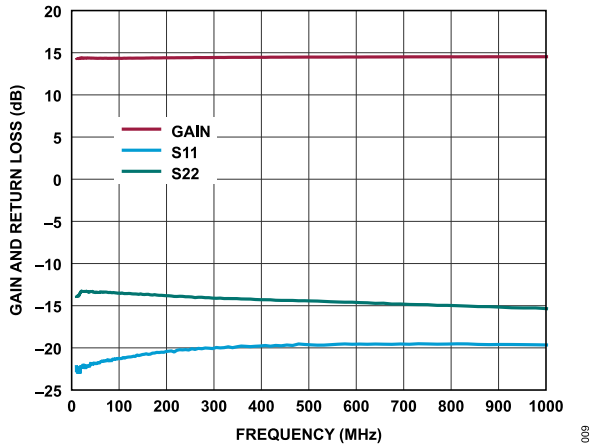


Figure 9. Gain and Return Loss vs. Frequency, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

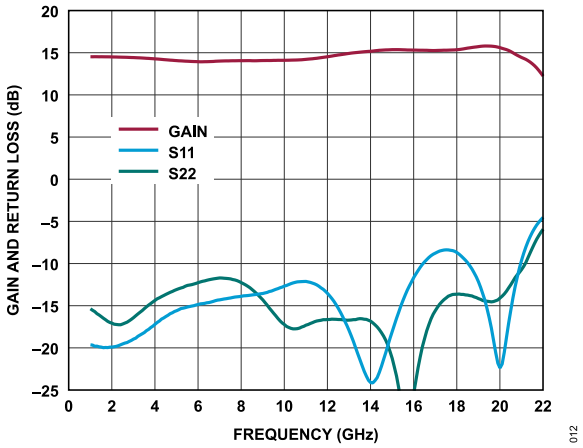


Figure 12. Gain and Return Loss vs. Frequency, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

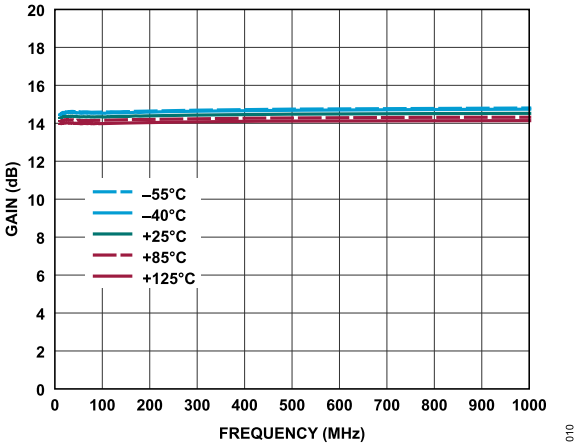


Figure 10. Gain vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

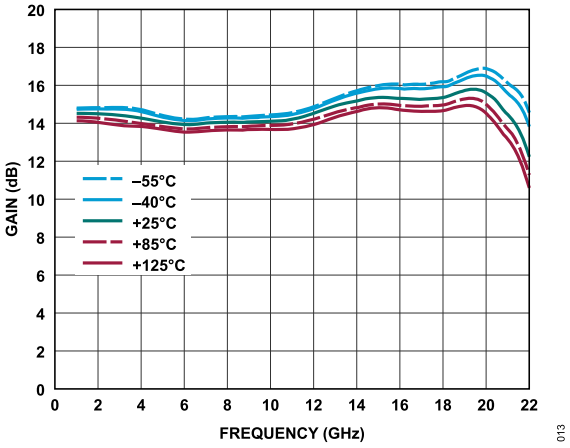


Figure 13. Gain vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

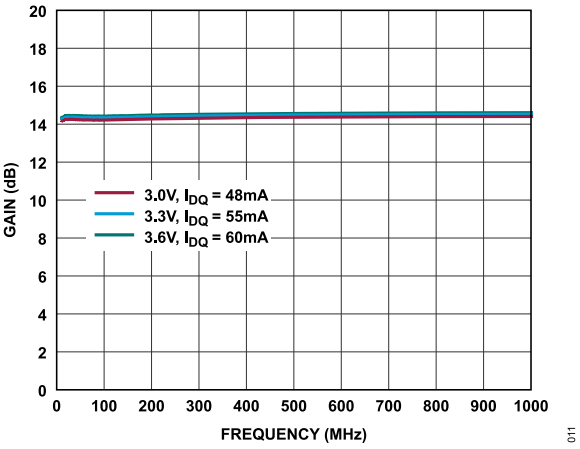


Figure 11. Gain vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

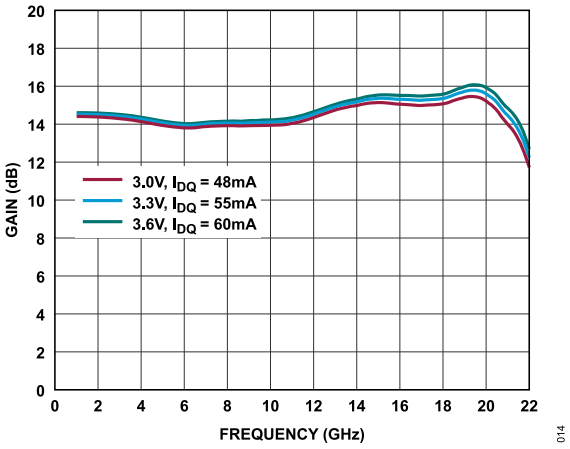


Figure 14. Gain vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

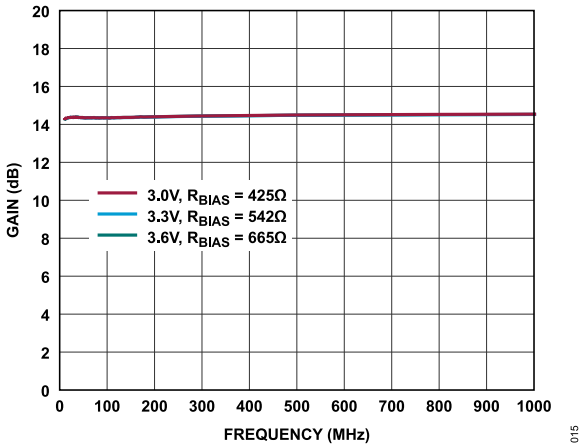


Figure 15. Gain vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

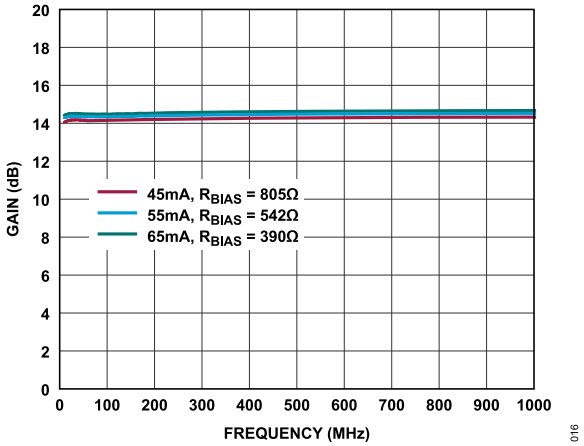


Figure 16. Gain vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

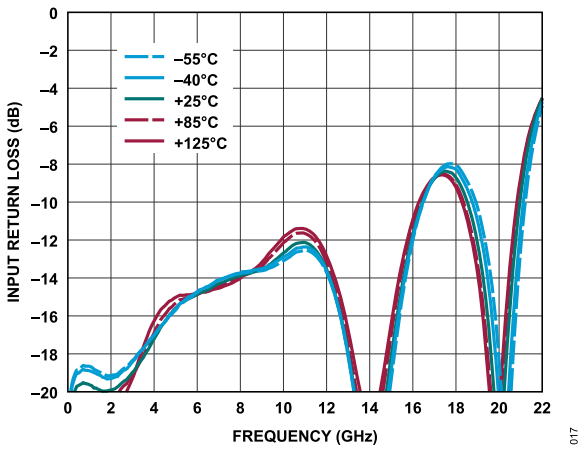


Figure 17. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

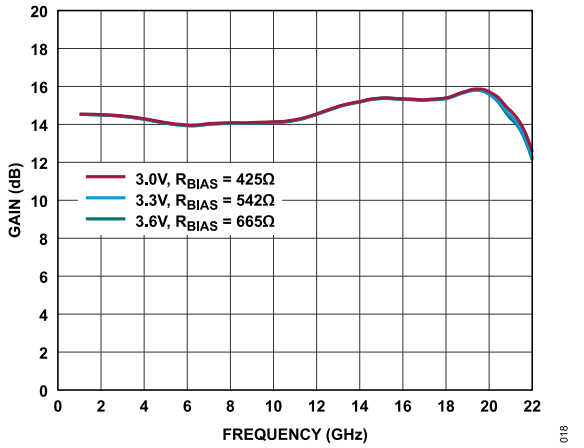


Figure 18. Gain vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

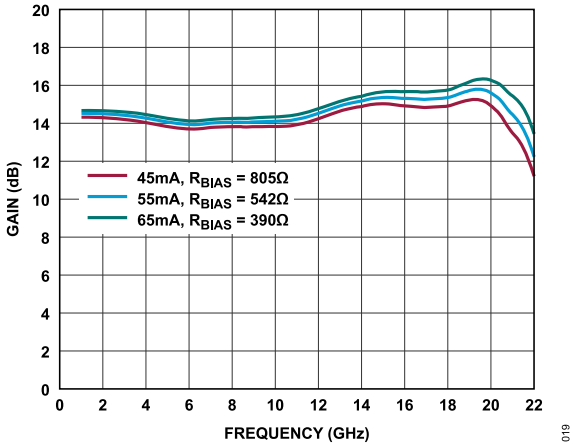


Figure 19. Gain vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

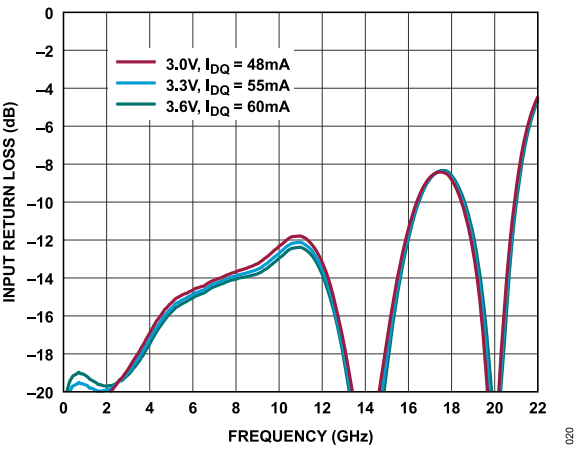


Figure 20. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 22 GHz, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

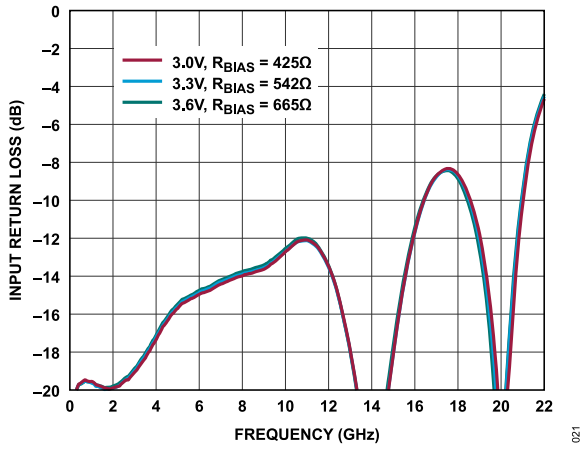


Figure 21. Input Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 22 GHz, I_{DQ} = 55 mA

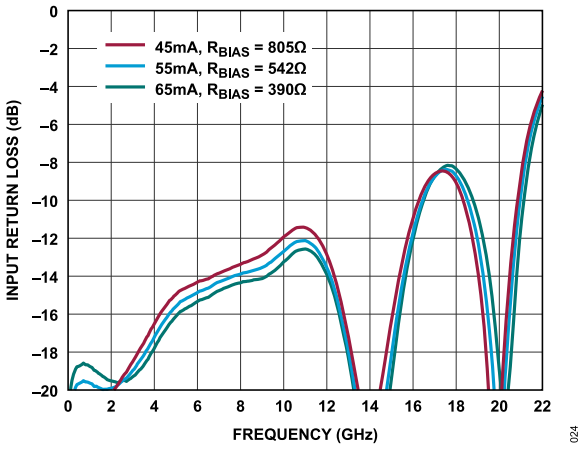


Figure 24. Input Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 22 GHz, V_{DD} = 3.3 V

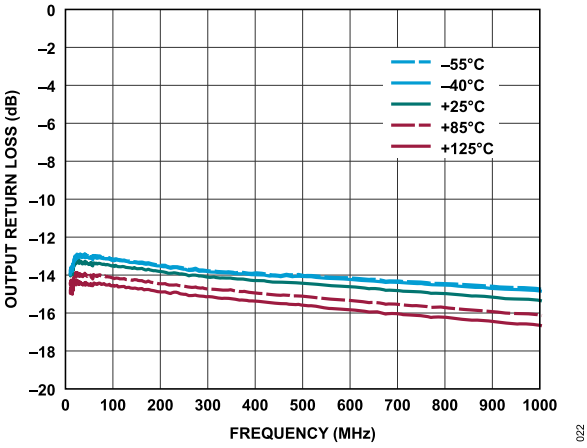


Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

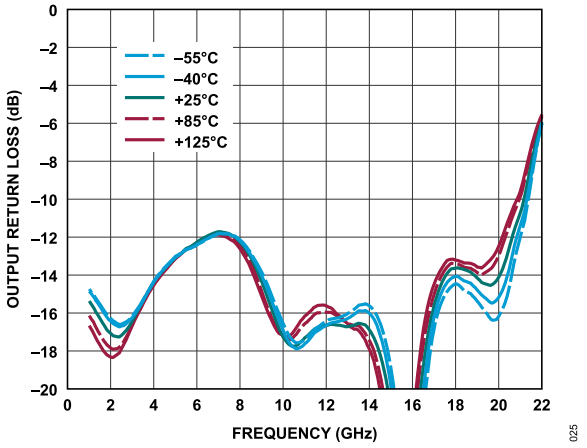


Figure 25. Output Return Loss vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

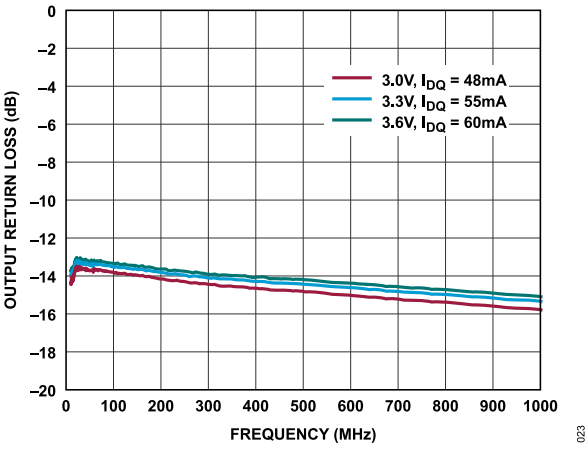


Figure 23. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

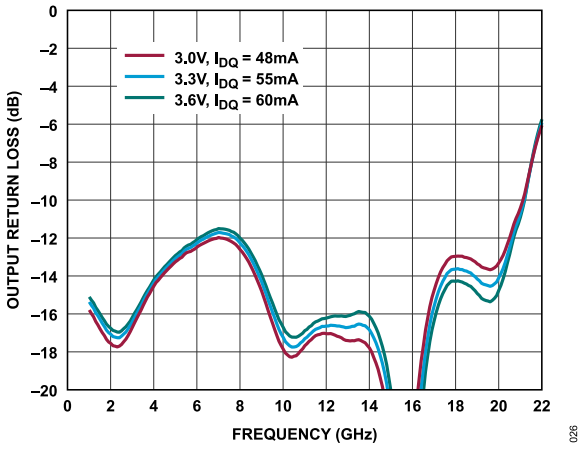


Figure 26. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

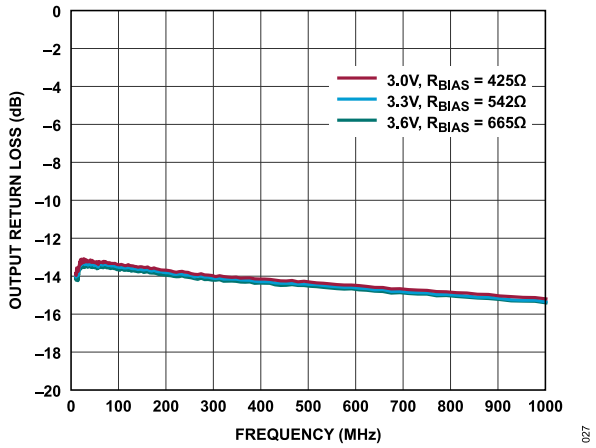


Figure 27. Output Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

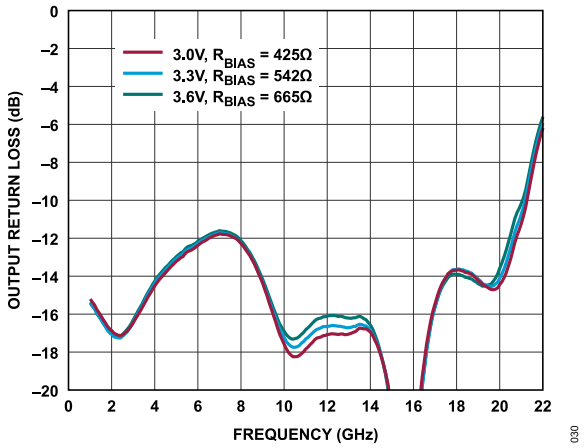


Figure 30. Output Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

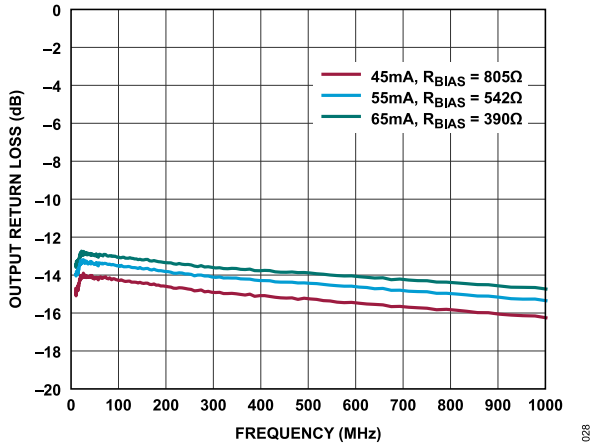


Figure 28. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

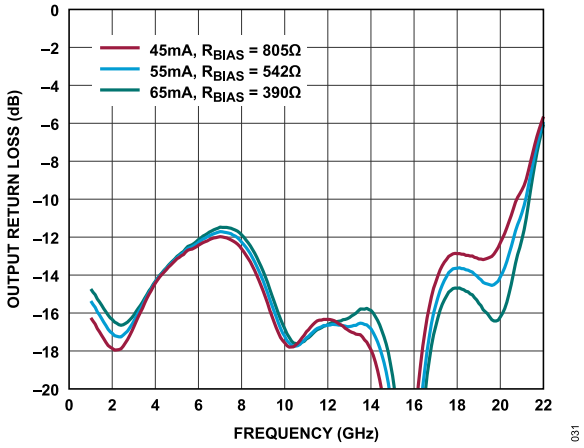


Figure 31. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

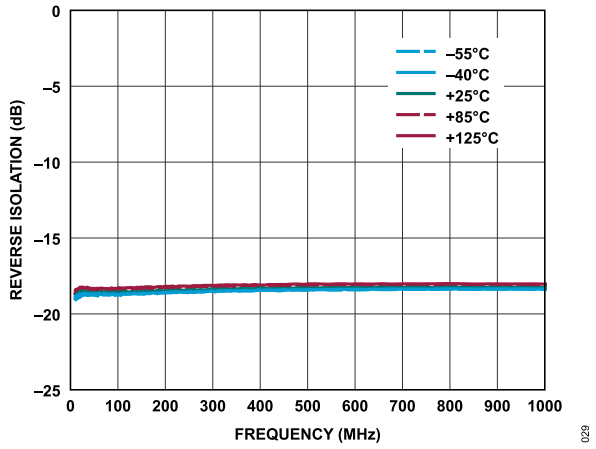


Figure 29. Reverse Isolation vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

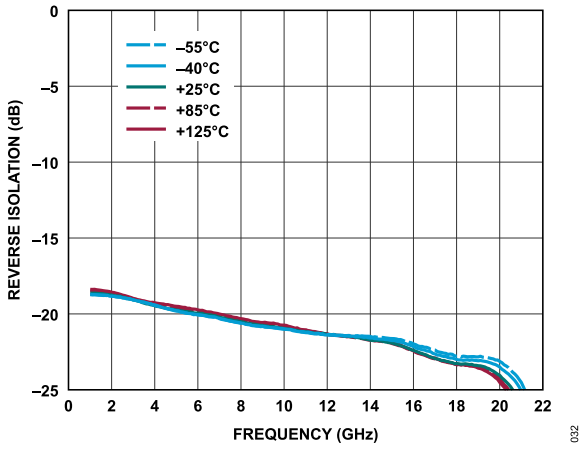


Figure 32. Reverse Isolation vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

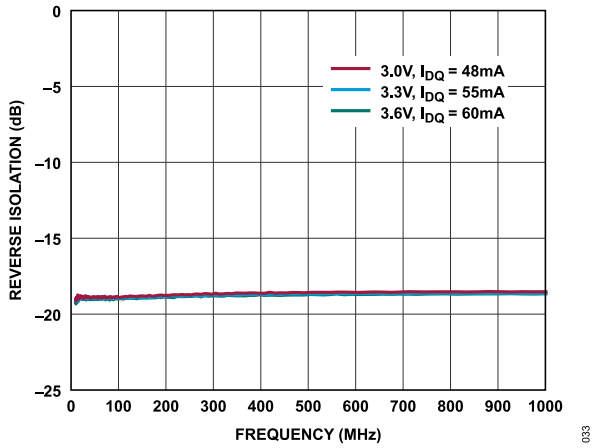


Figure 33. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

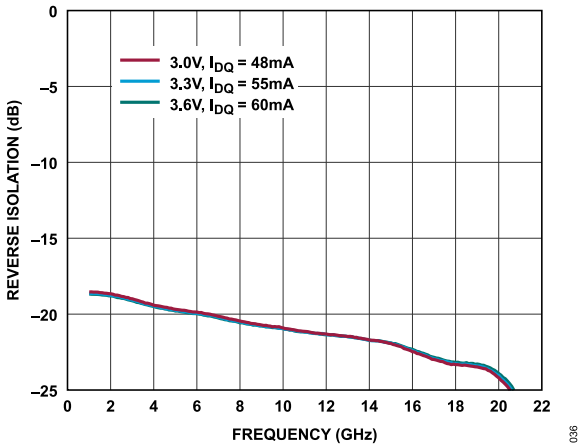


Figure 36. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

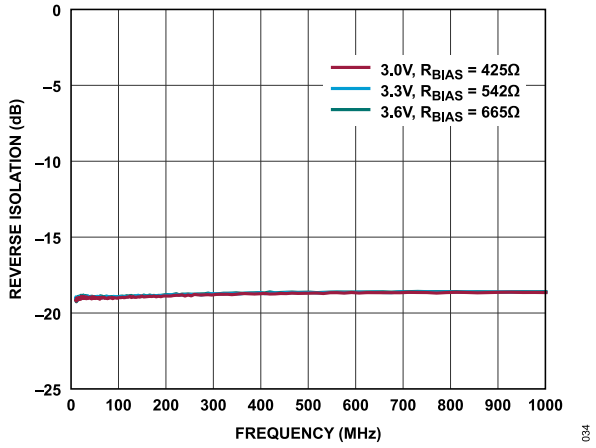


Figure 34. Reverse Isolation vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

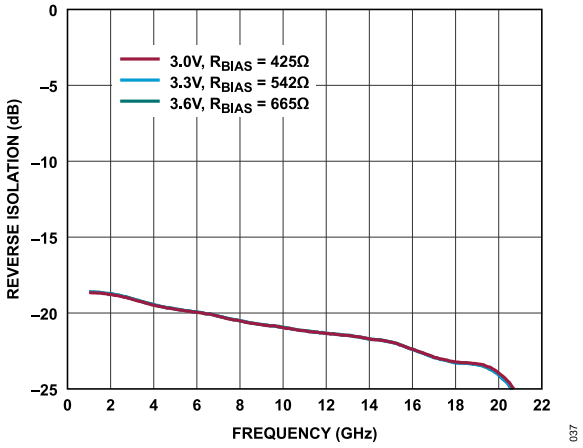


Figure 37. Reverse Isolation vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

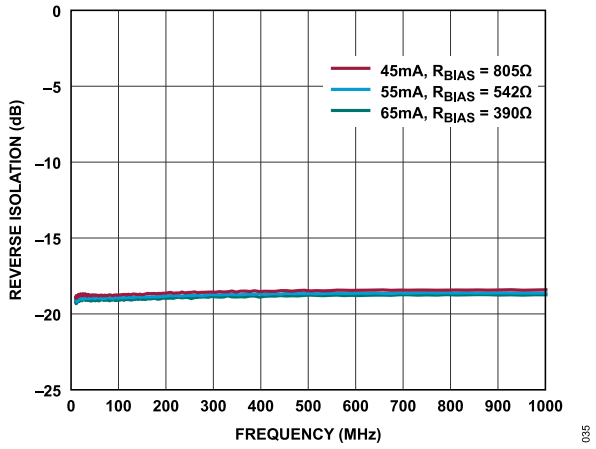


Figure 35. Reverse Isolation vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

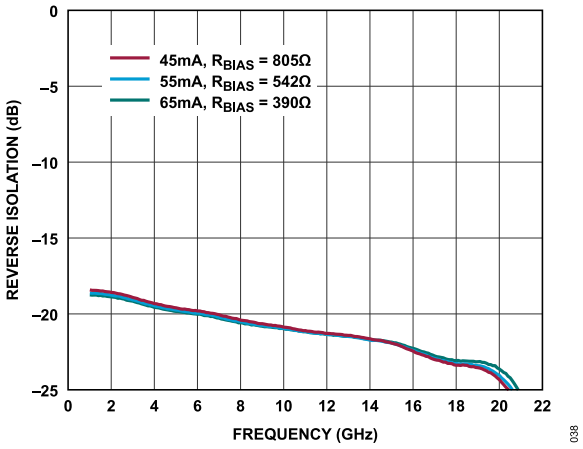


Figure 38. Reverse Isolation vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

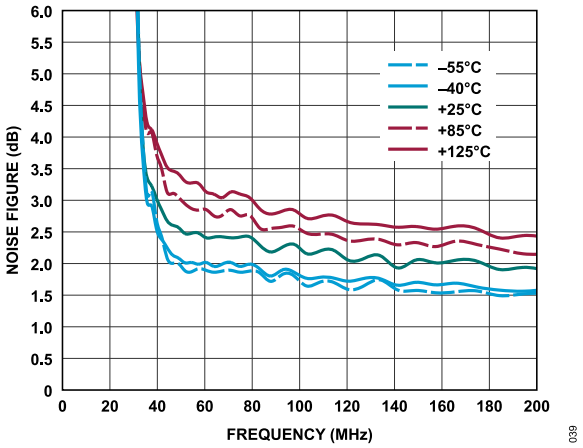


Figure 39. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

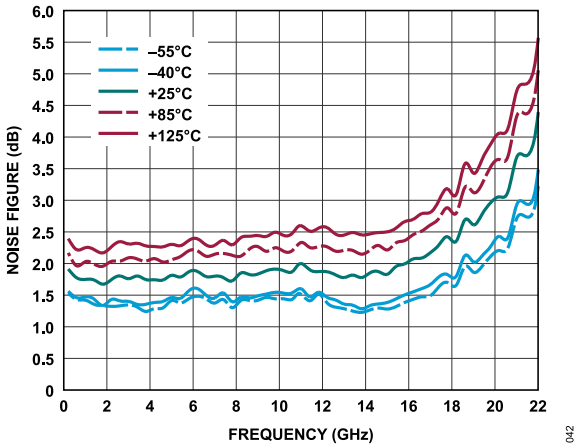


Figure 42. Noise Figure vs. Frequency for Various Temperatures, 200 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

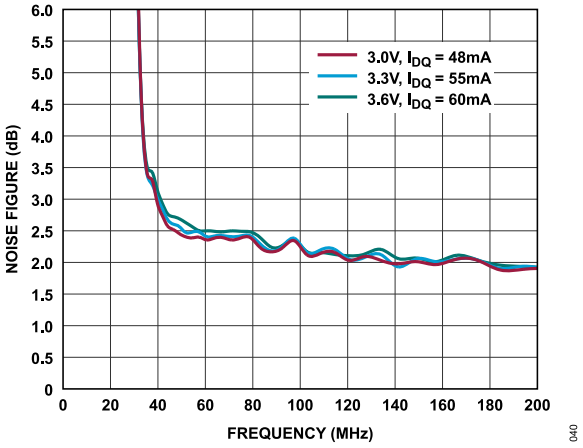


Figure 40. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 542 Ω

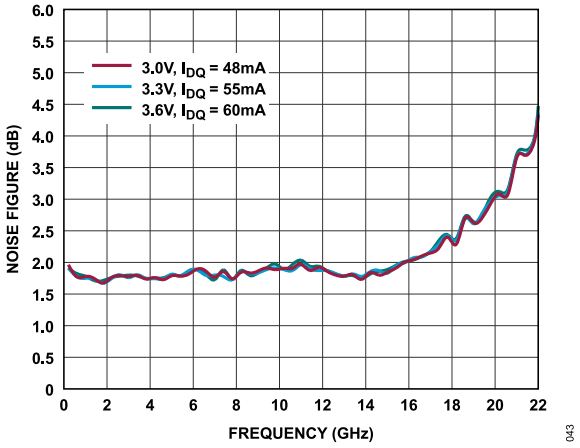


Figure 43. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 22 GHz, R_{BIAS} = 542 Ω

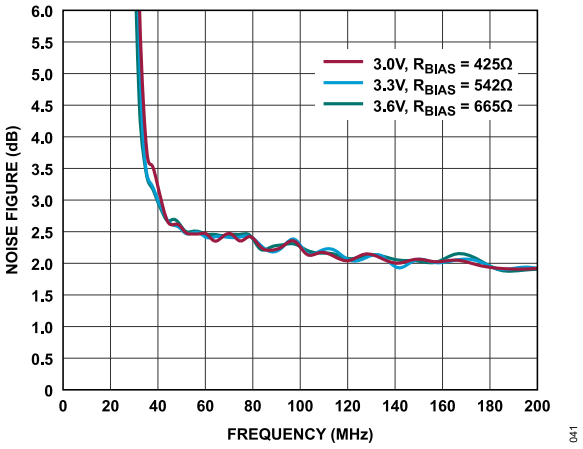


Figure 41. Noise Figure vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 200 MHz, I_{DQ} = 55 mA

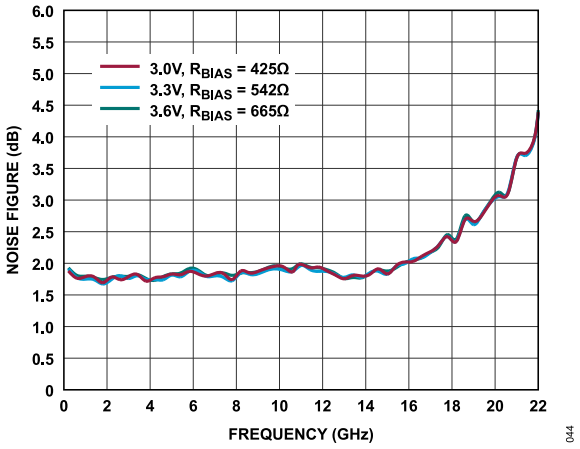


Figure 44. Noise Figure vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 200 MHz to 22 GHz, I_{DQ} = 55 mA

TYPICAL PERFORMANCE CHARACTERISTICS

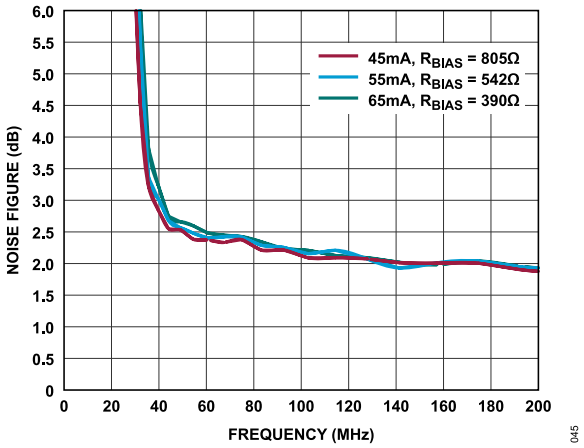


Figure 45. Noise Figure vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 200 MHz, V_{DD} = 3.3 V

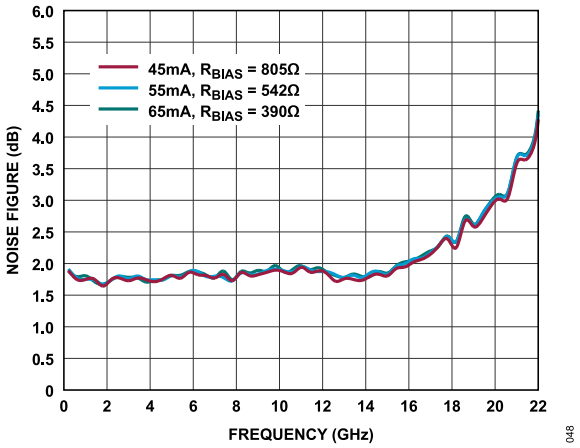


Figure 48. Noise Figure vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 200 MHz to 22 GHz, V_{DD} = 3.3 V

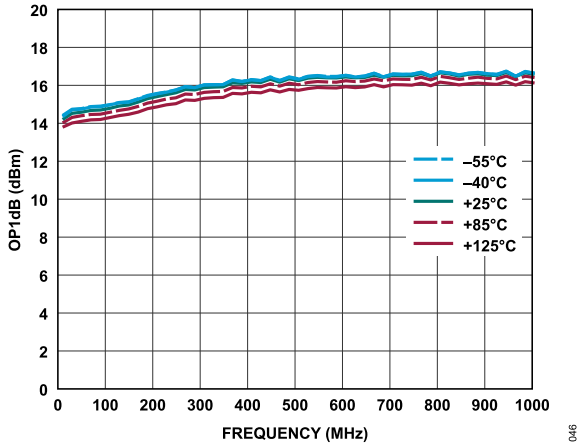


Figure 46. OP1dB vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

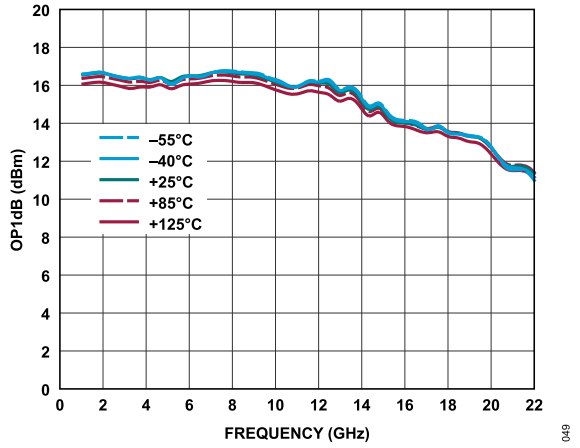


Figure 49. OP1dB vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

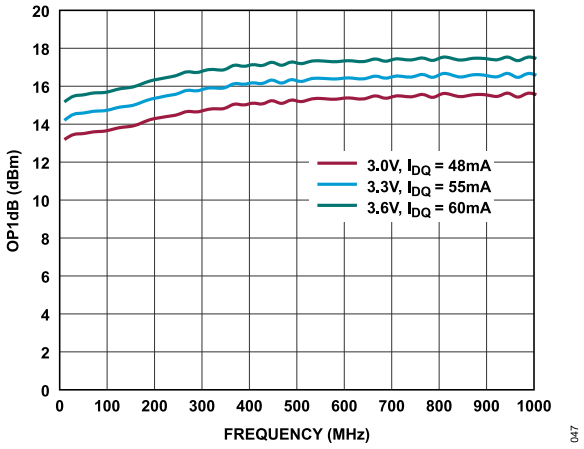


Figure 47. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

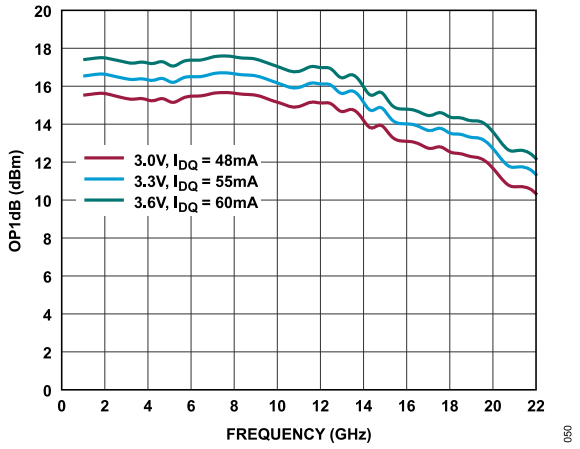


Figure 50. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

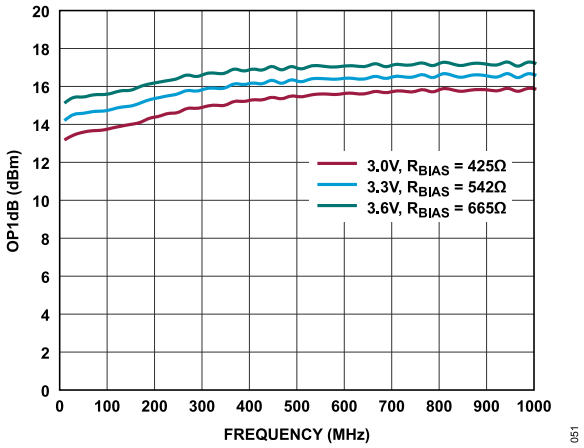


Figure 51. OP1dB vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

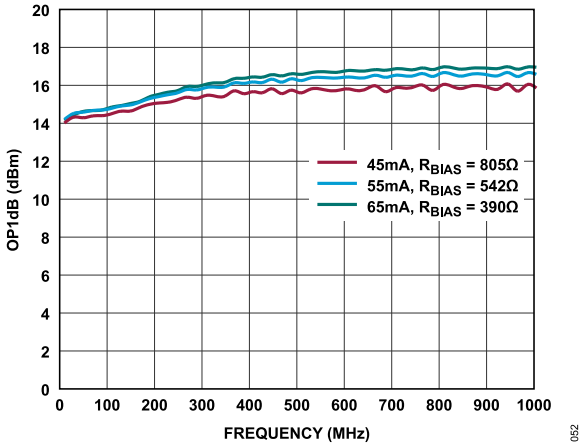


Figure 52. OP1dB vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

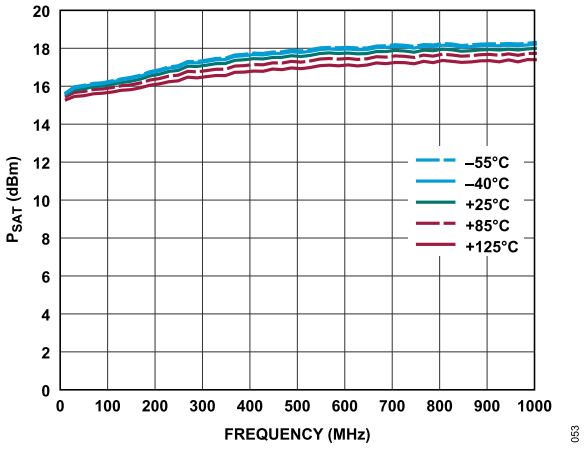


Figure 53. P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

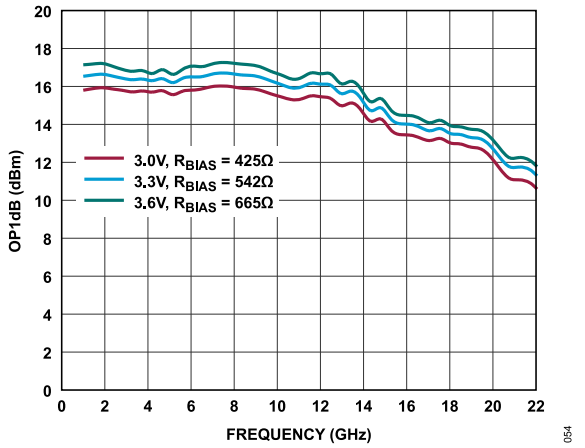


Figure 54. OP1dB vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

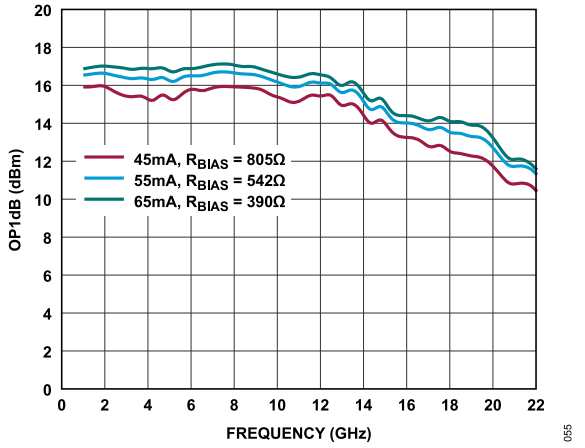


Figure 55. OP1dB vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

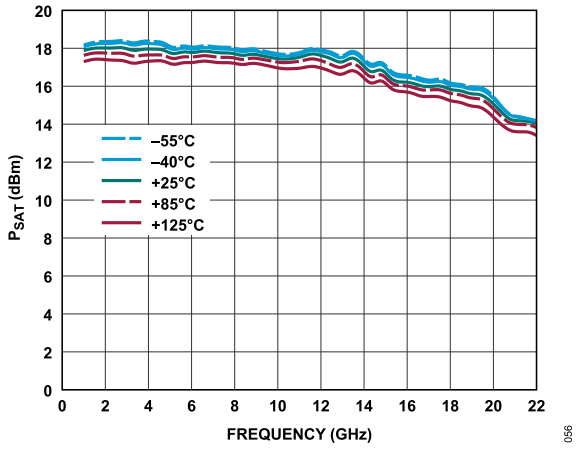


Figure 56. P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

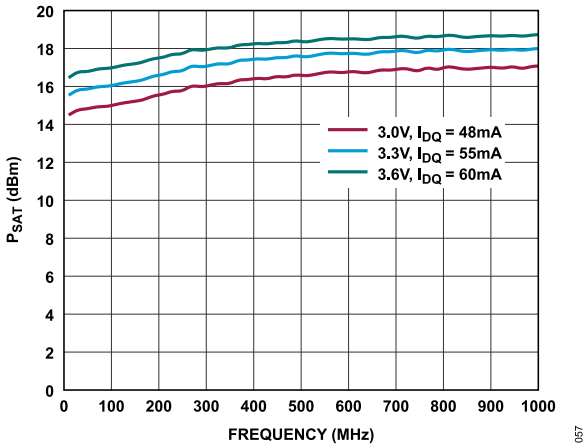


Figure 57. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

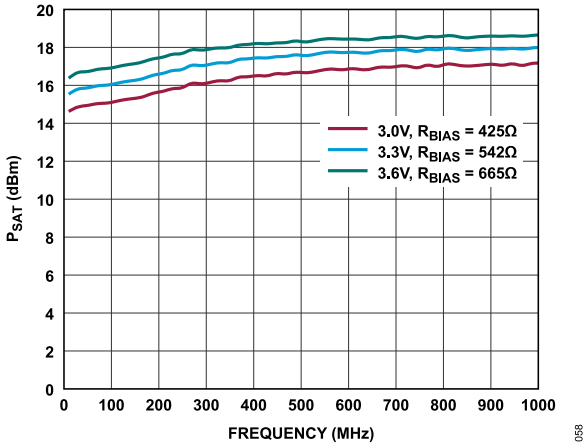


Figure 58. P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

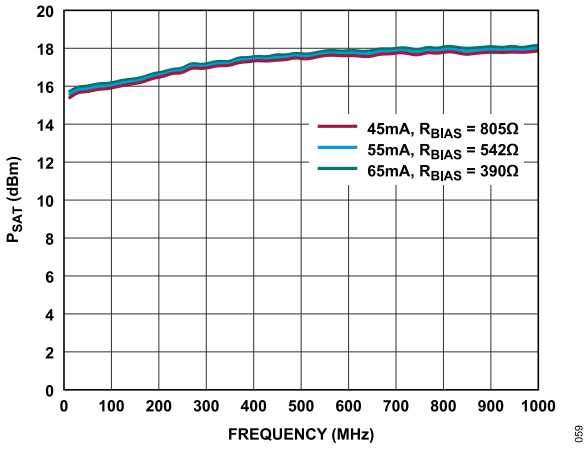


Figure 59. P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

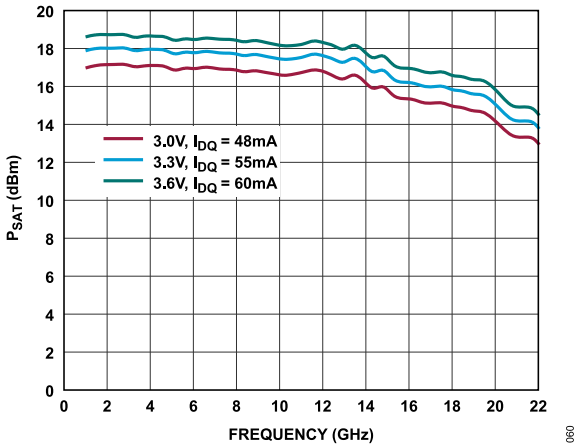


Figure 60. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

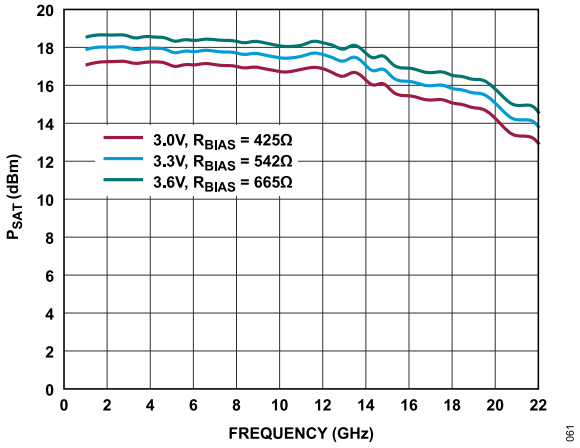


Figure 61. P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

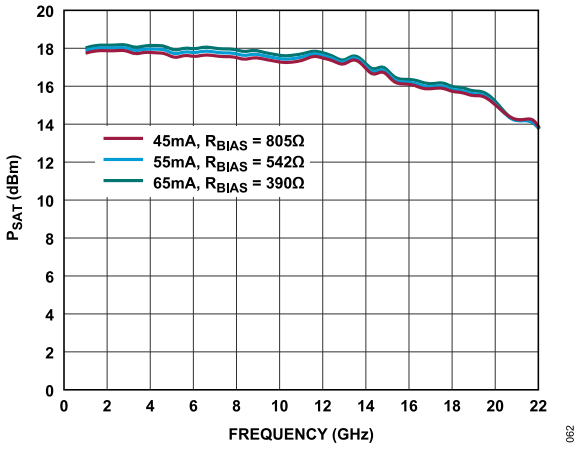


Figure 62. P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

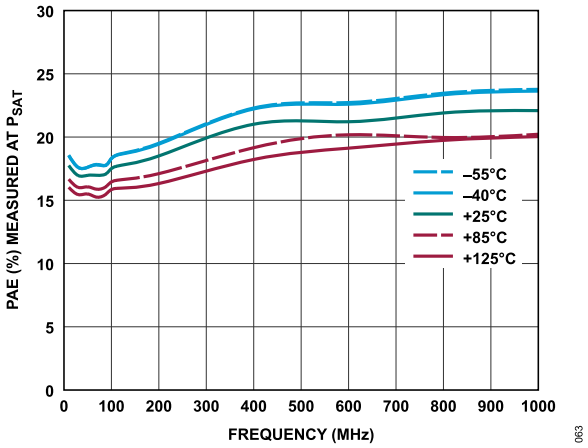


Figure 63. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

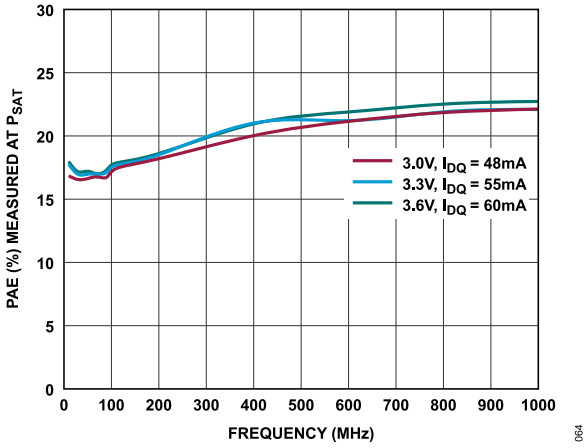


Figure 64. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

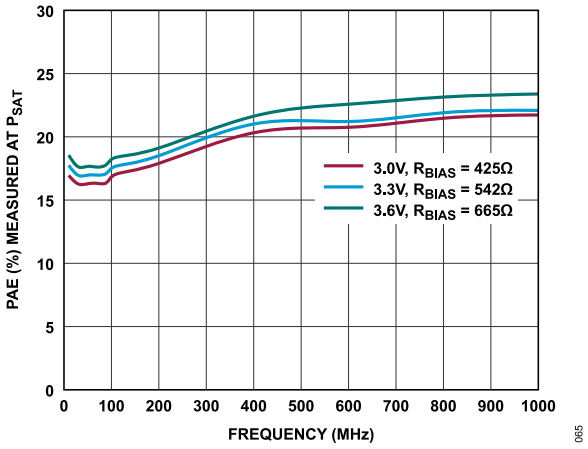


Figure 65. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

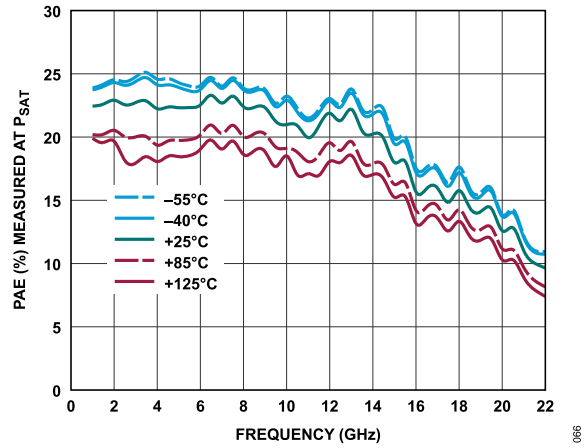


Figure 66. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

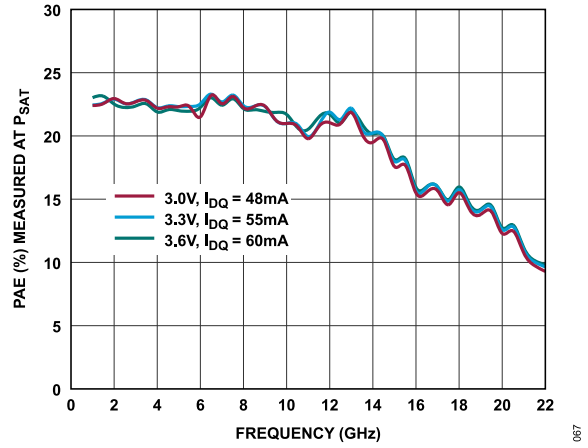


Figure 67. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

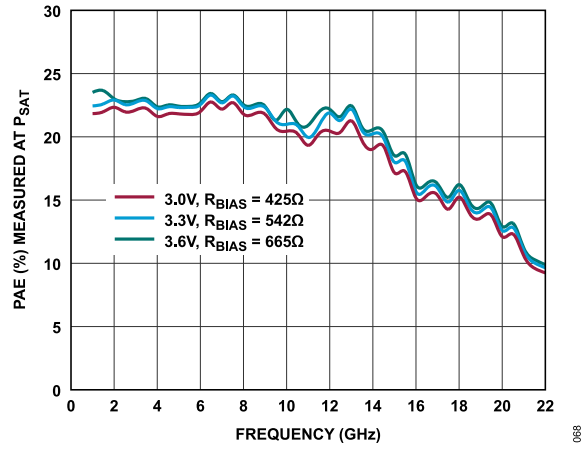


Figure 68. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

TYPICAL PERFORMANCE CHARACTERISTICS

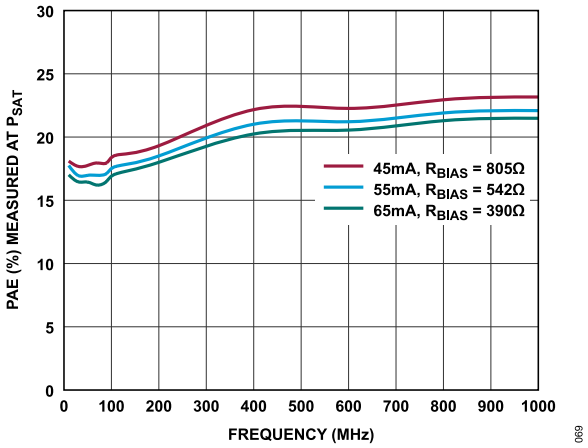


Figure 69. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

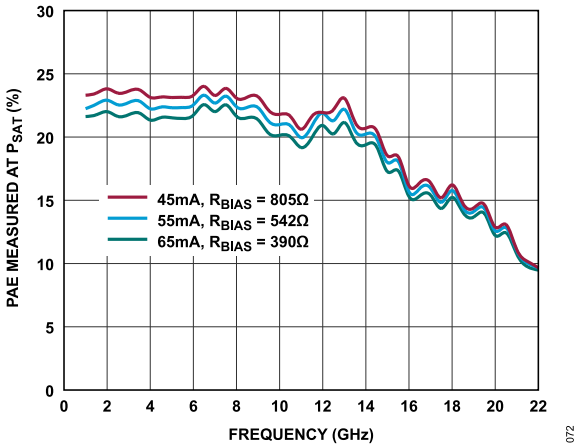


Figure 72. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

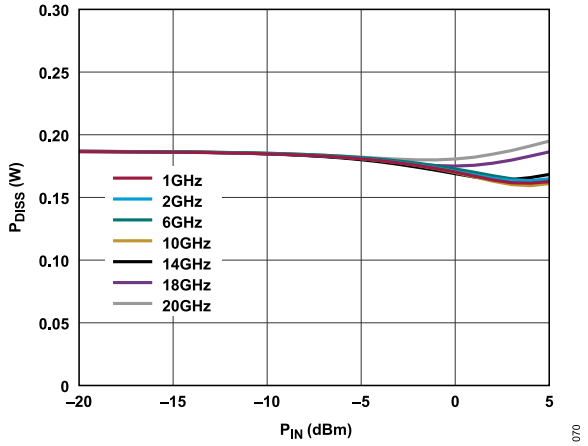


Figure 70. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, V_{DD} = 3.3 V

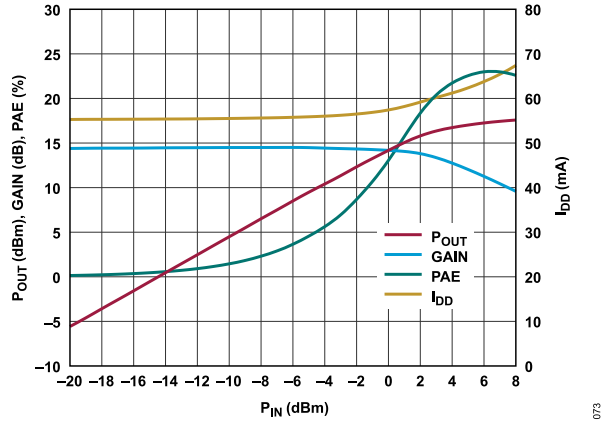


Figure 73. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 800 MHz, V_{DD} = 3.3 V, R_{BIAS} = 542 Ω

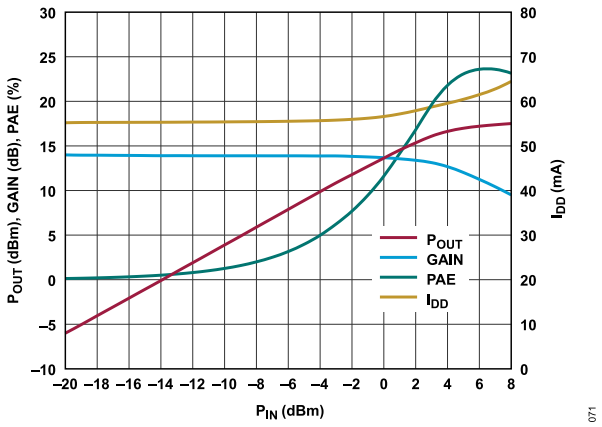


Figure 71. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. P_{IN}, Power Compression at 8 GHz, V_{DD} = 3.3 V, R_{BIAS} = 542 Ω

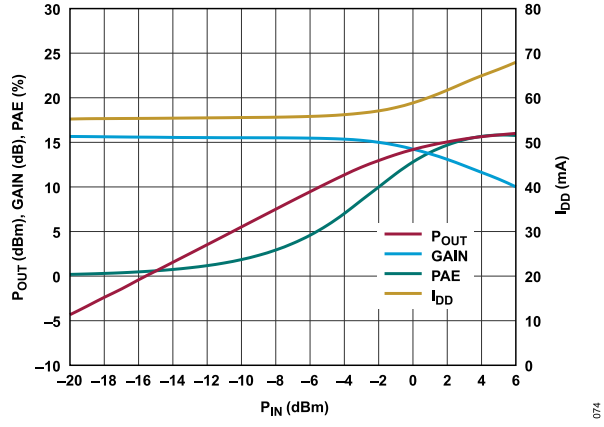


Figure 74. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 18 GHz, V_{DD} = 3.3 V, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

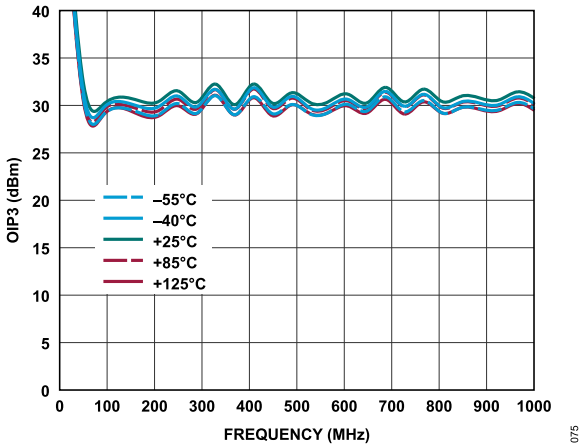


Figure 75. OIP3 vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

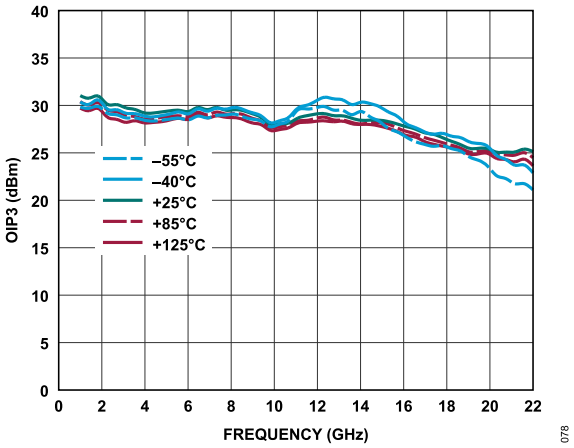


Figure 78. OIP3 vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

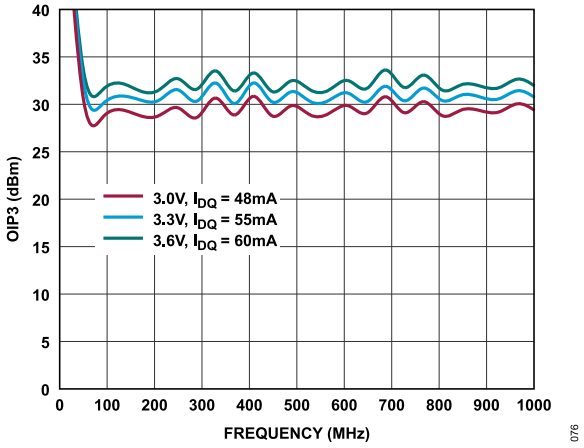


Figure 76. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

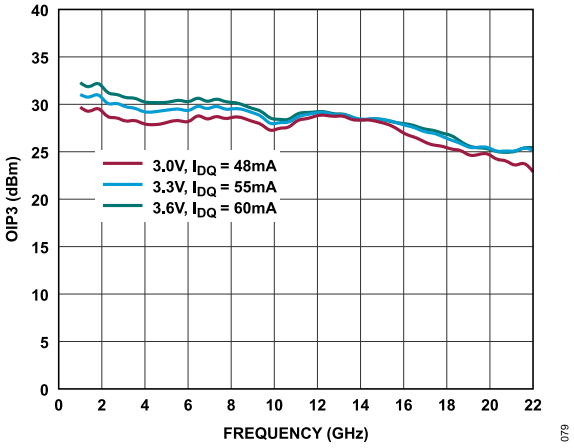


Figure 79. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

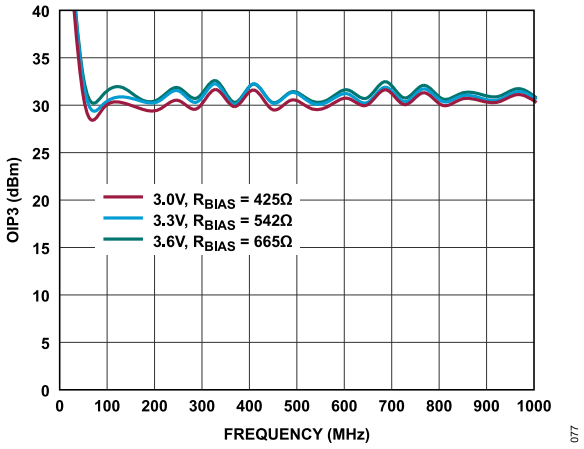


Figure 77. OIP3 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

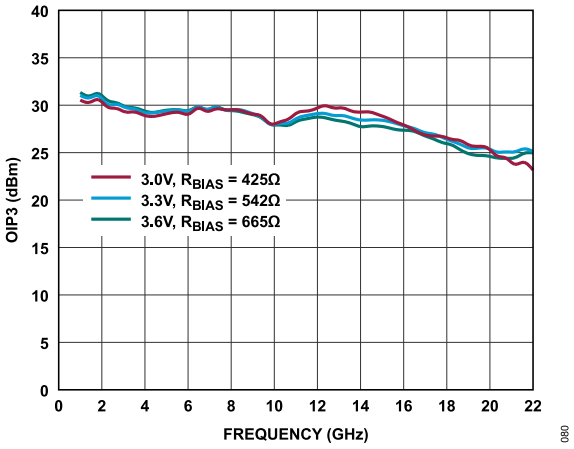


Figure 80. OIP3 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

TYPICAL PERFORMANCE CHARACTERISTICS

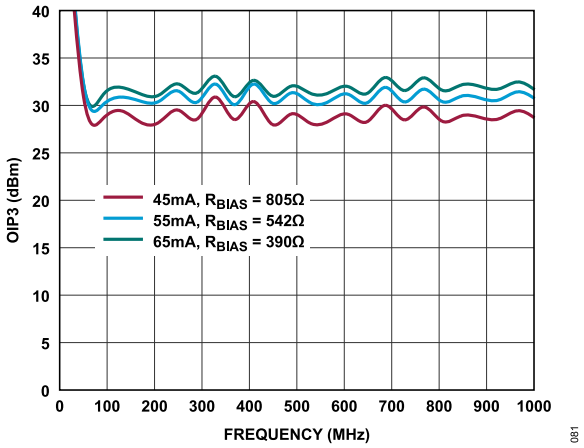


Figure 81. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

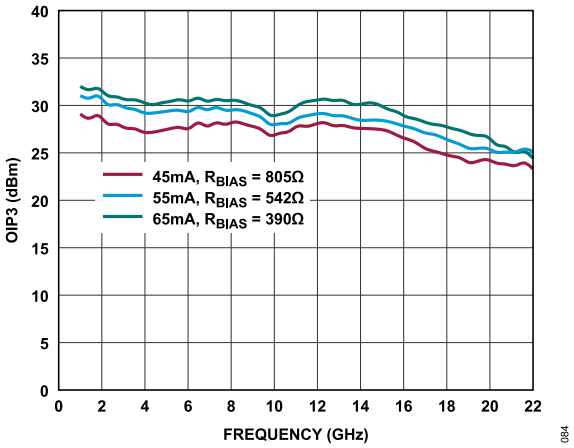


Figure 84. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

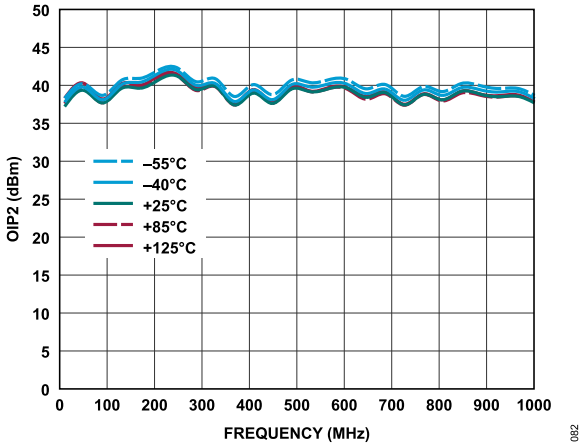


Figure 82. OIP2 vs. Frequency for Various Temperatures, 10 MHz to 1 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

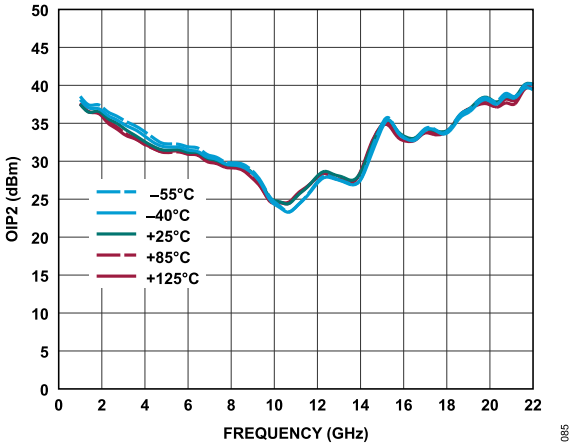


Figure 85. OIP2 vs. Frequency for Various Temperatures, 1 GHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

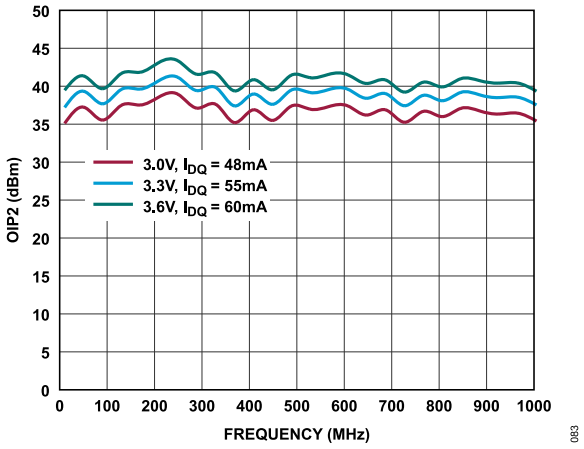


Figure 83. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1 GHz, R_{BIAS} = 542 Ω

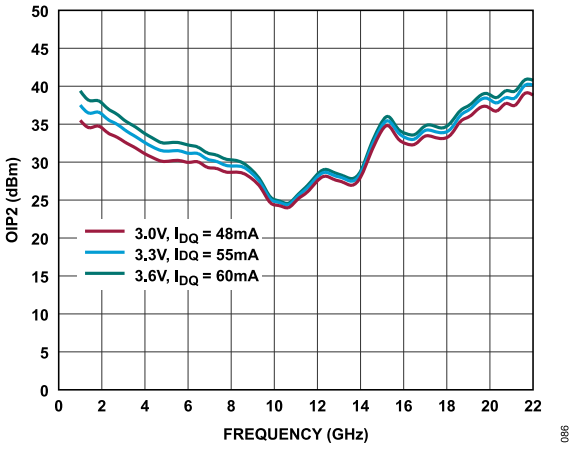


Figure 86. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 22 GHz, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

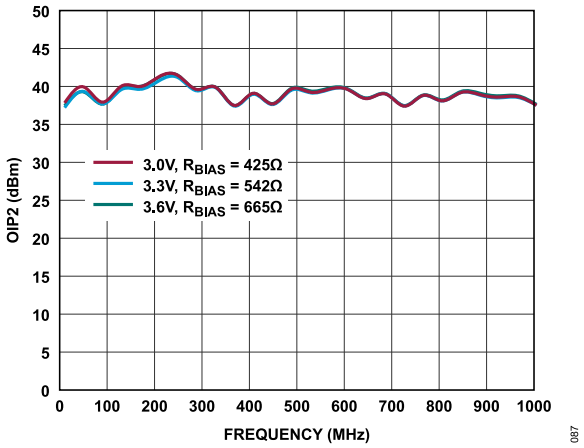


Figure 87. OIP2 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 10 MHz to 1 GHz, I_{DQ} = 55 mA

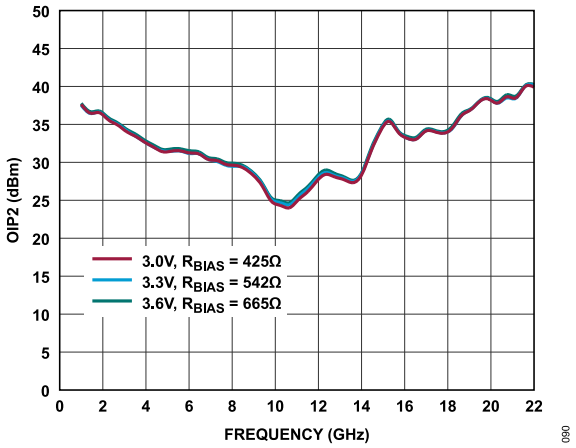


Figure 90. OIP2 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, 1 GHz to 22 GHz, I_{DQ} = 55 mA

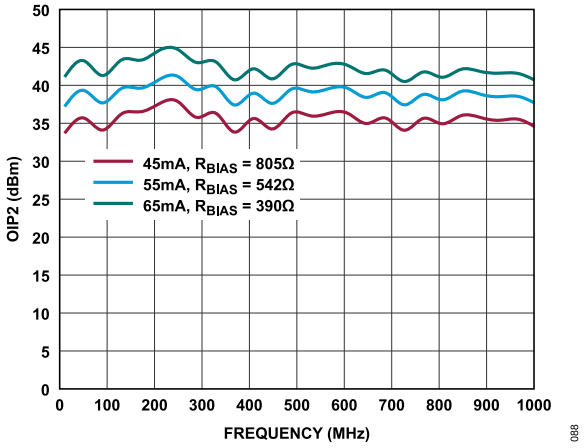


Figure 88. OIP2 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 10 MHz to 1 GHz, V_{DD} = 3.3 V

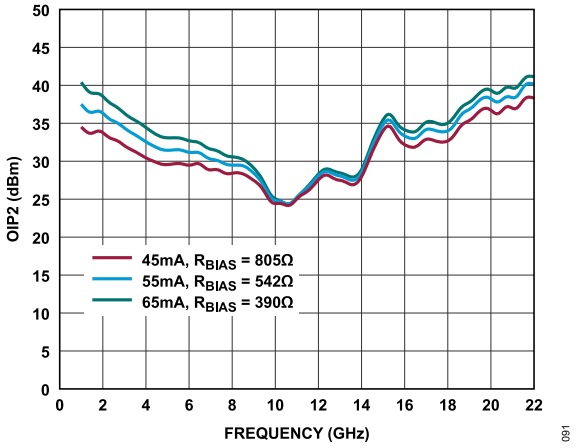


Figure 91. OIP2 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, 1 GHz to 22 GHz, V_{DD} = 3.3 V

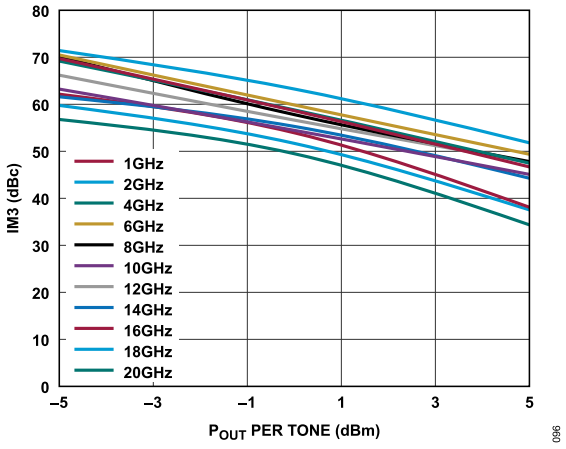


Figure 89. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.3 V, R_{BIAS} = 542 Ω

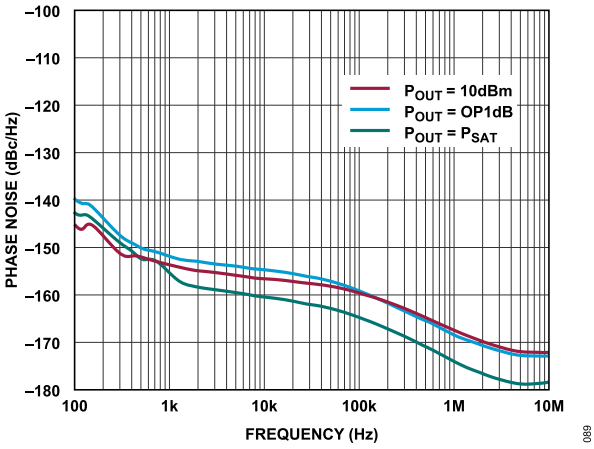


Figure 92. Phase Noise vs. Frequency at 5 GHz for Various P_{OUT} Values

TYPICAL PERFORMANCE CHARACTERISTICS

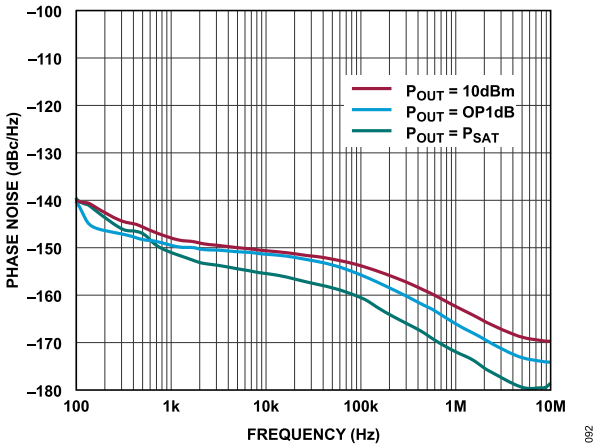


Figure 93. Phase Noise vs. Frequency at 10 GHz for Various P_{OUT} Values

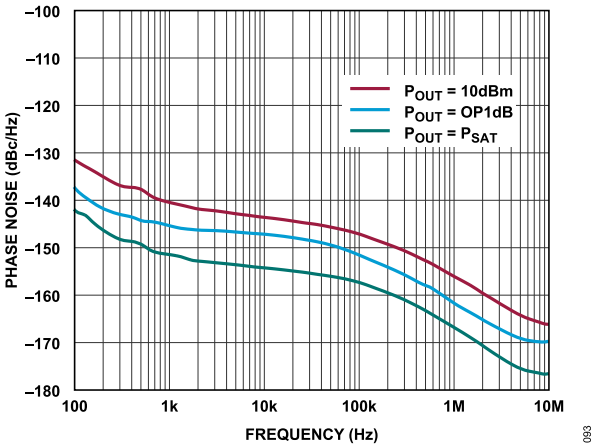


Figure 96. Phase Noise vs. Frequency at 15 GHz for Various P_{OUT} Values

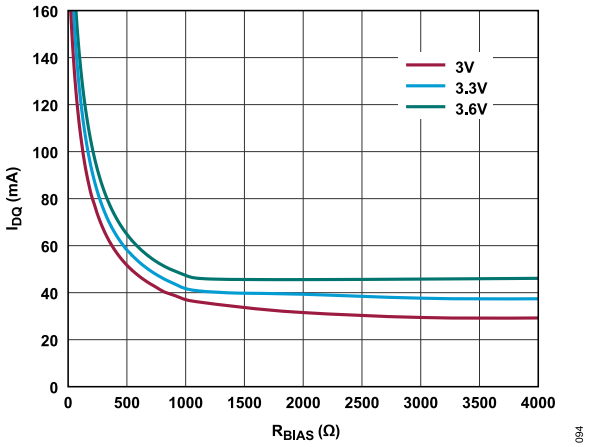


Figure 94. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 4000 Ω

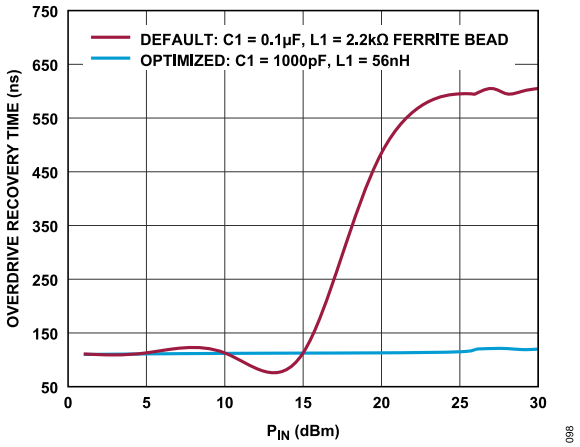


Figure 97. Overdrive Recovery Time vs. P_{IN} at 10 GHz, Recovery to Within 90% of Small Signal Gain Value, V_{DD} = 3.3 V, R_{BIAS} = 542 Ω

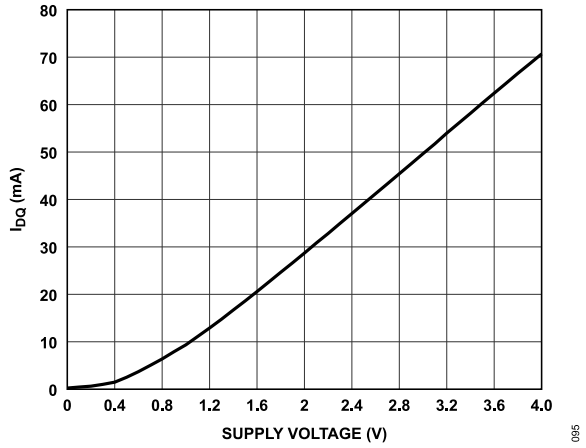


Figure 95. I_{DQ} vs. Supply Voltage, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

LOW FREQUENCY BIAS TEE

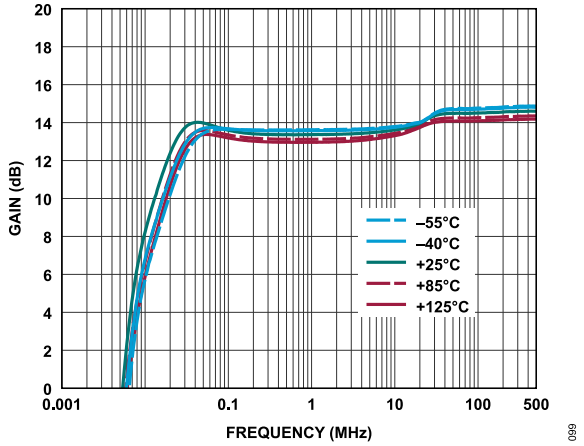


Figure 98. Gain vs. Frequency for Various Temperatures, 4 kHz to 500 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

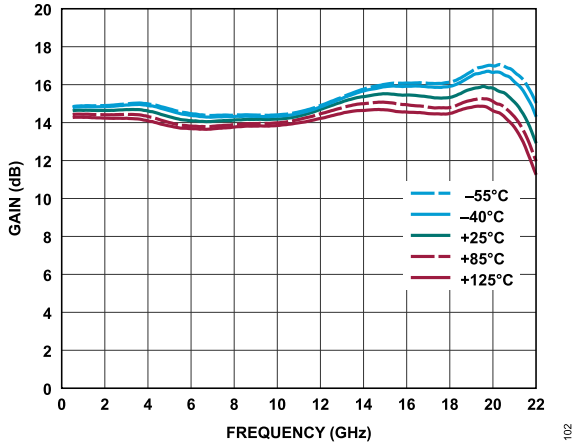


Figure 101. Gain vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

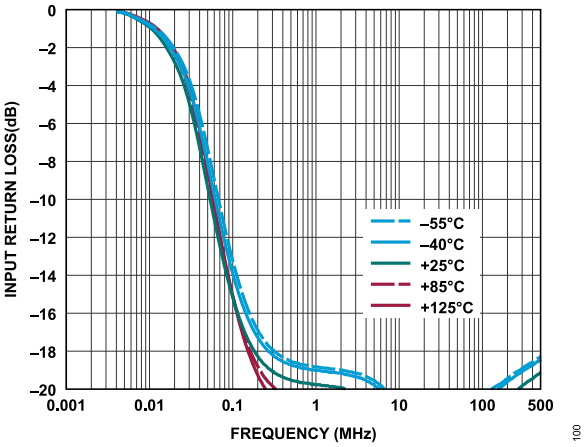


Figure 99. Input Return Loss vs. Frequency for Various Temperatures, 4 kHz to 500 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

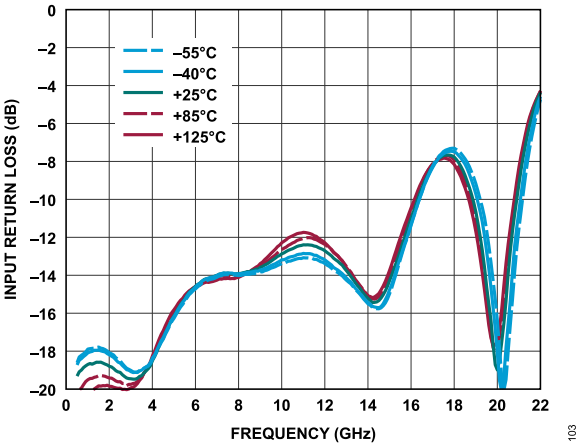


Figure 102. Input Return Loss vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

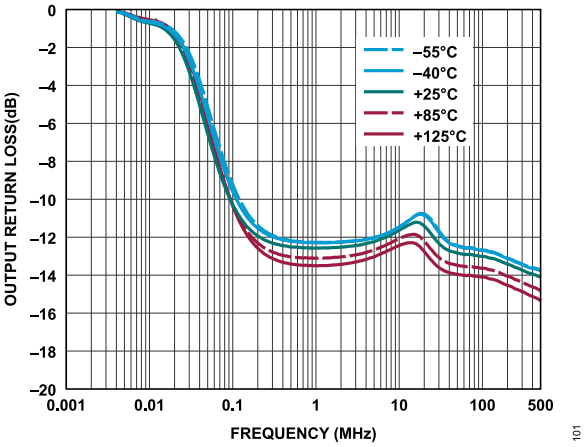


Figure 100. Output Return Loss vs. Frequency for Various Temperatures, 4 kHz to 500 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

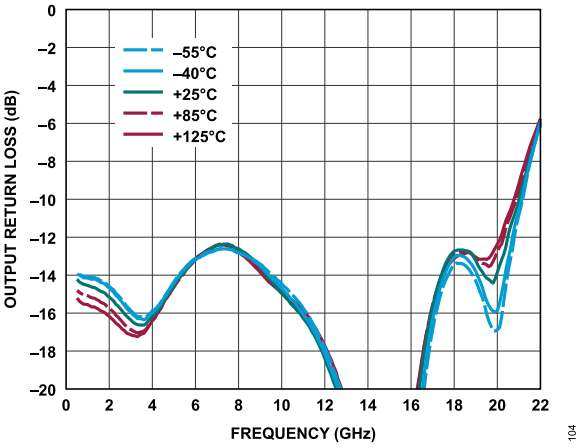


Figure 103. Output Return Loss vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

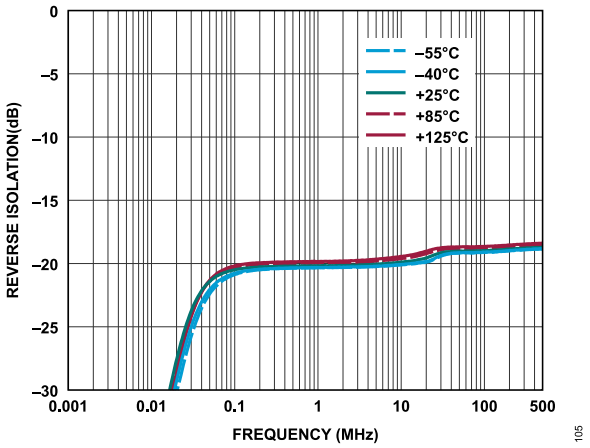


Figure 104. Reverse Isolation vs. Frequency for Various Temperatures, 4 kHz to 500 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

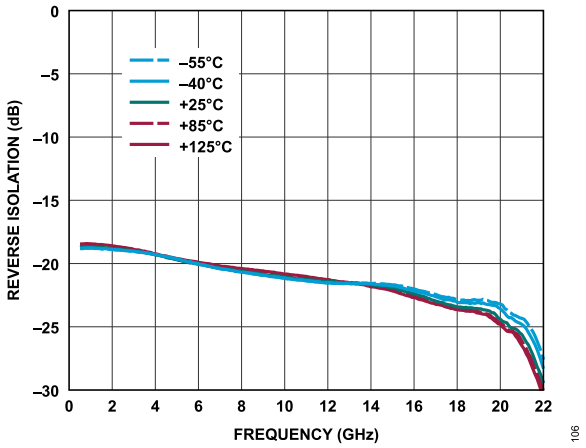


Figure 105. Reverse Isolation vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

THEORY OF OPERATION

The ADL8120 is a wideband LNA that operates from 30 kHz to 20 GHz. A simplified block diagram is shown in Figure 106.

The ADL8120 has DC-coupled, single-ended input and output ports with impedance that is nominally equal to 50 Ω over the specified frequency range. No external matching components are required; other than, AC input and output coupling capacitors and a bias inductor. To adjust I_{DQ}, connect an external resistor between the RBIAS and VDDx pins. The VBIAS output voltage provides a DC bias voltage; it connects to RFIN through a ferrite bead. The RFOUT/VDD1 pin provides the drain current. Additional drain biasing is applied through the VDD2 pin.

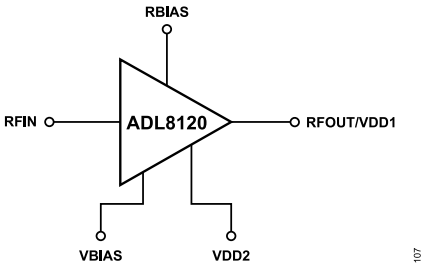


Figure 106. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8120 from 10 MHz to 20 GHz are shown in Figure 109. AC-couple the input and output of the ADL8120 with appropriately sized capacitors (such as American Technical Ceramics Part Number 560L104YTRN). Connect a ferrite bead between the VBIAS pin and RFIN to provide a DC bias voltage to the RF input. A 3.3 V DC bias is provided to the amplifier using two ferrite beads connected to the RFOUT/VDD1 pin. The recommended bias inductor is a TDK MMZ1005A222ET000 2.2 kΩ at 100 MHz.

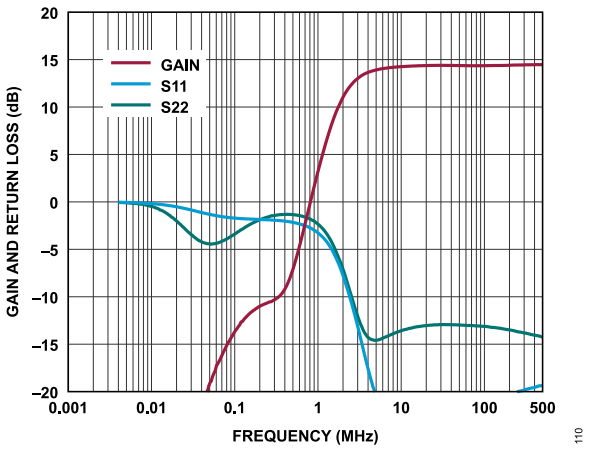


Figure 107. Gain and Return Loss vs. Frequency of 10 MHz to 20 GHz Application Circuit, 4 kHz to 500 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

The 3.3 V DC bias voltage must also be connected to the VDD2 pin. The bias conditions, V_{DD} = 3.3 V and I_{DQ} = 55 mA, are the recommended operating point to achieve specified performance. The gain and return loss of this circuit are shown in Figure 107 and Figure 108 across frequencies. To set other bias conditions, adjust the R_{BIAS} value. Table 8 shows the recommended R_{BIAS} values and their associated I_{DQ} values.

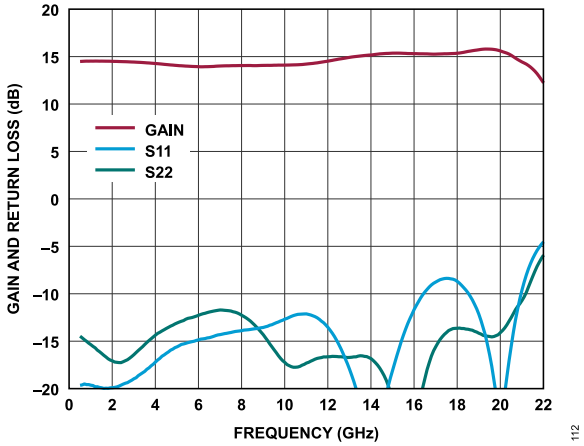


Figure 108. Gain and Return Loss vs. Frequency of 10 MHz to 20 GHz Application Circuit, 500 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

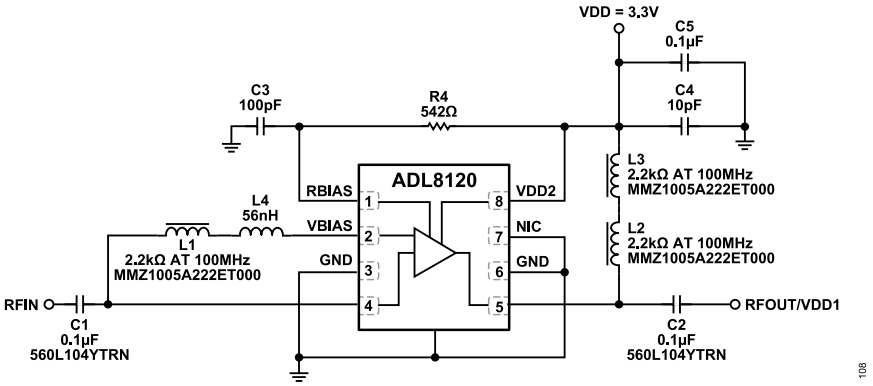


Figure 109. Typical Application Circuit for Operation from 10 MHz to 20 GHz

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

The correct sequencing of the DC and RF power is required to safely operate the ADL8120. During power-up, apply V_{DD} before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before V_{DD} is powered off.

For more information on using the evaluation board, refer to the EVAL-ADL8120 user guide.

Table 8. Recommended Bias Resistor Values for V_{DD} = 3.3 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
805	45	42.2	2.8
542	55	51	4
390	65	59.9	5.1

APPLICATIONS INFORMATION

LOW FREQUENCY OPERATION

Figure 112 shows the application circuit that was used to extend operation down to 30 kHz. Note that additional components, R2 and R3 = 300 Ω, L5 and L6 = 680 µH, C5 = 1 µF, and L4 = 2.2 kΩ at 100 MHz, have been added to support low frequency operation. The gain and the return loss of this circuit are shown in Figure 110 and Figure 111.

Further adjustments can be made to the external components of the device to operate at even lower frequencies. Specifically, the bias tee and DC blocking capacitors can be modified because these components are the limiting factor causing the low frequency cutoff. These external components can be interchanged to support low frequency operation.

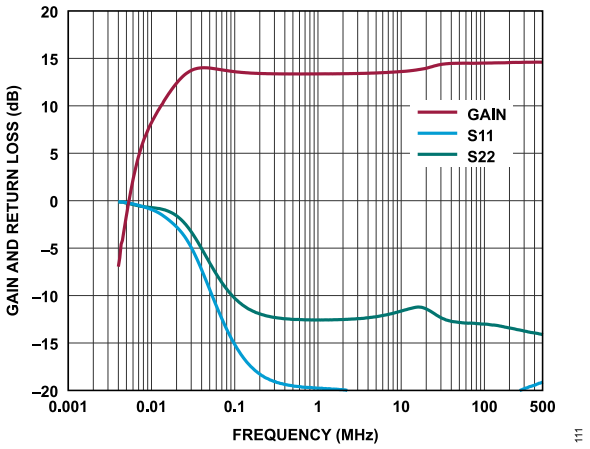


Figure 110. Gain and Return Loss vs. Frequency of 30 kHz to 20 GHz Application Circuit, 4 kHz to 500 MHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

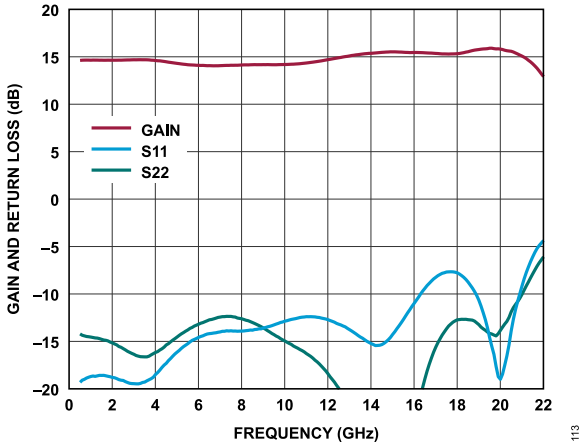


Figure 111. Gain and Return Loss vs. Frequency of 30 kHz to 20 GHz Application Circuit, 500 MHz to 22 GHz, V_{DD} = 3.3 V, I_{DQ} = 55 mA, R_{BIAS} = 542 Ω

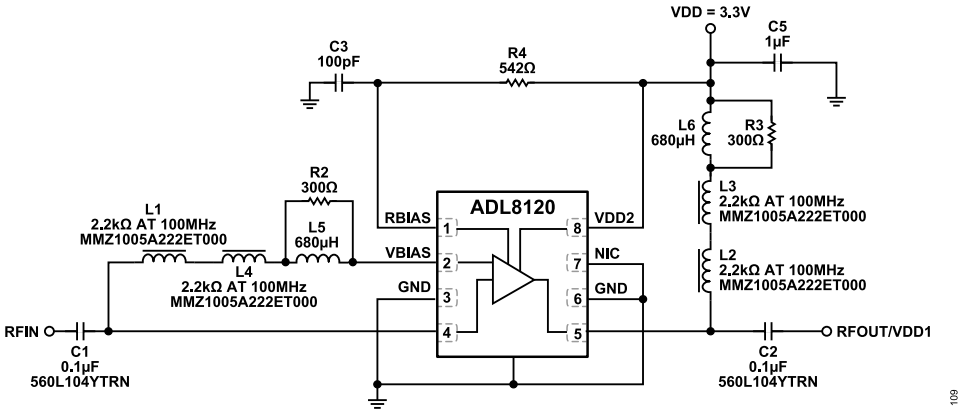


Figure 112. Typical Application Circuit for Operation from 30 kHz to 20 GHz

APPLICATIONS INFORMATION

OVERDRIVE RECOVERY OPTIMIZATION

The overdrive recovery performance of the 10 MHz to 20 GHz circuit (see Figure 109) can be improved by adjusting the C1 and L1 values shown in Figure 114. Figure 97 is the overdrive recovery time performance comparison of the baseline ADL8120-EVALZ configuration vs. the optimized ADL8120-EVALZ. The input DC blocking capacitors are the major component for slowing down the recovery time. C1 = 1000 pF along with L1 = 56 nH were the values selected that had the least affect on the recovery time performance. Figure 113 shows the gain and return loss of the modified optimized application circuit.

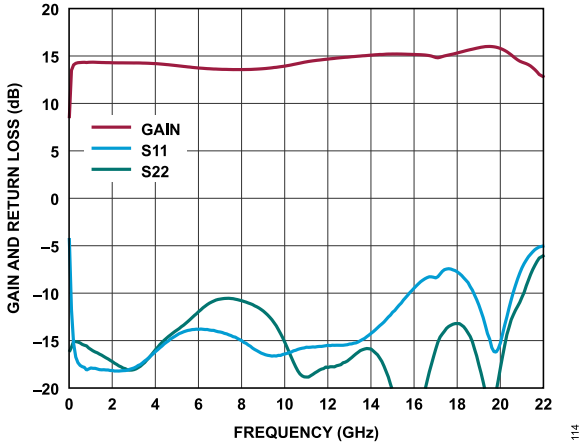


Figure 113. Gain and Return Loss vs. Frequency for ADL8120-EVALZ Overdrive Recovery Time Optimized Circuit, 10 MHz to 22 GHz, V_{DD} = 3.3 V, R_{BIAS} = 542 Ω

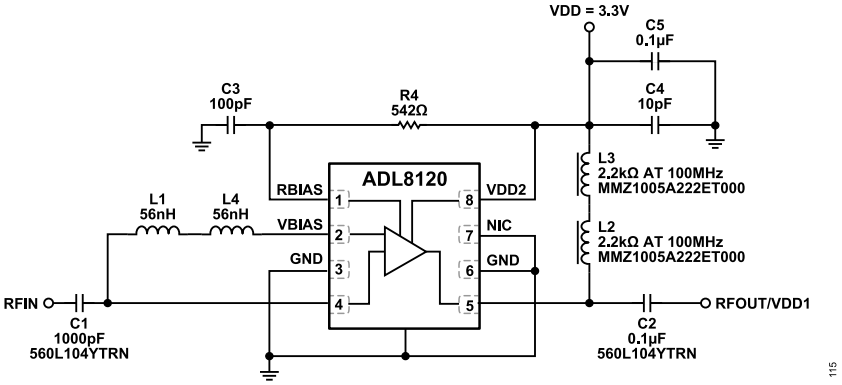


Figure 114. Application Circuit for ADL8120-EVALZ Optimized Overdrive Recovery Time

APPLICATIONS INFORMATION

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 115 shows a recommended power management circuit for the ADL8120. The LT8607 step-down regulator is used to step down a 12 V rail to 4.5 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 3.3 V output. Even though the circuit shown in Figure 115 has an input voltage (VIN) of 12 V, the input range to the LT8607 can be as high as 42 V.

The 4.5 V regulator output of the LT8607 is set by the R2 and R3 resistors, according to the following equation:

$R2 = R3((VOUT/0.778\ V) - 1)$, where VOUT is the output voltage.

The switching frequency (f_{SW}) is set to 2 MHz by the 18.2 kΩ resistor (R1) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.200 MHz.

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$VOUT = 100\ \mu A \times R4$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 3.3 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%). Therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 3.3 V output to give a convenient 0 V to 3.6 V voltage range. Table 9 provides the recommended resistor values for operation at 3.6 V to 3 V.

Table 9. Recommended Resistor Values for Operating at 3.6 V to 3 V

LDO VOUT (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
3.6	36.5	332	30.1
3.3	33.1	301	30.1
3	30.1	267	30.1

The LT8607 can source a maximum current of 750 mA, and the LT3042 can source a maximum current of 200 mA. If the 5 V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5 A and 3 A, respectively, and these devices are pin compatible with the LT8607. The LT3045 linear regulator, which is pin compatible with LT3042, can source a maximum current to 500 mA.

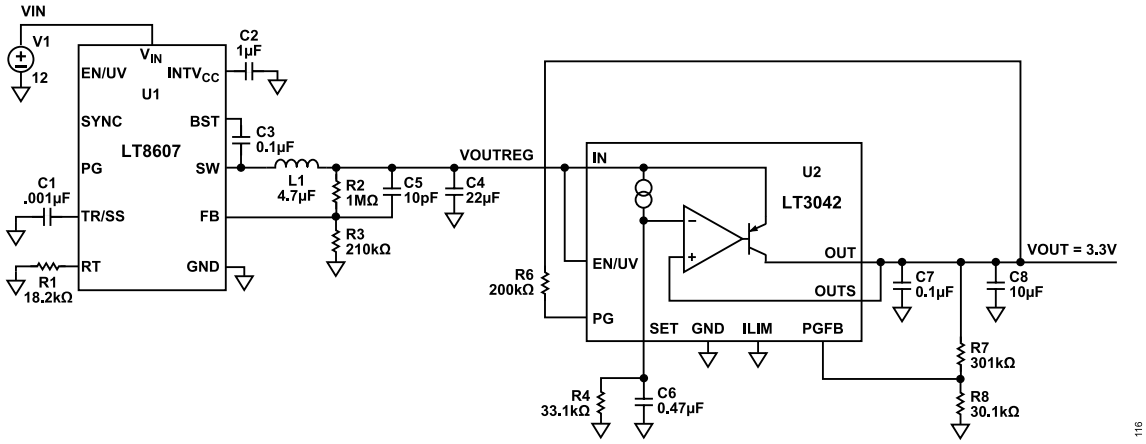


Figure 115. Recommended Power Management Circuit

OUTLINE DIMENSIONS

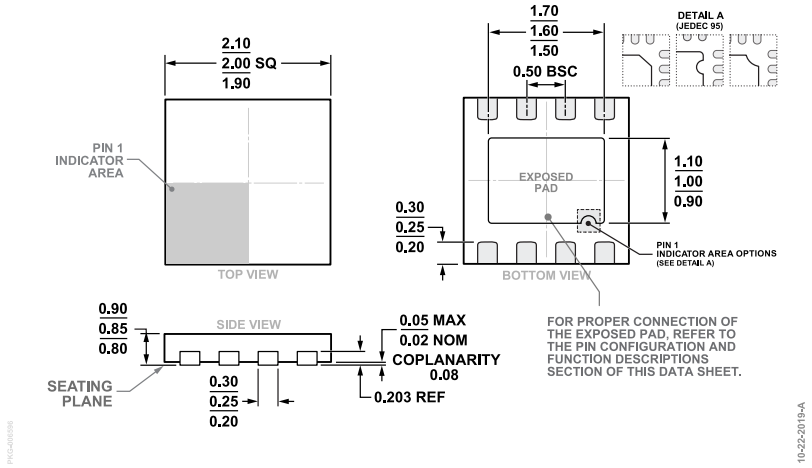


Figure 116. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

Updated: April 02, 2024

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8120ACPZN	−55°C to +125°C	8-lead LFCSP, 2 mm × 2 mm × 0.85 mm	Tape, 1	CP-8-30
ADL8120ACPZN-R7	−55°C to +125°C	8-lead LFCSP, 2 mm × 2 mm × 0.85 mm	Reel, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

[2] The lead finish of the ADL8120ACPZN and the ADL8120ACPZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model[1]	Description
ADL8120-EVALZ	ADL8120 Evaluation Board
ADL8120-EVAL1Z	ADL8120 Low Frequency Evaluation Board

[1] Z = RoHS Compliant Part.