LED Drivers for LCD Backlights

1ch Boost up type White LED Driver for large LCD

BD9409F

1.1 General Description

BD9409F is a high efficiency driver for white LEDs and is designed for large LCDs. BD9409F has a boost DCDC converter that employs an array of LEDs as the light source.

BD9409F has some protect functions against fault conditions, such as over-voltage protection (OVP), over current limit protection of DCDC (OCP), LED OCP protection, and Over boost protection (FBMAX). Therefore it is available for the fail-safe design over a wide range output voltage.

Key Specifications

- Operating power supply voltage range: 11.5V to 35.0V
- Oscillator frequency of DCDC: 150kHz (RT=100kΩ)
- Operating Current: 2.8 mA(Typ.)
- Operating temperature range: -40°C to +105°C

1.2 Package(s)

	W(Typ) x D(Typ) x H(Max)
SOP16	10.00mm x 6.20mm x 1.71mm
	Pin pitch 1.27mm

Features

- DCDC converter with current mode
- LED protection circuit (Over boost protection(FB_H), LED OCP protection)
- Over-voltage protection (OVP) for the output voltage Vout
- Adjustable soft start
- Adjustable oscillation frequency of DCDC
- UVLO detection for the input voltage of the power stage
- PWM Dimming and MS Dimming.

Applications

- TV, Computer Display, LCD Backlighting



Figure 1. SOP16

Typical Application Circuit

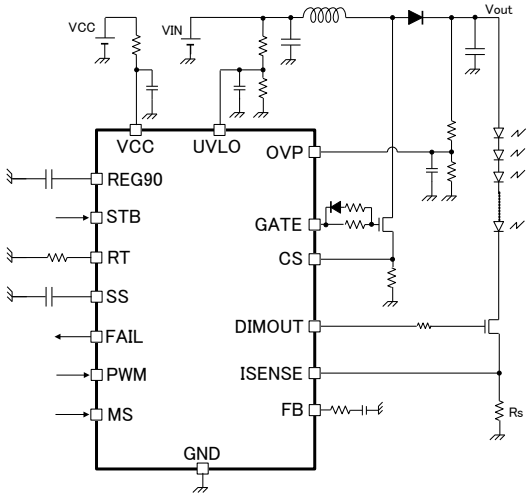


Figure 2. Typical Application Circuit

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1.3 Pin Configuration

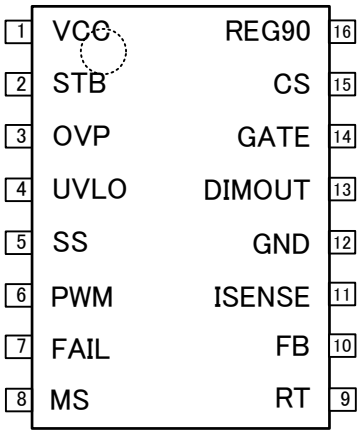


Figure 3. Pin Configuration

1.4 Pin Descriptions

No.	Pin name	Function
1	VCC	Power supply pin
2	STB	IC ON/OFF pin
3	OVP	Over voltage protection detection pin
4	UVLO	Under voltage lock out detection pin
5	SS	Soft start setting pin
6	PWM	External PWM dimming signal input pin
7	FAIL	Error detection output pin(Active High)
8	MS	Mode Select Dimming input pin.
9	RT	DC/DC switching frequency setting pin
10	FB	Error amplifier output pin
11	ISENSE	LED current detection input pin
12	GND	-
13	DIMOUT	Dimming signal output for NMOS
14	GATE	DC/DC switching output pin
15	CS	DC/DC output current detect pin, OCP input pin
16	REG90	9.0V output voltage pin

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1.5 Block Diagram

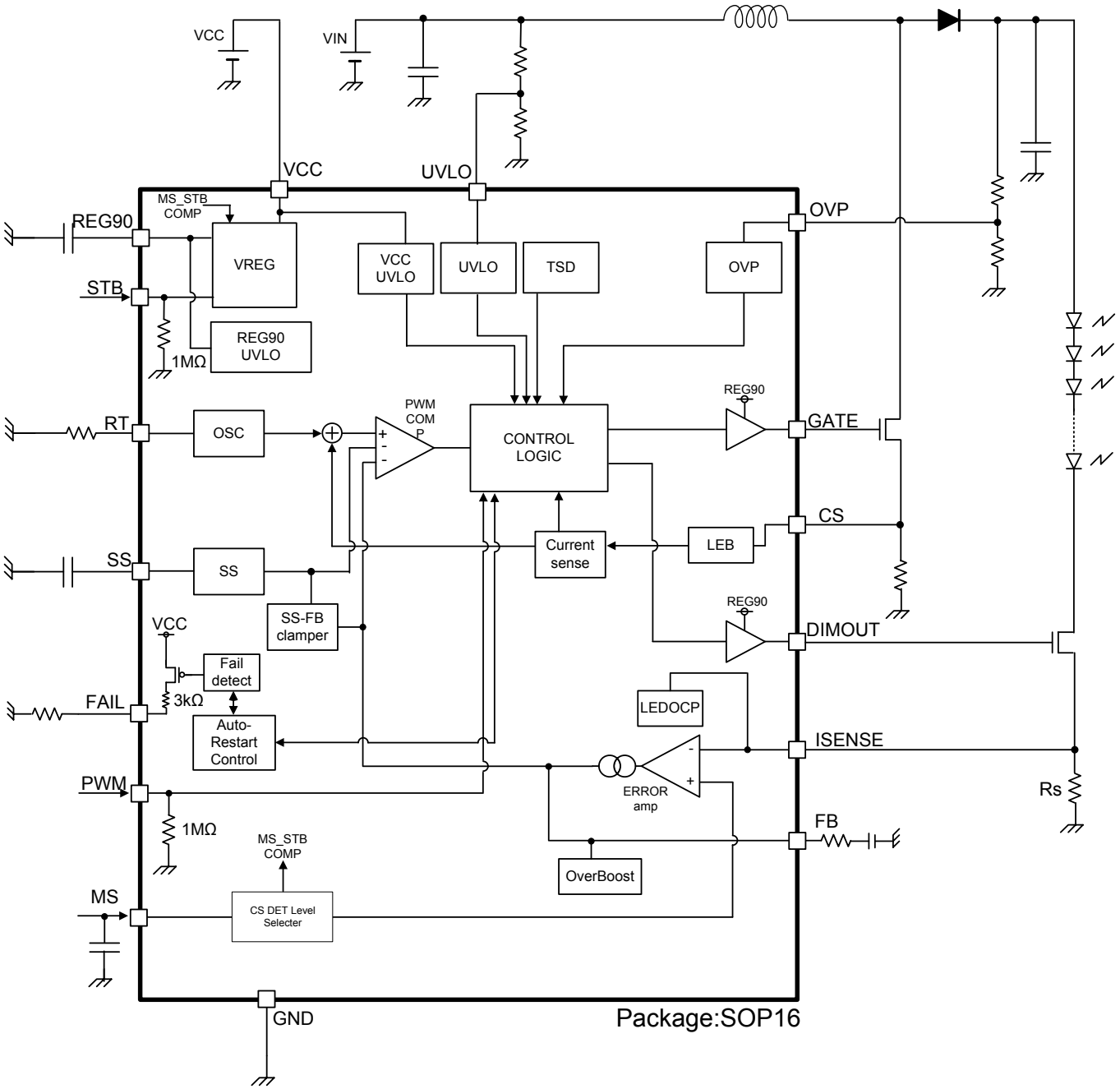


Figure 4. Block Diagram

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1.6 Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCC	-0.3 to +36	V
SS, RT, ISENSE, FB, CS Pin Voltage	SS, RT, ISENSE, FB, CS	-0.3 to +7	V
REG90, DIMOUT, GATE Pin Voltage	REG90, DIMOUT, GATE	-0.3 to +13	V
OVP, UVLO, PWM, MS, STB Pin Voltage	OVP, UVLO, PWM, MS, STB	-0.3 to +20	V
FAIL Pin Voltage	FAIL	-0.3 ~ VCC+0.3	V
Power Dissipation	Pd	0.74 (*1)	W
Operating Temperature Range	Topr	-40 to +105	°C
Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(*1) Derate by 5.92mW/°C when operating above Ta=25°C.. (Mounted on 1-layer 114.3mm x 76.2mm x 1.57mm board)

1.7 Recommended Operating Ranges

Parameter	Symbol	Range	Unit
Power Supply Voltage	VCC	11.5 to 35.0	V
DC/DC Oscillation Frequency	fsw	50 to 1000	kHz
PWM Input Frequency	FPWM	90 to 2000	Hz

1.8 Electrical Characteristics 1/2 (Unless otherwise specified VCC=24V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
【Total Current Consumption】						
Circuit Current	Icc	-	2.8	5.6	mA	VSTB=3.0V, PWM=3.0V
Circuit Current (standby)	IST	-	60	120	μA	VSTB=0V
Circuit Current (MS standby)	IST_MS	-	60	120	μA	VSTB=3.0V, MS=0V
【UVLO Block】						
Operation Voltage（VCC）	VUVLO_VCC	9.5	10.5	11.5	V	VCC=SWEEP UP
Hysteresis Voltage（VCC）	VUHYS_VCC	130	270	540	mV	VCC=SWEEP DOWN
UVLO Release Voltage	VUVLO	2.88	3.00	3.12	V	VUVLO=SWEEP UP
UVLO Hysteresis Voltage	VUHYS	250	300	350	mV	VUVLO=SWEEP DOWN
UVLO Pin Leak Current	UVLO_LK	-2	0	2	μA	VUVLO=4.0V
【DC/DC Block】						
ISENSE Threshold Voltage 1	VLED1	0.327	0.341	0.355	V	MS=1V(75% dimming)
ISENSE Threshold Voltage 2	VLED2	0.441	0.455	0.470	V	MS=2V(100% dimming)
ISENSE Threshold Voltage 3	VLED3	0.483	0.500	0.518	V	MS=3V(110% dimming)
MS Threshold Voltage 0	VMS0	-0.25	0.00	0.25	V	VSTB=3.0V, PWM=3.0V
MS Threshold Voltage 1	VMS1	0.70	1.00	1.25	V	VSTB=3.0V, PWM=3.0V
MS Threshold Voltage 2	VMS2	1.70	2.00	2.25	V	VSTB=3.0V, PWM=3.0V
MS Threshold Voltage 3	VMS3	2.70	3.00	10.0	V	VSTB=3.0V, PWM=3.0V
Oscillation Frequency	FCT	142.5	150	157.5	kHz	RT=100kΩ
RT Short Protection Range	RT_DET	-0.3	-	VRT ×90%	V	RT=SWEEP DOWN
RT Terminal Voltage	VRT	1.6	2.0	2.4	V	RT=100kΩ
GATE Pin MAX DUTY Output	MAX_DUTY	90	95	99	%	RT=100kΩ
GATE Pin ON Resistance (as source)	RONSO	2.5	5.0	10.0	Ω	
GATE Pin ON Resistance (as sink)	RONSI	2.0	4.0	8.0	Ω	
SS Pin Source Current	ISSSO	-3.75	-3.00	-2.25	μA	VSS=2.0V
SS Pin ON Resistance at OFF	RSS_L	-	3.0	5.0	kΩ	
Soft Start Ended Voltage	VSS_END	3.52	3.70	3.88	V	SS=SWEEP UP

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1.8 Electrical Characteristics 2/2 (Unless otherwise specified VCC=24V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
【DC/DC Block】						
FB Source Current	IFBSO	-115	-100	-85	μA	VISENSE=0.0V, VMS=3.0V, VFB=1.0V
FB Sink Current	IFBSI	85	100	115	μA	VISENSE=2.0V, VMS=3.0V, VFB=1.0V
【DC/DC Protection Block】						
OCP Detect Voltage	VCS1	360	400	440	mV	CS=SWEEP UP
OCP Latch OFF Detect Voltage	VCS2	0.85	1.00	1.15	V	CS=SWEEP UP
OVP Detect Voltage	VOVP	2.88	3.00	3.12	V	VOVP SWEEP UP
OVP Detect Hysteresis	VOVP_HYS	150	200	250	mV	VOVP SWEEP DOWN
OVP Pin Leak Current	OVP_LK	-1.8	0	1.8	μA	VOVP=4.0V, VSTB=3.0V
【LED Protection Block】						
LED OCP Detect Voltage	VLEDOCP	2.88	3.00	3.12	V	VISENSE=SWEEP UP
Over Boost Detection Voltage	VFBH	3.84	4.00	4.16	V	VFB=SWEEP UP
【Dimming Block】						
MS Pin Leak Current	ILMS	-1.8	0	1.8	μA	VMS=2.0V
ISENSE Pin Leak Current	IL_ISENSE	-2	0	2	μA	VISENSE=4.0V
DIMOUT Source ON Resistance	RONSO	5.0	10.0	20.0	Ω	
DIMOUT Sink ON Resistance	RONSI	4.0	8.0	16.0	Ω	
MS Pin HIGH Voltage (Active mode)	V_{MS_H}	0.70	-	20	V	MS=Sweep up
MS Pin LOW Voltage (Stand-by mode)	V_{MS_L}	-0.25	-	0.25	V	MS=Sweep down
【REG90 Block】						
REG90 Output Voltage 1	REG90_1	8.91	9.00	9.09	V	IO=0mA
REG90 Output Voltage 2	REG90_2	8.865	9.00	9.135	V	IO=-15mA
REG90 Available Source Current	| IREG90 |	15	-	-	mA	
REG90_UVLO Detect Voltage	REG90_TH	5.22	6.00	6.78	V	VREG90=SWEEP DOWN, VSTB=0V
REG90 Discharge Resistance	REG90_DIS	13.2	22.0	30.8	kΩ	STB=MS=ON->OFF, REG90=8.0V, PWM=H
【STB Block】						
STB Pin HIGH Voltage	STBH	2.0	-	18	V	
STB Pin LOW Voltage	STBL	-0.3	-	0.8	V	
STB Pull Down Resistance	RSTB	600	1000	1400	kΩ	VSTB=3.0V
【PWM Block】						
PWM Pin HIGH Voltage	PWM_H	1.5	-	18	V	
PWM Pin LOW Voltage	PWM_L	-0.3	-	0.8	V	
PWM Pin Pull Down Resistance	RPWM	600	1000	1400	kΩ	VPWM=3.0V
【Filter Block】						
Abnormal Detection Timer	tCP	-	20	-	ms	FCT=200kHz
AUTO Timer	tAUTO	-	655	-	ms	FCT=200kHz
【FAIL Block 】						
Pull Up Resistance of FAILB Pin Latch Off	RFAIL	-	3.0	6.0	kΩ	CS=1.15V

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1.9 Typical Performance Curves (Reference data)

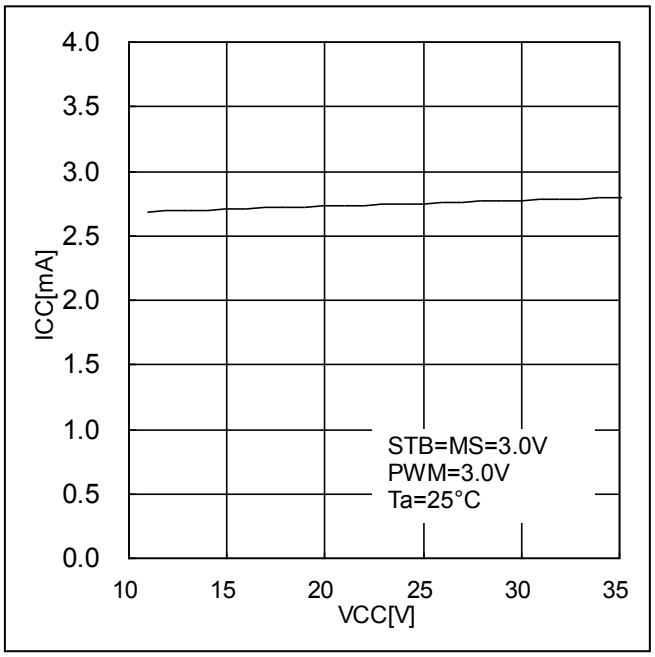


Figure 5. Operating circuit current

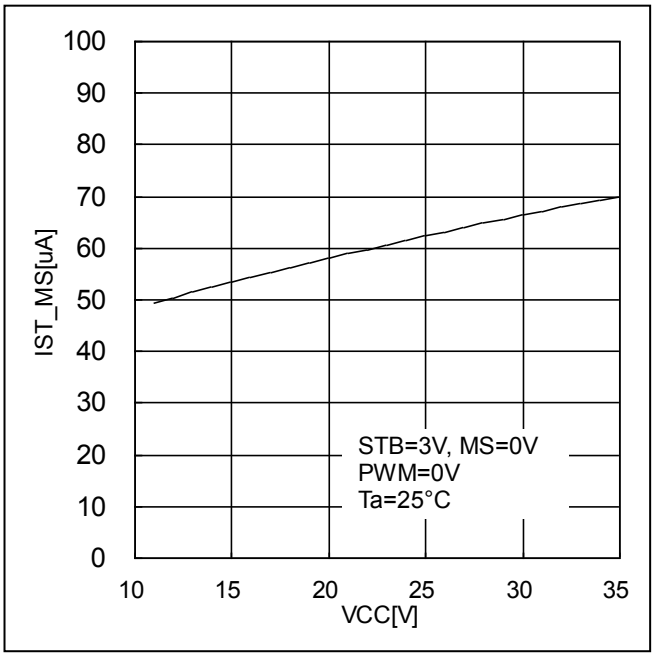


Figure 6. Standby circuit current MS

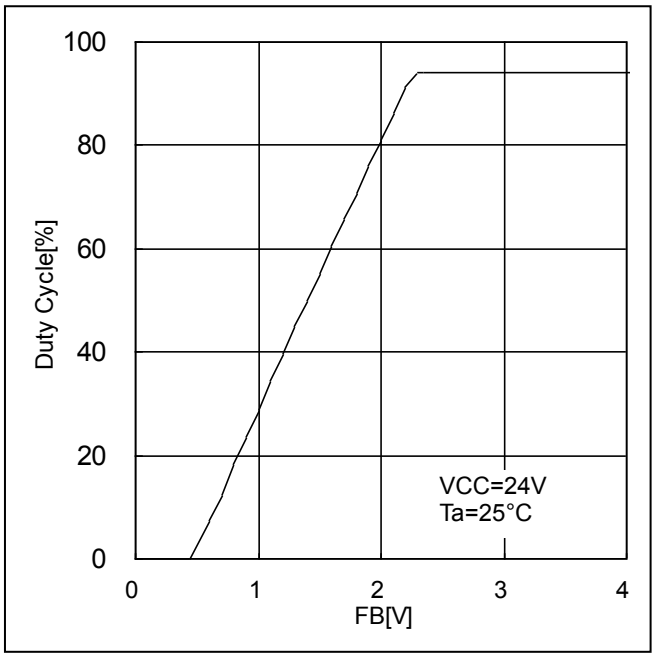


Figure 7. Duty cycle vs FB character

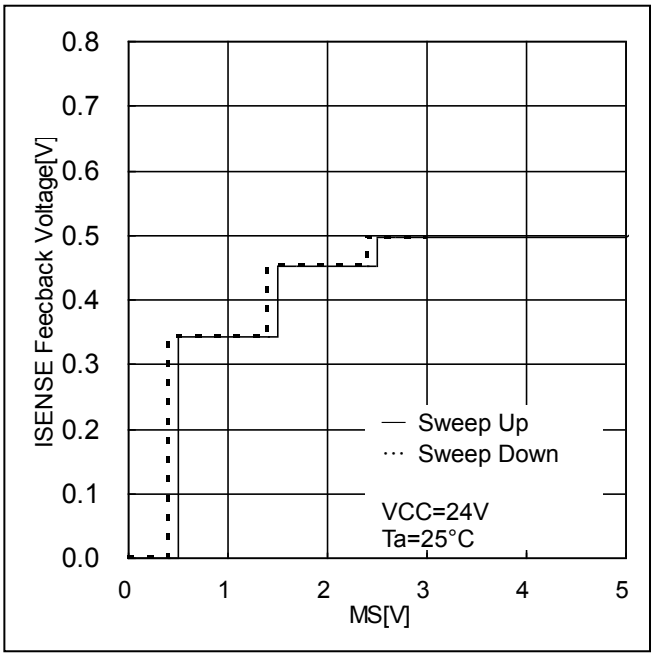


Figure 8. ISENSE feedback voltage vs MS character

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2.1 Pin Descriptions

○Pin 1: VCC

This is the power supply pin of the IC. Input range is from 11.5V to 35V.
The operation starts at more than 10.5V(typ.) and shuts down at less than 10.2V(typ.).

○Pin 2: STB

This is the ON/OFF setting terminal of the IC. Input reset-signal to this terminal to reset IC from latch-off.
At startup, internal bias starts at high level, and then PWM DCDC boost starts after PWM rise edge inputs.
Note: IC status (IC ON/OFF) transits depending on the voltage inputted to STB and MS terminal. Avoid the use of intermediate level (from 0.8V to 2.0V).

○Pin 3: OVP

The OVP terminal is the input for over-voltage protection. If OVP is more than 3.0V(typ), the over-voltage protection (OVP) will work. At the moment of these detections, it sets GATE=L, DIMOUT=L and starts to count up the abnormal interval. If OVP detection continued to count four GATE clocks, IC reaches latch off. (Please refer to “3.5.5 Timing Chart”)
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if OVP function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the section ”3.2.6 OVP Setting”.

○Pin 4: UVLO

Under Voltage Lock Out pin is the input voltage of the power stage. , IC starts the boost operation if UVLO is more than 3.0V(typ) and stops if lower than 2.7V(typ).
The UVLO pin is high impedance, because the internal resistance is not connected to a certain bias.
Even if UVLO function is not used, pin bias is still required because the open connection of this pin is not a fixed potential.
The setting example is separately described in the section ”3.2.5 UVLO Setting”

○Pin 5: SS

This is the pin which sets the soft start interval of DC/DC converter. It performs the constant current charge of 3.0 μA(typ.) to external capacitance Css. The switching duty of GATE output will be limited during 0V to 3.7V(typ.) of the SS voltage.
So the soft start interval Tss can be expressed as follows

$$T_{SS} = 1.23 \times 10^{6} \times C_{SS}[sec]$$ **Css: the external capacitance of the SS pin**.

The logic of SS pin asserts low is defined as the latch-off state or PWM is not input high level after STB reset release.
When SS capacitance is under 1nF, take note if the in-rush current during startup is too large, or if over boost detection (FBMAX) mask timing is too short.
Please refer to soft start behavior in the section “3.5.4 Timing Chart ”.

○Pin 6: PWM

This is the PWM dimming signal input terminal. The high / low level of PWM pins are the following.

State	PWM input voltage
PWM=H	PWM=1.5V to 18.0V
PWM=L	PWM=-0.3V to 0.8V

○Pin 7: FAIL

This is FAIL signal output (OPEN DRAIN) pin. At normal operation, PMOS will be OPEN state, during abnormality detection PMOS will be in ON (3kohm typ.) state. And Pull Up to VCC.

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○Pin 8: MS

This is the input pin for analog dimming signal. In this condition, the input current is caused. Please refer to <ISENSE> terminal explanation.

Relationship between MS Voltage and ISENSE Voltage.

V_{MS} =3V(2.70~10.0V) : V_{ISENSE} = 0.500V (110% dimming)
V_{MS} =2V(1.70~2.25V) : V_{ISENSE} = 0.455V (100% dimming)
V_{MS} =1V(0.70~1.25V) : V_{ISENSE} = 0.341V (75% dimming)
V_{MS} =0V(-0.25~0.25V) : MS Stand-by Mode

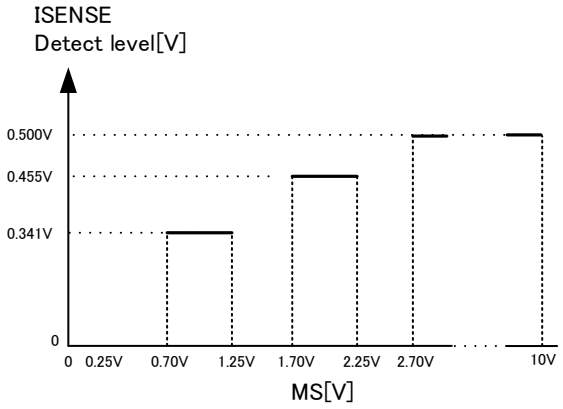


Figure 9. MS Dimming

○Pin 9: RT

This is the DC/DC switching frequency setting pin. DCDC frequency is decided by connected resistor.

○The relationship between the frequency and RT resistance value **(ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

The oscillation setting ranges from 50kHz to 1000kHz.
The setting example is separately described in the section ”3.2.4 DCDC Oscillation Frequency Setting”.

○Pin 10: FB

This is the output terminal of error amplifier.
FB pin rises with the same slope as the SS pin during the soft-start period.
After soft -start completion (SS>3.7V(typ.)), it operates as follows.

When PWM=H, it detects ISENSE terminal voltage and outputs error signal compared to analog dimming signal (MS).

It detects over boost (FBMAX) over FB=4.0V(typ). After the SS completion, if FB>4.0V and PWM=H continues 4clk GATE, the CP counter starts. After that, only the FB>4.0V is monitored, When CP counter reaches 4096clk (2^{12}clk), IC will be latched off. (Please refer to section “3.5.6 Timing Chart”.)

The loop compensation setting is described in section "3.4 Loop Compensation".

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○Pin 11: ISENSE

This is the input terminal for the current detection. Error amplifier will be 3 Dimming modes by the voltage input from the MS voltage. The 3 modes are compared with each DET voltage. And it detects abnormal LED overcurrent at ISENSE=3.0V(typ) over. If GATE terminal continues during four CLKs (equivalent to 40us at fosc = 100kHz), it becomes latch-off.
(Please refer to section “3.5.7 Timing Chart”.)

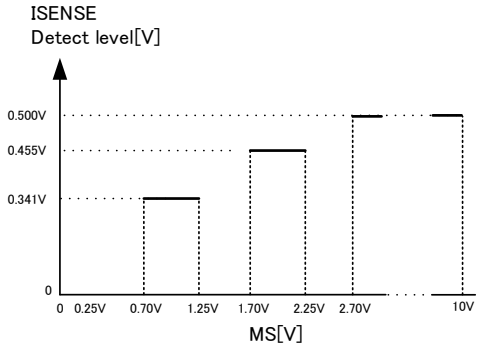


Figure 10. Relationship of the feedback voltage and MS

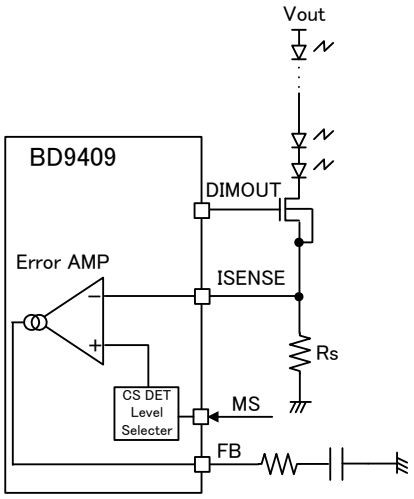


Figure 11. ISENSE terminal circuit example

○Pin 12: GND

This is the GND pin of the IC.

○Pin 13: DIMOUT

This is the output pin for external dimming NMOS. The table below shows the rough output logic of each operation state, and the output H level is REG90. Please refer to “3.5 Timing Chart” for detailed explanations, because DIMOUT logic has an exceptional behavior. Please insert the resistor R_{DIM} between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

Status	DIMOUT output
Normal	Same logic to PWM
Abnormal	GND Level

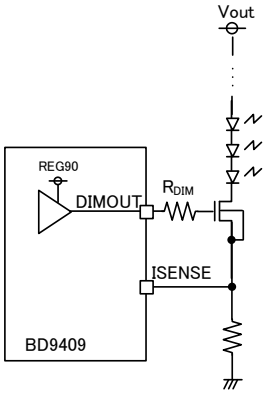


Figure 12. DIMOUT terminal circuit example

○Pin 14: GATE

This is the output terminal for driving the gate of the boost MOSFET. The high level is REG90. Frequency can be set by the resistor connected to RT. Refer to <RT> pin description for the frequency setting.

○Pin 15: CS

The CS pin has two functions.

1. DC / DC current mode Feedback terminal

The inductor current is converted to the CS pin voltage by the sense resistor R_{CS}. This voltage compared to the voltage set by error amplifier controls the output pulse.

2. Inductor current limit (OCP) terminal

The CS terminal also has an over current protection (OCP). If the voltage is more than 0.4V(typ.), the switching operation will be stopped compulsorily. And the next boost pulse will be restarted to normal frequency.
In addition, the CS voltage is more than 1.0V(typ.) during four GATE clocks, IC will be latch off. As above OCP operation, if the current continues to flow nevertheless GATE=L because of the destruction of the boost MOS, IC will stops the operation completely.

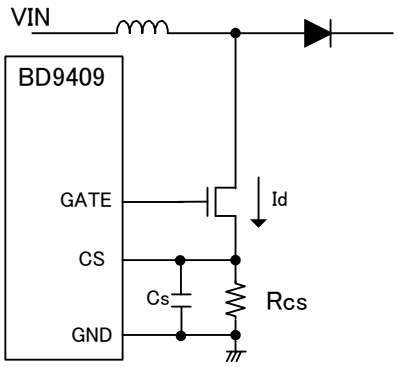


Figure 13. CS terminal circuit example

Both of the above functions are enabled after 300ns (typ) when GATE pin asserts high, because the Leading Edge Blanking function (LEB) is included into this IC to prevent the effect of noise.
Please refer to section “3.3.1 OCP Setting / Calculation Method for the Current Rating of DCDC Parts”, for detailed explanation.
If the capacitance Cs in the right figure is increased to a micro order, please be careful that the limited value of NMOS drain current Id is more than the simple calculation. Because the current Id flows not only through Rcs but also through Cs, as the CS pin voltage moves according to Id.

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○Pin 16: REG90

This is the 9.0V(typ.) output pin. Available current is 15mA (min).
The characteristic of VCC line regulation at REG90 is shown as figure. VCC must be used in more than 11.5V for stable 9V output.
Please place the ceramic capacitor connected to REG90 pin (1.0μF to 10μF) closest to REG90-GND pin.

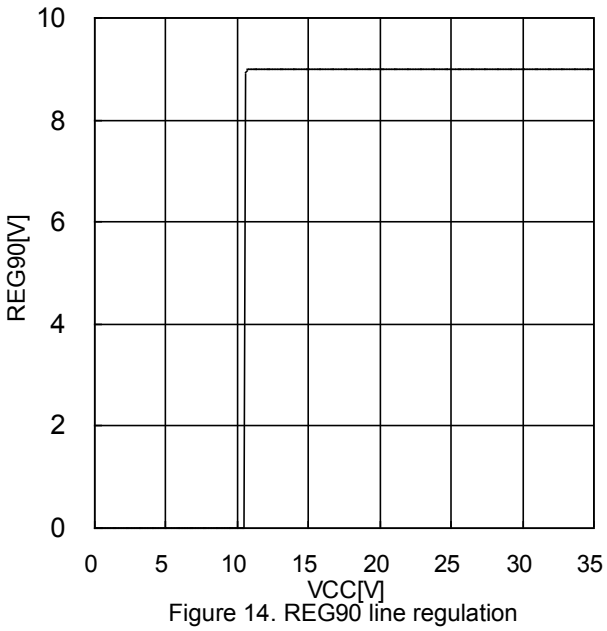


Figure 14. REG90 line regulation

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2.6 List of The Protection Function Detection Condition (Typ Condition)

Protect function	Detection pin	Detect condition			Release condition	Timer operation	Protection type
		Detection condition	PWM	SS			
FBMAX	FB	FB > 4.0V	H(4clk)	SS>3.7V	FB < 4.0V	2^{12}clk	Auto-restart after detection (Judge periodically whether normal or not)
LED OCP	ISENSE	ISENSE > 3.0V	-	-	ISENSE < 3.0V	4clk	Auto-restart after detection (Judge periodically whether normal or not)
RT GND SHORT	RT	RT<VRT×90%	-	-	Release RT=GND	NO	Restart by release
RT HIGH SHORT	RT	RT>5V	-	-	Release RT=HIGH	NO	Restart by release
UVLO	UVLO	UVLO<2.7V	-	-	UVLO>3.0V	NO	Restart by release
REG90UVLO	REG90	REG90<6.0V	-	-	REG90>6.5V	NO	Restart by release
VCC UVLO	VCC	VCC<10.2V	-	-	VCC>10.5V	NO	Restart by release
OVP	OVP	OVP>3.0V	-	-	OVP<2.8V	4clk	Auto-restart after detection (Judge periodically whether normal or not)
OCP	CS	CS>0.4V	-	-	-	NO	Pulse by pulse
OCP LATCH	CS	CS>1.0V	-	-	CS<1.0V	4clk	Auto-restart after detection (Judge periodically whether normal or not)

To reset the latch type protection, please set STB logic to 'L' once. Otherwise the detection of VCCUVLO, REG90UVLO is required.
The clock number of timer operation corresponds to the boost pulse clock.
Auto-restart clock = 2^{17}clk = 131072clk.

2.7 List of The Protection Function Operation

Protect function	Operation of the protect function			
	DC/DC gate output	Dimming transistor (DIMOUT) logic	SS pin	FAIL pin
FBMAX	Stop after latch	Low after latch	Discharge after latch	High after timer latch
LED OCP	Stop immediately	Immediately high, Low after latch	Discharge after latch	High after timer latch
RT GND SHORT	Stop immediately	Immediately low	Not discharge	Low
RT HIGH SHORT	Stop immediately	Immediately low	Not discharge	Low
STB	Stop immediately	Low after REG90UVLO detects	Discharge immediately	Low
MS_STB	Stop immediately	Low after REG90UVLO detects	Discharge immediately	Low
UVLO	Stop immediately	Immediately low	Discharge immediately	Low
REG90UVLO	Stop immediately	Immediately low	Discharge immediately	Low
VCC UVLO	Stop immediately	Immediately low	Discharge immediately	Low
OVP	Stop immediately	Immediately low	Discharge after latch	High after timer latch
OCP	Stop immediately	Normal operation	Not discharge	Low
OCP LATCH	Stop after latch	Low after latch	Discharge after latch	High after timer latch

Please refer to section "3.5 Timing Chart" for details.

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3.1 Application Circuit Example

Introduce an example application using the BD9409F.

3.1.1 Basic Application Example

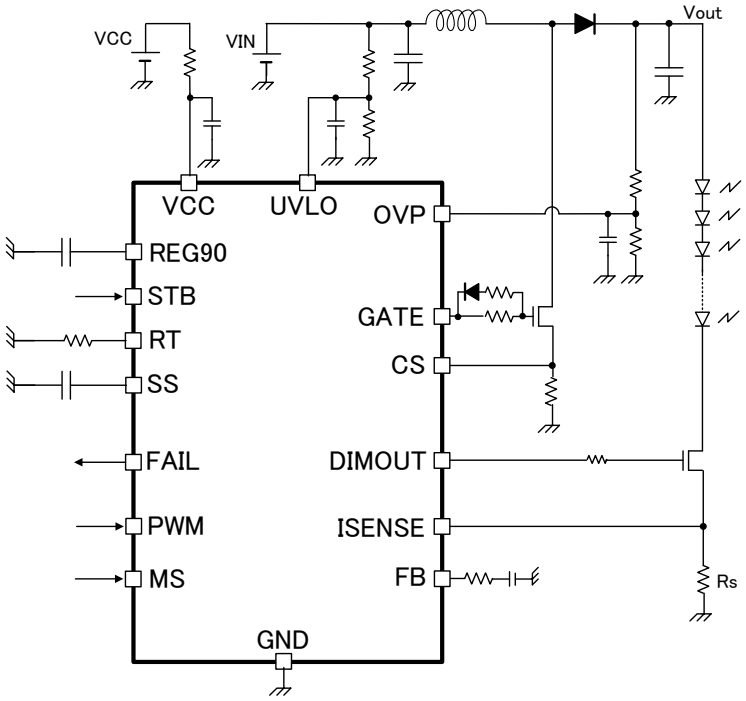


Figure 15. Basic application example

3.1.2 MS Dimming or PWM Dimming Examples

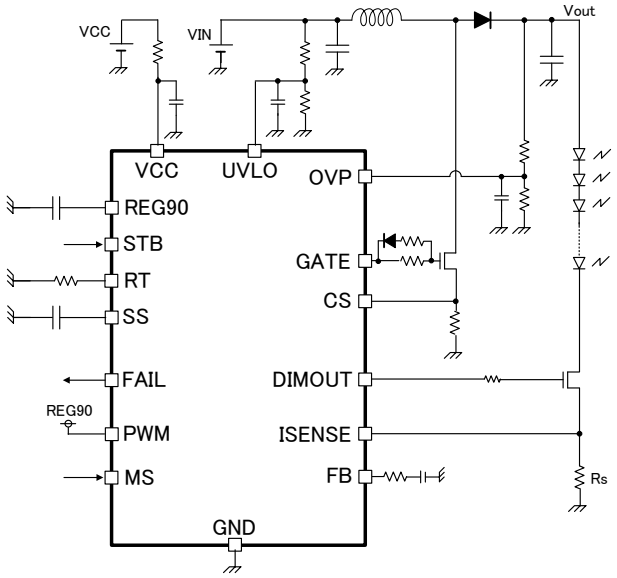


Figure 16. Example circuit for analog dimming

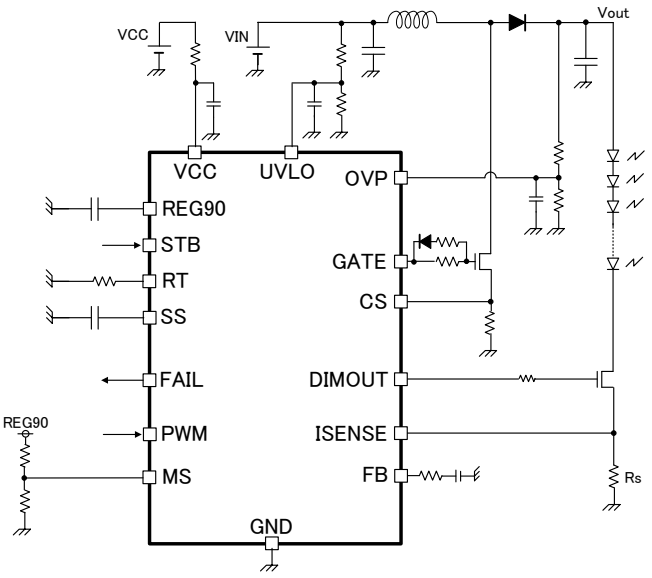


Figure 17. Example circuit for PWM dimming

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3.2 External Components Selection

3.2.1 Start Up Operation and Soft Start External Capacitance Setting

The below explanation is the start up sequence of this IC

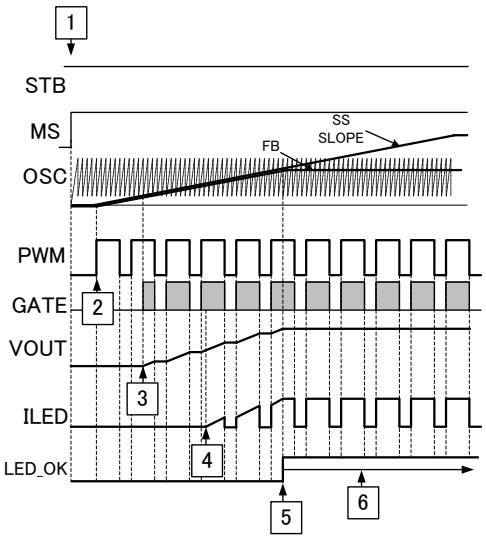


Figure 18. Startup waveform

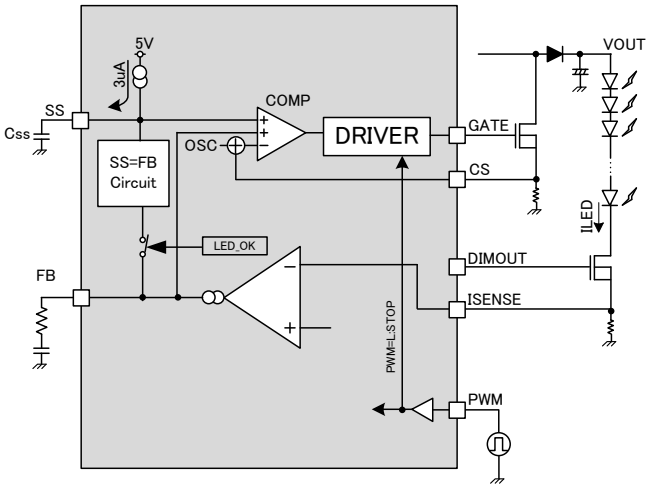


Figure 19. Circuit behavior at startup

○Explanation of start up sequence

1. Reference voltage REG90 starts by STB=MS=H.
2. SS starts to charge at the time of first PWM=H. At this moment, the SS voltage of slow-start starts to equal FB voltage,and the circuit becomes FB=SS regardless of PWM logic.
3. When FB=SS reaches the lower point of internal sawtooth waveform, GATE terminal outputs pulse and starts to boost VOUT.
4. It boosts VOUT and VOUT reaches the voltage to be able to flow LED current.
5. If LED current flows over decided level, FB=SS circuit disconnects and startup behavior completes.
6. Then it works normal operation by feedback of ISENSE terminal. If LED current doesn't flow when SS becomes over 3.7V(typ.), SS=FF circuit completes forcibly and FBMAX protection starts.

○Method of setting SS external capacitance

According to the sequence described above, start time Tss that startup completes with FB=SS condition is the time that FB voltage reaches the feedback point.
The capacitance of SS terminal is defined as Css and the feedback voltage of FB terminal is defined as VFB. The equality on T_{FB} is as follows.

$$T_{ss} = \frac{C_{ss}[\mu F] \times VFB[V]}{3[\mu A]} \quad [\mathrm{sec}]$$

If Css is set to a very small value, rush current flows into the inductor at startup.
On the contrary, if Css is enlarged too much, LED will light up gradually.
Since Css differs in the constant set up with the characteristic searched for and differs also by factors, such as a voltage rise ratio, an output capacitance, DCDC frequency, and LED current, please confirm with the system.

【Setting example】

When Css=0.1uF,Iss=3μA,and startup completes at VFB=3.7V, SS setting time is as follows.

$$T_{ss} = \frac{0.1 \times 10^{-6}[F] \times 3.7[V]}{3 \times 10^{-6}[A]} = 0.123[\mathrm{sec}]$$

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3.2.2 VCC Series Resistance Setting

Here are the following effects of inserting series resistor Rvcc into VCC line.
(i) In order to drop the voltage VCC, it is possible to suppress the heat generation of the IC.
(ii) It can limit the inflow current to VCC line.
However, if resistance RVCC is set bigger, VCC voltage becomes under minimum operation voltage (VCC<11.5V). RVCC must be set to an appropriate series resistance.

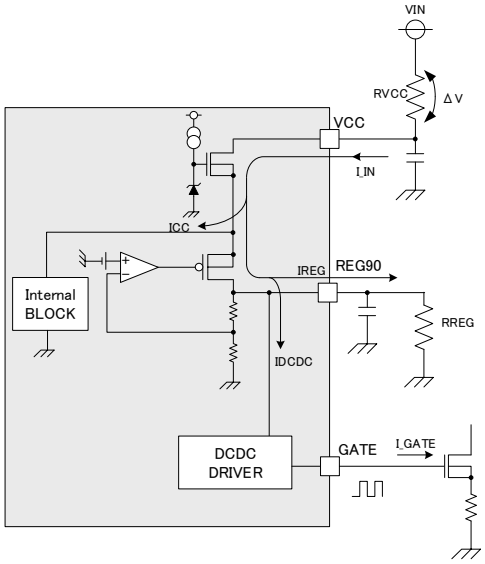


Figure 20. VCC series resistance circuit example

IC's inflow current line I_IN has the following inflow lines.
・IC's circuit current…ICC
・Current of RREG connected to REG90…IREG
・Current to drive FET's Gate…I_GATE
These decide the voltage ΔV at RVCC.
VCC terminal voltage at that time can be expressed as follows.

$$VCC[V] = VIN[V] - (ICC[A] + IDCDC[A] + IREG[A]) \times RVCC[\Omega] \quad > \quad 11.5[V]$$

Here, judgement is the 11.5V minimum operation voltage.
Please consider a sufficient margin when setting the series resistor of VCC.

【setting example】
Above equation is translated as follows.

$$RVCC[\Omega] \quad < \quad \frac{VIN[V] - 11.5[V]}{ICC[A] + IDCDC[A] + IREG[A]}$$

When VIN=24V, ICC=2.0mA, RREG=10kΩ and IDCDC=2mA, RVCC's value is calculated as follows.

$$RVCC[\Omega] \quad < \quad \frac{24[V] - 11.5[V]}{0.002[A] + 0.002[A] + 9.0[V]/10000[\Omega]} = 2.55[k\Omega]$$

(ICC is 2.8mA(typ.)) . Please set each values with tolerance and margin.

3.2.3 LED current setting

LED current can be adjusted by setting the resistance R_S [Ω] which connects to ISENSE pin and MS[V].

Relationship between R_S and I_{LED} current

With VMS2 dimming (1.7V<MS<2.25V)=100% Dimming.

$$R_S = \frac{0.455[V]}{I_{LED}[A]} \quad [\Omega]$$

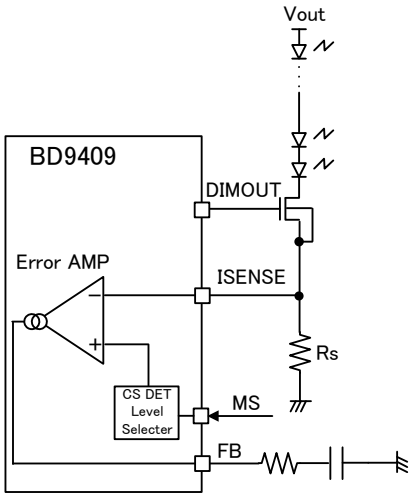


Figure 21. LED current setting example

【setting example】
If I_{LED} current is 200mA and MS is 2.0V, we can calculate R_S as below.

$$R_S = \frac{0.455[V]}{I_{LED}[A]} = \frac{0.455[V]}{0.150[A]} = 3.03[\Omega]$$

With VMS1 dimming (0.7V<MS<1.25V)=75% Dimming.

$$I_{LED} = \frac{0.341[V]}{R_S[\Omega]} = \frac{0.341[V]}{3.03[\Omega]} = 112.5[mA]$$

With VMS3 dimming (2.7V<MS<3.25V)=110% Dimming.

$$I_{LED} = \frac{0.500[V]}{R_S[\Omega]} = \frac{0.500[V]}{3.03[\Omega]} = 165[mA]$$

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3.2.4 DCDC Oscillation Frequency Setting

R_{RT} which connects to RT pin sets the oscillation frequency f_{SW} of DCDC.

○Relationship between frequency f_{SW} and RT resistance (ideal)

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

【setting example】

When DCDC frequency fsw is set to 200kHz, R_{RT} is as follows.

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} = \frac{15000}{200[kHz]} = 75[k\Omega]$$

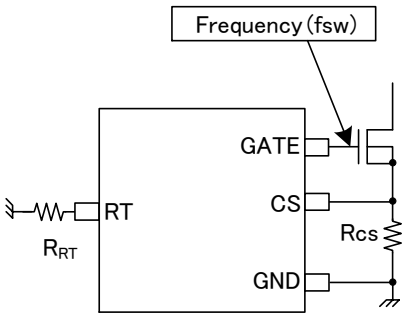


Figure 22. RT terminal setting example

3.2.5 UVLO Setting

Under Voltage Lock Out pin is the input voltage of the power stage. IC starts boost operation if UVLO is more than 3.0V(typ.) and stops if lower than 2.7V(typ.).
The UVLO pin is high impedance, because the internal resistance is not connected to a certain bias.
So, the bias by the external components is required, because the open connection of this pin is not a fixed potential.

Detection voltage is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

○UVLO detection equation

As VIN decreases, R1 and R2 values are set in the following formula by the VIN_{DET} that UVLO detects.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} [k\Omega]$$

○UVLO release equation

R1 and R2 setting is decided by the equation above. The equation of UVLO release voltage is as follows.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] - R2[k\Omega])}{R2[k\Omega]} [V]$$

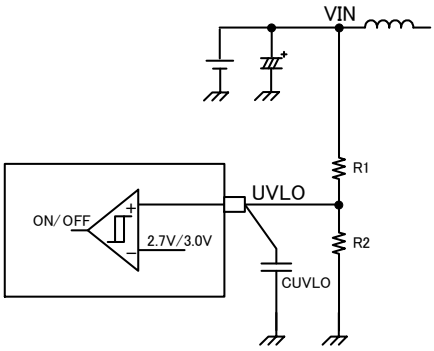


Figure 23. UVLO setting example

【setting example】

If the normal input voltage, VIN is 24V, the detect voltage of UVLO is 18V, R2 is 30kΩ, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.7[V])}{2.7[V]} = 30[k\Omega] \times \frac{(18[V] - 2.7[V])}{2.7[V]} = 170.0[k\Omega]$$

By using these R1 and R2, the release voltage of UVLO, VIN_{CAN}, can be calculated too as follows.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] - R2[k\Omega])}{R2[k\Omega]} = 3.0[V] \times \frac{(170.0[k\Omega] + 30[k\Omega])}{30[k\Omega]} [V] = 20.0[V]$$

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3.2.6 OVP Setting

The OVP terminal is the input for over-voltage protection of output voltage.
The OVP pin is high impedance, because the internal resistance is not connected to a certain bias.

Detection voltage of VOUT is set by dividing resistors R1 and R2. The resistor values can be calculated by the formula below.

○OVP detection equation

If VOUT is boosted abnormally, $VOVP_{DET}$, the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]}[k\Omega]$$

○OVP release equation

By using R1 and R2 in the above equation, the release voltage of OVP, $VOVP_{CAN}$ can be expressed as follows.

$$VIN_{CAN} = 2.8V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]}[V]$$

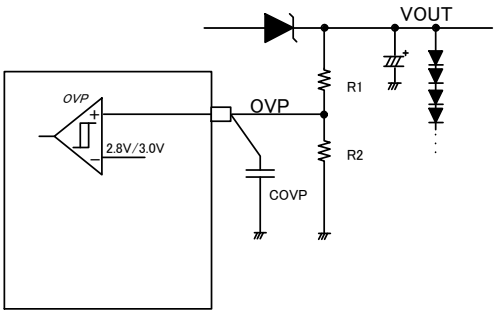


Figure 24. OVP setting example

【setting example】

If the normal output voltage, VOUT is 40V, the detect voltage of OVP is 48V, R2 is 10kΩ, R1 is calculated as follows.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} = 10[k\Omega] \times \frac{(48[V] - 3.0[V])}{3[V]} = 150[k\Omega]$$

By using these R1 and R2, the release voltage of OVP, $VOVP_{CAN}$ can be calculated as follows.

$$VIN_{CAN} = 2.8V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 2.8[V] \times \frac{150[k\Omega] + 10[k\Omega]}{10[k\Omega]}[V] = 44.8[V]$$

3.2.7 Timer Latch Time (CP Counter) Setting, Auto-Restart Timer Setting

About over boost protection (FBMAX), timer latch time (CP Counter) is set by counting the clock frequency which is set at the RT pin. About the behavior from abnormal detection to latch-off, please refer to the section “3.5.6 Timing Chart”.

The condition FB>4.0V(typ.) and PWM=H continues more than four GATE clocks, counting starts from the timing. After that, only the FB voltage is monitored and latch occurs after below time has passed.

$$LATCH_{TIME} = 2^{12} \times \frac{R_{RT}}{1.5 \times 10^7} = 4096 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^7}[s]$$

$$AUTO_{TIME} = 2^{17} \times \frac{R_{RT}}{1.5 \times 10^7} = 131072 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^7}[s]$$

Here, $LATCH_{TIME}$ = time until latch condition occurs, $AUTO_{TIME}$ = auto restart timer’s time
R_{RT} = Resistor value connected to RT pin

【setting example】

Timer latch time when RT=75kohm

$$LATCH_{TIME} = 4096 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^7} = 4096 \times \frac{75[k\Omega]}{1.5 \times 10^7} = 20.48[ms]$$

$$AUTO_{TIME} = 131072 \times \frac{R_{RT}[k\Omega]}{1.5 \times 10^7} = 131072 \times \frac{75[k\Omega]}{1.5 \times 10^7} = 655.36[ms]$$

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3.3 DCDC Parts Selection

3.3.1. OCP Setting / Calculation Method for the Current Rating of DCDC Parts

OCP detection stops the switching when the CS pin voltage is more than 0.4V(typ.). The resistor value of CS pin, R_{CS} needs to be considered by the coil L current. And the current rating of DCDC external parts is required more than the peak current of the coil.
Shown below are the calculation method of the coil peak current, the selection method of Rcs (the resistor value of CS pin) and the current rating of the external DCDC parts at Continuous Current Mode.

(the calculation method of the coil peak current, Ipeak at Continuous Current Mode)

At first, since the ripple voltage at CS pin depends on the application condition of DCDC, the following variables are used.
Vout voltage=VOUT[V]
LED total current=IOUT[A]
DCDC input voltage of the power stage =VIN[V]
Efficiency of DCDC =η[%]
And then, the average input current IIN is calculated by the following equation.

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]}[A]$$

And the ripple current of the inductor L (ΔIL[A]) can be calculated by using DCDC the switching frequency, fsw, as follows.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]}[A]$$

On the other hand, the peak current of the inductor Ipeak can be expressed as follows.

$$I_{PEAK} = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] \quad \cdots (1)$$

Therefore, the bottom of the ripple current Imin is

$$I_{\min} = I_{IN}[A] - \frac{\Delta IL[A]}{2} \quad \text{or } 0$$

If Imin>0, the operation mode is CCM (Continuous Current Mode), otherwise the mode is DCM (Discontinuous Current Mode).

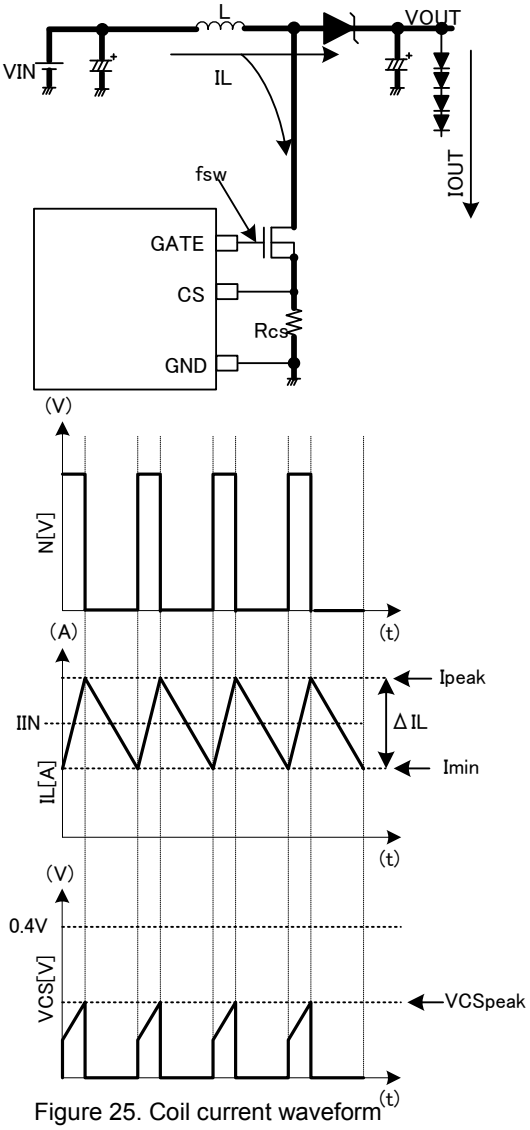


Figure 25. Coil current waveform

(the selection method of Rcs at Continuous Current Mode)

Ipeak flows into Rcs and that causes the voltage signal to CS pin. (Please refer to the timing chart at the right)
Peak voltage VCSpeak is as follows.

$$VCS_{PEAK} = R_{CS} \times I_{PEAK}[V]$$

As this VCSpeak reaches 0.4V(typ.), the DCDC output stops the switching. Therefore, Rcs value is necessary to meet the condition below.

$$R_{CS} \times I_{PEAK} \quad [V] \ << \ 0.4[V]$$

(the current rating of the external DCDC parts)

The peak current as the CS voltage reaches OCP level (0.4V (typ.)) is defined as Ipeak_det.

$$I_{PEAK_DET} = \frac{0.4[V]}{R_{CS}[\Omega]}[A] \quad \cdots (2)$$

The relationship among Ipeak (equation (1)), Ipeak_det (equation (2)) and the current rating of parts is required to meet the following

$$I_{PEAK} \ << \ I_{PEAK_DET} \ << \ \text{The current rating of parts}$$

Please make the selection of the external parts such as FET, Inductor, diode meet the above condition.

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[setting example]
Output voltage = VOUT [V] = 40V
LED total current = IOUT [A] = 0.48V
DCDC input voltage of the power stage = VIN [V] = 24V
Efficiency of DCDC =η[%] = 90%
Averaged input current IIN is calculated as follows.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89 \quad [A]$$

If the switching frequency, f_{SW} = 200kHz, and the inductor, L=100μH, the ripple current of the inductor L (ΔIL[A]) can be calculated as follows.

$$\Delta\ IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48 \quad [A]$$

Therefore the inductor peak current, Ipeak is

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2}[A] = 0.89[A] + \frac{0.48[A]}{2} = 1.13 \quad [A]}$$ …calculation result of the peak current

If Rcs is assumed to be 0.3Ω

$$\boxed{VCS_{peak} = Rcs \times Ipeak = 0.3[\Omega] \times 1.13[A] = 0.339 \quad [V] << 0.4V}$$ …Rcs value confirmation

The above condition is met.
And Ipeak_det, the current OCP works, is

$$I_{peak_det} = \frac{0.4[V]}{0.3[\Omega]} = 1.33 \quad [A]$$

If the current rating of the used parts is 2A,

$I_{peak} << I_{peak_det} <<$ The current rating $\boxed{= 1.13[A] << 1.33[A] << 2.0[A]}$ …current rating confirmation of DCDC parts

This inequality meets the above relationship. The parts selection is proper.
And I_{MIN}, the bottom of the IL ripple current, can be calculated as follows.

$$I_{MIN} = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

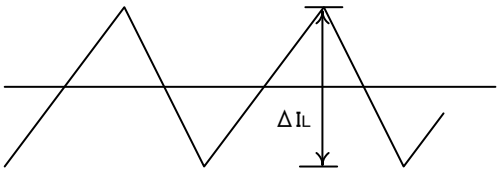
This inequality implies that the operation is continuous current mode.

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3.3.2. Inductor Selection

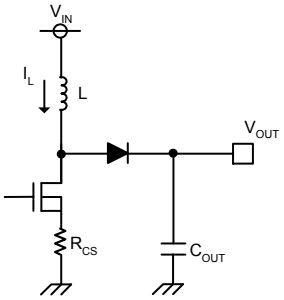
The inductor value affects the input ripple current, as shown the previous section 3.3.1.



$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]$$



Where
L: coil inductance [H] V_{OUT}: DCDC output voltage [V]
V_{IN}: input voltage [V]
I_{OUT}: output load current (the summation of LED current) [A]
I_{IN}: input current [A] f_{SW}: oscillation frequency [Hz]

Figure 26. Inductor current waveform and diagram

In continuous current mode, ⊿IL is set to 30% to 50% of the output load current in many cases.
In using smaller inductor, the boost is operated by the discontinuous current mode in which the coil current returns to zero at every period.

*The current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, results in decreasing in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.
*To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

3.3.3. Output Capacitance Cout Selection

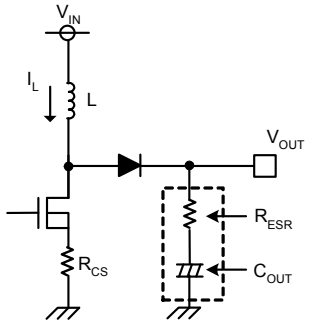


Figure 27. Output capacitor diagram

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple component is high.
Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

$$\Delta Vout = \Delta IL \times R_{ESR}[V] \quad \cdots\cdots \quad (4)$$

When the coil current is charged to the output capacitor as MOS turns off, much output ripple is caused. Much ripple voltage of the output capacitor may cause the LED current ripple.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.
*To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value transitionally in case that LED is provided with PWM dimming especially.

3.3.4. MOSFET Selection

There is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of C_{OUT} and the rectifying diode V_F. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

3.3.5. Rectifying Diode Selection

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than the tolerance voltage of C_{OUT}, and low forward voltage VF especially needs to be selected.

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3.4. Loop Compensation

A current mode DCDC converter has each one pole (phase lag) f_p due to CR filter composed of the output capacitor and the output resistance (= LED current) and zero (phase lead) f_Z by the output capacitor and the ESR of the capacitor.
Moreover, a step-up DCDC converter has RHP zero (right-half plane zero point) f_{ZRHP} which is unique with the boost converter. This zero may cause the unstable feedback. To avoid this by RHP zero, the loop compensation that the cross-over frequency f_c, set as follows, is suggested.

fc = f_{ZRHP} /5 (f_{ZRHP}: RHP zero frequency)

Considering the response speed, the calculated constant below is not always optimized completely. It needs to be adequately verified with an actual device.

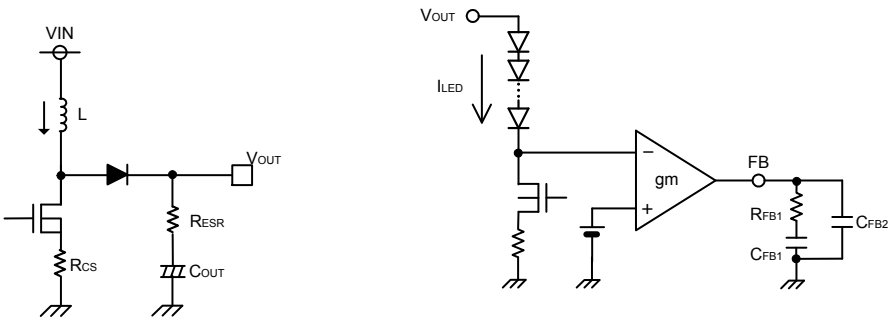


Figure 28. Output stage and error amplifier diagram

i. Calculate the pole frequency fp and the RHP zero frequency f_{ZRHP} of DC/DC converter

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Where I_{LED} = the summation of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous Current Mode)

ii. Calculate the phase compensation of the error amp output (f_c = f_{ZRHP}/5)

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega]$$

$$C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_c} = \frac{5}{2\pi \times R_{FB1} \times f_{ZRHP}} [F]$$

$$gm = 4.0 \times 10^{-4} [S]$$

Above equation is described for lighting LED without the oscillation. The value may cause much error if the quick response for the abrupt change of dimming signal is required.
To improve the transient response, R_{FB1} needs to be increased, and C_{FB1} needs to be decreased. It needs to be adequately verified with an actual device in consideration of variation from parts to parts since phase margin is decreased.

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3.5. Timing Chart
3.5.1 PWM Start up 1 (Input PWM Signal After Input STB Signal)

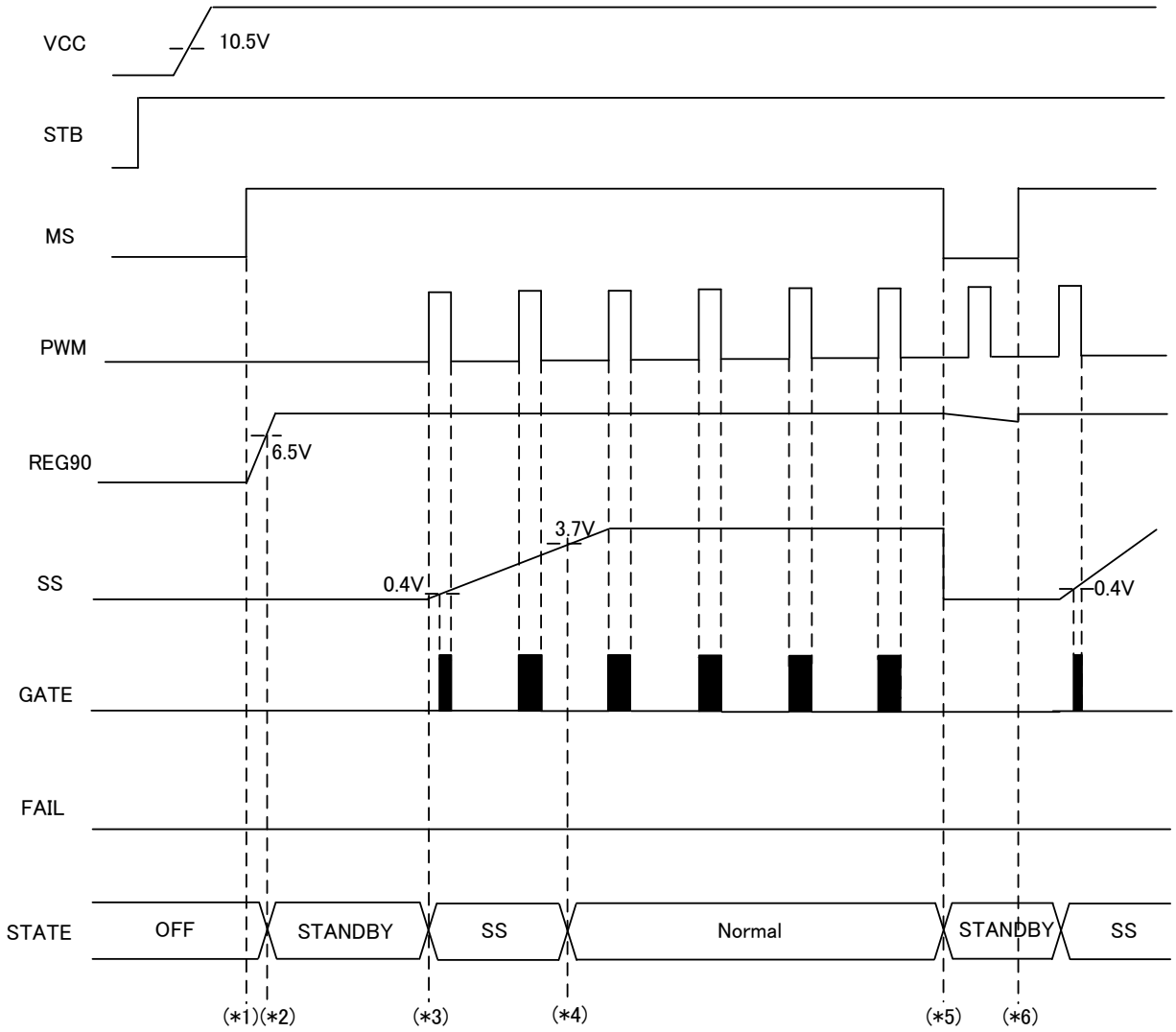


Figure 29. PWM Start up 1 (Input PWM Signal After Input STB Signal)

(*1)…REG90 starts up when STB and MS is changed from Low to High. In the state where the PWM signal is not inputted, SS terminal is not charged and DCDC doesn't start to boost, either.
(*2)…When REG90 is more than 6.5V(typ.), the reset signal is released.
(*3)…The charge of the pin SS starts at the positive edge of PWM=L to H, and the soft start starts. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*4)…The soft start interval will end if the voltage of the pin SS, Vss reaches 3.7V(typ.). By this time, it boosts V_{OUT} to the voltage where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.
(*5)…As STB or MS=L, the boost operation is stopped instantaneously. (Discharge operation continues in the state of STB=L and REGUVLO=L. Please refer to section 3.5.3)
(*6)…In this diagram, before the charge period is completed, MS is changed to High again. As MS=H again, the boost operation restarts the next PWM=H. It is the same operation as the timing of (*2). (For capacitance setting of SS terminal, please refer to the section 3.2.1.

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3.5.2 PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)

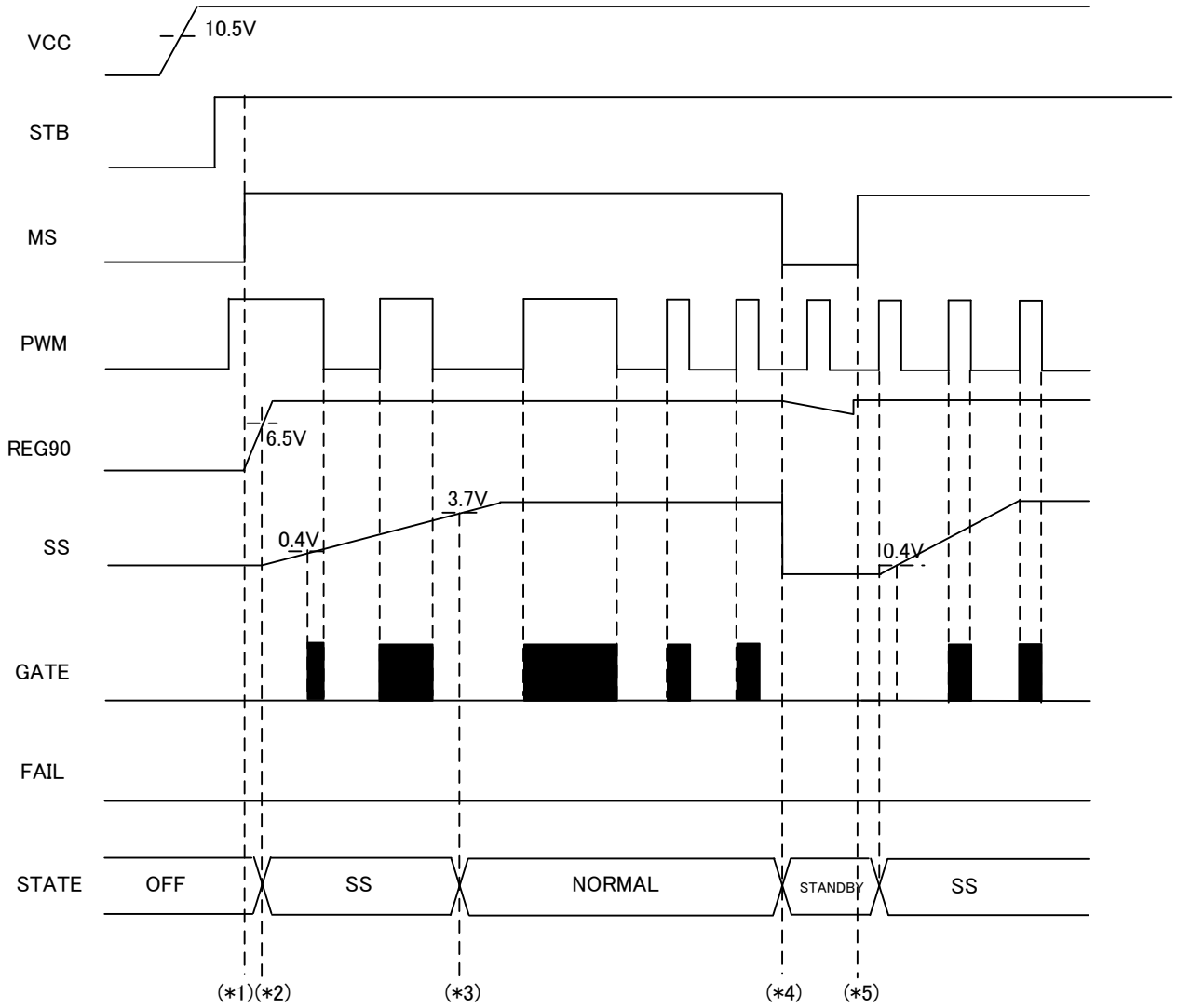


Figure 30. PWM Start Up 2 (Input STB Signal after Inputted PWM Signal)

(*1)…REG90 starts up when STB=MS=H.
(*2)…When REG90UVLO releases or PWM is inputted to the edge of PWM=L→H, SS charge starts and soft start period is started. And while the SS is less than 0.4V, the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*3)…The soft start interval will end if the voltage of the pin SS, Vss reaches 3.7V(typ.). By this time, it boosts V_{OUT} to the point where the set LED current flows. The abnormal detection of FBMAX starts to be monitored.
(*4)…As STB=L, the boost operation is stopped instantaneously (GATE=L, SS=L). (Discharge operation works in the state of STB or MS=L and REG90UVLO=H. Please refer to the section 3.5.3)
(*5)…In this diagram, before the discharge period is completed, MS is changed to High again. As MS=H again, operation will be the same as the timing of (*1).

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3.5.3 Turn Off

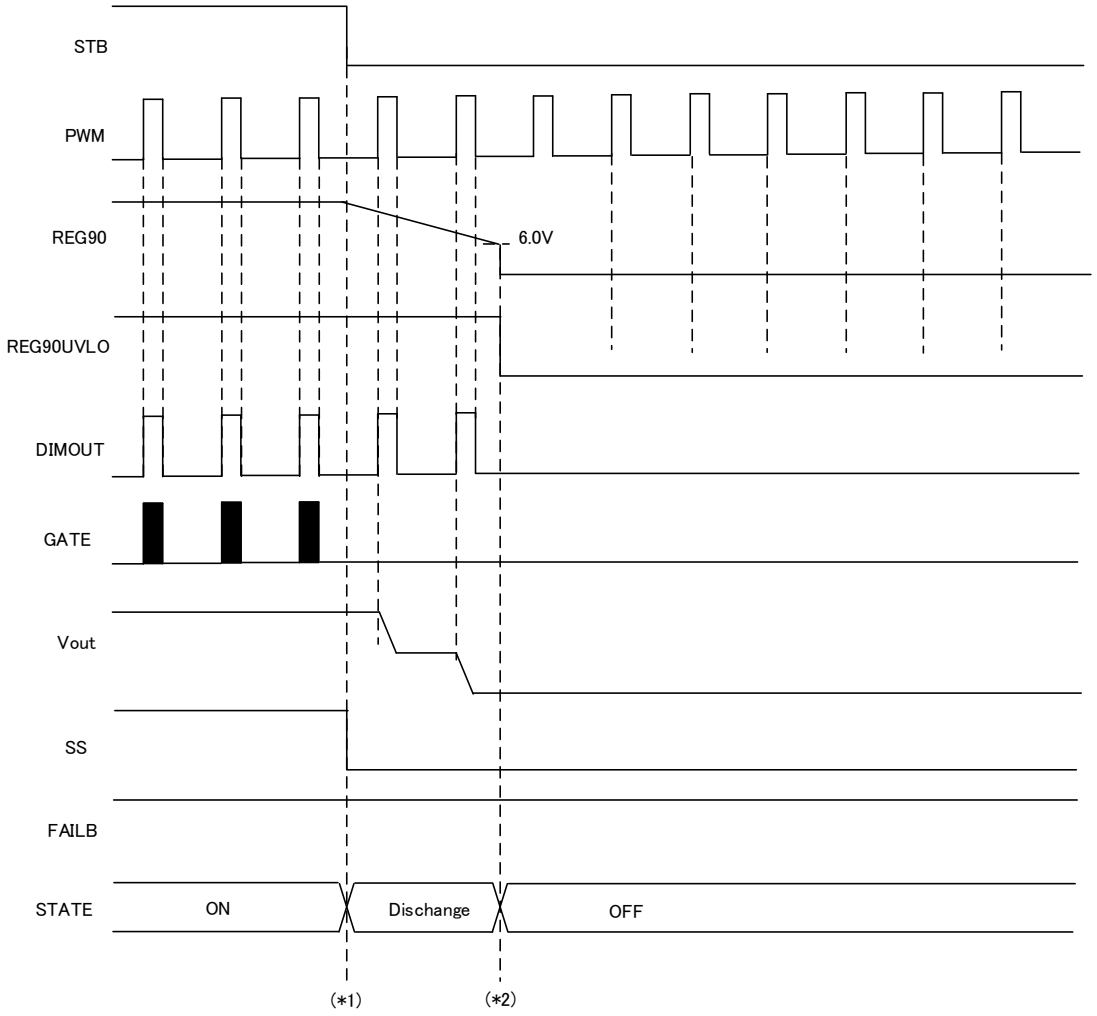


Figure 32. Turn Off

(*1)…As STB or MS=H→L, boost operation stops and REG90 starts to discharge. The discharge curve is decided by REG90 discharge resistance and the capacitor of the REG90 terminal.
(*2)…While STB or MS=L, REG90UVLO=H, DIMOUT becomes same as PWM. When REG90=9.0V is less than 6.0V(typ.), IC becomes OFF state. V_{OUT} is discharged completely until this time. It should be set to avoid a sudden brightness.

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3.5.4 Soft Start Function

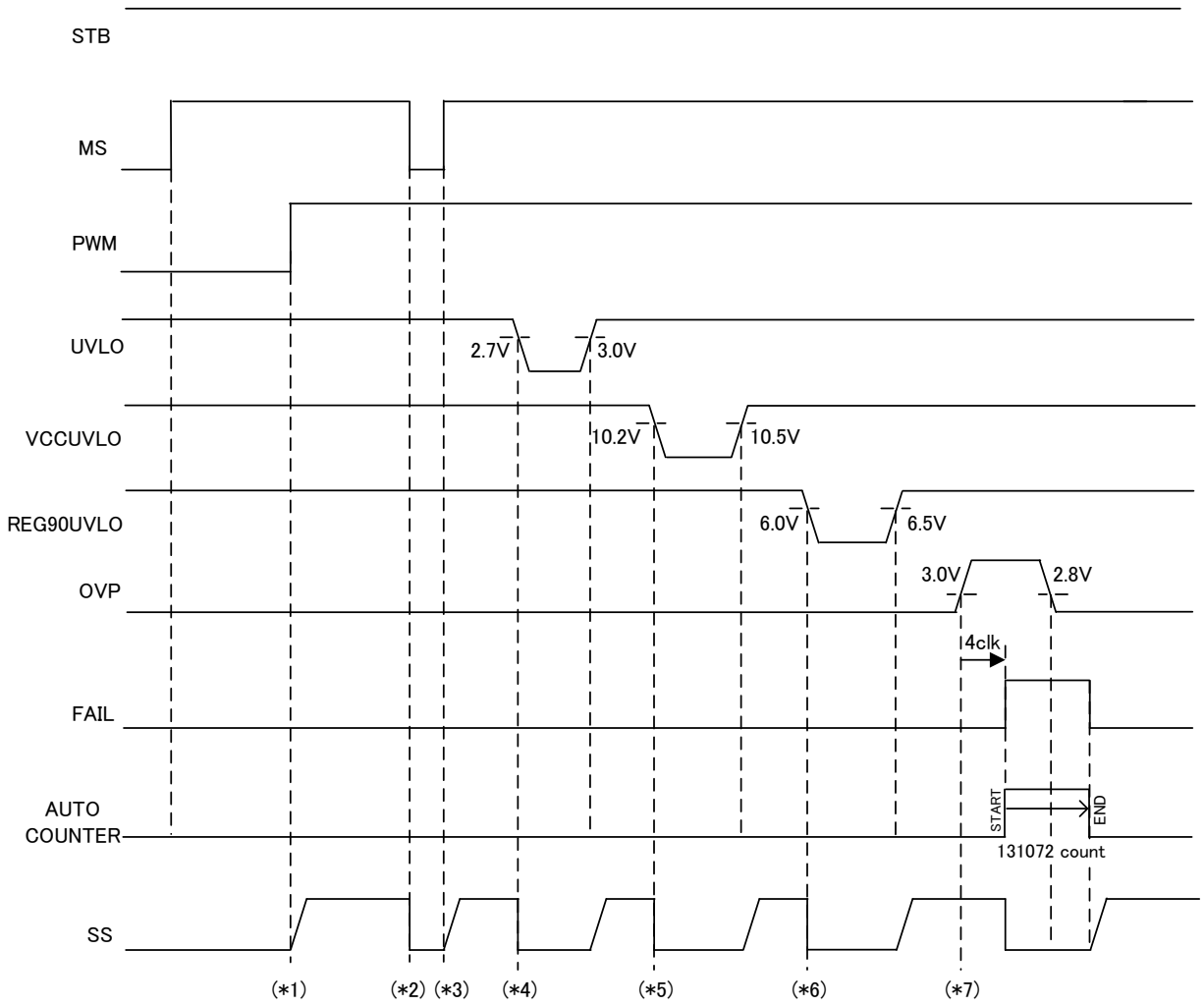


Figure 33. Soft Start Function

(*1)…The SS pin charge does not start by just STB=MS=H. PWM=H is required to start the soft start. In the low SS voltage, the GATE pin duty depends on the SS voltage. And while the SS is less than 0.4V, the pulse does not output.
(*2)…By the time STB or MS=L, the SS pin is discharged immediately.
(*3)…As the STB recovered to STB =MS=H, The SS charge starts immediately by the logic PWM=H in this chart.
(*4)…The SS pin is discharged immediately by the UVLO=L.
(*5)…The SS pin is discharged immediately by the VCCUVLO=L.
(*6)…The SS pin is discharged immediately by the REG90UVLO=L.
(*7)…The SS pin is not discharged by the abnormal detection of the latch off type such as OVP until the latch off.

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3.5.5 OVP Detection

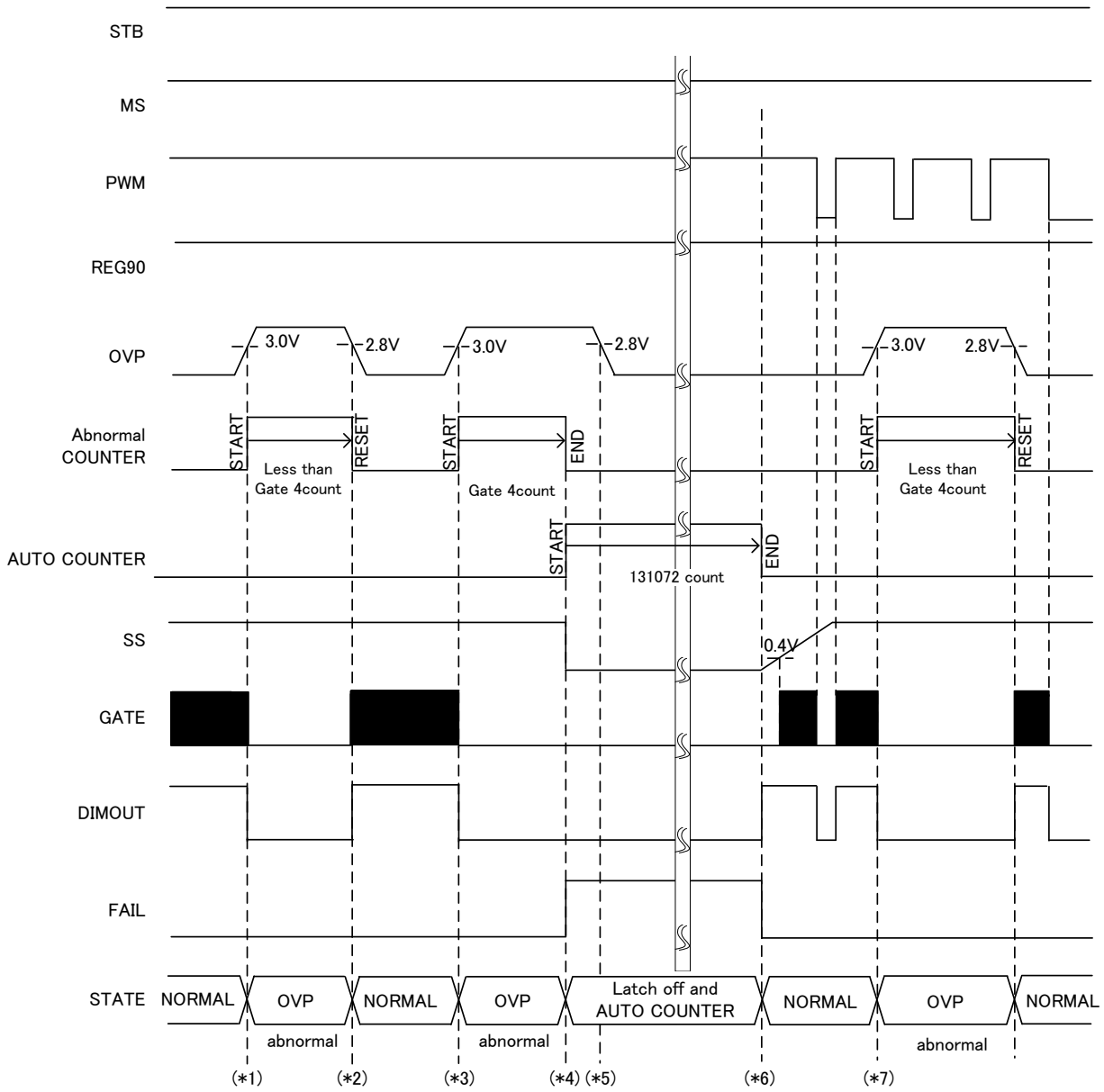


Figure 34. OVP Detection

(*1)…As OVP is detected, the output GATE=L, DIMOUT=L, and the abnormal counter starts.
(*2)…If OVP is released within 4 clocks of abnormal counter of the GATE pin frequency, the boost operation restarts.
(*3)…As the OVP is detected again, the boost operation is stopped.
(*4)…As the OVP detection continues up to 4 count by the abnormal counter, IC will be latched off. After latched off, auto counter starts counting.
(*5)… Once IC is latched off, the boost operation doesn't restart even if OVP is released.
(*6)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. The auto restart interval can be calculated by the external resistor of RT pin. (Please refer to the section 3.2.7.)
(*7)…The operation of the OVP detection is not related to the logic of PWM.

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3.5.6 FBMAX Detection

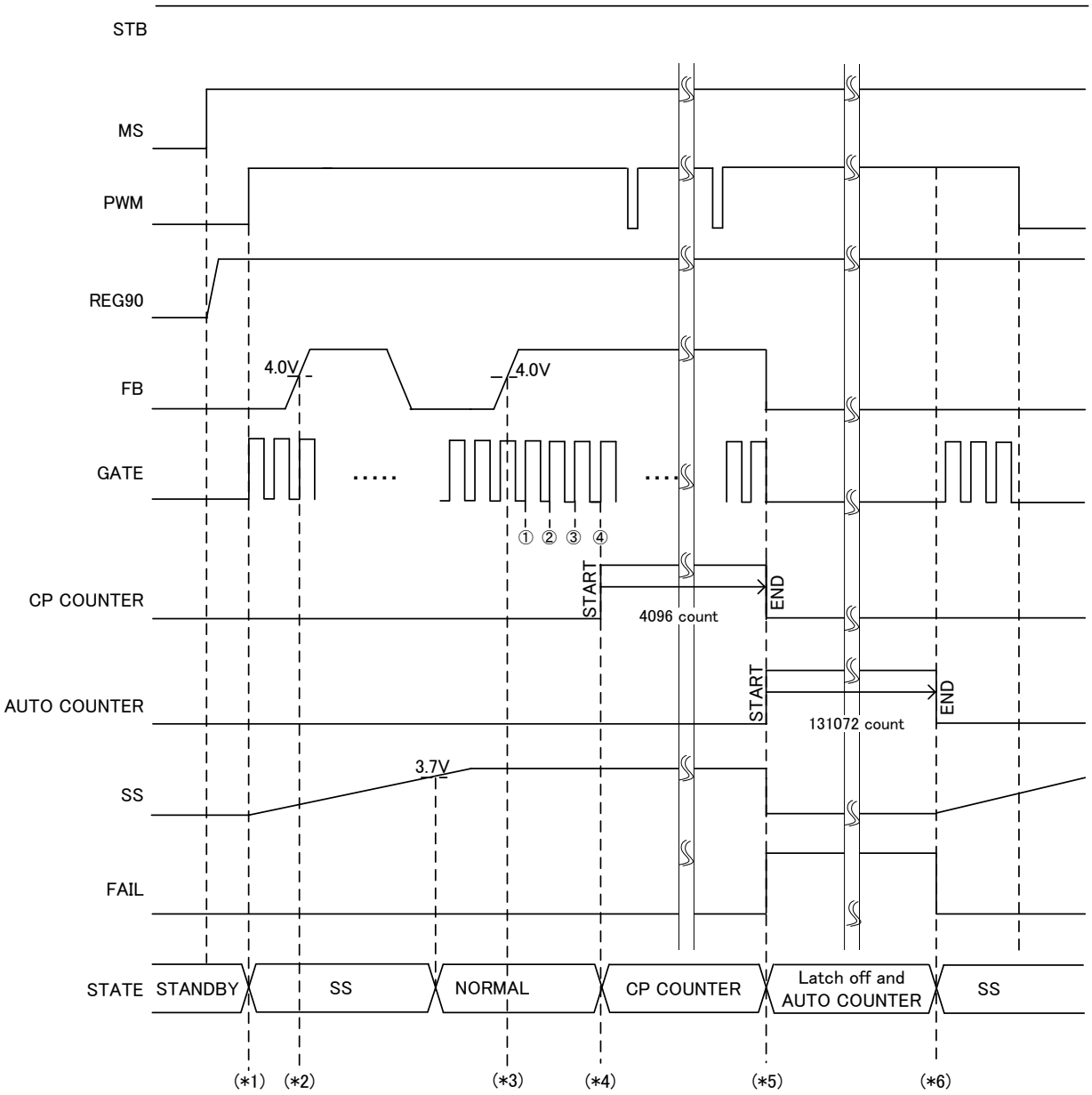


Figure 35. FBMAX Detection

(*2)…During the soft start, it is not judged to the abnormal state even if the FB=H(FB>4.0V(typ.)).
(*3)…When the PWM=H and FB=H, the abnormal counter doesn't start immediately.
(*4)…The CP counter will start if the PWM=H and the FB=H detection continues up to 4 clocks of the GATE frequency. Once the count starts, only FB level is monitored.
(*5)…When the FBMAX detection continues till the CP counter reaches 4096clk (2^{12}clk), IC will be latched off. The latch off interval can be calculated by the external resistor of RT pin. (Please refer to the section 3.2.7.)
(*6)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. The auto restart interval can be calculated by the external resistor of RT pin. (Please refer to the section 3.2.7.)

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3.5.7 LED OCP Detection

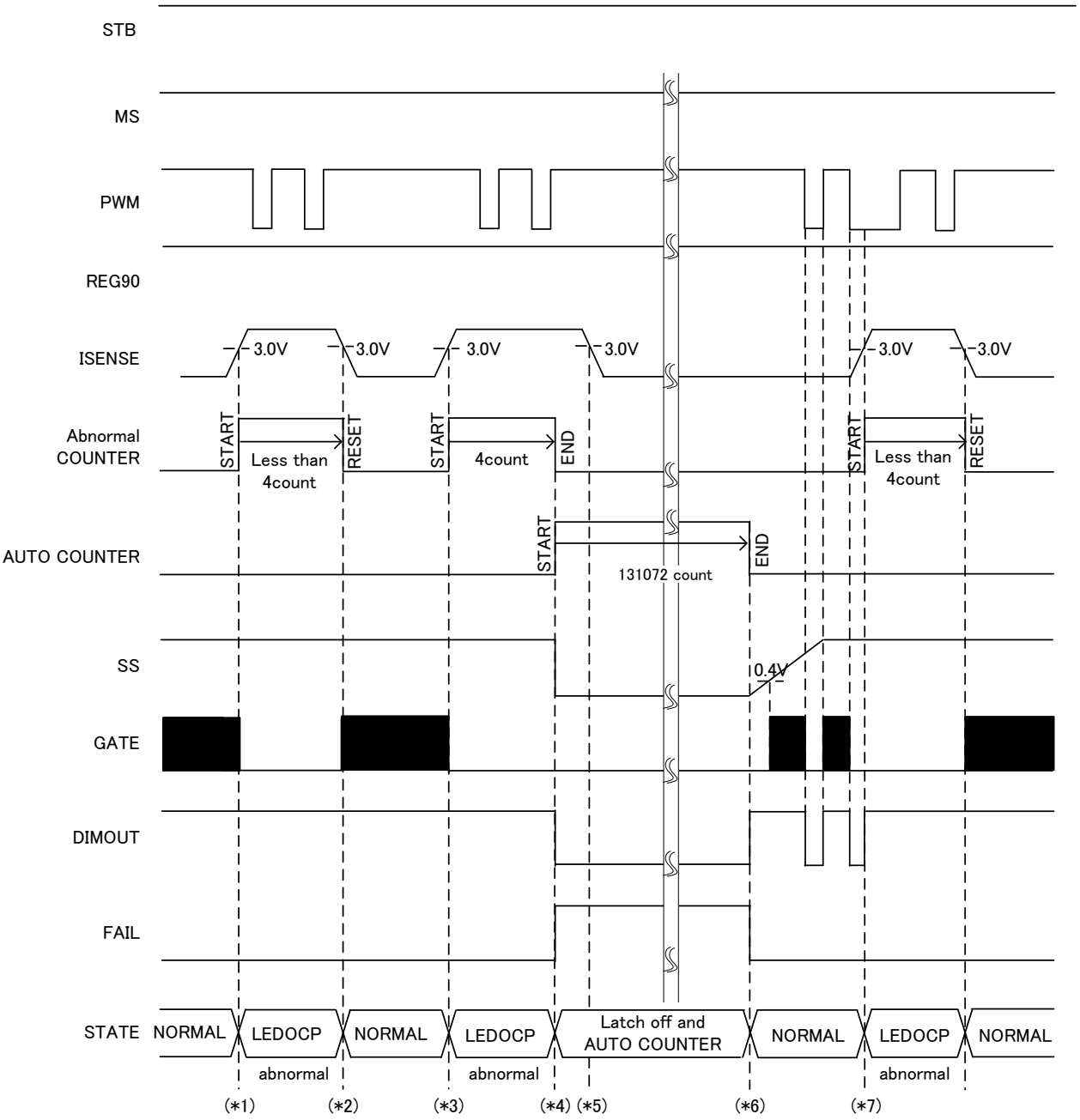


Figure 36. LED OCP Detection

(*1)…If ISENSE>3.0V(typ.), LEDOCP is detected, and GATE becomes L. To detect LEDOCP continuously, The DIMOUT is compulsorily high, regardless of the PWM dimming signal.
(*2)…When the LEDOCP releases within 4 counts of the GATE frequency, the boost operation restarts.
(*3) …As the LEDOCP is detected again, the boost operation is stopped.
(*4)…If the LEDOCP detection continues up to 4 counts of GATE frequency. IC will be latched off. After latched off, auto counter starts counting.
(*5)…Once IC is latched off, the boost operation doesn't restart even if the LEDOCP releases.
(*6)…When auto counter reaches 131072clk (2^{17}clk), IC will be auto-restarted. The auto restart interval can be calculated by the external resistor of RT pin. (Please refer to the section 3.2.7.)
(*7)…The operation of the LEDOCP detection is not related to the logic of the PWM.

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3.6 I/O Equivalent Circuits

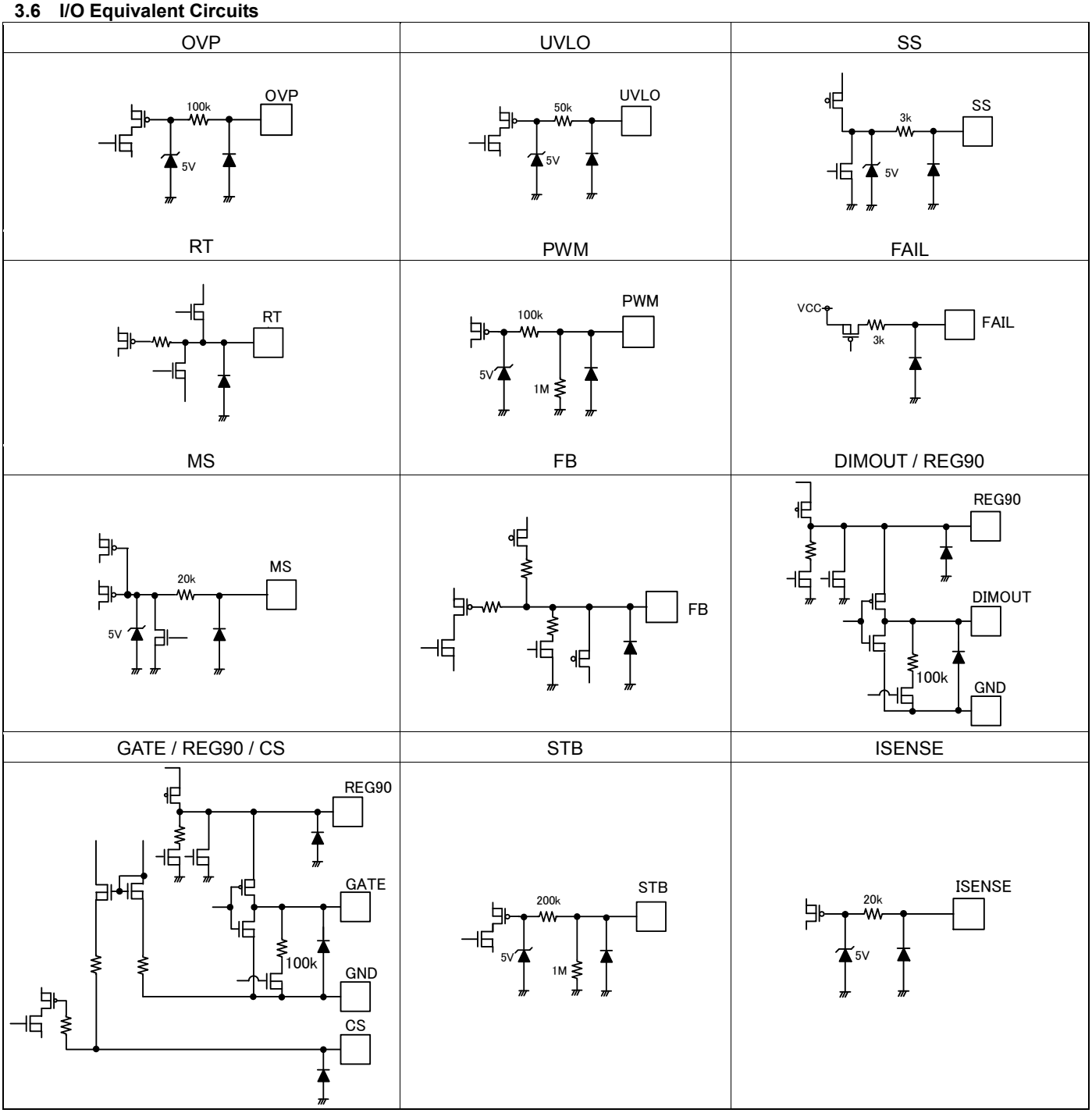


Figure 37. I/O Equivalent Circuits

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

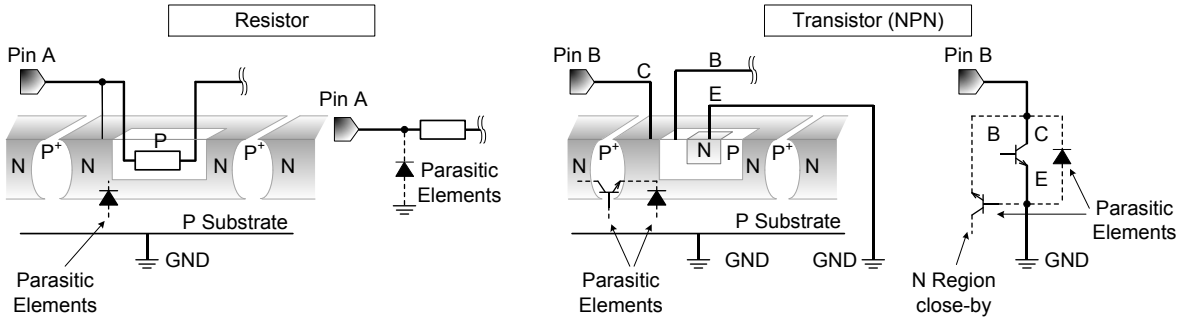


Figure 38. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

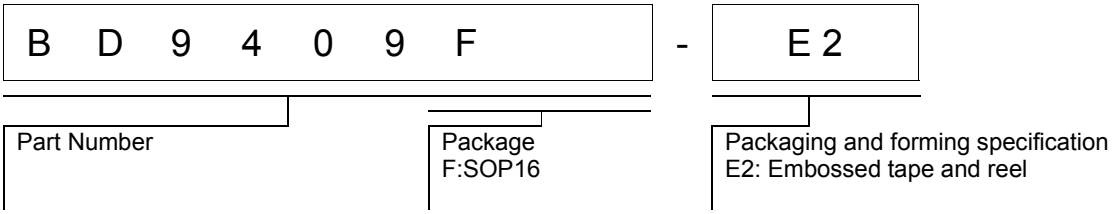
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

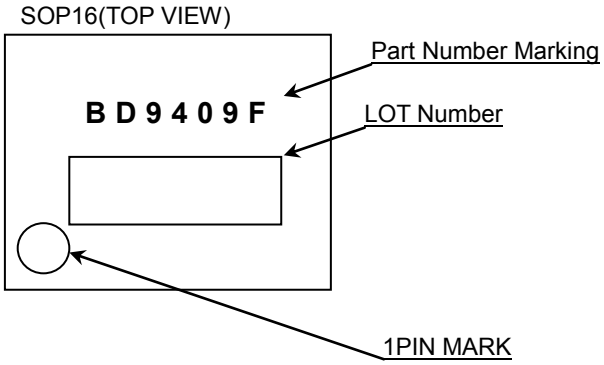
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Ordering Information



Marking Diagrams

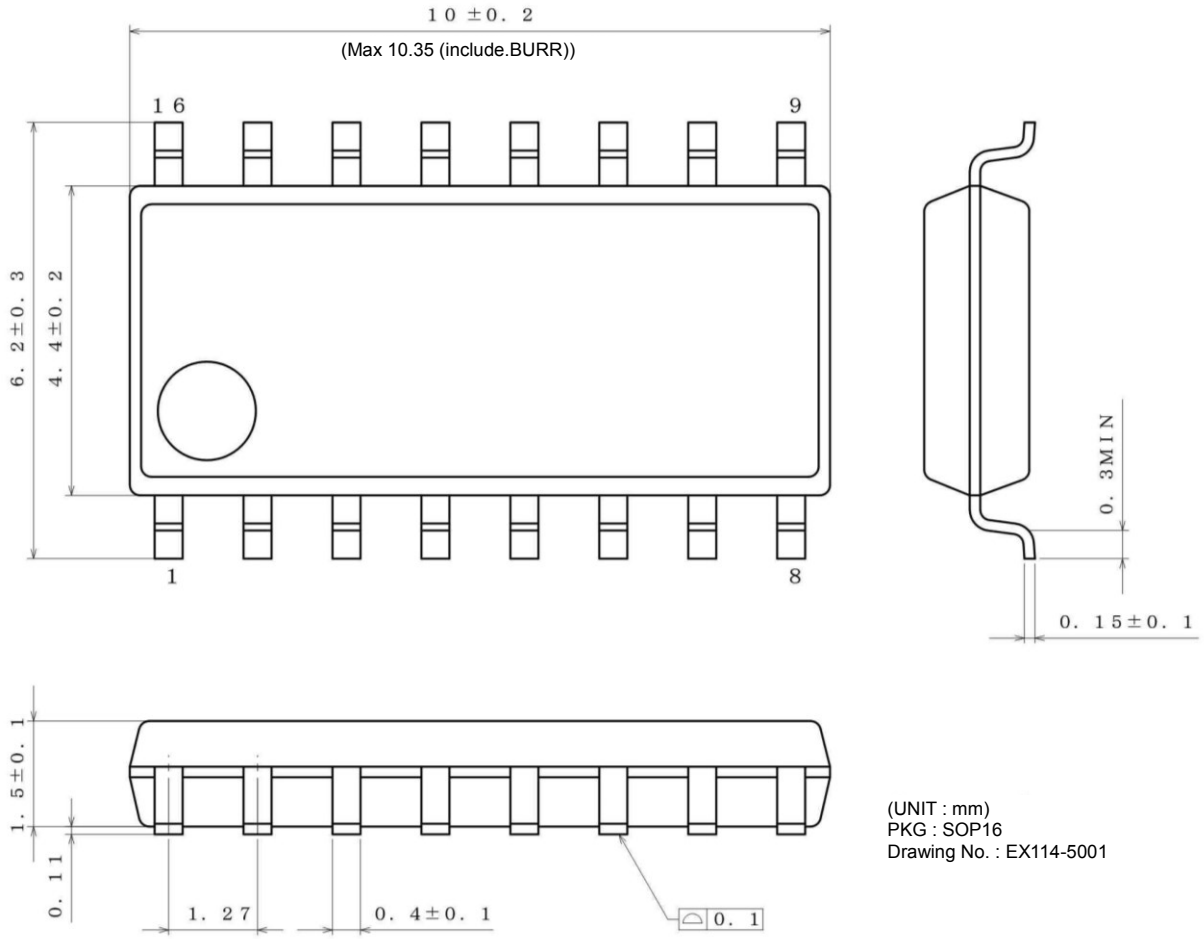


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Physical Dimension, Tape and Reel Information

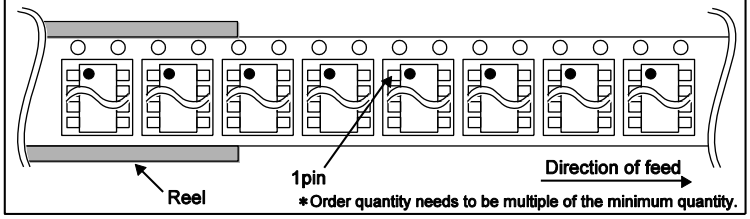
Package Name	SOP16



(UNIT : mm)
PKG : SOP16
Drawing No. : EX114-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
01 Nov 2016	Rev.001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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For details, please refer to ROHM Mounting specification

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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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