X9258

Low Noise/Low Power/2-Wire Bus/256 Taps Quad Digital Controlled Potentiometers (XDCP™)

FN8168
Rev 6.00
December 15, 2011

The X9258 integrates 4 digitally controlled potentiometers (XDCP™) on a monolithic CMOS integrated circuit.

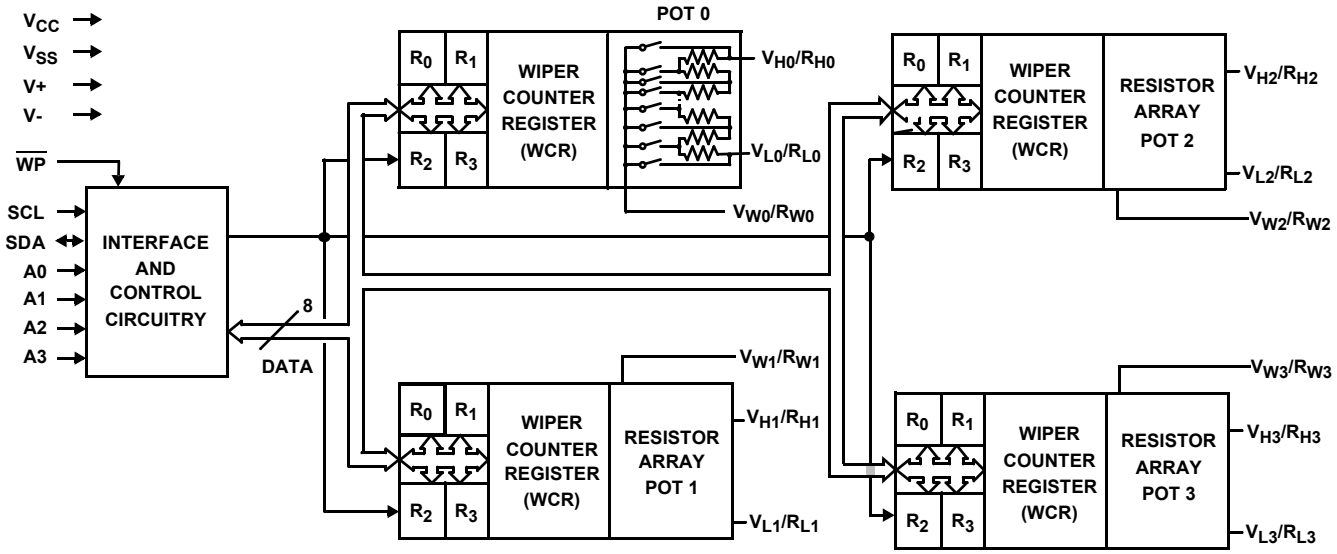
The digitally controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and 4 non-volatile Data Registers (DR0:DR3) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Power-up recalls the contents of DR0 to the WCR.

The XDCP™ can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Four potentiometers in one package
- 256 resistor taps/potentiometer..... 0.4% resolution
- 2-wire serial interface
- Wiper resistance, 40Ω typical @ V+ = 5V, V- = -5V
- Four nonvolatile data registers for each potentiometer
- Nonvolatile storage of wiper position
- Standby current <5µA max (total package)
- Power supplies
  - V_{CC} = 2.7V to 5.5V
  - V+ = 2.7V to 5.5V
  - V- = -2.7V to -5.5V
- 100kΩ, 50kΩ total potentiometer resistance
- High reliability
  - Endurance: 100,000 data changes per bit per register
  - Register data retention . . . . . 100 years
- 24 Ld SOIC, 24 Ld TSSOP
- Dual supply version of X9259
- Pb-free (RoHS compliant)

Block Diagram



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Ordering Information

PART NUMBER (Note 2)	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
X9258US24Z (Note 1)	X9258US Z	5 ±10	50	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9258US24IZ (Note 1)	X9258US ZI			-40 to +85	24 Ld SOIC (300 mil)	M24.3
X9258UV24IZ	X9258UV ZI			-40 to +85	24 Ld TSSOP (4.4mm)	MDP0044
X9258TS24Z	X9258TS Z		100	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9258TS24IZ (Note 1)	X9258TS ZI			-40 to +85	24 Ld SOIC (300 mil)	M24.3
X9258US24Z-2.7 (Note 1)	X9258US ZF	2.7 to 5.5	50	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9258US24IZ-2.7 (Note 1)	X9258US ZG			-40 to +85	24 Ld SOIC (300 mil)	M24.3
X9258UV24IZ-2.7	X9258UV ZG			-40 to +85	24 Ld TSSOP (4.4mm)	MDP0044
X9258TS24Z-2.7 (Note 1)	X9258TS ZF		100	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9258TS24IZ-2.7 (Note 1)	X9258TS ZG			-40 to +85	24 Ld SOIC (300 mil)	M24.3
X9258TV24IZ-2.7	X9258TV ZG			-40 to +85	24 Ld TSSOP (4.4mm)	MDP0044
X9258TV24Z-2.7	X9258TV ZF			0 to +70	24 Ld TSSOP (4.4mm)	MDP0044

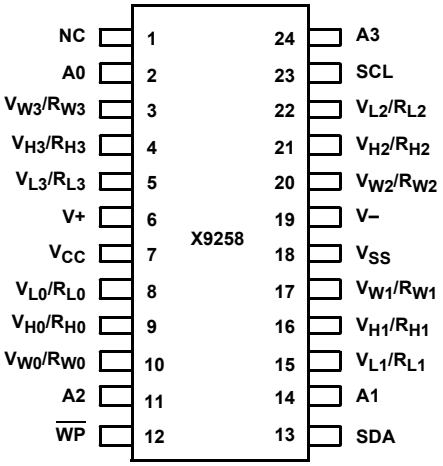
NOTES:

1. Add “T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for X9258. For more information on MSL please see tech brief TB363.

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Pinout

X9258
(24 LD SOIC, TSSOP)
TOP VIEW



Pin Descriptions

Host Interface Pins

SERIAL CLOCK (SCL)

The SCL input is used to clock data into and out of the X9258.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to “Guidelines for Calculating Typical Values of Bus Pull-Up Resistors” on page 10.

DEVICE ADDRESS (A_0 - A_3)

The Address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9258. A maximum of 16 devices may occupy the 2-wire serial bus.

Potentiometer Pins

V_H/R_H (V_{H0}/R_{H0} - V_{H3}/R_{H3}), V_L/R_L (V_{L0}/R_{L0} - V_{L3}/R_{L3})

The V_H/R_H and V_L/R_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W/R_W (V_{W0}/R_{W0} - V_{W3}/R_{W3})

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

Hardware Write Protect Input ($\overline{WP}$)

The $\overline{WP}$ pin when low prevents nonvolatile writes to the Data Registers.

Analog Supplies V+, V-

The Analog Supplies V+, V- are the supply voltages for the DCP analog section.

Pin Names

SYMBOL	DESCRIPTION
SCL	Serial Clock
SDA	Serial Data
A0 thru A3	Device Address
V_{H0}/R_{H0} thru V_{H3}/R_{H3}, V_{L0}/R_{L0} thru V_{L3}/R_{L3}	Potentiometer Pins (terminal equivalent)
V_{W0}/R_{W0} thru V_{W3}/R_{W3}	Potentiometers Pins (wiper equivalent)
$\overline{WP}$	Hardware Write Protection
V+, V-	Analog Supplies
V_{CC}	System Supply Voltage
V_{SS}	System Ground
NC	No Connection (Allowed)

Principles Of Operation

The X9258 is a highly integrated microcircuit incorporating four resistor arrays and their associated registers and counters and the serial interface logic providing direct communication between the host and the DCP potentiometers.

Serial Interface (2-Wire)

The X9258 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9258 will be considered a slave device in all applications.

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Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9258 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9258 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting 8 bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the 8 bits of data.

The X9258 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte, the X9258 will respond with a final acknowledge.

Array Description

The X9258 is comprised of four resistor arrays. Each array contains 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H/R_H and V_L/R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (V_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The 8 bits of the WCR are decoded to select, and enable, one of 256 switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant 4 bits of the slave address are the device type identifier (refer to Figure 1). For the X9258 this is fixed as 0101[B].

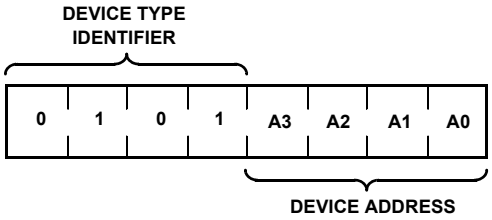


FIGURE 1. SLAVE ADDRESS

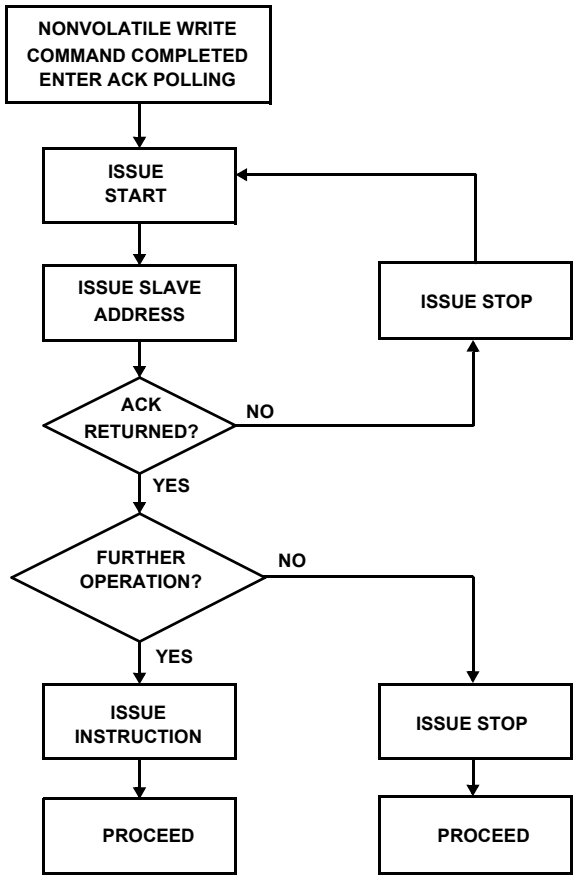
The next 4 bits of the slave address are the device address. The physical device address is defined by the state of the A0 thru A3 inputs. The X9258 compares the serial data stream with the address input state; a successful compare of all 4 address bits is required for the X9258 to respond with an acknowledge. The A_0 thru A_3 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Acknowledge Polling

The disabling of the inputs (during the internal nonvolatile write operation), can be used to take advantage of the typical 5ms nonvolatile write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command, the X9258 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9258 is still busy with the write operation, no ACK will be returned. If the X9258 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

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ACK Polling Sequence



Instruction Structure

The next byte sent to the X9258 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the two potentiometers and when applicable they point to one of four associated registers. The format is shown in Figure 2.

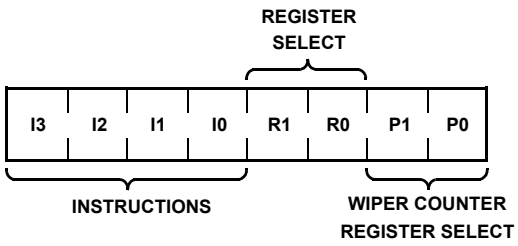


FIGURE 2. INSTRUCTION BYTE FORMAT

The four high order bits define the instruction. The next 2 bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last bits (P1, P0) select which one of the four potentiometers is to be affected by the instruction.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the Wiper Counter Register and one of the data registers. A transfer from a Data Register to a Wiper Counter Register is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{WRL}. A transfer from the Wiper Counter Register (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9258; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are: Read Wiper Counter Register (read the current wiper position of the selected potentiometer), Write Wiper Counter Register (change current wiper position of the selected potentiometer), Read Data Register (read the contents of the selected nonvolatile register) and Write Data Register (write a new value to the selected data register). The sequence of operations is shown in Figure 4.

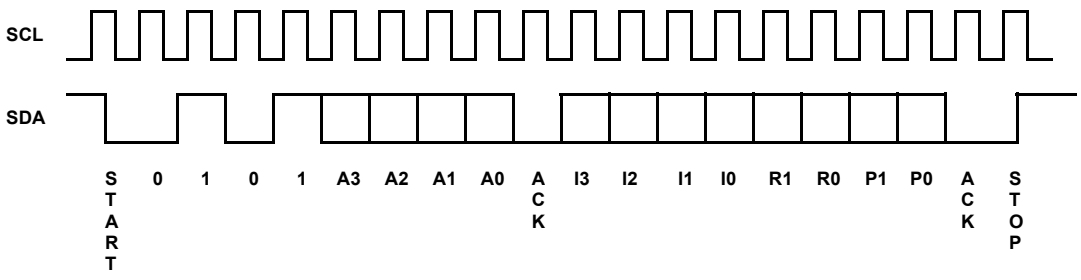


FIGURE 3. TWO-BYTE INSTRUCTION SEQUENCE

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The Increment/Decrement command is different from the other commands. Once the command is issued and the X9258 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H terminal.

Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L/R_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

TABLE 1. INSTRUCTION SET

INSTRUCTION	INSTRUCTION SET								OPERATION
	I_3	I_2	I_1	I_0	R_1	R_0	P_1	P_0	
Read Wiper Counter Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Counter Register pointed to by P_1 - P_0
Write Wiper Counter Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Counter Register pointed to by P_1 - P_0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P_1 - P_0 and R_1 - R_0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P_1 - P_0 and R_1 - R_0
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P_1 - P_0 and R_1 - R_0 to its associated Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Counter Register pointed to by P_1 - P_0 to the Data Register pointed to by R_1 - R_0
Global XFR Data Registers to Wiper Counter Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by R_1 - R_0 of all four potentiometers to their respective Wiper Counter Registers
Global XFR Wiper Counter Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by R_1 - R_0 of all four potentiometers
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P_1 - P_0

NOTE:

4. 1/0 = data is one or zero.

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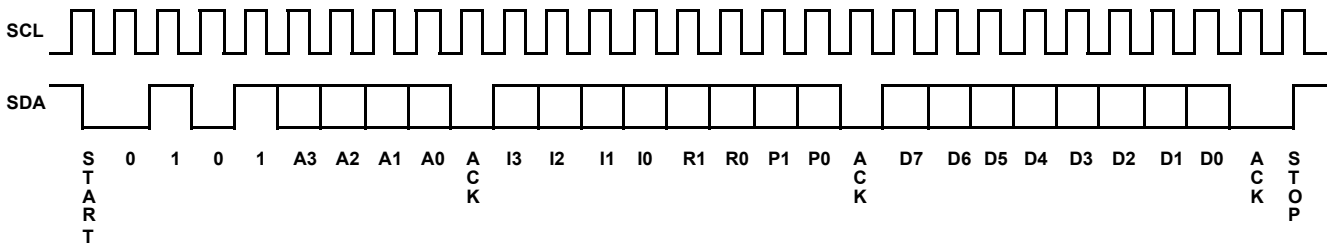


FIGURE 4. THREE-BYTE INSTRUCTION SEQUENCE

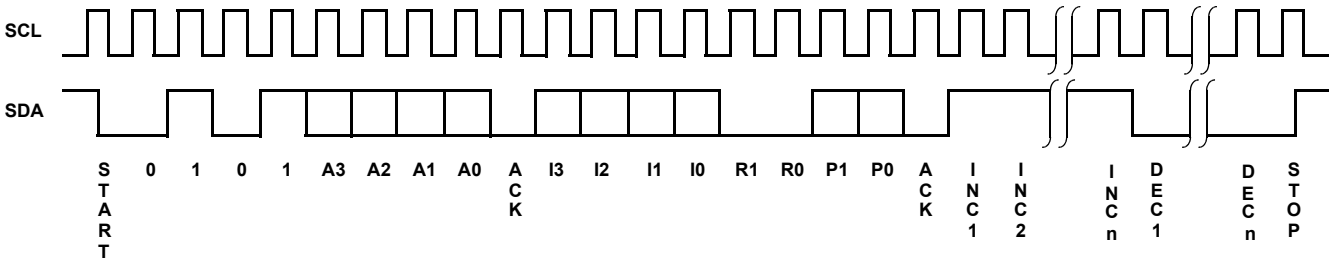


FIGURE 5. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

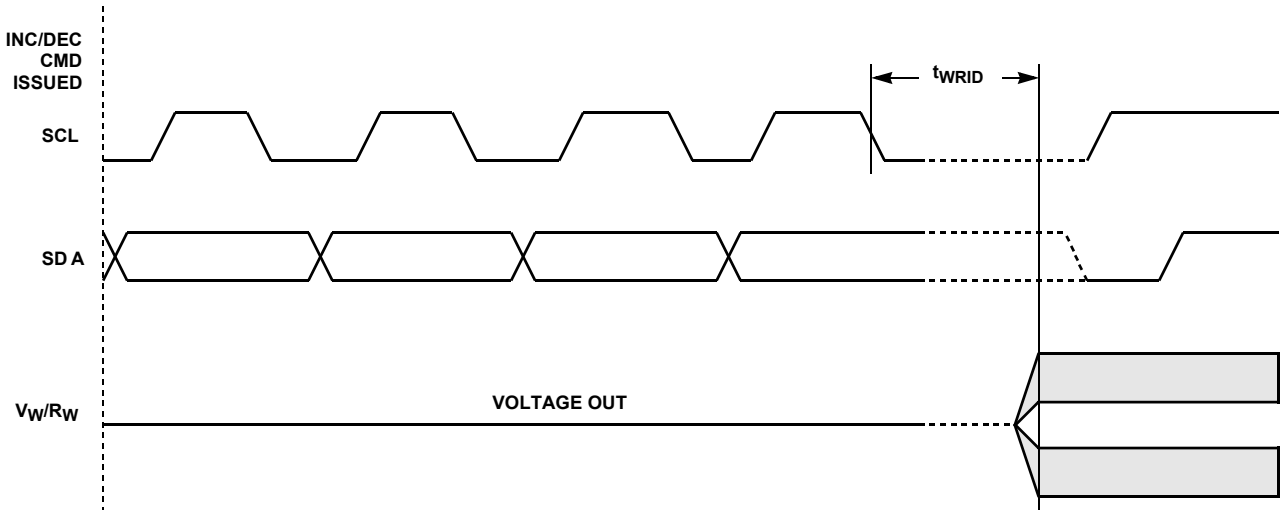


FIGURE 6. INCREMENT/DECREMENT TIMING LIMITS

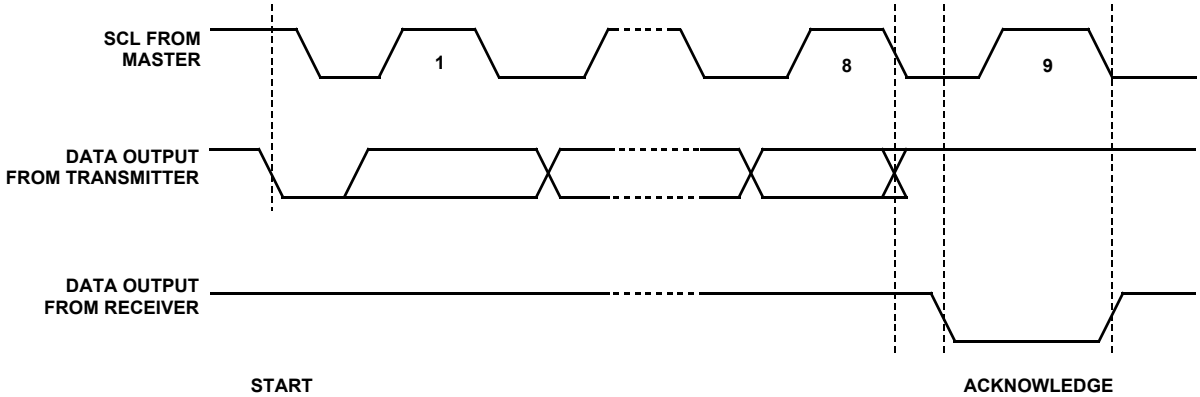


FIGURE 7. ACKNOWLEDGE RESPONSE FROM RECEIVER

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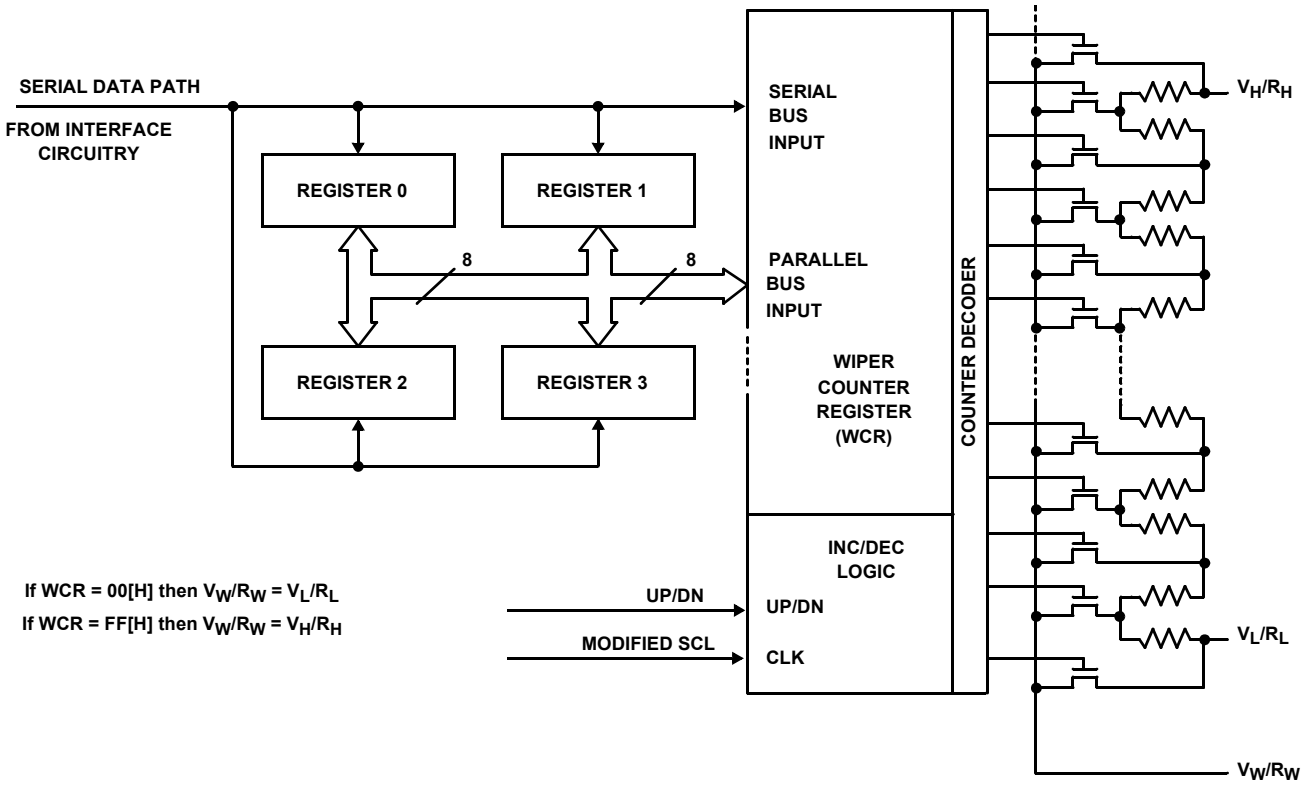


FIGURE 8. DETAILED POTENTIOMETER BLOCK DIAGRAM DETAILED OPERATION

All DCP potentiometers share the serial interface and share a common architecture. Each potentiometer has a Wiper Counter Register and four Data Registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9258 contains four Wiper Counter Registers, one for each DCP potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways:

1. Written directly by the host via the Write Wiper Counter Register instruction (serial load)
2. Written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction (parallel load)
3. Can be modified one step at a time by the Increment/Decrement instruction.
4. Loaded with the contents of its data register zero (R0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9258 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

Each potentiometer has four nonvolatile Data Registers. These can be read or written directly by the host and data can be transferred between any of the four Data Registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

Register Descriptions

Data Registers, (8-bit), Nonvolatile

WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0
NV	NV	NV	NV	NV	NV	NV	NV
(MSB)							(LSB)

Four 8-bit Data Registers for each DCP (sixteen 8-bit registers in total).

{D7~D0}: These bits are for general purpose not volatile data storage or for storage of up to four different wiper values. The contents of Data Register 0 are automatically moved to the wiper counter register on power-up.

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Wiper Counter Register, (8-bit), Volatile

WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0
V	V	V	V	V	V	V	V
(MSB)							(LSB)

One 8-bit Wiper Counter Register for each DCP (four 8-bit registers in total.)

{D7~D0}: These bits specify the wiper position of the respective DCP. The Wiper Counter Register is loaded on power-up by the value in Data Register 0. The contents of the WCR can be loaded from any of the other Data Register or directly. The contents of the WCR can be saved in a DR.

Instruction Format

NOTES:

5. “MACK”/”SACK”: stands for the acknowledge sent by the master/slave.
6. “A3 ~ A0”: stands for the device addresses sent by the master.
7. “X”: indicates that it is a “0” for testing purpose but physically it is a “don’t care” condition.
8. “I”: stands for the increment operation, SDA held high during active SCL phase (high).
9. “D”: stands for the decrement operation, SDA held low during active SCL phase (high).

Read Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				WCR ADDRESSES				S A C K	WIPER POSITION (SENT BY SLAVE ON SDA)								M A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	0	1	0	0	P1	P0		WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0		

Write Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				WCR ADDRESSES				S A C K	DATA BYTE (SENT BY MASTER ON SDA)								S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	0	0	0	P1	P0		WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0		

Read Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	DATA BYTE (SENT BY SLAVE ON SDA)								M A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	1	R1	R0	P1	P0		WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0		

Write Data Register (WR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	DATA BYTE (SENT BY MASTER ON SDA)								S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	1	0	0	R1	R0	P1	P0		WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0			

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XFR Data Register (DR) to Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	1	0	1	R1	R0	P1	P0		

XFR Wiper Counter Register (WCR) to Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR AND WCR ADDRESSES				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	1	1	0	R1	R0	P1	P0			

Increment/Decrement Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				WCR ADDRESSES				S A C K	INCREMENT/DECREMENT (SENT BY MASTER ON SDA)								S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	1	0	0	0	P1	P0		I/D	I/D	.	.	.	.	I/D	I/D	

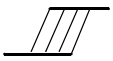
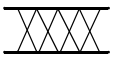
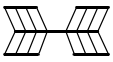
Global XFR Data Register (DR) to Wiper Counter Register (WCR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR ADDRESSES				S A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	0	1	R1	R0	0	0		

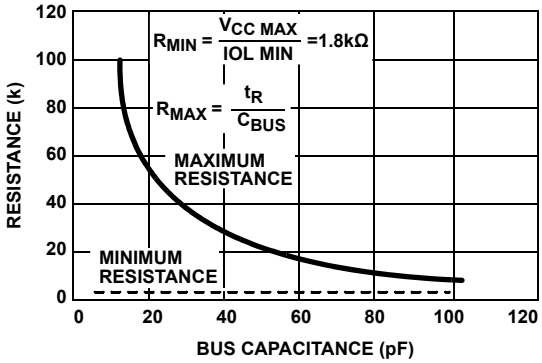
Global XFR Wiper Counter Register (WCR) to Data Register (DR)

S T A R T	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S A C K	INSTRUCTION OPCODE				DR ADDRESSES				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A3	A2	A1	A0		1	0	0	0	R1	R0	0	0			

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



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Absolute Maximum Ratings

Voltage on SDA, SCL or any Address Input with Respect to V_{SS} . . . . . -1V to +7V
Voltage on V+ (referenced to V_{SS}) 10V
Voltage on V- (referenced to V_{SS}) . . . . . -10V
(V+) - (V-) 12V
Any V_H/R_H . . . . . .V+
Any V_L/R_L . . . . . V-
I_W (10s) . . . . . ±15mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Lead SOIC (Notes 10, 11)	46	21
24 Lead TSSOP (Notes 10, 11)	68	17

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range (Typical)
X9258 . . . . . .5V ±10%
X9258-2.7 . . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

10. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
11. For θ_{JC}, the “case temp” location is taken at the package top center.

Analog Specifications

Over recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNIT
	End-to-end Resistance Tolerance					±20	%
	Power Rating		+25°C, each potentiometer			50	mW
I_W	Wiper Current		Wiper current = ±1mA			±7.5	mA
R_W	Wiper Resistance		I_W = ± 1mA @ V+ = 3V, V- = -3V		150	250	Ω
R_W	Wiper Resistance		I_W = ± 1mA @ V+ = 5V, V- = -5V		40	100	Ω
V+	Voltage on V+ Pin	X9258		+4.5		+5.5	V
		X9258-2.7		+2.7		+5.5	V
V-	Voltage on V- Pin	X9258		-5.5		-4.5	V
		X9258 -2.7		-5.5		-2.7	V
V_{TERM}	Voltage on any V_H/R_H or V_L/R_L Pin			V-		V+	V
	Noise		Ref: 1kHz		-120		dBV
	Resolution (Note 16)				0.6		%
	Absolute Linearity (Note 13)		$V_{w(n)(actual)} - V_{w(n)(expected)}$			±1	MI (Note 15)
	Relative Linearity (Note 14)		$V_{w(n+1)} - [V_{w(n)} + MI]$			±0.6	MI (Note 15)
	Temperature Coefficient of R_{TOTAL}				±300		ppm/°C
	Ratiometric Temperature Coefficient					±20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitance		See “Test Circuit #3 SPICE Macro Model” on page 13		10/10/25		pF

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DC Operating Characteristics

Over recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 12)	TYP	MAX (Note 12)	UNIT
I_{CC1}	V_{CC} Supply Current (Nonvolatile Write)	f_{SCL} = 400kHz, SDA = Open, Other Inputs = V_{SS}		1		mA
I_{CC2}	V_{CC} Supply Current (Move Wiper, Write, Read)	f_{SCL} = 400kHz, SDA = Open, Other Inputs = V_{SS}			100	µA
I_{SB}	V_{CC} Current (Standby)	SCL = SDA = V_{CC}, Addr. = V_{SS}			5	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}			10	µA
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 0.1	V
V_{IL}	Input LOW Voltage		-0.5		V_{CC} x 0.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			0.4	V

NOTES:

12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
13. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
14. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
15. MI = R_TO_T/255 or (V_H/R_H—V_L/R_L)/255, single potentiometer.
16. Max = all four arrays cascaded together; typical = individual array resolutions.

Endurance and Data Retention

PARAMETER	MIN (Note 12)	UNIT
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	years

Capacitance

SYMBOL	PARAMETER	TEST CONDITIONS	MAX (Note 12)	UNIT
$C_{I/O}$ (Note 17)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 17)	Input Capacitance (A0, A1, A2, A3, and SCL)	V_{IN} = 0V	6	pF

Power-Up Timing

SYMBOL	PARAMETER	MIN (Note 12)	MAX (Note 12)	UNIT
t_{PUR} (Note 18)	Power-up to Initiation of Read Operation		1	ms
t_{PUW} (Note 18)	Power-up to Initiation of Write Operation		5	ms
t_R V_{CC} (Note 19)	V_{CC} Power-up Ramp	0.2	50	V/ms

NOTES:

17. This parameter is periodically sampled and not 100% tested.
18. t_{PUR} and t_{PUW} are the delays required from the time the third (last) power supply (V_{CC}, V+ or V-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.
19. Sample tested only.

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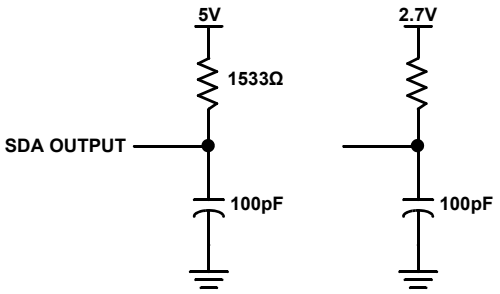
Power-Up and Power-Down Requirement

The are no restrictions on the sequencing of the bias supplies V_{CC}, V+, and V- provided that all three supplies reach their final values within 1ms of each other. At all times, the voltages on the potentiometer pins must be less than V+ and more than V-. The recall of the wiper position from nonvolatile memory is not in effect until all supplies reach their final value. The V_{CC} ramp rate specification is always in effect.

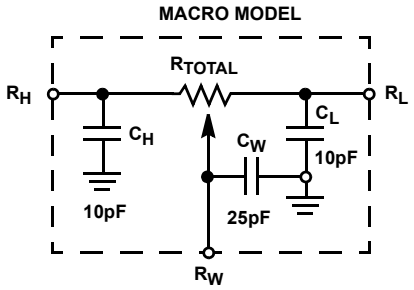
AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

Equivalent AC Load Circuit



Test Circuit #3 SPICE Macro Model



AC Timing Over recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	MIN (Note 12)	MAX (Note 12)	UNIT
f_{SCL}	Clock Frequency		400	kHz
t_{CYC}	Clock Cycle Time	2500		ns
t_{HIGH}	Clock High Time	600		ns
t_{LOW}	Clock Low Time	1300		ns
$t_{SU:STA}$	Start Setup Time	600		ns
$t_{HD:STA}$	Start Hold Time	600		ns
$t_{SU:STO}$	Stop Setup Time	600		ns
$t_{SU:DAT}$	SDA Data Input Setup Time	100		ns
$t_{HD:DAT}$	SDA Data Input Hold Time	30		ns
t_R	SCL and SDA Rise Time (Note 20)		300	ns
t_F	SCL and SDA Fall Time (Note 20)		300	ns
t_{AA}	SCL Low to SDA Data Output Valid Time		900	ns
t_{DH}	SDA Data Output Hold Time	50		ns
T_I	Noise Suppression Time Constant at SCL and SDA Inputs	50		ns
t_{BUF}	Bus Free Time (Prior to any Transmission)	1300		ns
$t_{SU:WPA}$	$\overline{WP}$, A0, A1, A2 and A3 Setup Time	0		ns
$t_{HD:WPA}$	$\overline{WP}$, A0, A1, A2 and A3 Hold Time	0		ns

NOTE:

20. A device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

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High-Voltage Write Cycle Timing

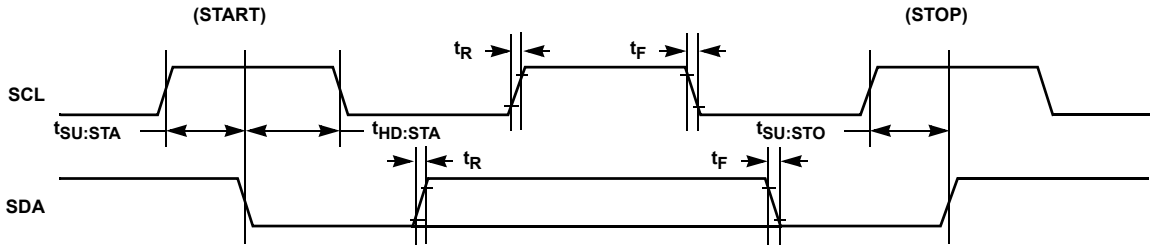
SYMBOL	PARAMETER	TYP	MAX (Note 12)	UNIT
t_{WR}	High-Voltage Write Cycle Time (Store Instructions)	5	10	ms

DCP Timing

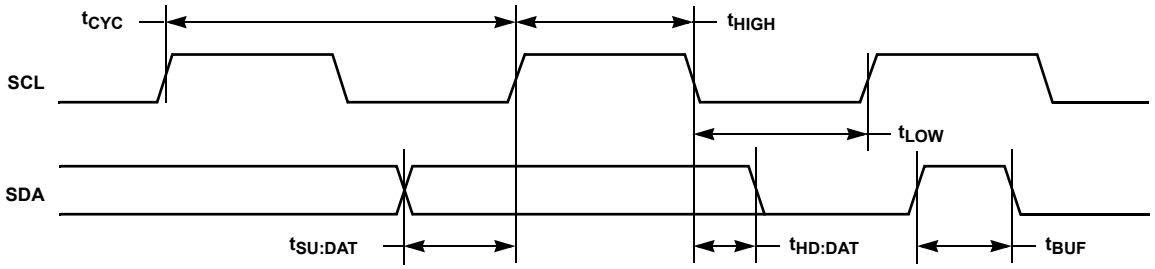
SYMBOL	PARAMETER	MIN (Note 12)	MAX (Note 12)	UNIT
t_{WRPO}	Wiper Response Time After the Third (Last) Power Supply is Stable		10	µs
t_{WRL}	Wiper Response Time After Instruction Issued (All Load Instructions)		10	µs
t_{WRID}	Wiper Response Time from an Active SCL/SCK Edge (Increment/Decrement Instruction)		10	µs

Timing Diagrams 2-Wire Interface

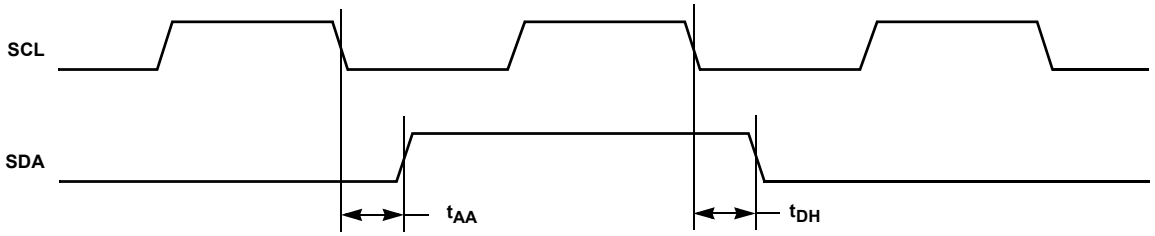
Start and Stop Timing



Input Timing

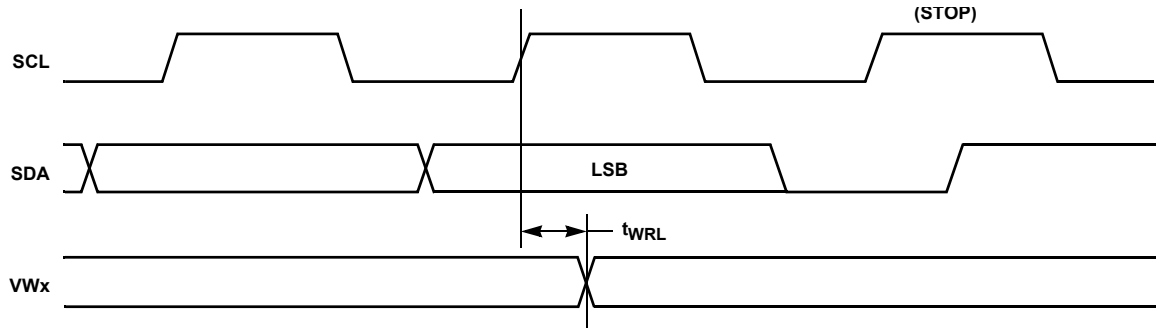


Output Timing

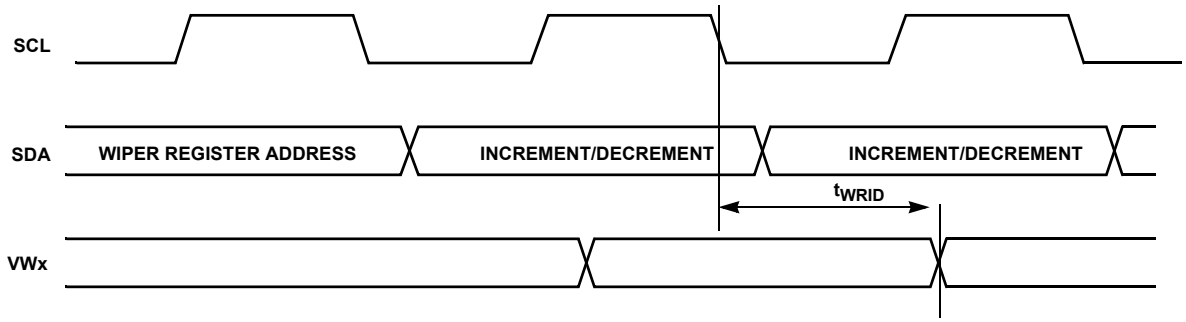


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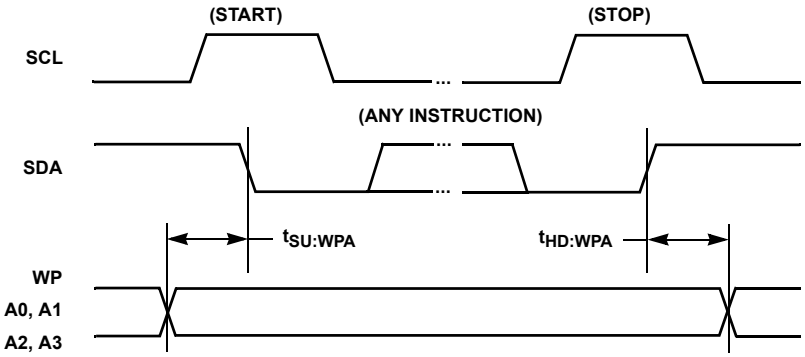
DCP Timing (for All Load Instructions)



DCP Timing (for Increment/Decrement Instruction)



Write Protect and Device Address Pins Timing



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Applications information

Basic Configurations of Electronic Potentiometers

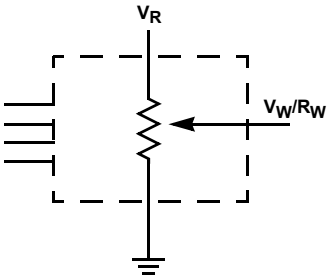


FIGURE 9. THREE TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER

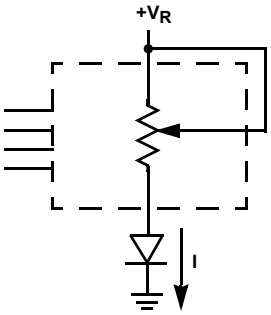


FIGURE 10. TWO-TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

Application Circuits

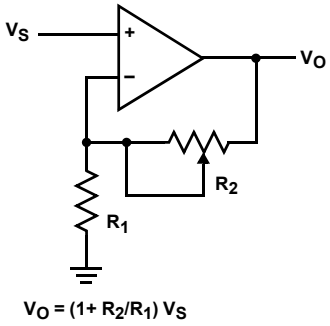


FIGURE 11. NON-INVERTING AMPLIFIER

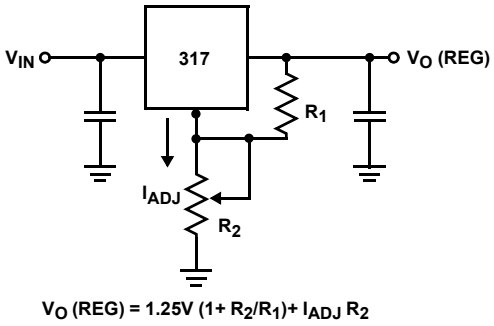


FIGURE 12. VOLTAGE REGULATOR

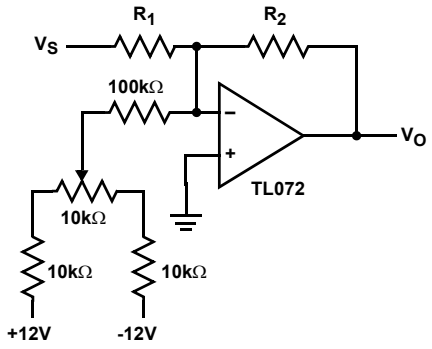


FIGURE 13. OFFSET VOLTAGE ADJUSTMENT

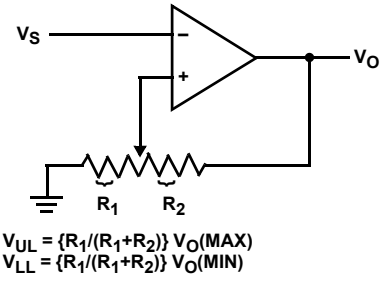
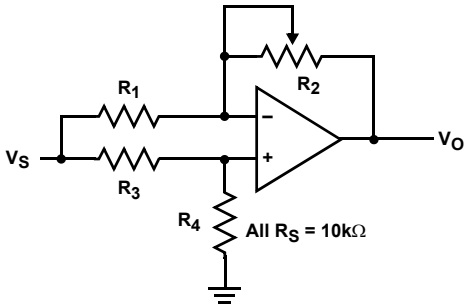


FIGURE 14. COMPARATOR WITH HYSTERESIS

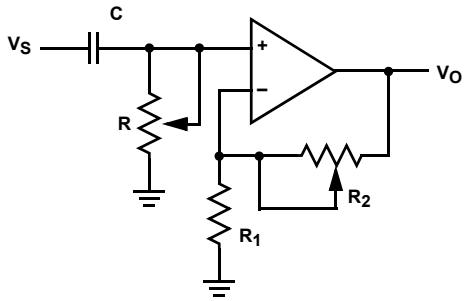
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Application Circuits (Continued)



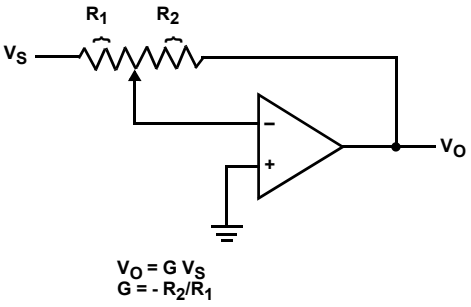
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

FIGURE 15. ATTENUATOR



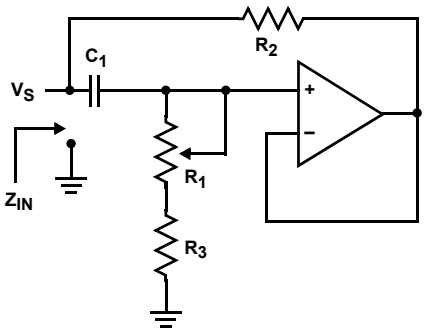
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

FIGURE 16. FILTER



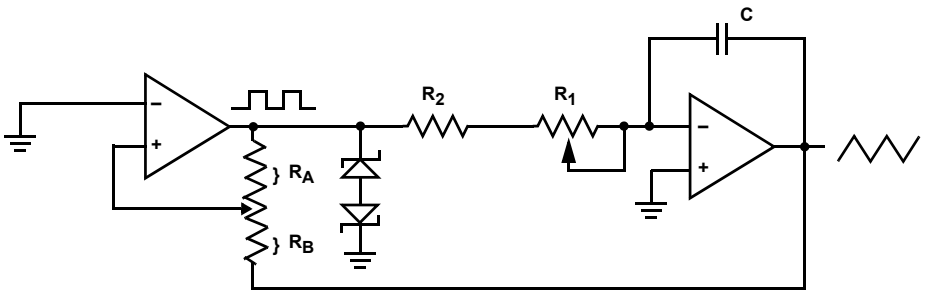
$V_O = G\ V_S$
$G = -R_2/R_1$

FIGURE 17. INVERTING AMPLIFIER



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

FIGURE 18. EQUIVALENT L-R CIRCUIT

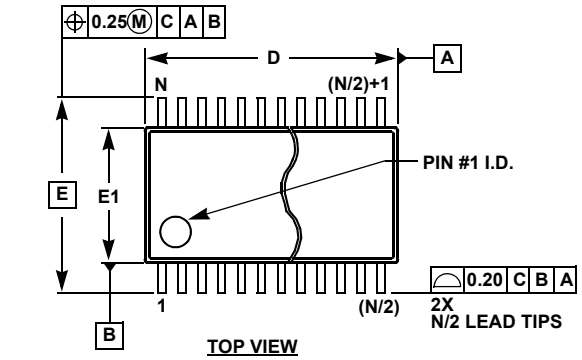


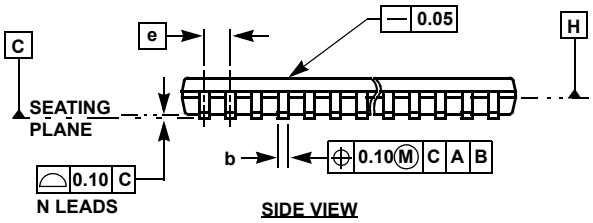
FREQUENCY ∝ R_1, R_2, C
AMPLITUDE ∝ R_A, R_B

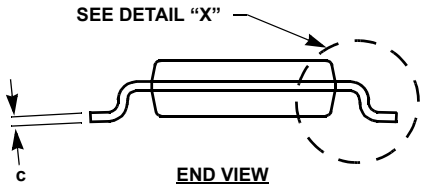
FIGURE 19. FUNCTION GENERATOR

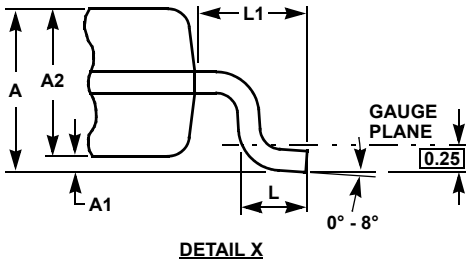
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Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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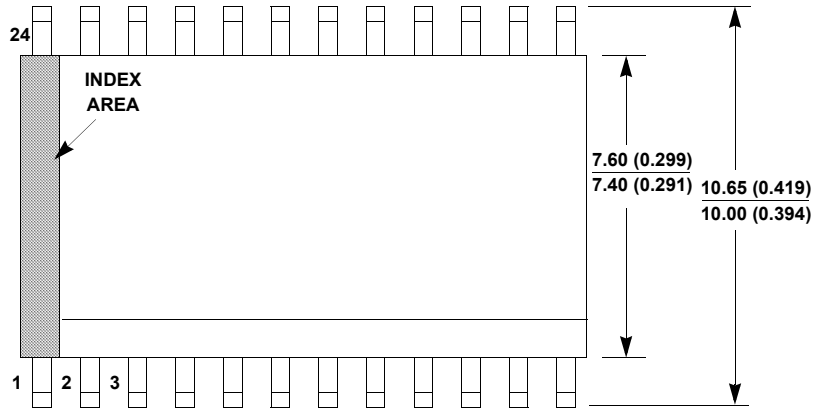
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Package Outline Drawing

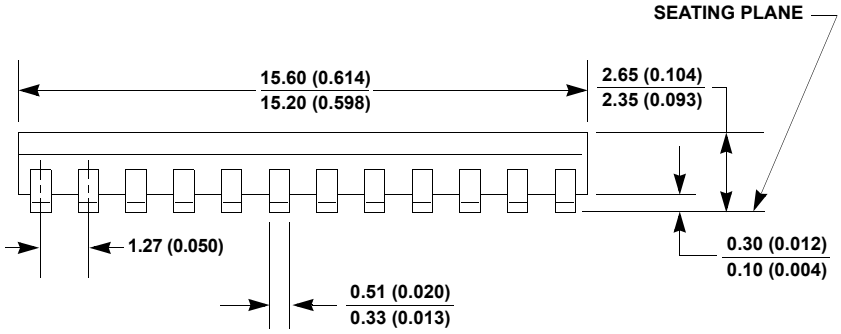
M24.3

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

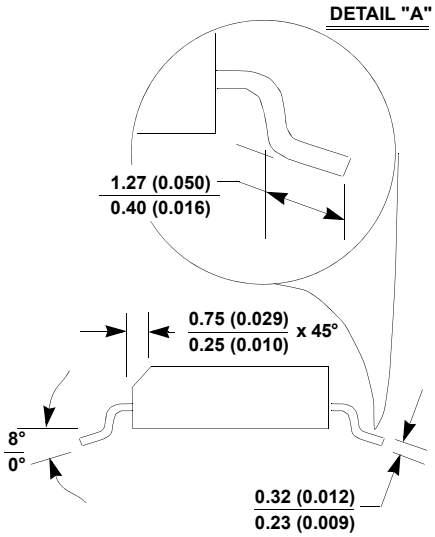
Rev 2, 3/11



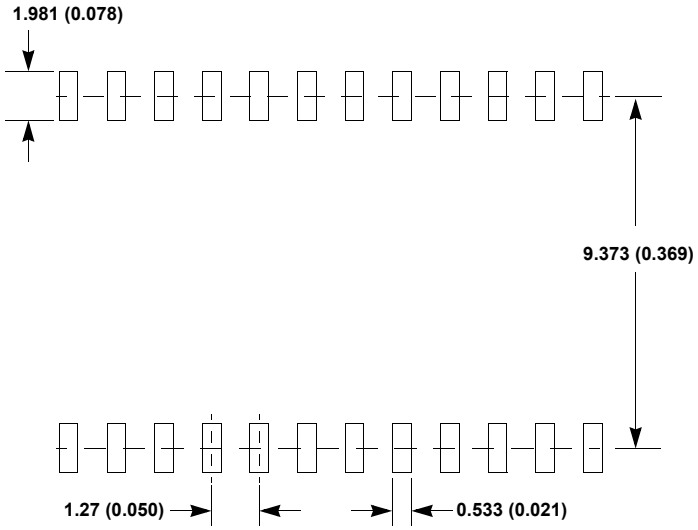
TOP VIEW



SIDE VIEW “A”



SIDE VIEW “B”



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions in ( ) are not necessarily exact.
8. This outline conforms to JEDEC publication MS-013-AD ISSUE C.

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