NTR3A30PZ

MOSFET – Power, Single P-Channel, SOT-23, 2.4 x 2.9 x 1.0 mm

-20 V, -5.5 A

ON Semiconductor®

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Features

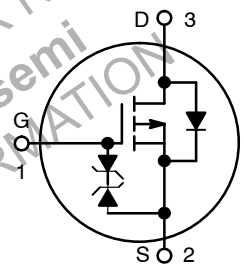
- Low $R_{DS(on)}$ Solution in 2.4 mm x 2.9 mm Package
- ESD Diode−Protected Gate
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Load Switch
- Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Smart Phones, Media Tablets, PMP, DSC, GPS, and Others

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D MAX
−20 V	38 mΩ @ −4.5 V	−5.5 A
	50 mΩ @ −2.5 V	
	73 mΩ @ −1.8 V	

P−Channel MOSFET



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

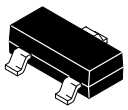
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−20	V
Gate−to−Source Voltage			V_{GS}	±8	V
Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−3.0	A
Drain Current (Note 1)		T_A = 85°C		−2.2	
	t ≤ 5 s	T_A = 25°C		−5.5	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.48	W
	t ≤ 5 s			1.58	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	−9.1	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
ESD HBM, JESD22−A114			V_{ESD}	2000	V
Source Current (Body Diode) (Note 2)			I_S	−0.48	A
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

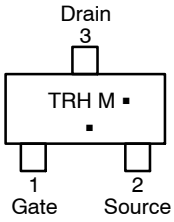
Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	260	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 1)	$R_{\theta JA}$	79	

1. Surface−mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [2 oz] including traces).
2. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.



SOT−23
CASE 318
STYLE 21

MARKING DIAGRAM & PIN ASSIGNMENT



TRH = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTR3A30PZT1G	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		−20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			10.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V	T_J = 25°C			−1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V				±10	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.4	−0.65	−1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				10.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V	I_D = −3 A		31	38	mΩ
		V_{GS} = −2.5 V	I_D = −2.5 A		36	50	
		V_{GS} = −1.8 V	I_D = −1.5 A		51	73	
Forward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −3 A			30		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −15 V			1651		pF
Output Capacitance	C_{oss}				148		
Reverse Transfer Capacitance	C_{rss}				129		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −3 A			17.6		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.7		
Gate−to−Source Charge	Q_{GS}				2.4		
Gate−to−Drain Charge	Q_{GD}				4.9		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −3 A, R_G = 6.0 Ω			100		ns
Rise Time	t_r				208		
Turn−Off Delay Time	$t_{d(off)}$				1043		
Fall Time	t_f				552		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −0.4 A	T_J = 25°C		0.65	1.0	V
			T_J = 125°C		0.47		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

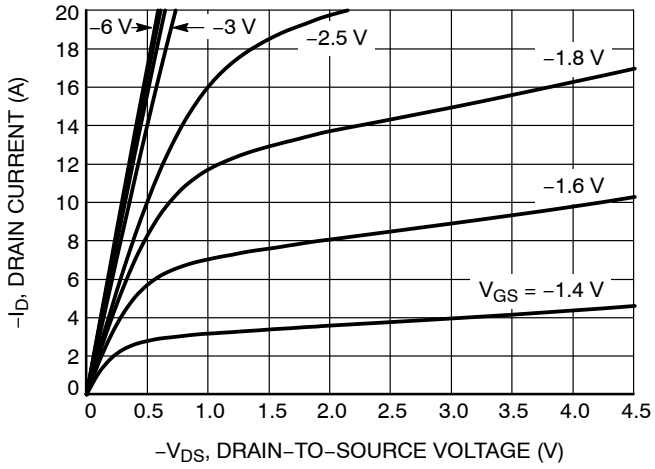


Figure 1. On−Region Characteristics

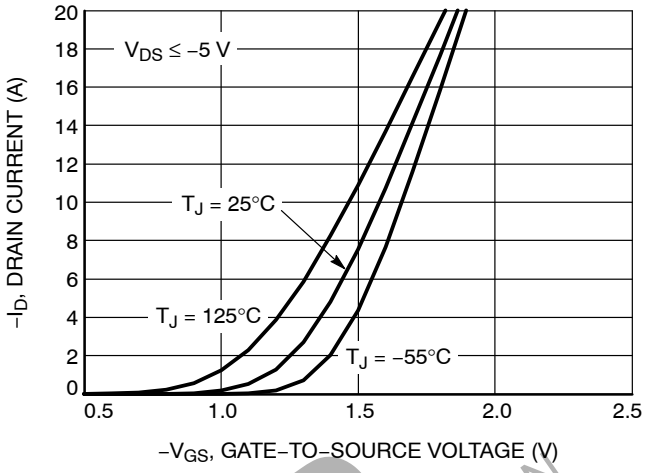


Figure 2. Transfer Characteristics

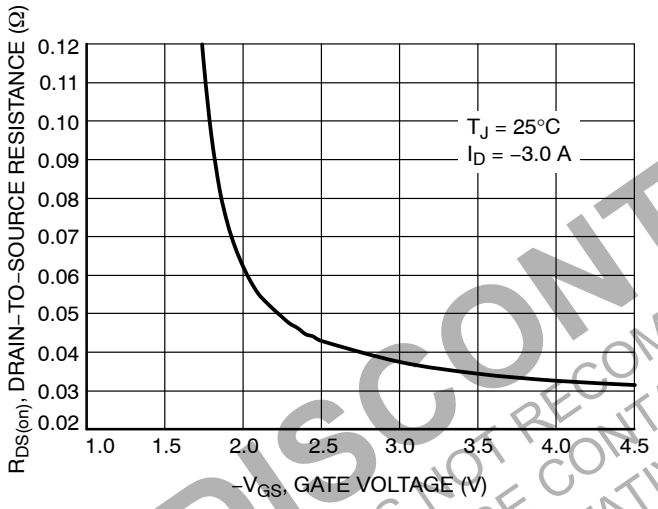


Figure 3. On−Resistance vs. Gate−to−Source Voltage

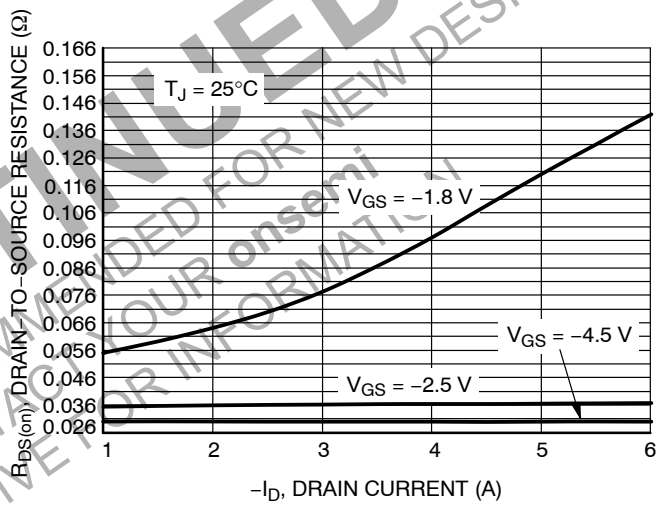


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

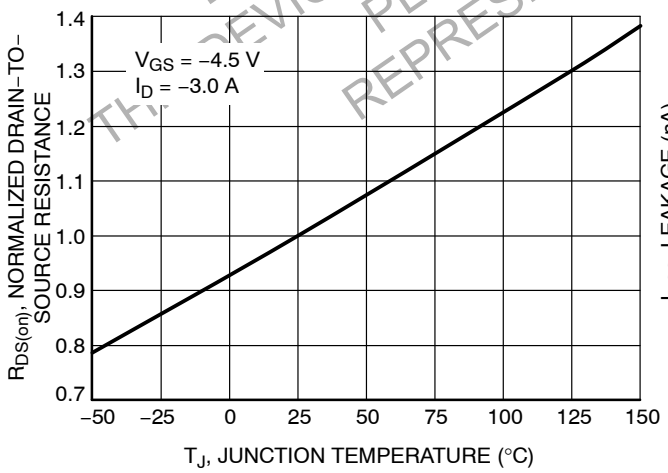


Figure 5. On−Resistance Variation with Temperature

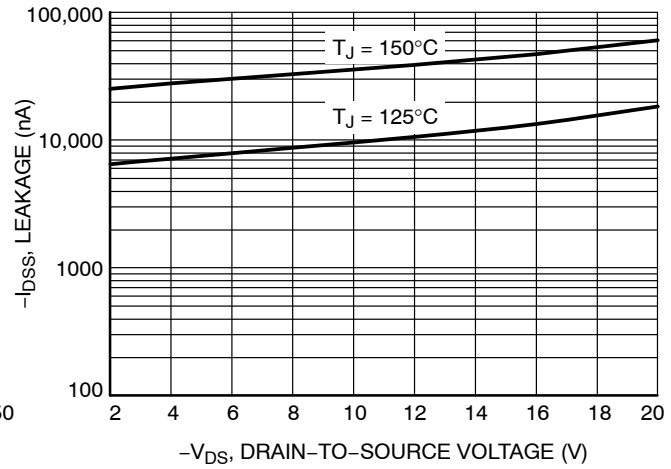


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

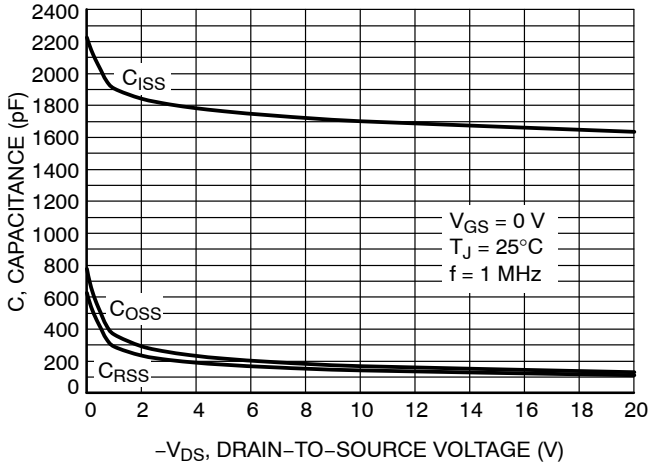


Figure 7. Capacitance Variation

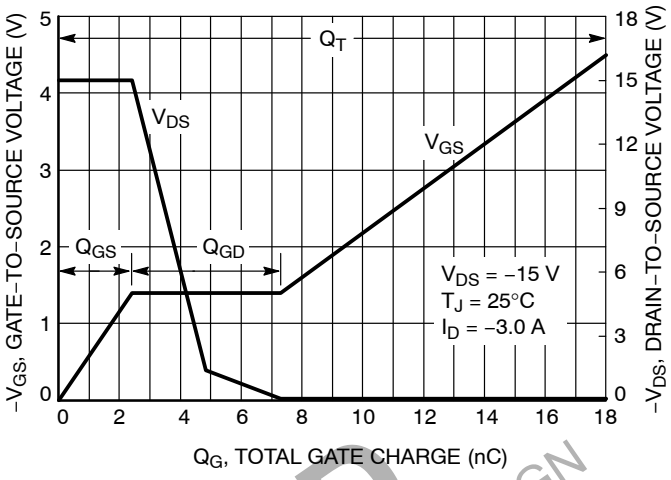


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

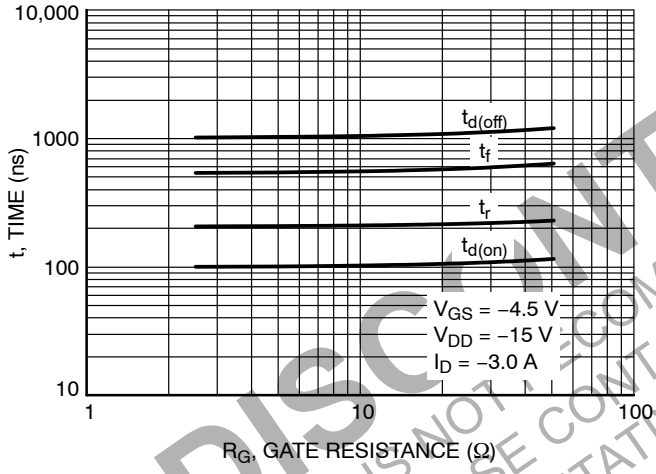


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

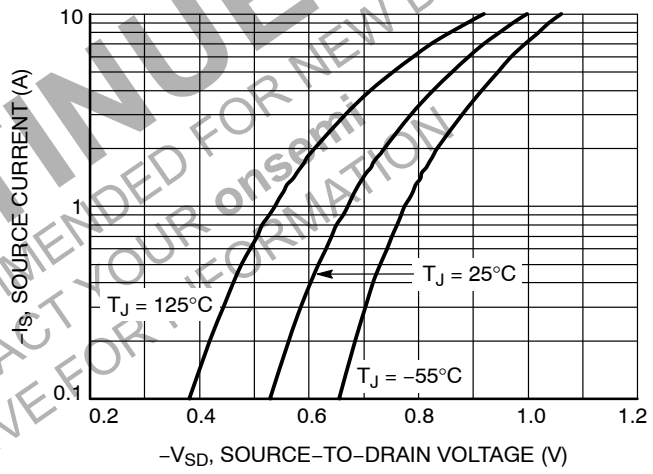


Figure 10. Diode Forward Voltage vs. Current

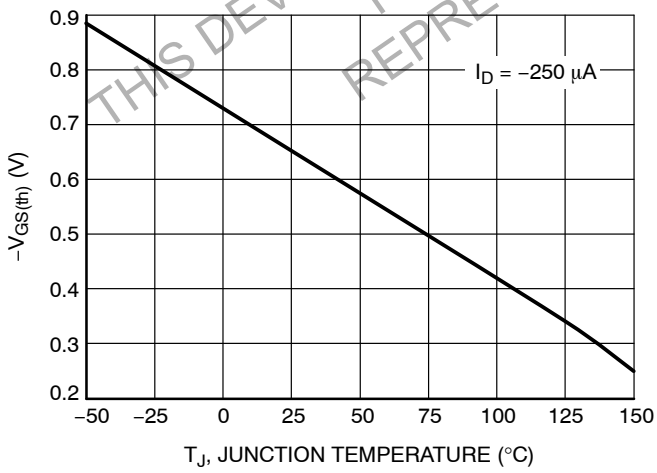


Figure 11. Threshold Voltage

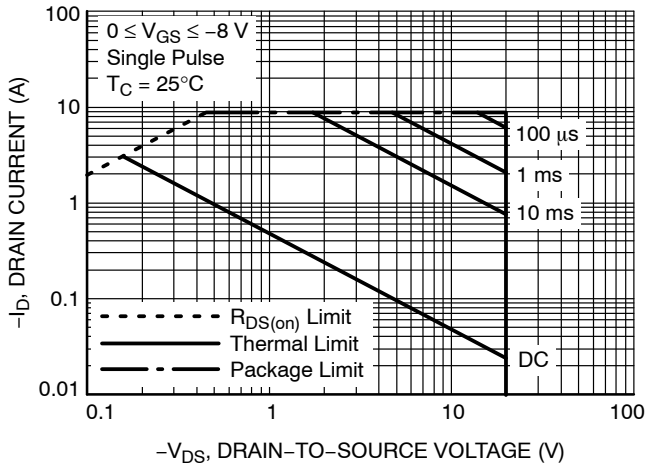


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

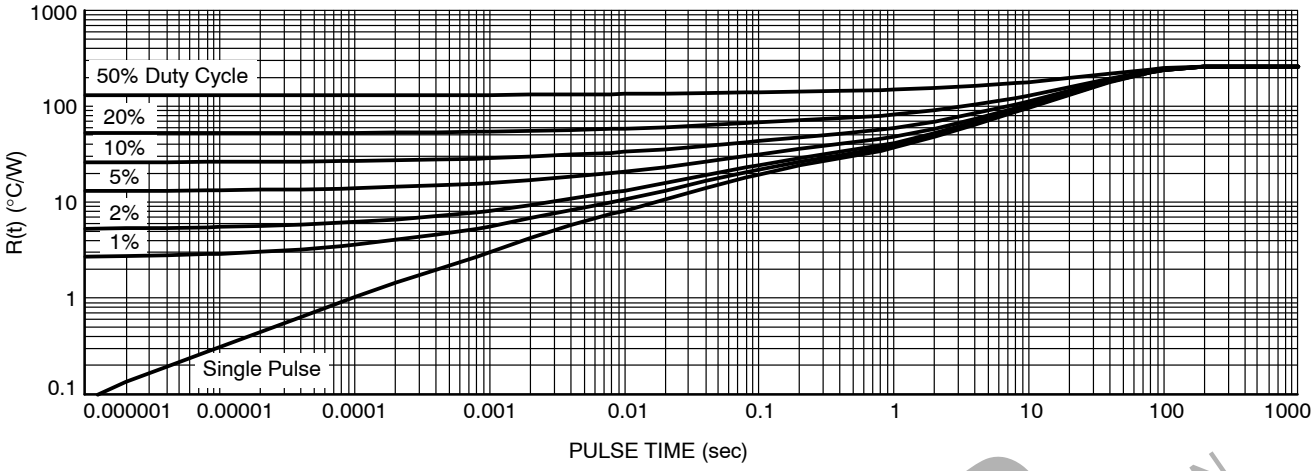
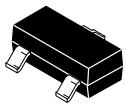


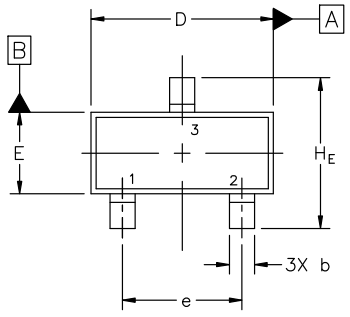
Figure 13. FET Thermal Response



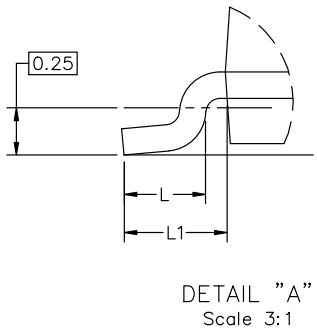
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

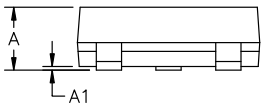
DATE 14 AUG 2024



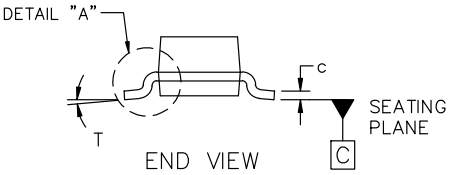
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

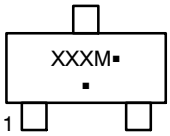


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

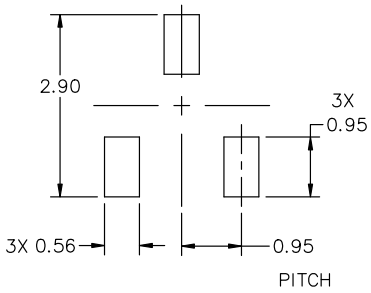
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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