User's Manual

16

SubGHz Transceiver (RAA604S00)

RF Transceiver

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (http://www.renesas.com).

Renesas Electronics
www.renesas.com

Rev. 1.20 Nov 2016

Downloaded from Arrow.com.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(2012.4)

Downloaded from Arrow.com.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Downloaded from Arrow.com.

CONTENTS

1. OVERVIEW 1
1.1 Features 1
1.2 Applications 2
1.3 Block Diagram 2
1.3.1 RAA604S00 (32-pin) 2
1.4 Package/Pin Layout Diagram 3
1.4.1 RAA604S00 (32-pin) 3
1.5 Pin Function Description 4

2. PIN FUNCTIONS 5
2.1 Pin Block Diagram 5
2.2 Connection of Unused Pins 5

3. BASEBAND FUNCTION 6
3.1 Baseband Block Diagram 7
3.2 Frame configuration 8
3.2.1 Transmission frame configuration 8
3.2.2 Preamble value 9
3.2.3 Configuration of PHR 10
3.3 Baseband Interrupt 12
3.4 Baseband Function Controlling Register 13
3.4.1 RF start register (BBRFCON) 15
3.4.2 Transmit/receive reset register (BBTXRXRST) 16
3.4.3 Transmit/receive mode register 0 (BBTXRXMODE0) 17
3.4.4 Transmit/receive mode register 1 (BBTXRXMODE1) 19
3.4.5 RSSI/CCA result register (BBRSSICCARSLT) 21
3.4.6 Enhanced-ACK mode register (BBEACKMODE) 26
3.4.7 Transmit/receive status register 0 (BBTXRXST0) 27
3.4.8 Transmit/receive mode register 2 (BBTXRXMODE2) 29
3.4.9 Transmit/receive mode register 3 (BBTXRXMODE3) 30
3.4.10 Transmit/receive status register 1 (BBTXRXST1) 32
3.4.11 Transmit/receive control register (BBTXRXCON) 33
3.4.12 CSMA control register 0 (BBCSMACON0) 34
3.4.13 CCA level threshold setting register (BBCCAVTH) 35
3.4.14 Transmit/receive status register 2 (BBTXRXST2) 35
3.4.15 Transmit/receive mode register 4 (BBTXRXMODE4) 36
3.4.16 CSMA control register 1 (BBCSMACON1) 37
3.4.17 CSMA control register 2 (BBCSMACON2) 38
3.4.18 PAN identifier register 0 (BBPANID0) 39
3.4.19 Short address register 0 (BBSHORTAD0) 39
3.4.20 Extended address register 0 (BBEXTENDAD00 to BBEXTENDAD03) 40
3.4.21 Timer read registers (BBTIMEREAD0, BBTIMEREAD1) 41
3.4.22 Timer compare registers 42
3.4.23 Time stamp registers 0 and 1 (BBTSTAMP0, BBTSTAMP1) 43
3.4.24 Timer control register (BBTIMECON) 44

Downloaded from Arrow.com.

3.4.25 Back off period register (BBBOFFPROD) 46
3.4.26 Baseband interrupt source register 0 (BBINTREQ0) 46
3.4.27 Baseband interrupt source register 1 (BBINTREQ1) 48
3.4.28 Baseband interrupt source register 2 (BBINTREQ2) 50
3.4.29 Baseband interrupt enable register 0 (BBINTEN0) 51
3.4.30 Baseband interrupt enable register 1 (BBINTEN1) 52
3.4.31 Baseband interrupt enable register 2 (BBINTEN2) 53
3.4.32 CSMA control register 3 (BBCSMACON3) 54
3.4.33 Calibration register (BBCAL) 54
3.4.34 ACK counter compare registers 0 and 1 (ACKCOMP0 and ACKCOMP1) 55
3.4.35 ACK counter initial value register (ACKINI) 55
3.4.36 Receive level threshold setting register (BBLVLVTH) 57
3.4.37 ACK reply time setting register (ACKRTNTIM) 58
3.4.38 Automatic receive switch compare register (AUTORCVCNT) 59
3.4.39 Back off cycle register (BOFFPERIOD) 60
3.4.40 CSMA-CA end count register (CSMAENDCOUNT) 60
3.4.41 CSMA-CA start count register (CSMASTACOUNT) 61
3.4.42 Communication status register 1 (COMSTATE1) 62
3.4.43 Communication status register 2 (COMSTATE2) 63
3.4.44 Estimate control register (BBEVAREG) 64
3.4.45 Back off period register 2 (BBBOFFPROD2) 67
3.4.46 Communication status register 3 (COMSTATE3) 67
3.4.47 ACK receive wait time setting register (ACKRCVWIT) 68
3.4.48 Retransmission start compare register (RETRNWUP) 68
3.4.49 ANTSW output timing setting register (BBANTSWTIMG) 69
3.4.50 Receive frame length register (BBRXFLEN) 69
3.4.51 Receive data counter register (BBRXCOUNT) 70
3.4.52 Transmit frame length register (BBTXFLEN) 70
3.4.53 Preamble length setting register (BBPAMBL) 71
3.4.54 Frequency setting register (BBFREQ) 71
3.4.55 Symbol rate setting register (BBSYMBLRATE) 72
3.4.56 SUBG control register (BBSUBGCON) 73
3.4.57 Modulation method setting register (BBMODSET) 74
3.4.58 CCA time register (CCATIME) 75
3.4.59 Antenna diversity mode register (BBANTDIV) 75
3.4.60 Mode switch frame transmit register (BBTXMODESW) 77
3.4.61 Mode switch frame receive register (BBRXMODESW) 77
3.4.62 Transmit data counter register (BBTXCOUNT) 78
3.4.63 PHY header receive register (BBPHRRX) 79
3.4.64 Preamble setting register (BBPABL) 80
3.4.65 SFD setting register (BBSFD) 80
3.4.66 SHR control register (BBSHRCON) 81
3.4.67 ANT0 read register (BBANT0RD) 82
3.4.68 ANT1 read register (BBANT1RD) 82
3.4.69 Antenna switch time register (BBANTDIVTIM) 83
3.4.70 Receive start timeout setting register (BBANTTIMOUT) 83
3.4.71 Number-of-receive-byte interrupt compare register (BBRCVINTCOMP) 84
3.4.72 Back off period total number register (BBBOPTOTAL) 84
3.4.73 CCA total number register (BBCCATOTAL) 85

Downloaded from Arrow.com.

3.4.74 RF initial setting register 00 to 02 (RFINI00 to RFINI02) 86
3.4.75 RF initial setting register 10 to 12 (RFINI10 to RFINI12) 87
3.4.76 PAN identifier register 1 (BBPANID1) 88
3.4.77 Short address register 1 (BBSHORTAD1) 88
3.4.78 Extended address register 1 (BBEXTENDAD10 to BBEXTENDAD13) 89
3.4.79 Receive timeout register (BBTIMEOUT) 90
3.4.80 ANTSW control register (ANTSWCON) 91
3.4.81 Clock output control register (CLKOUTCON) 92
3.4.82 Port direction register (GPIODIR) 93
3.4.83 Port data register (GPIODATA) 94
3.4.84 SFD setting register 2 (BBSFD2) 95
3.4.85 SFD setting register 3 (BBSFD3) 96
3.4.86 SFD setting register 4 (BBSFD4) 96
3.4.87 FEC control register (BBFECCON) 97
3.4.88 Address filter extension address control register (BBADFCON) 99
3.4.89 Antenna diversity mode register 2 (BBANTDIV2) 100
3.4.90 Lower limit threshold setting register after SFD detection (PWRLOWTH2) 101

4. SERIAL INTERFACE 102
4.1 Communication Format 102
4.1.1 Address part and R/W part 102
4.1.2 Data part 103

5. STATE TRANSITION 104
5.1 Wake Up (SLEEP → IDLE) 105
5.2 Power Down (IDLE → SLEEP) 108
5.3 Other State Transition 109
5.3.1 Example of Procedure for Transmission 109
5.3.2 Example of Procedure for Reception 109
5.3.3 Example of Procedure for CCA 110
5.3.4 Example of Procedure for CSMA-CA 110
5.3.5 Example of Procedure for Calibration 110
5.3.6 Setting for Each Data Rate 111

6. EXAMPLE OF PROCEDURE FOR FUNCTION SETTING 120
6.1 Example of Procedure for Transmission Output Power Setting 120
6.2 RF frequency setting for transmission 135
6.3 RF frequency setting for reception 136

7. NOTICE FOR USING BASEBAND FUNCTION 147
7.1 Notice About Transmission 147
7.2 Cautions on First and Second Address Filter Match Monitor Bits 147

8. PERIPHERAL CIRCUIT CONNECTION DIAGRAM 148
8.1 RAA604S00 (32-pin) 148

9. ELECTRIC CHARACTERISTICS 152
9.1 Absolute Maximum Ratings 152

Downloaded from Arrow.com.

9.2 Recommended Operating Conditions 153
9.3 XIN Frequency Deviation 153
9.3.1 Compatible with IEEE802.15.4g 153
9.3.2 Compatible with ARB Standard 154
9.4 DC Characteristics 155
9.5 AC Characteristics. 156
9.6 Calibration Timing Characteristic 158
9.7 Power Supply Current 159
9.8 Transceiver Reception Characteristics 160
9.9 Transceiver Transmission Characteristics 161
9.10 IEEE802.15.4g Frequency/Data Rate Table 162

10. OUTLINE DRAWING 163

APPENDIX A REVISION HISTORY 1
A.1 Major Revisions in This Edition 1
A.2 Revision History of Preceding Editions 2

Downloaded from Arrow.com.

CHAPTER 1 OVERVIEW

RAA604S00 is an RF transceiver with low power consumption.

1.1 Features

Low power consumption

- Receiving current: 6.9 mA (TYP) @3.0 V
- Transmission current: 21 mA (TYP) @3.0 V +10 dBm

Transceiver

- RF frequency range: 863 to 928 MHz
- Modulation method: 2FSK/GFSK, 4FSK/GFSK
- Data rate:
  2FSK/GFSK; 10 k to 300 kbps
  4FSK/GFSK; 200 k/400 kbps
- Forward Error Correction (FEC) function

MAC

- 32-bit timer function
- Transmission RAM/Receiving RAM: both 256 bytes
- 16-bit/32-bit auto CRC function
- Address filter & auto ACK reply function
- Antenna diversity function
- Auto CSMA-CA function

Operating voltage: 1.8 to 3.6 V

Operating ambient temperature: –40 to +85 °C

Package: 32-pin HVQFN (5×5) (0.5 mm pitch)

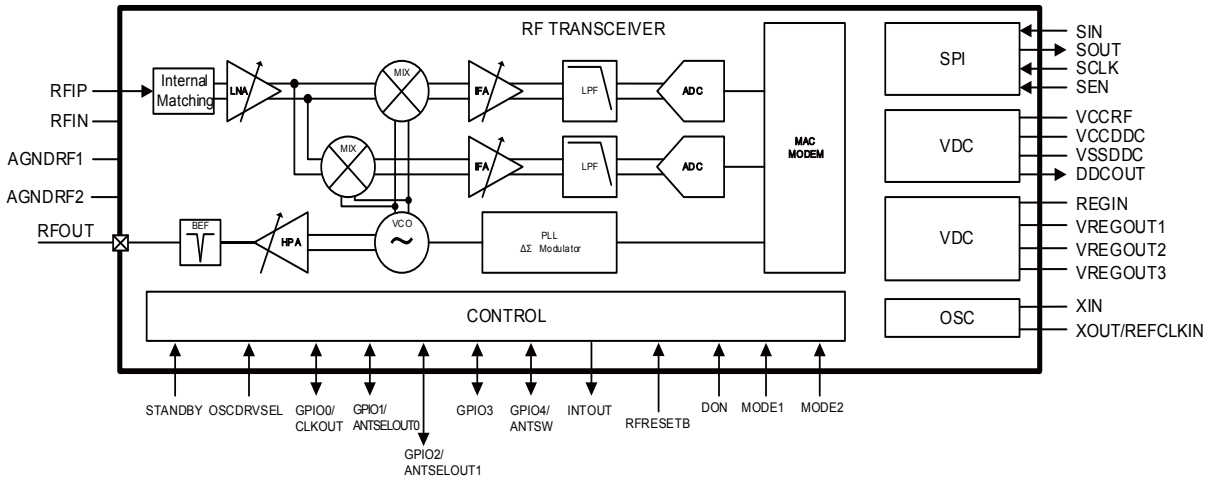
Downloaded from Arrow.com.

1.2 Applications

Smart meter (Electricity, gas, tap water) supporting products, HEMS controller, wireless sensor network, and others

1.3 Block Diagram

1.3.1 RAA604S00 (32-pin)



(1) LNA block

This is a low noise amplifier which input the high frequency signal captured by antenna.
It switches the gain according to the input signal.

(2) MIX block

This is a mixer circuit which uses the high frequency RF output signal from the LNA as input signal and converts it into low frequency IF (Intermediate Frequency) signal by changing the frequency.

(3) VGA part

This block controls the input amplitudes under the constant state that are transmitted to the AD converter which is connected to the subsequent stage, by changing the gain depending on the input signal level.

(4) Filter block

This removes unnecessary input signals from antenna.

(5) ADC block

This converts analog signal to digital signal.

(6) VCO and PLL blocks

They generate the carrier frequency which is used upon reception/transmission based on the reference clock which is input by the crystal oscillator or TCXO.

(7) PA block

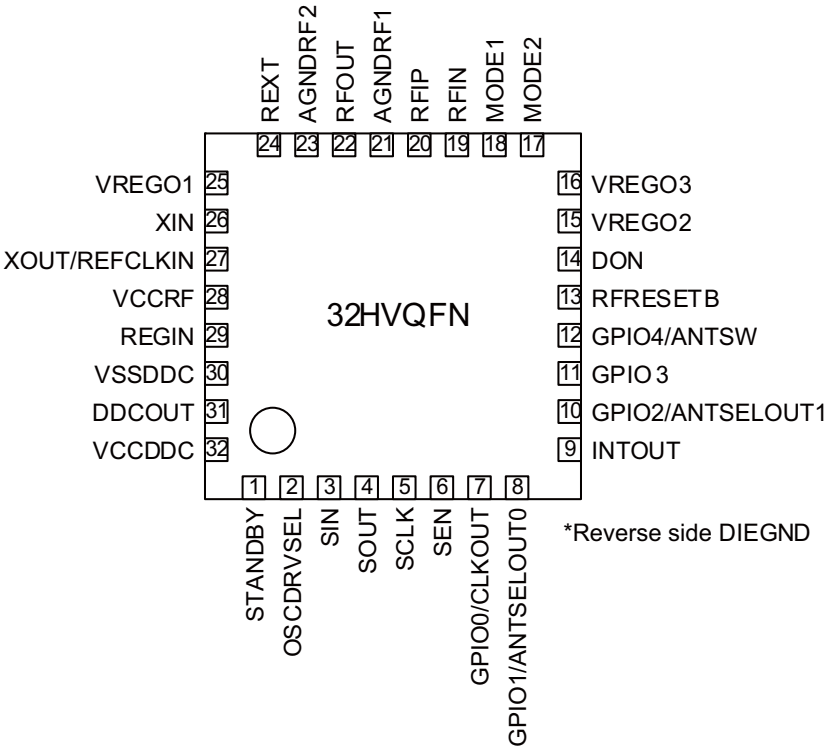
This is a power amplifier which is located at the output stage in the analog circuit in order to output the high frequency signal from antenna. It demodulates the carrier (carrier wave) from PLL, and then outputs them to antenna with power amplification.

Downloaded from Arrow.com.

1.4 Package/Pin Layout Diagram

1.4.1 RAA604S00 (32-pin)

• 32-pin, plastic HVQFN (5×5 mm, 0.5 mm pitch)



Downloaded from Arrow.com.

1.5 Pin Function Description

The RAA604S00 pin functions are shown in **Table 1 - 1**.

Table 1 - 1 RAA604S00 (32-pin) Pin Function List

Pin No.	Pin name	I/O	Function
1	STANDBY	Input	Power down control input pin for transceiver
2	OSCDRVSEL	Input	Buffer drive capacity switch pin for 48-MHz crystal oscillator
3	SIN	Input	Serial input pin
4	SOUT	Output	Serial output pin
5	SCLK	Input	Clock pin for serial I/O
6	SEN	Input	Serial enable pin
7	GPIO0/CLKOUT	I/O	Transceiver I/O port 0 and CLKOUT pin
8	GPIO1/ANTSELOUT0	I/O	Transceiver I/O port 1 and ANTSELOUT0 pin
9	INTOUT	Output	Transceiver interrupt output pin
10	GPIO2/ANTSELOUT1	I/O	Transceiver I/O port 2 and ANTSELOUT1 pin
11	GPIO3	I/O	Transceiver I/O port 3
12	GPIO4/ANTSW	I/O	Transceiver I/O port 4 and ANTSW pin
13	RFRESETB	Input	Reset pin
14	DON	Input	DCDC converter enable pin
15	VREGO2	—	Stabilization capacitor connection pin for VCO (1.1 V)
16	VREGO3	—	Power supply stabilization capacitor connection pin for PLL (1.1 V)
17	MODE2	Input	Mode switch pin 2
18	MODE1	Input	Mode switch pin 1
19	RFIN	—	Transceiver GND pin
20	RFIP	Input	RF input pin
21	AGNDRF1	—	Transceiver GND pin
22	RFOUT	Output	RF output pin
23	AGNDRF2	—	Transceiver GND pin
24	REXT	—	External reference resistor connecting pin
25	VREGO1	—	RF power supply stabilization capacitor connection pin (1.1 to 1.25 V)
26	XIN	Input	48 MHz crystal resonator input pin
27	XOUT/REFCLKIN	I/O	48 MHz crystal resonator output and external clock input pin
28	VCCRF	—	3V-system power supply input pin (1.8 to 3.6 V)
29	REGIN	—	Analog power supply input (1.4 to 1.6 V), external connecting pin with DDCOUT
30	VSSDDC	—	DCDC converter GND pin
31	DDCOUT	—	DCDC converter output (1.4 to 1.6 V), external connecting pin with REGIN
32	VCCDDC	—	DCDC converter power supply pin (1.8 to 3.6 V)
Reverse side	DIEGND	—	GND

Downloaded from Arrow.com.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Block Diagram

The pin block diagrams are shown in **Figure 2 - 1** to **2 - 3**.

Figure 2 - 1 Block Diagram for STANDBY, OSCDRVSEL, SIN, SCLK, SEN, RFRESETB, DON, MODE1, MODE2

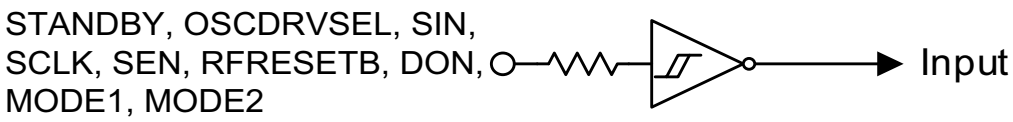


Figure 2 - 2 Block Diagram for Pins GPIO0 to GPIO4

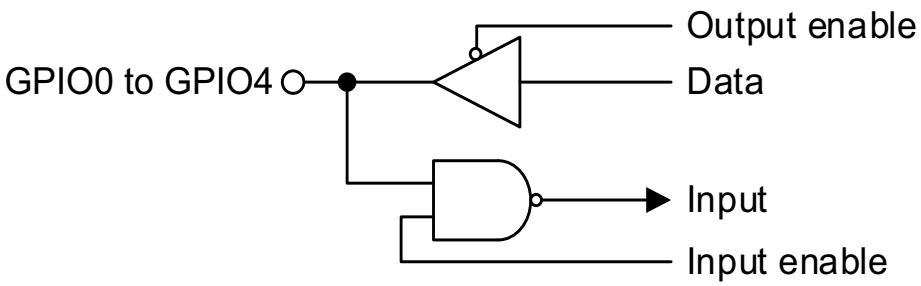
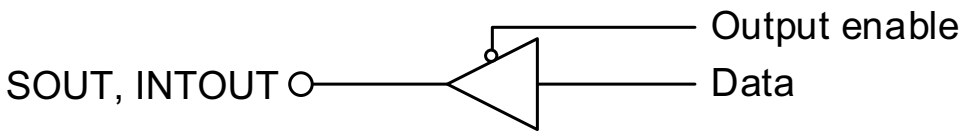


Figure 2 - 3 Block Diagram for Pins SOUT and INTOUT



<R> 2.2 Connection of Unused Pins

Table 2 - 1 shows the connection of unused pins.

Table 2 - 1 Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
GPIO0/CLKOUT	I/O	Input: Leave open or independently connect to VCCDDC or VSSDDC via a resistor. Output: Leave open.
GPIO1/ANTSELOUT0		
GPIO1/ANTSELOUT1		
GPIO3		
GPIO4/ANTSW		

Downloaded from Arrow.com.

CHAPTER 3 BASEBAND FUNCTION

BASEBAND FUNCTION

The baseband functions shown below are included in the hardware.

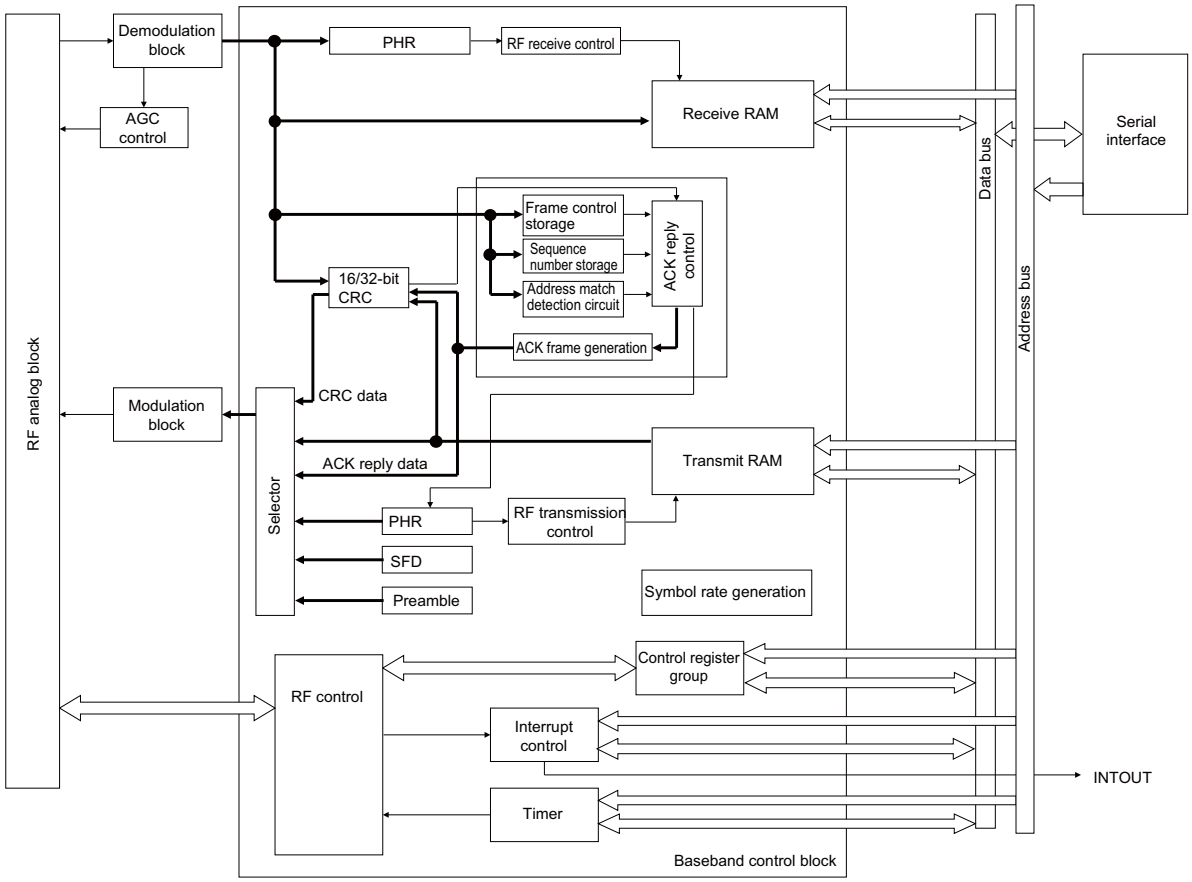
- 32-bit timer
- Transmission RAM
- Reception RAM
- Frame configuration
- Filter function
- Interrupt
- CRC calculation circuit
- Auto ACK reply function
- Auto ACK receive function
- Auto receive switch function
- ANTSW output switch function
- Auto CSMA-CA function
- Antenna diversity function
- Port control list
- Baseband-related register

Downloaded from Arrow.com.

3.1 Baseband Block Diagram

Figure 3 - 1 shows the baseband block diagram.

Figure 3 - 1 Baseband Block Diagram



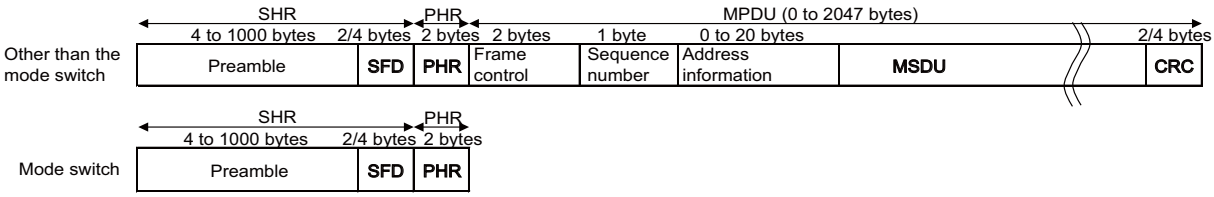
Downloaded from Arrow.com.

3.2 Frame configuration

3.2.1 Transmission frame configuration

Automatically generates and outputs the transmission frame. **Figure 3 - 2** shows the transmission frame configuration. The frame configurations after the PHR other than those of the mode switch frame and the mode switch frame change.

Figure 3 - 2 Transmission Frame Configuration



SHR: Synchronization Header
PHR: PHY Header
MPDU: MAC Protocol Data Unit
SFD: Start of Frame Delimiter
MSDU: MAC Service Data Unit
CRC: Cyclic Redundancy Check

<1> Preamble: 4 to 1000 bytes

<2> SFD: 2 bytes or 4 bytes

<3> PHR: 2 bytes

Value varies when it is transmitted by the frame other than the mode switch frame or the mode switch frame.

- Frames other than the mode switch frame: The value written in the BBTXFLEN register (the length of MPDU), the CRCBIT value (FCSType), and the DWEN value (Data Whitening)
- Mode switch frame: the value written in the BBTXMODESW register

<4> MPDU: data whose length ranged from the minimum 3 bytes to the maximum 2047 bytes. The data written in the transmission RAM is output sequentially.

Note that the CR data which is generated in the CRC calculation circuit is automatically added to the last 2 bytes or 4 bytes when the NOCRC bit in the BBTXRXMODE2 register is “0.”

- Frame control: 2 bytes (4 symbols)
  - Frame type (bit 2 to 0)
    000b: Beacon frame
    001b: the data frame
    010b: the ACK frame
    011b: the MAC command frame
    100b to 111b: reserved
  - With/without security (bit 3). Transmission pending bit (bit 4)
  - ACK request (bit 5), Transmission in the PAN (bit 6)
  - Transmission source address mode (bits 10 and 11), Transmission destination address mode (bits 14 and 15)
  - Frame version (bits 12, 13)
- Sequence number: 1 byte
- Address information: PADNID and address for transmission destination and source
- MSDU (MAC payload): frame payload
- CRC: 2-byte or 4-byte frame CRC inspection array

Downloaded from Arrow.com.

3.2.2 Preamble value

Table 3 - 1 shows the difference between the preamble value and the SFD value according to the modulation method.

Table 3 - 1 For Normal Receive

<R>

Condition			Preamble length
Way	Symbol rate (ksps)	Modification index	
2FSK/2GFSK	10	0.5	4
2FSK/2GFSK	20	0.5	4
2FSK/2GFSK	40	0.5	4
2FSK/2GFSK	50	1	4
2FSK/2GFSK	100	0.5	4
2FSK/2GFSK	100	1	4
2FSK/2GFSK	150	0.5	5
2FSK/2GFSK	200	0.5	6
2FSK/2GFSK	200	1	6
2FSK/2GFSK	300	0.5	7
4FSK/4GFSK	100	0.33	5
4FSK/4GFSK	200	0.33	6

Table 3 - 2 For Antenna Diversity Receive

<R>

Condition			Preamble length
Way	Symbol rate (ksps)	Modification index	
2FSK/2GFSK	10	0.5	8
2FSK/2GFSK	20	0.5	8
2FSK/2GFSK	40	0.5	8
2FSK/2GFSK	50	1	8
2FSK/2GFSK	100	0.5	15
2FSK/2GFSK	100	1	15
2FSK/2GFSK	150	0.5	18
2FSK/2GFSK	200	0.5	23
2FSK/2GFSK	200	1	23
2FSK/2GFSK	300	0.5	24
4FSK/4GFSK	100	0.33	15
4FSK/4GFSK	200	0.33	23

Downloaded from Arrow.com.

3.2.3 Configuration of PHR

(1) In the case other than the Mode Switch frame

Figure 3 - 3 shows the PHR bit configuration in the case other than the Mode Switch frame.

The respective PHR bits automatically capture the set value and transmit it to the corresponding register.

Figure 3 - 3 PHR Bit Configuration in the Case Other Than the Mode Switch Frame

Bit array	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit configuration	MS	R1	R0	FCS	DW	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0

MS: Mode Switch

Mode switch enable bit value: Mode switch frame transmission register bit 0

Automatically transmits the following values when this bit value is 0.

R1, R0: Reserved

Fixed to 00b

FCS: FCS Type

The-number-of-CRC-bit switch bit value: SUBG control register bit 3

DW: Data Whitening

DW enable bit value: SUBG control register bit 4

L10 - L0: Frame Length

Transmission frame length register value: Transmit frame length register bits 0 to 10

Downloaded from Arrow.com.

(2) In the case of the Mode Switch frame

Figure 3 - 4 shows the PHR bit configuration in the case of the Mode Switch frame.

The respective PHR bits automatically capture the set value and transmit it to the corresponding register.

Only the register values are transmitted on the hardware while no Checksum or Parity Check function is included.

Figure 3 - 4 PHR Bit Configuration in the Case of the Mode Switch Frame

Bit array	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit configuration	MS	M1	M0	FEC	New Mode							B3	B2	B1	B0	PC

MS: Mode Switch

Mode switch enable bit value: Mode switch frame transmission register bit 0

Automatically transmits the following values when this bit value is 1.

M1, M0: Mode Switch Parameter Entry

Mode switch frame transmission register bits 1 and 2

FEC: New Mode FEC

Mode switch frame transmission register bit 3

New Mode: New Mode

Mode switch frame transmission register bits 4 -10

B3-B0: Checksum

Mode switch frame transmission register bits 11 -14

PC: Parity Check

Mode switch frame transmission register bit 15

Downloaded from Arrow.com.

3.3 Baseband Interrupt

Table 3 – 3 shows the interrupt sources.

If one or more bits are “1” in interrupt source bits in the table enabled by baseband interrupt registers 0 to 2, INTOUT pin outputs high level. If the all interrupt source bits are “0”, the pin outputs low level.

The polarity of INTOUT output can be changed by INTOUTSEL bit.

Table 3 - 3 Interrupt Sources List

Number	Interrupt Name	Interrupt Occurrence Condition
1	Timer compare 0	Interrupt request occurs when timer value matches timer compare 0 value
2	Timer compare 1	Interrupt request occurs when timer value matches timer compare 1 value
3	Timer compare 2	Interrupt request occurs when timer value matches timer compare 2 value
4	Frame transmit completion	Interrupt request occurs when a frame transmission completes However, interrupt request does not occur at transmit completion when automatic ACK receive mode is enabled, if the transmit frame includes ACK request. The interrupt request occurs at completion of ACK reception or ACK receive timeout
5	Bank 0 transmit completion	Interrupt request occurs when transmit RAM data transmission of bank 0 completes
6	Bank 1 transmit completion	Interrupt request occurs when transmit RAM data transmission of bank 1 completes
7	Calibration completion	Interrupt request occurs when calibration completes
8	CCA completion Note 1	Interrupt request occurs when CCA sequence completes
9	CSMA-CA completion Note 1	Interrupt request occurs when CSMA-CA sequence completes
10	Frame receive completion	Interrupt request occurs when a frame reception completes However, interrupt request does not occur at receive completion when automatic ACK reply mode is enabled, if the receive frame includes ACK request. The interrupt request occurs at completion of ACK reply
11	Bank 0 receive completion	Interrupt request occurs when bank 0 of receive RAM becomes full
12	Bank 1 receive completion	Interrupt request occurs when bank 1 of receive RAM becomes full
13	Start reception	Interrupt request occurs when SFD is detected
14	Address filter Note4	Interrupt request occurs when address match is recognized
15	Receive overrun	Interrupt request occurs in the following cases - Receive RAM bank 0 status bit is kept 1 and data reception to receive RAM bank 0 is started again - Receive RAM bank 1 status bit is kept 1 and data reception to receive RAM bank 1 is started again
16	Mode switch receive completion	Interrupt request occurs when a mode switch frame is received
<R> 17	Receive level filter Note 2	Interrupt request occurs when a communication error occurs such as no signal state during frame reception
18	Receive byte counts	Interrupt request occurs when setting count of bytes are received
19	Frame length	Interrupt request occurs when the frame length is received
20	Byte reception Note 3	Interrupt request occurs for each receive byte data
21	Automatic receive timeout Note 3	Interrupt request occurs when timeout occurs with no receive frame, if the automatic receive timeout function is enabled

Note 1. CCA completion interrupt and CSMA-CA completion interrupt are switched by CCATINTSEL bit.

<R> **Note 2.** See 3.4.90 for setting condition of threshold level occurring receive level interrupt causing detection of no communication state.

Note 3. Byte reception interrupt and automatic receive timeout interrupt are switched by TIMEOUTINTSEL bit.

<R> **Note 4.** When the frame length is short and the frame has no address information or incomplete address information, address filter interrupt might not occur and only frame receive completion occurs.

Downloaded from Arrow.com.

3.4 Baseband Function Controlling Register

The following registers control the baseband function.

Table 3 - 4 Baseband Function Controlling Register (1/2)

RF start register (BBRFCON)
Transmit/receive reset register (BBTXRXRST)
Transmit/receive mode register 0 (BBTXRXMODE0)
Transmit/receive mode register 1 (BBTXRXMODE1)
RSSI/CCA result register (BBRSSICCARSLT)
Enhanced-ACK mode register (BBEACKMODE)
Transmit/receive status register 0 (BBTXRXST0)
Transmit/receive mode register 2 (BBTXRXMODE2)
Transmit/receive mode register 3 (BBTXRXMODE3)
Transmit/receive status register 1 (BBTXRXST1)
Transmit/receive control register (BBTXRXCON)
CSMA control register 0 (BBCSMACON0)
CCA level threshold setting register (BBCCAVTH)
Transmit/receive status register 2 (BBTXRXST2)
Transmit/receive mode register 4 (BBTXRXMODE4)
CSMA control register 1 (BBCSMACON1)
CSMA control register 2 (BBCSMACON2)
PAN identifier register 0 (BBPANID0)
Short address register 0 (BBSHORTAD0)
Extended address register 0 (BBEXTENDAD00 - BBEXTENDAD03)
Timer read register (BBTIMEREAD0 - BBTIMEREAD1)
Timer compare register (BBTCOMP0REG0 - BBTCOMP2REG0, BBTCOMP0REG1 - BBTCOMP2REG1)
Time stamp register (BBTSTAMP0, BBTSTAMP1)
Timer control register (BBTIMECON)
Back off period register (BBBOFFPROD)
Baseband interrupt source register 0 (BBINTREQ0)
Baseband interrupt source register 1 (BBINTREQ1)
Baseband interrupt source register 2 (BBINTREQ2)
Baseband interrupt enable register 0 (BBINTEN0)
Baseband interrupt enable register 1 (BBINTEN1)
Baseband interrupt enable register 2 (BBINTEN2)
CSMA control register 3 (BBCSMACON3)
Calibration register (BBCAL)
ACK counter compare register (ACKCOMP0, ACKCOMP1)
ACK counter initial value register (ACKINI)
Receive level threshold setting register (BBLVLVTH)
ACK reply time setting register (ACKRTNTIM)
Automatic receive switch compare register (AUTORCVCNT)
Back off cycle register (BOFFPERIOD)
CSMA-CA end count register (CSMAENDCOUNT)
CSMA-CA start count register (CSMASTACOUNT)
Communication status register 1 (COMSTATE1)
Communication status register 2 (COMSTATE2)

Downloaded from Arrow.com.

Table 3 - 4 Baseband Function Controlling Register (2/2)

Estimate control register (BBEVAREG)
Back off period register 2 (BBBOFFPROD2)
Communication status register 3 (COMSTATE3)
ACK receive wait time setting register (ACKRCVWIT)
Retransmission start compare register (RETRNWUP)
ANTSW output timing setting register (BBANTSWTIMG)
Receive frame length register (BBRXFLEN)
Receive data counter register (BBRXCOUNT)
Transmit frame length register (BBTXFLEN)
Preamble length setting register (BBPAMBL)
Frequency setting register (BBFREQ)
Symbol rate setting register (BBSYMBLRATE)
SUBG control register (BBSUBGCON)
Modulation method setting register (BBMODSET)
CCA time register (CCATIME)
Antenna diversity mode register (BBANTDIV)
Mode switch frame transmit register (BBTXMODESW)
Mode switch frame receive register (BBRXMODESW)
Transmit data counter register (BBTXCOUNT)
PHY header receive register (BBPHRRX)
Preamble setting register (BBPABL)
SFD setting register (BBSFD)
SHR control register (BBSHRCON)
ANT0 read register (BBANT0RD)
ANT1 read register (BBANT1RD)
Antenna switch time register (BBANTDIVTIM)
Receive start timeout setting register (BBANTTIMOUT)
Number-of-receive-byte interrupt compare register (BBRCVINTCOMP)
Back off period total number register (BBBOPTOTAL)
CCA total number (BBCCATOTAL)
RF Initial setting register0 (RFINI00-RFINI02)
RF Initial setting register1 (RFINI10-RFINI12)
PAN identifier register 1 (BBPANID1)
Short address register 1 (BBSHORTAD1)
Extended address register 1 (BBEXTENDAD10 to BBEXTENDAD13)
Receive timeout register (BBTIMEOUT)
ANTSW control register (ANTSWCON)
Clock output control register (CLKOUTCON)
Port direction register (GPIODIR)
Port data register (GPIODATA)
SFD setting register2 (BBSFD2)
SFD setting register3 (BBSFD3)
SFD setting register4 (BBSFD4)
FEC control register (BBFECCON)
Address filter extended address control register (BBADFCON)
Antenna diversity mode register2 (BBANTDIV2)

Downloaded from Arrow.com.

3.4.1 RF start register (BBRFCON)

Enables the RF function by setting 1 to the RF function enable bit.
Releases the analog circuit reset by setting 1 to the analog reset release bit.
Calibration control is enabled by setting the calibration control bit to 1. Set CSONSET bit to 0 after calibration.

The BBRFCON register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 01H.

Figure 3 - 5 RF Start Register (BBRFCON) Format

Address: 0000H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBRFCON	0	0	0	0	0	CSONSET	ANARESETB	RFSTART

CSONSET	Calibration control bit
0	Calibration not used
1	Calibration used

ANARESETB	Analog reset release bit
0	Analog circuit reset status
1	Analog circuit reset release

RFSTART	RF function enable bit
0	RF function disabled
1	RF function enabled

Caution Be sure to set “0” to bits 3 to 7.

Downloaded from Arrow.com.

3.4.2 Transmit/receive reset register (BBTXRXRST)

This register stops the RF communication.

Processes of reception, during the CCA and calibration can be stopped by setting 1 to the RF communication stop bit. (It enters into the IDLE state after the stop) In addition, the processes of automatic ACK reply, the automatic receive switch mode function, and others are also canceled. Note that this bit is automatically cleared to 0. However, the values of the respective registers can be retained.

Reset by RFRESETB pin after setting RFSTOP bit to 1 for stopping transmission.

The BBTXRXRST register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 6 Transmit/Receive Reset Register (BBTXRXRST) Format

Address: 0001H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXRST	0	0	0	0	0	0	0	RFSTOP

RFSTOP	RF communication stop trigger bit
0	Nothing is performed. (The RF communications are under the enabled status.)
1	Stops the RF communication. (It is under the IDLE state after the stop while this bit is automatically cleared to 0.)

Caution Be sure to set “0” to bits 1 to 7.

Downloaded from Arrow.com.

3.4.3 Transmit/receive mode register 0 (BBTXRXMODE0)

This register sets the various types of the RF transmit/receive mode.

Set 1 to the CCA type bit when performing the CCA or ED.

Enables the selection whether to perform the automatic ACK reply action after the completion of receive by using the automatic ACK mode enable bit.

Enables the setting to automatically transit to the receive mode after the completion of transmit by using the automatic receive switch mode 0 enable bit. Enables the setting to automatically transit to the receive mode after the completion of receive by using the automatic receive switch mode 1 enable bit. However, note that the ACK reply takes precedence if all of the ACK reply conditions are satisfied when 1 (enable) is set to the automatic ACK enable bit.

The battery life extension mode bit can set the battery life extension mode to enable for the branch condition when performing the CSMA-CA process.

The BEACON mode bit can switch between Non-beacon/Beacon modes.

The intraPAN enable bit can set enable/disable by the intraPAN bit condition of the receive frame when the address filter is enabled.

The BBTXRXMODE0 register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Downloaded from Arrow.com.

Figure 3 - 7 Transmit/Receive Mode Register 0 (BBTXRXMODE0) Format

Address: 0002H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXMODE0	INTRAPANEN	BEACON	BATLIFEEXT	AUTORCV1	AUTORCV0	AUTOACKEN	0	CCATYPE0

INTRAPANEN	intraPAN enable bit
0	intraPAN disabled
1	intraPAN enabled

BEACON	BEACON mode bit
0	Non-beacon mode
1	BEACON mode

BATLIFEEXT	Battery life extension mode bit
0	Battery life extension mode disabled
1	Battery life extension mode enabled

AUTORCV1	Automatic receive switch mode 1 enable bit (Receive → Receive)
0	Auto receive switch function disabled
1	Auto receive switch function enabled

AUTORCV0	Automatic receive switch mode 0 enable bit (Transmit → Receive)
0	Auto receive switch function disabled
1	Auto receive switch function enabled

AUTOACKEN	Automatic ACK mode enable bit
0	Automatic ACK disabled
1	Automatic ACK enabled

CCATYPE0	CCA type bit
0	Normal
1	CCA/ED

Caution Be sure to set “0” to bit 1.

Downloaded from Arrow.com.

3.4.4 Transmit/receive mode register 1 (BBTXRXMODE1)

This register sets the various types of the RF transmit/receive mode.
The CCA result select bit can be used to select between the CCA/ED value and the RSSI value when reading the RSSI/CCA result register.
The ACK reply frame version setting enable bit can switch the value of the version upon automatic ACK reply between the frame version value of the received frame, and the values of the ACK replay frame version setting bits 0 and 1.
The ACK replay frame version setting bit 0 can be used to set the value of bit 12 for the frame version value upon automatic ACK reply when the ACK reply frame version setting enable bit = 1.
The ACK replay frame version setting bit 1 can be used to set the value of bit 13 for the frame version value upon automatic ACK reply when the ACK reply frame version setting enable bit = 1.
The sequence number suppress bit can be used to set the enable/disable to the sequence number suppress bit of the received frame. There is also no sequence number for the ACK frame upon the automatic ACK reply when there is no sequence number for the received frame when this bit is set to enable.
The ACK receive point setting bit can be used to set the ACK receive recognition point during the ACK receive wait time to the point upon completion of the reception or upon reception of the PHR.
The BBTXRXMODE1 register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to C0H.

Downloaded from Arrow.com.

Figure 3 - 8 Transmit/Receive Mode Register 1 (BBTXRXMODE1) Format

Address: 0003H After reset: C0H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXMODE1	ACKRCVPOINT	SQCNUMSUPEN	ACKFV1	ACKFV0	ACKFVEN	0	0	CCASEL

ACKRCVPOINT	ACK receive point setting bit
0	Upon completion of the receive
1	Upon reception of the PHR

SQCNUMSUPEN	Sequence number suppress bit
0	Sequence number suppress enabled
1	Sequence number suppress disabled

ACKFV1	ACK reply frame version setting bit 1
0	Frame version bit 13 =0
1	Frame version bit 13 =1

ACKFV0	ACK reply frame version setting bit 0
0	Frame version bit 12 =0
1	Frame version bit 12 =1

ACKFVEN	ACK reply frame version setting enable bit
0	Version value of the receive frame
1	Values of the ACK reply frame version setting bits 0 and 1

CCASEL	CCA result select bit
0	CCA/ED
1	RSSI

Caution Be sure to set “0” to bits 1 and 2.

Downloaded from Arrow.com.

3.4.5 RSSI/CCA result register (BBRSSICCARSLT)

Stores the result data of CCA/ED or RSSI.

The CCA result select bit can be used to switch between the CCA/ED value and the RSSI value.

The result corresponding to the save bank which is specified by the receive data save bank select bit is read out when reading the RSSI value.

The read data is expressed as 2's complement. The unit is dBm (**ex.** "19EH" is "-98dBm").

The BBRSSICCARSLT register is read by the serial interface in 8-bit units.

Reset signal generation clears this register to 0000H.

Figure 3 - 9 RSSI/CCA Result Register (BBRSSICCARSLT) Format

Address: 0005H, 0004H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBRSSICCARSLT	0	0	0	0	0	0	0	CCARSLT8
	7	6	5	4	3	2	1	0
	CCARSLT7	CCARSLT6	CCARSLT5	CCARSLT4	CCARSLT3	CCARSLT2	CCARSLT1	CCARSLT0

CCARSLT8 to CCARSLT0	RSSI/CCA result data

Caution "0" is always read for bits 15 to 9.

The loss of antenna input signal revel defers causing LSI board layout and usage of RFSW or SAW filter. Therefore, setting values are required modification to match the input level and value of RSSI/CCA result register (BBRSSICCARSLT). The value of receive level threshold setting register (BBLVLVTH) also required modification.

Set values in Table 3 - 5 Register setting for loss of input signal level from antenna in IDLE state to cancel the loss. The values are deferent for operation enabled/disabled FEC.

The values in Table 5 - 8 Settings Required for Each Data Rate are reference measured on evaluation board of Renesas Electronics.

Caution Refer to the latest application note for setting data in Table 3 - 5 when to use the product.

Downloaded from Arrow.com.

Table 3 - 5 Register setting for loss of input signal level from antenna **(1/4)**

Frequency band identifier	PHY	Mode	Data rate (kbps)	1dB loss						
				0044		0483	047C	047D	047E	047F
				FEC: Enabled	FEC: Disable					
4	863MHz (Europe)	001	50	87	8F	3F	1B	0F	03	34
		002	100	8E	96	3F	1A	0E	02	33
		003	200	8E	96	3F	1A	0E	02	34
5	896MHz (US)	004	10	84	8C	0A	1B	0F	03	34
		005	20	88	90	04	1A	0F	03	34
		006	40	8C	94	04	1A	0F	03	34
6	901MHz (US)	007	10	84	8C	0A	1B	0F	03	34
		008	20	88	90	04	1A	0F	03	34
		009	40	8C	94	04	1A	0F	03	34
7	915MHz (US)	010	50	8D	95	3C	1B	0F	03	34
		011	150	92	9A	0A	1B	0F	03	34
		012	200	91	99	0A	1B	0F	03	34
8	917MHz (Korea)	013	50	8D	95	3F	1A	0E	02	33
		014	150	92	9A	0A	1B	0F	03	34
		015	200	91	99	0A	1B	0F	03	34
9	920MHz (Japan)	016	50	8D	95	3D	1B	0F	03	34
		000	100	8E	96	3E	1B	0F	03	34
		017	200	93	9B	3D	1B	0F	03	34
		018	400	8D	95	3D	1B	0F	03	34
other		019	300	95	9D	1A	19	0D	03	33
		020	100	8E	96	3E	1B	0F	03	34
		021	300	95	9D	1A	19	0D	03	33

Downloaded from Arrow.com.

Table 3 - 5 Register setting for loss of input signal level from antenna **(2/4)**

Frequency band identifier	PHY	Mode	Data rate (kbps)	2dB loss						
				0044		0483	047C	047D	047E	047F
				FEC: Enabled	FEC: Disable					
4	863MHz (Europe)	001	50	88	90	3F	1A	0E	02	33
		002	100	8F	97	3F	19	0D	01	32
		003	200	8F	97	3F	19	0D	01	33
5	896MHz (US)	004	10	85	8D	0B	1B	0F	03	34
		005	20	89	91	05	1A	0F	03	34
		006	40	8D	95	05	1A	0F	03	34
6	901MHz (US)	007	10	85	8D	0B	1B	0F	03	34
		008	20	89	91	05	1A	0F	03	34
		009	40	8D	95	05	1A	0F	03	34
7	915MHz (US)	010	50	8E	96	3D	1B	0F	03	34
		011	150	93	9B	0B	1B	0F	03	34
		012	200	92	9A	0B	1B	0F	03	34
8	917MHz (Korea)	013	50	8E	96	3F	19	0D	01	32
		014	150	93	9B	0B	1B	0F	03	34
		015	200	92	9A	0B	1B	0F	03	34
9	920MHz (Japan)	016	50	8E	96	3E	1B	0F	03	34
		000	100	8F	97	3F	1B	0F	03	34
		017	200	94	9C	3E	1B	0F	03	34
		018	400	8E	96	3E	1B	0F	03	34
other		019	300	96	9E	1B	19	0D	03	33
		020	100	8F	97	3F	1B	0F	03	34
		021	300	96	9E	1B	19	0D	03	33

Downloaded from Arrow.com.

Table 3 - 5 Register setting for loss of input signal level from antenna **(3/4)**

Frequency band identifier	PHY	Mode	Data rate (kbps)	3dB loss						
				0044		0483	047C	047D	047E	047F
				FEC: Enabled	FEC: Disable					
4	863MHz (Europe)	001	50	89	91	3F	19	0D	01	32
		002	100	90	98	3F	18	0C	00	31
		003	200	90	98	3F	18	0C	00	32
5	896MHz (US)	004	10	86	8E	0C	1B	0F	03	34
		005	20	8A	92	06	1A	0F	03	34
		006	40	8E	96	06	1A	0F	03	34
6	901MHz (US)	007	10	86	8E	0C	1B	0F	03	34
		008	20	8A	92	06	1A	0F	03	34
		009	40	8E	96	06	1A	0F	03	34
7	915MHz (US)	010	50	8F	97	3E	1B	0F	03	34
		011	150	94	9C	0C	1B	0F	03	34
		012	200	93	9B	0C	1B	0F	03	34
8	917MHz (Korea)	013	50	8F	97	3F	18	0C	00	31
		014	150	94	9C	0C	1B	0F	03	34
		015	200	93	9B	0C	1B	0F	03	34
9	920MHz (Japan)	016	50	8F	97	3F	1B	0F	03	34
		000	100	90	98	3F	1A	0E	02	33
		017	200	95	9D	3F	1B	0F	03	34
		018	400	8F	97	3F	1B	0F	03	34
other		019	300	97	9F	1C	19	0D	03	33
		020	100	90	98	3F	1A	0E	02	33
		021	300	97	9F	1C	19	0D	03	33

Downloaded from Arrow.com.

Table 3 - 5 Register setting for loss of input signal level from antenna **(4/4)**

Frequency band identifier	PHY	Mode	Data rate (kbps)	4dB loss						
				0044		0483	047C	047D	047E	047F
				FEC: Enabled	FEC: Disable					
4	863MHz (Europe)	001	50	8A	92	3F	18	0C	00	31
		002	100	91	99	3F	17	0B	3F	30
		003	200	91	99	3F	17	0B	3F	31
5	896MHz (US)	004	10	87	8F	0D	1B	0F	03	34
		005	20	8B	93	07	1A	0F	03	34
		006	40	8F	97	07	1A	0F	03	34
6	901MHz (US)	007	10	87	8F	0D	1B	0F	03	34
		008	20	8B	93	07	1A	0F	03	34
		009	40	8F	97	07	1A	0F	03	34
7	915MHz (US)	010	50	90	98	3F	1B	0F	03	34
		011	150	95	9D	0D	1B	0F	03	34
		012	200	94	9C	0D	1B	0F	03	34
8	917MHz (Korea)	013	50	90	98	3F	17	0B	3F	30
		014	150	95	9D	0D	1B	0F	03	34
		015	200	94	9C	0D	1B	0F	03	34
9	920MHz (Japan)	016	50	90	98	3F	1A	0E	02	33
		000	100	91	99	3F	19	0D	01	32
		017	200	96	9E	3F	1A	0E	02	33
		018	400	90	98	3F	1A	0E	02	33
other		019	300	98	A0	1D	19	0D	03	33
		020	100	91	99	3F	19	0D	01	32
		021	300	98	A0	1D	19	0D	03	33

Downloaded from Arrow.com.

3.4.6 Enhanced-ACK mode register (BBEACKMODE)

This register sets the enhanced ACK mode.

The BBEACKMODE register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 01H.

Figure 3 - 10 Enhanced ACK Mode Register (BBEACKMODE) Format

Address: 0006H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBEACK MODE	0	0	0	0	0	0	0	ENHACKMO DEBIT

ENHACKMO DEBIT	Enhanced ACK Mode bit
0	Enhanced ACK Mode function disabled
1	Enhanced ACK Mode

Caution Be sure to set “0” to bits 1 to 7.

Downloaded from Arrow.com.

3.4.7 Transmit/receive status register 0 (BBTXRXST0)

This register stores the RF transmit/receive status.

It stores the CCA judge result in bit 0.

It stores the CRC judge result in bit 1. The CRC result corresponding to the save bank which is specified by the receive data save bank select bit is read out when reading.

It stores the CSMA-CA judge result in bit 2.

The transmit/receive operation completion judge result bit is used to store the result of transmit/receive operation sequence (CSMA-CA → Transmit → ACK receive → Retransmit → ACK receive, and so on) judge upon completion. The result is NG (no good) when the ACK receive cannot be performed even if the sequences from the transmission of the number of setting times to the ACK receive are repeated.

The receive RAM bank 0 status bit and the receive RAM bank 1 status bit can be used as flags upon data capture for the respective receive RAM banks 0 and 1.

1 is automatically set upon completion of the data receive. Later on, they are cleared to 0 by software after reading the receive RAM data. Set 1 when no data is written because setting 0 enables writing. A receive overrun interrupt occurs when data is received again under the status that 1 is set to these bits resulting in the occurrence of write to each receive RAM.

It stores the pending bit data of the received ACK data in the receive pending bit upon completion of the reception of only the ACK data.

The receive RAM bank pointer bit can be used to check the receive RAM bank after the completion of receive. It indicates 1 after reset or initialization. This bit changes when the receive RAM bank is full or when the frame receive is complete.

The BBTXRXST0 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 80H.

Downloaded from Arrow.com.

Figure 3 - 11 Transmit/Receive Status Register 0 (BBTXRXST0) Format

Address: 0007H After reset: 80H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBTXRXST0	RCVRAMST	RCVPEND	RCVBANK1	RCVBANK0	TRNRCVSQC	CSMACA	CRC	CCA

RCVRAMST	Receive RAM bank pointer bit
0	Receive RAM bank 0
1	Receive RAM bank 1

RCVPEND	Receive pending bit
0	No pending
1	Pending exists

RCVBANK1	Receive RAM bank 1 status bit
0	Receive enabled
1	Receive data exists

RCVBANK0	Receive RAM bank 0 status bit
0	Receive enabled
1	Receive data exists

TRNRCVSQC	Transmit/receive operation completion judge result bit
0	OK
1	NG

CSMACA	CSMA-CA judge result bit
0	OK
1	NG

CRC	CRC judge result bit
0	OK
1	NG

CCA	CCA judge result bit
0	Channel clear
1	Channel busy

Note Bits 0 to 3, 6, and 7 are Read Only.

Downloaded from Arrow.com.

3.4.8 Transmit/receive mode register 2 (BBTXRXMODE2)

This register sets the various types of the RF transmit/receive mode.

The automatic CRC disable bit can be used to select between to transmit with the CRC calculation result automatically attached upon transmit, and to transmit the data on the RAM.

The frame pending bit can be used to set with/without the frame pending upon ACK reply when the address matches on the first address side. Information on this bit is automatically included in the ACK replay data.

The frame pending status bit is used to display whether the reply is made with frame pending or not upon the automatic ACK reply. The display is updated at the same time of the occurrence of interrupt request upon completion of the transmission. The information on the frame pending upon reply by the save bank which is selected by the receive data save bank select bit is read upon reading because this bit left the result of the automatic ACK reply for every received save bank.

The enhanced ACK enable bit can be used to support the enhanced ACK reply function.

It can be used to set the number of retransmission times by using the retransmission counter when there is no ACK reply even if the automatic ACK receive mode is enabled. The value ranged from 0000b through 1000b can be set.

The BBTXRXMODE2 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 30H.

Figure 3 - 12 Transmit/Receive Mode Register 2 (BBTXRXMODE2) Format

Address: 0009H After reset: 30H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBTXRX MODE2	RETRN3	RETRN2	RETRN1	RETRN0	ENHACKEN	FLMPENDST	FLMPEND	NOCRC

RETRN3 to RETRN0	Retransmission counter (From 0000B up to 1000B can be set.)

ENHACKEN	Enhanced ACK Enable bit
0	Enhanced ACK disabled
1	Enhanced ACK enabled

FLMPENDST	Frame pending status bit
0	No frame pending
1	Frame pending exists

FLMPEND	Frame pending bit
0	No frame pending
1	Frame pending exists

NOCRC	Automatic CRC enable bit
0	Enable
1	Disable

Note Bit 2 is Read Only.

Downloaded from Arrow.com.

3.4.9 Transmit/receive mode register 3 (BBTXRXMODE3)

This register sets the various types of the RF transmit/receive mode.
The address filter enable bit can be used to enable the address filter upon receiving.
When this bit is set to “1”, address filter on first address side is enabled.
The PAN coordinator bit can be used to set whether the PAN coordinator is set as one of the address filter conditions on first address side.
Reception is enabled by receive enable bit. The bit must be set to 1 in receive operation.
Receive level filter enable bit can be used to suspend reception and enable receive level filter interrupt when a communication error occurs such as no signal state during frame reception. The state enters to waiting reception again after the suspension through IDLE automatically. Receive completion interrupt does not occur because the suspension is done during frame reception. Destroy the receive frame when receive level filter interrupt occurs. An overwrite enable processing might be required depending on the destroyed timing. Then changing to enable reception of receive bank 0, 1 status bits for corresponding bank, or enabling receive RAM overwrite enable bit is required. Set this bit and receive level filter interrupt enable bit to “1” in initialization.
The receive data save bank select bit specifies the save bank to access the read of the receive-related data (other than the receive RAM).
The receive RAM overwrite enable bit can control the overwrite to the receive RAM. However, the receive data is not overwritten when write access to each receive RAM occurs when the above bit is 0 and receive RAM bank status bit is 1. The receive data is overwritten when write access to each receive RAM occurs when the receive RAM overwrite enable bit is 1 even if the receive RAM bank status bit is 1.
The address filter address extension bit can extend the first address and the second address in two ways.
The address filter general-purpose mode bit can set the address filter operation to the general-purpose mode.
The BBTXRXMODE3 register is set by the serial interface in 8-bit units.
Reset signal generation clears this register to 00H.

Downloaded from Arrow.com.

Figure 3 - 13 Transmit/Receive Mode Register 3 (BBTXRXMODE3) Format

Address: 000AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXMODE3	ADFGENMODE	ADFEXTEN	RCVOVERWREN	RCVBANKSEL	LVLFILEN	RXEN	PANCORD	ADRSFILEN

ADFGENMODE	Address filter general-purpose mode bit
0	The WiSUN mode
1	The general purpose mode

ADFEXTEN	Address filter address extension bit
0	PANID&Address expansion disabled
1	PANID&Address expansion enabled

RCVOVERWREN	Receive RAM overwrite enable bit
0	Overwrite disabled
1	Overwrite enabled

RCVBANKSEL	Receive data save bank select bit
0	Select receive data save bank 0
1	Select receive data save bank 1

LVLFILEN	Receive level filter enable bit
0	Filter disabled
1	Filter enabled

RXEN	Receive enable bit
0	Receive disabled
1	Receive enabled

PANCORD	PAN coordinator bit
0	Not a PAN coordinator
1	PAN coordinator

ADRSFILEN	Address filter enable bit
0	Address filter disabled
1	Address filter enabled

Downloaded from Arrow.com.

3.4.10 Transmit/receive status register 1 (BBTXRXST1)

The receive data save bank pointer bit can be used to check the bank which stores the data, for example frame length of the received frame. It indicates 1 after reset or initialization.

The BBTXRXST1 register is read by the serial interface in 8-bit units.

Reset signal generation clears this register to 02H.

Figure 3 - 14 Transmit/Receive Status Register 1 (BBTXRXST1) Format

Address: 000BH After reset: 02H R

Symbol	7	6	5	4	3	2	1	0
BBTXRXST1	0	0	0	0	0	0	RCVSTOREST	X

RCVSTOREST	Receive data save bank pointer bit
0	Receive data save bank 0
1	Receive data save bank 1

Caution “0“ is always read for bits 2 to 7.
Bit 0 is read as x (undefined).

Downloaded from Arrow.com.

3.4.11 Transmit/receive control register (BBTXRXCON)

This register controls the RF transmit/receive.
Setting “1” to the receive trigger bit starts warm-up of the RF circuit and enters into the reception available state after 240 µs.
Setting “1” to the transmit trigger bit starts warm-up of the RF circuit and enters transmission after 350 µs.
Setting “1” to the CCA trigger bit starts warm-up of the RF circuit and enters CCA operation after 240 µs. Set value other than 0H to BEMIN bits to perform CCA.

Be sure to set these bits under the state they are IDLE. Note that these bits are automatically cleared to “0” upon completion of transmit/receive or of CCA. Stop the reception by using the RF communication stop bit when you want to stop the operation in the middle.
Do not stop transmission during the operation.
The automatic ACK receive mode bit can select whether to perform the automatic ACK receive operation.
The BBTXRXCON register is set by the serial interface in 8-bit units.
Reset signal generation clears this register to 00H.

Figure 3 - 15 Transmit/Receive Control Register (BBTXRXCON) Format

Address: 000CH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBTXRXCON	0	0	0	0	ACKRCVEN	CCATRG	TRNTRG	RCVTRG

ACKRCVEN	Automatic ACK receive mode bit
0	Auto ACK receive disabled
1	Auto ACK receive enabled

CCATRG	CCA trigger bit
0	Nothing performed
1	CCA start

TRNTRG	Transmission trigger bit
0	Nothing performed
1	Transmission start

RCVTRG	Receive trigger bit
0	Nothing performed
1	Receive start

Caution **Be sure to set “0” to bits 4 to 7.**

Note Bits 2 to 0 are Write Only.

Downloaded from Arrow.com.

3.4.12 CSMA control register 0 (BBCSMACON0)

This register controls the CSMA-CA operation.

Setting “1” to the automatic CSMA-CA start bit starts the CSMA-CA operation. Be sure to set this bit under the state it is IDLE. Note that these bits are automatically cleared to “0” upon completion of the CSMA-CA operation. In addition, setting “0” also disables writing.

Stop the CSMA-CA operation by using the RF communication stop bit when you want to stop the CSMA-CA operation.

Setting “1” to the transmit after automatic CSMA-CA bit automatically performs the transmission process if it's okay after the completion of the CSMA-CA operation.

Setting “1” to the reception during CSMA-CA function enable bit enables the reception during the wait time for the CCA operation in the CSMA-CA operation.

The back off period count stops during a frame reception.

The unicast frame bit sets the unicast frame value. Setting “1” to the unicast frame enable bit enables the function.

The BBCSMACON0 register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 16 CSMA Control Register 0 (BBCSMACON0) Format

Address: 000DH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBCSMACON0	0	0	0	UNICASTFRM	0	CSMARCVEN	CSMATRNST	CSMAST

UNICASTFRM	Unicast frame bit
0	Unicast frame value = 0
1	Unicast frame value = 1

CSMARCVEN	Reception during CSMA-CA function enable bit
0	Receive function disabled
1	Receive function enabled

CSMATRNST	Transmit after automatic CSMA-CA bit
0	Nothing performed
1	Transmit after CSMA-CA process

CSMAST	Automatic CSMA-CA start bit
0	Nothing performed
1	Automatic CSMA-CA start

Caution Be sure to set “0” to bits 3, 5 to 7.

Note Bits 0 is Write Only.

Downloaded from Arrow.com.

3.4.13 CCA level threshold setting register (BBCCAVTH)

This register is used to set the threshold level to judge the CCA. It judges as busy for the CCA value which is the value set to this register or greater.The value is set as 2's complement. The setting unit is dBm (**ex.** "19EH" is " -98dBm").

The BBCCAVTH register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 0100H.

Figure 3 - 17 CCA Level Threshold Setting Register (BBCCAVTH) Format

Address: 000FH, 000EH After reset: 0100H R/W

Symbol	15	14	13	12	11	10	9	8
BBCCAVTH	0	0	0	0	0	0	0	CCAVTH8
	7	6	5	4	3	2	1	0
	CCAVTH7	CCAVTH6	CCAVTH5	CCAVTH4	CCAVTH3	CCAVTH2	CCAVTH1	CCAVTH0

CCAVTH8 to CCAVTH0	CCA threshold level value

Caution Be sure to set "0" to bits 9 to 15.

3.4.14 Transmit/receive status register 2 (BBTXRXST2)

This register stores the information on the various types of the RF transmit/receive status.

The receive RAM bank flag bit is used to indicate the receive RAM bank upon start of the reception.

The receive data storage bank flag bit is used to indicate the reception storage bank upon start of the reception.

The BBTXRXST2 register is read by the serial interface in 8-bit units.

Reset signal generation sets this register to 03H.

Figure 3 - 18 Transmit/Receive Status Register 2 (BBTXRXST2) Format

Address: 0010H After reset: 03H R

Symbol	7	6	5	4	3	2	1	0
BBTXRXST2	0	0	0	0	0	0	RCVSTORE FLG	RCVBANKF LG

RCVSTORE FLG	Receive data storage bank flag bit
0	Receive data storage bank 0
1	Receive data storage bank 1

RCVBANKF LG	Receive RAM bank flag bit
0	Receive RAM bank 0
1	Receive RAM bank 1

Caution "0" is always read for bits 2 to 7.

Downloaded from Arrow.com.

3.4.15 Transmit/receive mode register 4 (BBTXRXMODE4)

This register sets the various types of the RF transmit/receive mode.

The CCA interrupt select bit can be used to select the CCA interrupt source between the time upon completion of the CCA sequence and the time upon completion of the CSMA-CS sequence.

The INT output polarity switch bit can be used to select the interrupt polarity of the interrupt output from the INTOUT pin.

Automatic receive with timeout after transmit enable bit enables automatic receive with timeout after transmit by automatic receive switch mode 0 enable bit. Byte receive interrupt and receive timeout interrupt can be switched by receive timeout interrupt switch bit.

The BBTXRXMODE4 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 01H.

Figure 3 - 19 Transmit/Receive Mode Register 4 (BBTXRXMODE4) Format

Address: 0011H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXMODE4	TIMEOUTINTSEL	TIMEOUTRCV	0	INTOUTSEL	0	0	0	CCAINTSEL

TIMEOUTINTSEL	Receive timeout interrupt switch bit
0	Byte receive interrupt
1	Receive timeout interrupt

TIMEOUTRCV	Automatic receive with timeout after transmit enable bit
0	Automatic normal reception mode
1	Automatic reception with timeout mode

INTOUTSEL	INT output polarity switch bit
0	When with the interrupt request = high level
1	When with the interrupt request = low level

CCAINTSEL	CCA interrupt select bit
0	Upon completion of the CCA sequence
1	Upon completion of the CSMA-CA sequence

Caution Be sure to set “0” to bit 1 to 3 and 5.

Downloaded from Arrow.com.

3.4.16 CSMA control register 1 (BBCSMACON1)

This register controls the CSMA-CA operation.

The NB bit is used to set the macMaxCSMABackoff value. (Initial value is 0H)

The CW bit is used to set the CW value. (Initial value is 2H)

The BBCSMACON1 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 20H.

Figure 3 - 20 CSMA Control Register 1 (BBCSMACON1) Format

Address: 0012H After reset: 20H R/W

Symbol	7	6	5	4	3	2	1	0
BBCSMACON1			CW1	CW0		NB2	NB1	NB0

CW1, CW0	CW value

NB2 to NB0	The macMaxCSMABackoff value

Caution Be sure to set “0” to bits 3, 6 and 7.

Downloaded from Arrow.com.

3.4.17 CSMA control register 2 (BBCSMACON2)

This register controls the CSMA-CA operation.

The BEMAX bit is used to set the macMaxBE value. (Initial value is 5H) Set the greater value for the BEMAX bit than the BEMIN bit setting value.

The MacMinBE control bit can be used to set with/without the CCA operation when “000b” is set to macMinBE which is a parameter of automatic CSMA-CA.

The unicast frame enable bit can be used to set the operation by the unicast frame bit.

The BBCSMACON2 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 05H.

Figure 3 - 21 CSMA Control Register 2 (BBCSMACON2) Format

Address: 0013H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
BBCSMACON2	0	0	UNICASTFREN	MACMINBECON	BEMAX3	BEMAX2	BEMAX1	BEMAX0

UNICASTFREN	Unicast frame enable bit
0	Unicast frame disabled
1	Unicast frame enabled

MACMINBECON	MacMinBE control bit
0	Without the CCA operation
1	With the CCA operation

BEMAX3 to BEMAX0	MacMaxBE value

Caution Be sure to set “0” to bits 6 and 7.

Downloaded from Arrow.com.

3.4.18 PAN identifier register 0 (BBPANID0)

This register is used to set the PAN identifier of the first address filter. It consists of 16 bits and is used to detect the match with a received PAN identifier.

The BBPANID0 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to FFFFH.

Figure 3 - 22 PAN Identifier Register 0 (BBPANID0) Format

Address: 0015H, 0014H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBPANID0								

7	6	5	4	3	2	1	0

BBPANID0	PAN identifier

3.4.19 Short address register 0 (BBSHORTAD0)

This register is used to set the short address of the first address filter. It consists of 16 bits and is used to detect the match with a received PAN identifier.

The BBSHORTAD0 register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to FFFFH.

Figure 3 - 23 Short Address Register 0 (BBSHORTAD0) Format

Address: 0017H, 0016H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBSHORTAD0								

7	6	5	4	3	2	1	0

BBSHORTAD0	Short address

Downloaded from Arrow.com.

3.4.20 Extended address register 0 (BBEXTENDAD00 to BBEXTENDAD03)

These registers are used to set the extended address of the first address filter. They consist of 64 bits (16 bit timed by 4) and are used to detect the match with a received extended address.
The BBEXTENDAD00 to BBEXTENDAD03 registers are set by the serial interface in 8-bit units.
Reset signal generation clears these registers to 0000H.

Figure 3 - 24 Extended Address Register 0 (BBEXTENDAD00-BBEXTENDAD03) Format

Address: 001FH, 001EH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD03								
	7	6	5	4	3	2	1	0

BBEXTENDAD03	Extended address bits 63 to 48

Address: 001DH, 001CH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD02								
	7	6	5	4	3	2	1	0

BBEXTENDAD02	Extended address bits 47 to 32

Address: 001BH, 001AH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD01								
	7	6	5	4	3	2	1	0

BBEXTENDAD01	Extended address bits 31 to 16

Address: 0019H, 0018H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD00								
	7	6	5	4	3	2	1	0

BBEXTENDAD00	Extended address bits 15 to 0

Downloaded from Arrow.com.

3.4.21 Timer read registers (BBTIMEREAD0, BBTIMEREAD1)

These registers are used to read the current count value of the 32-bit timer. Read from the lower bytes when reading the timer count value. Then continue to read the upper bytes because the count value is latched when reading the 0020H address of LSB.

The BBTIMEREAD0 and BBTIMEREAD1 registers are read by the serial interface in 8-bit units.

Reset signal generation clears these registers to 0000H.

Figure 3 - 25 Timer Read Register 0 (BBTIMEREAD0) Format

Address: 0021H, 0020H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTIMEREAD0								
	7	6	5	4	3	2	1	0

BBTIMEREAD0	Lower bits of the 32-bit timer (bits 15 to 0)

Figure 3 - 26 Timer Read Register 1 (BBTIMEREAD1) Format

Address: 023H, 0022H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTIMEREAD1								
	7	6	5	4	3	2	1	0

BBTIMEREAD1	Upper bits of the 32-bit timer (bits 31 to 16)

Downloaded from Arrow.com.

3.4.22 Timer compare registers

(BBTCOMP0REG0 to BBTCOMP2REG0, BBTCOMP0REG1 to BBTCOMP2REG1)

These registers are used to compare with the 32-bit timer. Each of them includes three channels to compare each of the channels with the 32-bit timer.

The BBTCOMP0REG0 to BBTCOMP2REG0 registers and BBTCOMP0REG1 to BBTCOMP2REG1 registers are set by the serial interface in 8-bit units.

Reset signal generation clears these registers to 0000H.

Figure 3 - 27 Timer Compare Register 0 (BBTCOMP0REG0 to BBTCOMP2REG0) Format

Address: 002DH, 002CH (BBTCOMP2REG0), 0029H, 0028H (BBTCOMP1REG0), 0025H, 0024H (BBTCOMP0REG0)
After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTCOMPnREG0 (n = 0 to 2)								
	7	6	5	4	3	2	1	0

BBTCOMPnREG0	Lower bits of the 32-bit compare (bits 15 to 0) (n = 0 to 2)

Figure 3 - 28 Timer Compare Register 1 (BBTCOMP0REG1 to BBTCOMP2REG1) Format

Address: 002FH, 002EH (BBTCOMP2REG1), 002BH, 002AH (BBTCOMP1REG1), 0027H, 0026H (BBTCOMP0REG1)
After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTCOMPnREG1 (n = 0 to 2)								
	7	6	5	4	3	2	1	0

BBTCOMPnREG1	Upper bits of the 32-bit compare (bits 31 to 16) (n = 0 to 2)

Downloaded from Arrow.com.

3.4.23 Time stamp registers 0 and 1 (BBTSTAMP0, BBTSTAMP1)

These registers are used to store the timer values upon the packet data receive start, upon the completion of the packet data reception, or upon completion of the packet data transmission. The respective time stamps of receive/transmit are stored. Therefore, the read value can be selected among the values of the receive start stamp, receive completion stamp, and the transmission stamp by using the stamp value read switch bit.

The timer count value upon completion of receive is automatically stored in the time stamp register while the stamp value is retained until the next packet receive completion. The time stamp value corresponding to the save bank which is specified by the receive data save bank select bit is read out when reading.

In addition, the timer count upon completion of the transmission is automatically stored in the time stamp register. The stamp value is retained until the next packet transmission completion. However, the transmission time stamp value is not updated upon automatic ACK reply.

The BBTSTAMP0 and BBTSTAMP1 registers are read by the serial interface in 8-bit units.

Reset signal generation clears these registers to 0000H.

Figure 3 - 29 Time Stamp Register 0 (BBTSTAMP0) Format

Address: 0031H, 0030H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTSTAMP0								
	7	6	5	4	3	2	1	0

BBTSTAMP0	Lower bits of the 32-bit timer (bits 15 to 0)

Figure 3 - 30 Time Stamp Register 1 (BBTSTAMP1) Format

Address: 0033H, 0032H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTSTAMP1								
	7	6	5	4	3	2	1	0

BBTSTAMP1	Lower bits of the 32-bit timer (bits 31 to 16)

Downloaded from Arrow.com.

3.4.24 Timer control register (BBTIMECON)

This register is used to control the timer in this transceiver.

The timer count enable bit controls the 32-bit timer count operation. Setting “1” enables the timer count. In addition, setting “0” stops the timer while the count value is initialized to 00000000H.

The RF transmit can be started when the compare 0 value and timer value match by using the COMP0 transmit trigger enable bit. Warm-up starts immediately after the match and starts transmit after 350 µs. Be sure to set these bit under the state they are IDLE.

The stamp timing switch bit can be used to select the stamp timing of the timer value. The value is updated at the timing of receive start regardless of the address filter function when selecting the receive start time.

The COMP0 trigger function select bit can be used to select the CSMA-CA for the start function when COMP0TRG is enabled.

The stamp value read switch bit can be used to select the time stamp register read value among the receive start stamp value, receive completion stamp value, and the transmission completion stamp value.

The count source switch bit can be used to select the count source for the timer count between the prescaler output and the data rate.

The BBTIMECON register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Downloaded from Arrow.com.

Figure 3 - 31 Timer Control Register (BBTIMECON) Format

Address: 0034H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTIMECON	0	CNTSRCSEL	STAMPRDSEL1	STAMPRDSEL0	COMP0TRGSEL	STAMPTIMSEL	COMP0TRG	TIMEEN

CNTSRCSEL	Count source switch bit
0	Prescaler output (1 μs)
1	Data rate

STAMPRDSEL1	STAMPRDSEL0	Stamp value read switch bit
0	0	Receive start stamp value
0	1	Receive completion stamp value
1	0	Transmit completion stamp value
1	1	

COMP0TRGSEL	COMP0 trigger function select bit
0	Transmit trigger
1	CSMA-CA trigger

STAMPTIMSEL	Stamp timing switch bit
0	Upon receive start
1	Upon interrupt of receive FL

COMP0TRG	COMP0 transmit trigger enable bit
0	Transmit trigger disabled
1	Transmit trigger enabled

TIMEEN	Timer count enable bit
0	Timer count stop
1	Timer count enable

Caution Be sure to set “0” to bit 7.

Downloaded from Arrow.com.

3.4.25 Back off period register (BBBOFFPROD)

This register is used to control the back off period.

The back off period auto random enable bit is used to automatically generate the random value with setting the value set to the back off period bit as an initial value, and to set the back off period value in the CSMA-CA circuit. Set the random value to the back-off period register 2, and then set “1” to the back off period auto random enable bit of the back off period register.

The BBBOFFPROD register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 32 Back off Period Register (BBBOFFPROD) Format

Address: 0035H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBBOFFPROD	0	0	0	0	0	0	0	BOFFPRODEN

BOFFPRODEN	Back-off period automatic random enable bit
0	Disable
1	Automatic random value generation enabled

Caution Be sure to set “0” to bits 1 to 7.

3.4.26 Baseband interrupt source register 0 (BBINTREQ0)

This register is used to indicate the baseband interrupt source.

This register indicates that “1” is set to the interrupt source corresponding to each interrupt occurrence timing so that there is an interrupt request. When reading this register, only the bit from which 1 is read is cleared to 0. Note that perform the dummy read when you clear the bit because writing is disabled.

The BBINTREQ0 register is read by the serial interface in 8-bit units.Note

Reset signal generation clears this register to 00H.

Note When reading this register, read 3 bytes of the baseband interrupt source registers 0 to 2 (BBINTREQ0 to BBINTREQ2) continuously (leave SEN pin low level).

Downloaded from Arrow.com.

Figure 3 - 33 Baseband Interrupt Source Register 0 (BBINTREQ0) Format

Address: 0036H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBINTREQ0	CCAINTREQ	CALINTREQ	TRN1INTREQ	TRN0INTREQ	TRNFININTREQ	TIM2INTREQ	TIM1INTREQ	TIM0INTREQ

CCAINTREQ	CCA completion interrupt source bit
0	No request
1	Request exists

CALINTREQ	Calibration completion interrupt source bit
0	No request
1	Request exists

TRN1INTREQ	Bank 1 transmit completion interrupt source bit
0	No request
1	Request exists

TRN0INTREQ	Bank 0 transmit completion interrupt source bit
0	No request
1	Request exists

TRNFININTREQ	Frame transmit completion interrupt source bit
0	No request
1	Request exists

TIM2INTREQ	Timer compare 2 interrupt source bit
0	No request
1	Request exists

TIM1INTREQ	Timer compare 1 interrupt source bit
0	No request
1	Request exists

TIM0INTREQ	Timer compare 0 interrupt source bit
0	No request
1	Request exists

Downloaded from Arrow.com.

3.4.27 Baseband interrupt source register 1 (BBINTREQ1)

This register is used to indicate the baseband interrupt source.

A bit of this register indicates that “1” is set to the interrupt source corresponding to each interrupt occurrence timing so that there is an interrupt request. When reading this register, only the bit from which 1 is read is cleared to 0. Note that perform the dummy read when you clear the bit because writing is disabled.

The BBINTREQ1 register is read by the serial interface in 8-bit units.Note

Reset signal generation clears this register to 00H.

Note When reading this register, read 3 bytes of the baseband interrupt source registers 0 to 2 (BBINTREQ0 to BBINTREQ2) continuously (leave SEN pin low level).

Downloaded from Arrow.com.

<R>

Figure 3 - 34 Baseband Interrupt Source Register 1 (BBINTREQ1) Format

Address: 0037H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBINTREQ1	LVLFILINTREQ	MODESWINTREQ	ROVRINTREQ	ADRSINTREQ	RCVSTINTREQ	RCV1INTREQ	RCV0INTREQ	RCVFININTREQ

LVLFILINTREQ	Receive level filter interrupt source bit
0	No request
1	Request exists

MODESWINTREQ	Mode switch receive completion interrupt source bit
0	No request
1	Request exists

ROVRINTREQ	Receive overrun interrupt source bit
0	No request
1	Request exists

ADRSINTREQ	Address filter interrupt source bit
0	No request
1	Request exists

RCVSTINTREQ	Receive start interrupt source bit
0	No request
1	Request exists

RCV1INTREQ	Bank 1 receive completion interrupt source bit
0	No request
1	Request exists

RCV0INTREQ	Bank 0 receive completion interrupt source bit
0	No request
1	Request exists

RCVFININTREQ	Frame receive completion interrupt source bit
0	No request
1	Request exists

Downloaded from Arrow.com.

3.4.28 Baseband interrupt source register 2 (BBINTREQ2)

This register is used to indicate the baseband interrupt source.

This register indicates that “1” is set to the interrupt source corresponding to each interrupt occurrence timing so that there is an interrupt request. When reading this register, only the bit from which 1 is read is cleared to 0. Note that perform the dummy read when you clear the bit because writing is disabled.

Register BBINTREQ2 is read by the serial interface in 8-bit units.Note

Reset signal generation clears this register to 00H.

Note When reading this register, read 3 bytes of the baseband interrupt source registers 0 to 2 (BBINTREQ0 to BBINTREQ2) continuously (leave SEN pin low level).

<R> **Figure 3 - 35 Baseband Interrupt Source Register 2 (BBINTREQ2) Format**

Address: 0038H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBINTREQ2	X	BYTERCVINTREQ	FLINTREQ	RCVCUNTINTREQ	X	X	X	X

BYTERCVINTREQ	Byte receive completion interrupt source bit
0	No request
1	Request exists

FLINTREQ	Frame length interrupt source bit
0	No request
1	Request exists

RCVCUNTINTREQ	Number of received byte interrupt source bit
0	No request
1	Request exists

Caution Bit 0 to 3 , 7 are x (undefined).

Downloaded from Arrow.com.

3.4.29 Baseband interrupt enable register 0 (BBINTEN0)

This register is used to enable the baseband interrupt.

This register enables the interrupt output from the INTOUT pin upon generation of each interrupt. Set “1” to the corresponding interrupt enable bit when you want to enable the interrupt output.

The BBINTEN0 register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 36 Baseband Interrupt Enable Register 0 (BBINTEN0) Format

Address: 0039H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINTEN0	CCAINTEN	CALINTEN	TRN1INTEN	TRN0INTEN	TRNFININTEN	TIM2INTEN	TIM1INTEN	TIM0INTEN

CCAINTEN	CCA completion interrupt enable bit
0	Disabled
1	Enabled

CALINTEN	Calibration completion interrupt enable bit
0	Disabled
1	Enabled

TRN1INTEN	Bank 1 transmit completion interrupt enable bit
0	Disabled
1	Enabled

TRN0INTEN	Bank 0 transmit completion interrupt enable bit
0	Disabled
1	Enabled

TRNFININTEN	Frame transmit completion interrupt cause bit
0	Disabled
1	Enabled

TIM2INTEN	Timer compare 2 interrupt enable bit
0	Disabled
1	Enabled

TIM1INTEN	Timer compare 1 interrupt enable bit
0	Disabled
1	Enabled

TIM0INTEN	Timer compare 0 interrupt enable bit
0	Disabled
1	Enabled

Downloaded from Arrow.com.

3.4.30 Baseband interrupt enable register 1 (BBINTEN1)

This register is used to enable the baseband interrupt.

This register enables the interrupt output from the INTOUT pin upon generation of each interrupt. Set “1” to the corresponding interrupt enable bit when you want to enable the interrupt output.

<R> Set receive level filter interrupt enable bit (LVLFILINTEN) and receive level filter enable bit (LVLFILEN) to “1” in initialization.

The BBINTEN1 register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

<R> **Figure 3 - 37 Baseband Interrupt Enable Register 1 (BBINTEN1) Format**

Address: 003AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINTEN1	LVLFILINTEN	MODESWINTEN	ROVRINTEN	ADRSINTEN	RCVSTINTEN	RCV1INTEN	RCV0INTEN	RCVFININTEN

LVLFILINTEN	Receive level filter interrupt enable bit
0	Disabled
1	Enabled

MODESWINTEN	Mode switch receive completion interrupt enable bit
0	Disabled
1	Enabled

ROVRINTEN	Receive Overrun interrupt enable bit
0	Disabled
1	Enabled

ADRSINTEN	Address filter interrupt enable bit
0	Disabled
1	Enabled

RCVSTINTEN	Receive start interrupt enable bit
0	Disabled
1	Enabled

RCV1INTEN	Bank 1 receive completion interrupt enable bit
0	Disabled
1	Enabled

RCV0INTEN	Bank 0 receive completion interrupt enable bit
0	Disabled
1	Enabled

RCVFININTEN	Frame receive completion interrupt enable bit
0	Disabled
1	Enabled

Downloaded from Arrow.com.

3.4.31 Baseband interrupt enable register 2 (BBINTEN2)

This register is used to enable the baseband interrupt.

This register enables the interrupt output from the INTOUT pin upon generation of each interrupt. Set “1” to the corresponding interrupt enable bit when you want to enable the interrupt output.

<R> The BBINTEN2 register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

<R> **Figure 3 - 38 Baseband Interrupt Enable Register 2 (BBINTEN2) Format**

Address: 003BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINTEN2	X	BYTERCVINTEN	FLINTEN	RCVCUNTINTEN	X	X	X	X

BYTERCVINTEN	Byte receive completion interrupt enable bit
0	Disabled
1	Enabled

FLINTEN	Frame length interrupt enable bit
0	Disabled
1	Enabled

RCVCUNTINTEN	Number of received byte interrupt enable bit
0	Disabled
1	Enabled

Caution Be sure to set “0” to bit 0 to 3, 7. These are read as x (undefined).

Downloaded from Arrow.com.

3.4.32 CSMA control register 3 (BBCSMACON3)

This register controls the CSMA-CA operation.
The BEMIN bit is used to set the macMinBE value. (Initial value is 3H.)
Set the smaller value for the BEMIN bit than the BEMAX bit setting value.
Set value other than 0H to these bits to perform CCA.
The BBCSMACON3 register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 03H.

Figure 3 - 39 CSMA Control Register 3 (BBCSMACON3) Format

Address: 003EH After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
BBCSMACON3	0	0	0	0	BEMIN3	BEMIN2	BEMIN1	BEMIN0

BEMIN3 to BEMIN0	BEMIN bit (Sets the macMinBE value.)

Caution Be sure to set “0” to bits 4 to 7.

3.4.33 Calibration register (BBCAL)

This register is used to control calibration.
The calibration start bit is used to start calibration.
The BBCAL register is set by the serial interface in 8-bit units.
Reset signal generation clears this register to 00H.

Figure 3 - 40 Calibration Register (BBCAL) Format

Address: 003FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBCAL	0	0	0	0	0	0	0	CALSTART

CALSTART	Calibration start bit
0	Nothing performed
1	Calibration starts

Caution Be sure to set “0” to bits 1 to 7.

Downloaded from Arrow.com.

3.4.34 ACK counter compare registers 0 and 1 (ACKCOMP0 and ACKCOMP1)

These registers are used to set each of the timings upon automatic ACK reply mode.
The ACKCOMP0 and ACKCOMP1 registers are set by the serial interface in 8-bit units.
Reset signal generation sets these registers to 0014H and 000EH.

Figure 3 - 41 ACK Counter Compare Register 0 (ACKCOMP0) Format

Address: 0041H, 0040H After reset: 0014H R/W

Symbol	15	14	13	12	11	10	9	8
ACKCOMP0								
	7	6	5	4	3	2	1	0
	ACKCOMP0				ACK counter compare 0 value			

Figure 3 - 42 ACK Counter Compare Register 1 (ACKCOMP1) Format

Address: 0043H, 0042H After reset: 000EH R/W

Symbol	15	14	13	12	11	10	9	8
ACKCOMP1								
	7	6	5	4	3	2	1	0
	ACKCOMP1				ACK counter compare 1 value			

3.4.35 ACK counter initial value register (ACKINI)

This register is used to set each of the timings upon automatic ACK reply mode.
The ACKINI register is set by the serial interface in 8-bit units.
Reset signal generation clears this register to 0000H.

Figure 3 - 43 ACK Counter Initial Value Register (ACKINI) Format

Address: 005FH, 005EH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
ACKINI								
	7	6	5	4	3	2	1	0
	ACKINI				ACK counter initial value			

Downloaded from Arrow.com.

(Setting example) In the BEACON mode

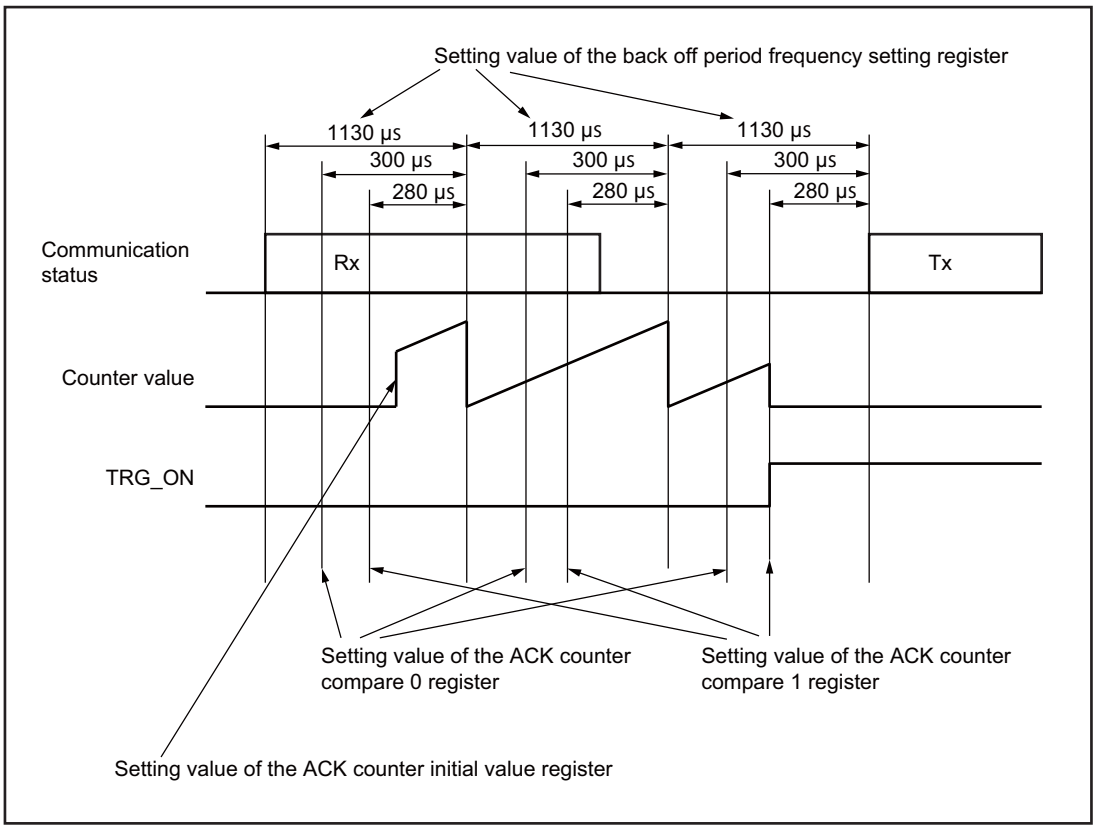
The ACK counter compare 0 register, ACK counter compare 1 register, ACK counter initial value register, and back off cycle setting register are used to control the ACK reply timing in the BEACON mode.

ACK counter compare 0 register: Set the time subtracted 300 µs from the back off cycle.
Initial value: 0014H = 20 symbols (Set value: 1H = 1 symbol)

ACK counter compare 1 register: Set the time subtracted 144 µs from the back off cycle.
Initial value: 000EH = 15 symbols (Set value: 1H = 1 symbol)

ACK counter initial value register: Set the time until the baseband block recognizes the receive start.
Total time of preamble plus SFD plus FL.
Initial value: 0000H = 0 symbols (Set value: 1H = 1 symbol)

Figure 3 - 44 Count Operation in the BEACON Mode



Downloaded from Arrow.com.

3.4.36 Receive level threshold setting register (BBLVLVTH)

This register is used to set the threshold value of the receive level.
The value is set as 2's complement The setting unit is dBm (**ex.** ”19EH” is ”-98dBm”).
Reception is done for level beyond the setting value.
The minimum setting value is recommended for the data rate and value of RSSI/CCA result register (BBRSSICCARSLT). For details, see 3.4.5 RSSI/CCA result register (BBRSSICCARSLT).

The BBLVLVTH register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 0100H.

Figure 3 - 45 Receive Level Threshold Setting Register (BBLVLVTH) Format

Address: 0045H, 0044H After reset: 0100H R/W

Symbol	15	14	13	12	11	10	9	8
BBLVLVTH	0	0	0	0	0	0	0	LVLVTHT8
	7	6	5	4	3	2	1	0
	LVLVTHT7	LVLVTHT6	LVLVTHT5	LVLVTHT4	LVLVTHT3	LVLVTHT2	LVLVTHT1	LVLVTHT0

<R>

LVLVTHT8to LVLVTHT0	Threshold value of the receive level

Caution Be sure to set “0” to bits 9 to 15.

Downloaded from Arrow.com.

3.4.37 ACK reply time setting register (ACKRTNTIM)

This register is used to set the ACK reply time in the non-BEACON mode.

The ACKRTNTIM register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 0002H.

Figure 3 - 46 ACK Reply Time Setting Register (ACKRTNTIM) Format

Address: 0047H, 0046H After reset: 0002H R/W

Symbol	15	14	13	12	11	10	9	8
ACKRTNTIM								

7	6	5	4	3	2	1	0

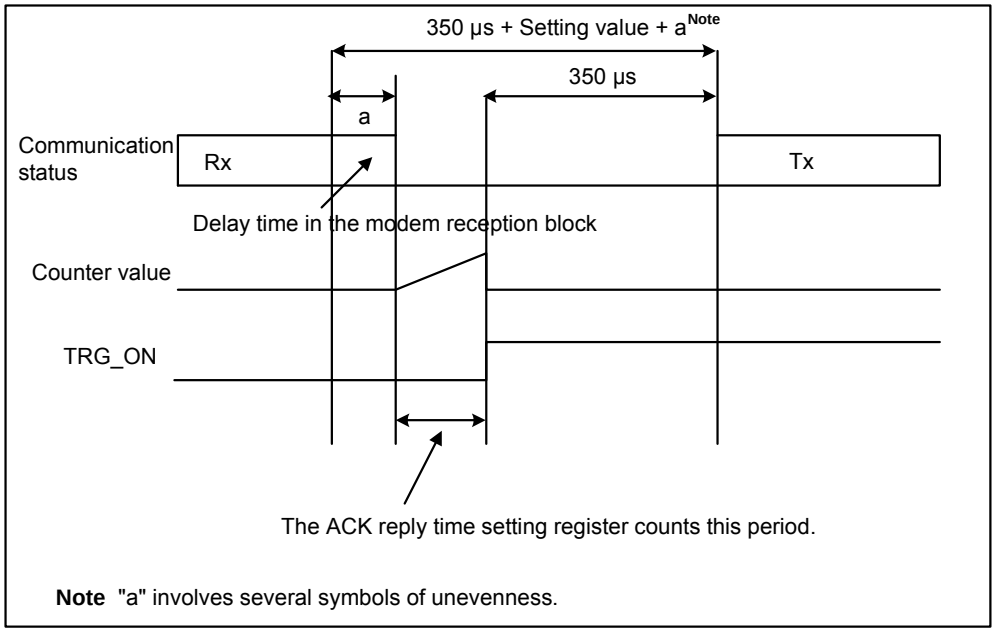
ACKRTNTIM	ACK reply time in the non-BEACON mode

(Setting example) In the non-BEACON mode

Only the ACK counter compare 3 register is used to set the time from the completion of packet receive to the TRG_ON time. Initial value: 0002H = 2 symbols (Set value: 1H = 1 symbol).

Counter stops and H is set to the TRG_ON signal when the 10-bit timer for the ACK reply mode starts from 000H upon completion of receive and it match with the ACK reply time setting register value in the non-BEACON mode.

Figure 3 - 47 Count Operation in the Non-BEACON Mode



Note "a" involves several symbols of unevenness.

Downloaded from Arrow.com.

3.4.38 Automatic receive switch compare register (AUTORCVCNT)

This register is used to set the time until the TRG_ON signal is set to the high level for the automatic receive switch after the completion of transmit/receive when the mode is set to the automatic receive switch mode. Initial value: 000AH = 10 symbols (Set value: 1H = 1 symbol).

The AUTORCVCNT register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 000AH.

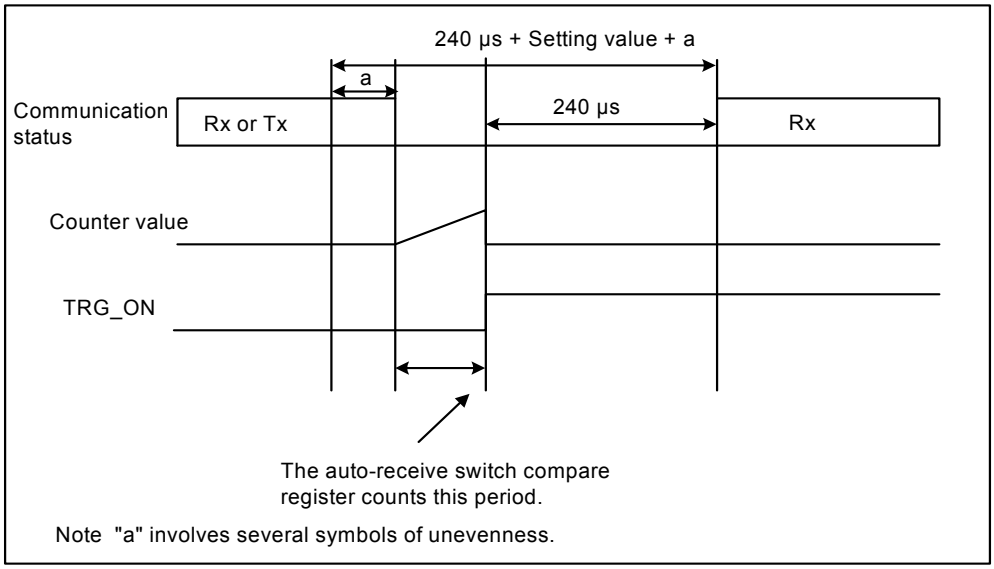
Figure 3 - 48 Automatic Receive Switch Compare Register (AUTORCVCNT) Format

Address: 0049H, 0048H After reset: 000AH R/W

Symbol	15	14	13	12	11	10	9	8
AUTORCVCNT								
	7	6	5	4	3	2	1	0

AUTORCVCNT	Time until the TRG_ON signal is set to the high level

Figure 3 - 49 Automatic Receive Switch Compare Register Count Operation



Downloaded from Arrow.com.

3.4.39 Back off cycle register (BOFFPERIOD)

This register is used to set the back off cycle. Initial value: 0071H= 113 symbols (Set value: 1H = 1 symbol).
The BOFFPERIOD register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 0071H.

Figure 3 - 50 Back-off Cycle Register (BOFFPERIOD) Format

Address: 004BH, 004AH After reset: 0071H R/W

Symbol	15	14	13	12	11	10	9	8
BOFFPERIOD								
	7	6	5	4	3	2	1	0

BOFFPERIOD	Back off cycle setting value

3.4.40 CSMA-CA end count register (CSMAENDCOUNT)

This register is used to set the time until the wait status after the completion of CCA when the automatic CSMA-CA sequence is used.
Initial value is 0080H = 128 µs. (Set value: 1H =1 µs)
The CSMAENDCOUNT register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 0080H.

Figure 3 - 51 CSMA-CA End Count Register (CSMAENDCOUNT) Format

Address: 004DH, 004CH After reset: 0080H R/W

Symbol	15	14	13	12	11	10	9	8
CSMAENDCOUNT								
	7	6	5	4	3	2	1	0

CSMAENDCOUNT	Time until the wait status after completion of the CCA

Downloaded from Arrow.com.

3.4.41 CSMA-CA start count register (CSMASTACOUNT)

This register is used to set the time of warm-up until the start of CCA when the automatic CSMA-CA sequence is used. Set the minimum number of symbols which is greater than 144 µs. Initial value: 000EH = 15 symbols (Set value: 1H = 1 symbol).

The CSMASTACOUNT register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 000EH.

Figure 3 - 52 CSMA-CA Start Count Register (CSMASTACOUNT) Format

Address: 004FH, 004EH After reset: 000EH R/W

Symbol	15	14	13	12	11	10	9	8
CSMASTACOUNT								
	7	6	5	4	3	2	1	0

CSMASTACOUNT	CCA start warm-up time

Downloaded from Arrow.com.

3.4.42 Communication status register 1 (COMSTATE1)

This register is used to confirm each state in communication.

Transmitting status bit shows transmit state.

CCA status bit shows CCA state.

Receiving frame status bit shows frame receive state.

Figure 3 - 53 Communication status register 1 (COMSTATE1) Format

Address: 0066H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
COMSTATE1	x	x	x	x	FRCV STATE	CCASTATE	TRNSTATE	x

FRCV STATE	Receiving frame status bit
0	Unreceived
1	Receiving

CCASTATE	CCA status bit
0	Not CCA
1	CCA

TRNSTATE	Transmitting status bit
0	Untransmitted
1	Transmitting

Caution Bits 0, 4 to 7 are read as x (undefined).

Downloaded from Arrow.com.

3.4.43 Communication status register 2 (COMSTATE2)

This register is used to confirm each state in communication.

ACK reply status bit shows ACK reply state.

Figure 3 - 54 Communication status register 2 (COMSTATE2) Format

Address: 0067H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
COMSTATE2	x	x	x	x	x	x	x	ACKSTATE

ACKSTATE	ACK reply status bit
0	Unreplied ACK
1	Replying ACK

Caution Bits 1 to 7 are read as x (undefined)..

Downloaded from Arrow.com.

3.4.44 Estimate control register (BBEVAREG)

This register is used to set the evaluation mode which is required when obtaining the certification of conformance to technical standards.

Setting “1” to both continuous transmission mode and transmit trigger bit enters into the continuous transmission mode. In the continuous transmission mode, the data of the number subtracted CRC byte count from the value set in the transmission frame length is repetitively transmitted. Note that the transmission data is the value which is written in the transmit RAM.Reset by RFRESETB pin after stopping the continuous transmission mode.

The non-modulation switch bit can switch between the modulation signal and non-modulation signal.

Setting “1” to both continuous receive mode bit and receive trigger bit enters into the continuous receive mode. In the continuous receive mode, the completion of the data reception cannot enter into the IDLE state. The receive state is left as it is.

Setting “1” to both special transmission mode and transmit trigger bit can transmit frames regardless of the IEEE802.15.4 standard.

Setting “1” to both special receive mode bit and receive trigger bit can receive frames regardless of the IEEE802.15.4 standard.

The BBEVAREG register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Downloaded from Arrow.com.

Figure 3 - 55 Estimate Control Register 1 (BBEVAREG) Format

Address: 0068H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBEVAREG	0	0	0	NOSPECRX	NOSPECTX	CONTRX	NOMOD	CONTTX

NOSPECRX	Special receive mode bit
0	Normal operation
1	Special receive operation

NOSPECTX	Special transmit operation
0	Normal operation
1	Special transmit operation

CONTRX	Continuous receive mode bit
0	Normal operation
1	Continuous receive operation

NOMOD	Non-modulation switch bit
0	Modulation signal
1	Non-modulation signal

CONTTX	Continuous transmit mode bit
0	Normal operation
1	Continuous transmit operation

Caution Be sure to set “0” to bits 7 to 5.

Supplemental explanation 1. Special transmit mode

• Preamble part
- Transmits the pattern which is set in the preamble setting register. (1 byte or 2 bytes)
- Repetitively transmits the number of bytes which is set by the number-of-preamble-byte setting bit.
- Transmits the byte length which is set in the preamble setting register.

• SFD part
- Transmits the pattern which is set in the SFD setting register. (1 byte, 2, or 4 bytes)
- Transmits the number of bytes which is set by the number-of-SFD-byte setting bit.

• PHR part
- Transmits the 16-bit data which is set in the mode switch frame transmit register.
  Be sure to set bits 0 and 4 of the mode switch frame transmit register to “0”.
- Transmits data regardless of the transmit frame length register setting value.

• Transmit data part
- Transmits data which is set in the transmit RAM from the 0200H address.
- Transmits data of the 0200H address again after the transmission of the data of the 02FFH address in the transmit RAM.
- Generates the bank transmit completion interrupt upon every completion of transmitting the transmit RAM bank.

Downloaded from Arrow.com.

• CRC part
- The automatic CRC function does not operate.
- Perform the CRC calculation by using software in order to add the CRC data to the final data part.

• End of transmission
- Terminate the transmission by using the RF communication stop bit.
  Be sure to reset by RFRESETB pin after stopping.

Supplemental explanation 2. Special receive mode

• Preamble part
- Operates to receive the pattern which is set in the preamble setting register as a preamble pattern.
  (1 byte or 2 bytes)
- The number of bytes which is set by the number-of-preamble-byte setting bit is defined as a repetitive pattern.

• SFD part
- The pattern which is set in the SFD setting register is defined as the source data for checking the SFD match.
  (1 byte, 2, or 4 bytes)
- The number of bytes which is set by the number-of-SFD-byte setting bit is defined as the source data for checking the SFD match.

• PHR part
- Stores the received PHR part (the 2 bytes of data immediately after the SFD) to the mode switch frame receive register.
  The bit 0 (corresponds to MODESW bit) and bit 4 (corresponds to DW bit) of the first byte of PHR can be received only “0s”.
- Ignores the received frame length.

• Receive data part
- Stores the receive data part (the 3rd byte and subsequent data immediately after the SFD) to the receive RAM.
- Generates the bank receive completion interrupt upon every completion of receiving the receive RAM bank.
- Generates the number-of-received-byte interrupt when receiving the number of bytes which is set in the-number-of-receive-byte interrupt compare register.
- Enables the generation of the receive byte interrupt for every single bit of the receive data after the SFD.
- The number of bytes stored in the receive RAM can be checked by the receive data count register.

• CRC part
- The automatic CRC function does not operate.
- Perform the CRC calculation by using software in order to check the CRC data when it is added to the final data part.

• End of reception
- Terminate the reception by using the RF communication stop bit.

Downloaded from Arrow.com.

3.4.45 Back off period register 2 (BBBOFFPROD2)

This register is used to set the random value of the back off period when performing the CSMA-CA by using the back off period bits 0 to 7. Set the random value to back off period register 2, and then set “1” to the back off period auto-random enable bit of the back off period register.

The BBBOFFPROD2 register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 56 Back off Period Register2 (BBBOFFPROD2) Format

Address: 0069H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBBOFFPROD2	BOFFPROD7	BOFFPROD6	BOFFPROD5	BOFFPROD4	BOFFPROD3	BOFFPROD2	BOFFPROD1	BOFFPROD0

BOFFPROD7 to BOFFPROD0	Back off period bit value

3.4.46 Communication status register 3 (COMSTATE3)

This register is used to display the communication status.

The number of retransmissions can be read when the auto-ACK receive mode is enabled by the number-of-retransmission read bit.

The number of times finally performing the CCA can be read by using the number-of-CCA-time read bit.

The CCADATARD register is read by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 57 Communication Status Register 3 (COMSTATE3) Format

Address: 006FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
COMSTATE3	0	CCARD			RETRNRD			

CCARD	The number of CCA times which is finally performed (3 bits)

RETRNRD	The number of retransmissions (4 bits) when the auto-ACK receive mode is enabled.

Caution “0” is always read for bit 7.

Downloaded from Arrow.com.

3.4.47 ACK receive wait time setting register (ACKRCVWIT)

This register is used to set the ACK receive wait time after the data transmission. Retransmits data when there is no ACK reply even if it waits for the specified time. Initial value: 0300H = 768 symbols). (Set value: 1H = 1 symbol)

The ACKRCVWIT register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 0300H.

Figure 3 - 58 ACK Receive Wait Time Setting Register (ACKRCVWIT) Format

Address: 0071H, 0070H After reset: 0300H R/W

Symbol	15	14	13	12	11	10	9	8
ACKRCVWIT								
	7	6	5	4	3	2	1	0

ACKRCVWIT	ACK receive wait time

3.4.48 Retransmission start compare register (RETRNWUP)

This register is used to set the time to wait until the power supply is turned on again when performing retransmission.

Initial value: 0004H= 4 symbols (Set value: 1H = 1 symbol).

The RETRNWUP register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 0004H.

Figure 3 - 59 Retransmission Start Compare Register (RETRNWUP) Format

Address: 0073H, 0072H After reset: 0004H R/W

Symbol	15	14	13	12	11	10	9	8
RETRNWUP								
	7	6	5	4	3	2	1	0

RETRNWUP	Time to wait until the power-on again

Downloaded from Arrow.com.

3.4.49 ANTSW output timing setting register (BBANTSWTIMG)

This register is used to set the timing for the ANTSW pin output.
The time to set the ANTSW pin output to high level can be set after the setting of “1” to the transmission trigger bit.
The value ranged from 001H to 154H can be set while the initial value is 072H (The set value is 1H = approx.1 µs).
Do not set the values other than those ranged from 001H (Approx. 1 µs) to 154H (Approx.340 µs).
The BBANTSWTIMG register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 0072H.

Figure 3 - 60 ANTSW Output Timing Setting Register (BBANTSWTIMG) Format

Address: 007BH, 007AH After reset: 0072H R/W

Symbol	15	14	13	12	11	10	9	8
BBANTSWTIMG	0	0	0	0	0	0		
	7	6	5	4	3	2	1	0

BBANTSWTIMG	Time till the ANTSW pin output is set to high level

Caution “0” is always read for bits 10 to 15.

3.4.50 Receive frame length register (BBRXFLEN)

This register is used to store the frame length value upon reception. The value is stores at the timing when the packet data reception is started. The value is retained until the start of the next packet data reception. However, the register is updated when the address match is recognized when the address filter is enabled.
The reading value is corresponding save bank specified by receive data save bank select bit.
The BBRXFLEN register is read by the serial interface in 8-bit units.
Reset signal generation clears this register to 0000H.

Figure 3 - 61 Receive Frame Length Register (BBRXFLEN) Format

Address: 00A1H, 00A0H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBRXFLEN	0	0	0	0	0	RCVFLEN10	RCVFLEN9	RCVFLEN8
	7	6	5	4	3	2	1	0
	RCVFLEN7	RCVFLEN6	RCVFLEN5	RCVFLEN4	RCVFLEN3	RCVFLEN2	RCVFLEN1	RCVFLEN0

RCVFLEN10 to RCVFLEN0	The frame length value upon receive

Caution Be sure to set “0” to bits 11 to 15.

Downloaded from Arrow.com.

3.4.51 Receive data counter register (BBRXCOUNT)

This register is used to indicate the receive data counter value upon reception. It enables the checking of how many bytes of receive data are currently stored to the receive RAM. The value is cleared to “0” when the packet receive ends.

The BBRXCOUNT register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 0000H.

Figure 3 - 62 Receive Data Counter Register (BBRXCOUNT) Format

Address: 00A3H, 00A2H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBRXCOUNT	0	0	0	0	0	RXCOUNT10	RXCOUNT9	RXCOUNT8
	7	6	5	4	3	2	1	0
	RXCOUNT7	RXCOUNT6	RXCOUNT5	RXCOUNT4	RXCOUNT3	RXCOUNT2	RXCOUNT1	RXCOUNT0

RXCOUNT10 to RXCOUNT0	Receive data counter value

Caution Be sure to set “0” to bits 11 to 15.

3.4.52 Transmit frame length register (BBTXFLEN)

This register is used to set the frame length value upon transmission. Set the total value of payload data length and the CRC length (in 2 or 4 bytes) for the frame length value. Transmits data regardless of the transmit frame length value when the ACK auto-reply function is enabled to automatically reply with ACK.

The BBTXFLEN register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 0000H.

Figure 3 - 63 Transmit Frame Length Register (BBTXFLEN) Format

Address: 00A5H, 00A4H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTXFLEN	0	0	0	0	0	TRNFLEN10	TRNFLEN9	TRNFLEN8
	7	6	5	4	3	2	1	0
	TRNFLEN7	TRNFLEN6	TRNFLEN5	TRNFLEN4	TRNFLEN3	TRNFLEN2	TRNFLEN1	TRNFLEN0

TRNFLEN10 to TRNFLEN0	The frame length value upon transmission

Caution Be sure to set “0” to bits 11 to 15.

Downloaded from Arrow.com.

3.4.53 Preamble length setting register (BBPAMBL)

This register is used to set the preamble length upon transmission. Set value over values shown in Table 3 - 1 and Table 3 - 2.

The BBPAMBL register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 0004H.

Figure 3 - 64 Preamble Length Setting Register (BBPAMBL) Format

Address: 00A7H, 00A6H After reset: 0004H R/W

Symbol	15	14	13	12	11	10	9	8
BBPAMBL	0	0	0	0	0	0	PAMBLLEN9	PAMBLLEN8
	7	6	5	4	3	2	1	0
	PAMBLLEN7	PAMBLLEN6	PAMBLLEN5	PAMBLLEN4	PAMBLLEN3	PAMBLLEN2	PAMBLLEN1	PAMBLLEN0

PAMBLLEN9 to PAMBLLEN0	Preamble length setting value

Caution Be sure to set “0” to bits 10 to 15.

3.4.54 Frequency setting register (BBFREQ)

This register is used to set frequency. This register consists of 30 bits.

The value ranged from 100 MHz to 1000 MHz can be set in 1 Hz step. Initial value: 36FC3BA0H = 922.5 MHz.

BBFREQ register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 36FC3BA0H.

Figure 3 - 65 Frequency Setting Register (BBFREQ) Format

Address: 00ABH to 00A8H After reset: 36FC3BA0H R/W

Symbol	31	30	29	28	27	26	25	24
BBFREQ	0	0	FREQ29	FREQ28	FREQ27	FREQ26	FREQ25	FREQ24
	23	22	21	20	19	18	17	16
	FREQ23	FREQ22	FREQ21	FREQ20	FREQ19	FREQ18	FREQ17	FREQ16
	15	14	13	12	11	10	9	8
	FREQ15	FREQ14	FREQ13	FREQ12	FREQ11	FREQ10	FREQ9	FREQ8
	7	6	5	4	3	2	1	0
	FREQ7	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0

FREQ29 to FREQ0	Frequency setting value

Caution Be sure to set “0” to bits 30 and 31.

For details, refer to **6.2 RF frequency setting for transmission** and **6.3 RF frequency setting for reception**.

Downloaded from Arrow.com.

3.4.55 Symbol rate setting register (BBSYMBLRATE)

This register is used to set the symbol rate. This register consists of 24 bits.

Table 3 - 6 shows the symbol rate setting examples. The symbol rate is set by using the calculation below.

BBSYMBLRATE register is set via serial interface in 8-bit units.

Symbol rate = (f_{Xin}/2)/(value of symbol rate setting bits)

BBSYMBLRATE register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 0000F0H.

Figure 3 - 66 Symbol Rate Setting Register (BBSYMBLRATE) Format

Address: 00AEH to 00ACH After reset: 0000F0H R/W

Symbol	23	22	21	20	19	18	17	16
BBSYMBLRATE	SYMBLRATE23	SYMBLRATE22	SYMBLRATE21	SYMBLRATE20	SYMBLRATE19	SYMBLRATE18	SYMBLRATE17	SYMBLRATE16
	15	14	13	12	11	10	9	8
	SYMBLRATE15	SYMBLRATE14	SYMBLRATE13	SYMBLRATE12	SYMBLRATE11	SYMBLRATE10	SYMBLRATE9	SYMBLRATE8
	7	6	5	4	3	2	1	0
	SYMBLRATE7	SYMBLRATE6	SYMBLRATE5	SYMBLRATE4	SYMBLRATE3	SYMBLRATE2	SYMBLRATE1	SYMBLRATE0

SYMBLRATE23 to SYMBLRATE0	Symbol rate setting bit value

<R> **Caution Set registers described in “Table 5 - 6 Settings Required for Each Data Rate” to change contents of BBSYMBLRATE register.**

Table 3 - 6 Symbol Setting Comparison Table

Symbol rate setting bit value	Symbol rate
000050H	300 ksps
000078H	200 ksps
0000A0H	150 ksps
0000F0H	100 ksps
0001E0H	50 ksps
000258H	40 ksps
0004B0H	20 ksps
000960H	10 ksps

Downloaded from Arrow.com.

3.4.56 SUBG control register (BBSUBGCON)

This register is used to control the SubGHz transceiver.
The FEC enable bit for reception is used to enable FEC (CODE) of reception.
The FEC mode switch bit is used to switch the FEC encode mode.
The number-of-CRC-bit switch bit is used to switch the number of bits for the CRC calculation process upon transmission. Note that the number of the CRC bits of the receive frame is used for those upon auto-ACK reply.
The DW enable bit is used to enable the data whitening upon transmission.
The PHR transmit bit 1 is used to transmit bit 1 of the PHR upon transmission.
The PHR transmit bit 2 is used to transmit bit 2 of the PHR upon transmission.
The interleaving enable bit is used to enable the interleaving. Set INTERLEAVEEN bit to 1 to use FEN.
The BBSUBGCON register is set by the serial interface in 8-bit units.
Reset signal generation sets this register to 0CH.

Figure 3 - 67 SUBG Control Register (BBSUBGCON) Format

Address: 00B0H After reset: 0CH R/W

Symbol	7	6	5	4	3	2	1	0
BBSUBGCON	0	INTERLEAVEEN	PHRTX2	PHRTX1	DWEN	CRCBIT	FECMODE	FECENRX

INTERLEAVEEN	Interleaving enable bit
0	Interleaving disabled
1	Interleaving enabled

PHRTX2	PHR transmission bit 2 value

PHRTX1	PHR transmission bit 1 value

DWEN	DW enable bit
0	DW disabled
1	DW enabled

CRCBIT	Number-of-CRC-bit switch bit
0	32-bit CRC
1	16-bit CRC

FECMODE	FEC mode switch bit
0	NRNSC encoder
1	RSC encoder

FECENRX	FEC enable bit for reception
0	FEC disabled
1	FEC enabled

Caution Be sure to set “0” to bit 7.

Downloaded from Arrow.com.

3.4.57 Modulation method setting register (BBMODSET)

This register is used to set the modulation method.

The modulation method setting bit is used to set the modulation method.

The modulation index setting bit is used to set the modulation index. **Table 3 - 7** shows the setting value setting examples for the modulation index setting bit.

The BBMODSET register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 42H.

Figure 3 - 68 Modulation Method Setting Register (BBMODSET) Format

Address: 00B1H After reset: 42H R/W

Symbol	7	6	5	4	3	2	1	0
BBMODSET	MODINDEX1	MODINDEX0	0	0	0	0	MODSET1	MODSET0

MODINDEX1	MODINDEX0	Modulation index setting bit
0	0	0.5
0	1	1.0
1	0	0.33
1	1	Setting prohibited

MODSET1	MODSET0	Modulation method setting bit
0	0	2FSK
0	1	4FSK
1	0	2GFSK (Initial value)
1	1	4GFSK

Caution 1. Be sure to set “0” to bits 2 to 5.

<R> **Caution 2. Set registers described in “Table 5 - 6 Settings Required for Each Data Rate” to change contents of BBMODSET register.**

Table 3 - 7 Modulation Index Setting Bit Setting Examples

MODINDEX1	MODINDEX0	Data rate	Modulation method	Modulation index	Deviation
0	0	50 kbps	2FSK/GFSK	0.5	±12.5 kHz
0	0	100 kbps	2FSK/GFSK	0.5	±25 kHz
0	1	50 kbps	2FSK/GFSK	1.0	±25 kHz
0	1	100 kbps	2FSK/GFSK	1.0	±50 kHz
1	0	200 kbps	4FSK/GFSK	0.33	±25 kHz

Downloaded from Arrow.com.

3.4.58 CCA time register (CCATIME)

This register is used to set the time taken for the CCA processing. Initial value: 000DH = 13 symbols (Set value: 1H = 1 symbol).

Setting value is up to 2000 symbols.

CCATIME register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 000DH.

Figure 3 - 69 CCA Time Register (CCATIME) Format

Address: 00B3H, 00B2H After reset: 000DH R/W

Symbol	15	14	13	12	11	10	9	8
CCATIME								
	7	6	5	4	3	2	1	0
	CCATIME	CCA time setting value						

Caution The lower limit of setting value is in accordance with data rate. Refer to the latest application note for setting values when to use the product.

3.4.59 Antenna diversity mode register (BBANTDIV)

This register is used to set the antenna diversity mode.

The antenna diversity enable bit is used to enable the antenna diversity mode. Enabling this bit switches the GPIO1 pin and the GPIO2 pin to the ANTSELOUT0 pin and the ANTSELOUT1 pin.

Transmission antenna switch setting bit is used to fix antenna selection for transmission.

The ACK reply antenna switch setting disable bit is used to set the antenna selection upon ACK reply to the antenna setting upon receive instead of the antenna switch setting bit value.

The ACK receive antenna switch setting disable bit is used to set the antenna selection upon ACK receive to the antenna selection operation instead of the antenna switch setting bit value.

The number-of-antenna-selection-judge bit is used to set the number of judges for the antenna input power value when the antenna diversity mode is enabled. Setting 3 to 5 is available (initial value is three times).

The ANTSELOUT pin status bit is used to indicate which ANTSELOUT pin is currently in the high level output state.

The BBANTDIV register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 30H.

Downloaded from Arrow.com.

Figure 3 - 70 Antenna Diversity Mode Register (BBANTDIV) Format

Address: 00B4H After reset: 30H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBANTDIV	ANTST	ANTCOUNT2	ANTCOUNT1	ANTCOUNT0	ANTACKRCVDIS	ANTACKRTNDIS	ANTSWTRNSET	ANTDIVEN

ANTST	Pins ANTSELOUT0 and ANTSELOUT1 status bit
0	ANTSELOUT0 pin = High level
1	ANTSELOUT1 pin = High level

ANTCOUNT2	ANTCOUNT1	ANTCOUNT0	Number-of-antenna-selection-judge bit
0	1	1	Three times (Initial value)
1	0	0	Four times
1	0	1	Five times
Other than those described above			Setting prohibited

ANTACKRCVDIS	ACK receive antenna switch setting disable bit
0	ANTSWSET bit enabled
1	ANTSWSET bit disabled

ANTACKRTNDIS	ACK reply antenna switch setting disable bit
0	ANTSWSET bit enabled
1	ANTSWSET bit disabled

ANTSWTRNSET	Transmission antenna switch setting bit
0	ANTSELOUT0 pin = High level
1	ANTSELOUT1 pin = High level

ANTDIVEN	Antenna diversity enable bit
0	Disable
1	Enable

Note Bits 7 is Read Only.

Downloaded from Arrow.com.

3.4.60 Mode switch frame transmit register (BBTXMODESW)

This register is used to transmit the mode switch frame. The MODESW bit enables the transmission of the mode switch frame. Setting transmission trigger to 1 by setting 1 to this bit transmits the mode switch frame.
Set bits 1 to 15 by using the TXMODESW bits 1 to 15 when transmitting the mode switch frame.
BBTXMODESW register is set via serial interface in 8-bit units.
Reset signal generation clears this register to 0000H.

Figure 3 - 71 Mode Switch Frame Transmit Register (BBTXMODESW) Format

Address: 00B9H, 00B8H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTXMODESW	TXMODESW15	TXMODESW14	TXMODESW13	TXMODESW12	TXMODESW11	TXMODESW10	TXMODESW9	TXMODESW8

7	6	5	4	3	2	1	0
TXMODESW7	TXMODESW6	TXMODESW5	TXMODESW4	TXMODESW3	TXMODESW2	TXMODESW1	MODESW

TXMODESW15 to TXMODESW1	The values of PHR bits 1 to 15 of the transmitted mode switch frame

MODESW	Mode switch control bit
0	Disable
1	Enable

3.4.61 Mode switch frame receive register (BBRXMODESW)

This register is used to store the PHY header data (PHR) when the mode switch frame is received. The stored data is retained until when the next mode switch frame is received.
BBRXMODESW register is read via serial interface in 8-bit units.
Reset signal generation clears this register to 0000H.

Figure 3 - 72 Mode Switch Frame Receive Register (BBRXMODESW) Format

Address: 00BBH, 00BAH After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBRXMODESW	RXMODESW15	RXMODESW14	RXMODESW13	RXMODESW12	RXMODESW11	RXMODESW10	RXMODESW9	RXMODESW8

7	6	5	4	3	2	1	0
RXMODESW7	RXMODESW6	RXMODESW5	RXMODESW4	RXMODESW3	RXMODESW2	RXMODESW1	RXMODESW0

RXMODESW15 to RXMODESW0	The values of PHR bits 0 to 15 of the received mode switch frame

Downloaded from Arrow.com.

3.4.62 Transmit data counter register (BBTXCOUNT)

This register is used to indicate the transmit data counter value upon transmission. It enables the checking of how many bytes of transmit data are currently transferred to transmitter from the transmit RAM. The value is cleared to “0” when the packet transmission ends. Be sure to read data in the order from the lower byte to the upper byte because the upper three bits are stored at the timing when the data of lower 8 bits is read.

BBTXCOUNT register is set via serial interface in 8-bit units.

Reset signal generation clears this register to 0000H.

Figure 3 - 73 Transmit Data Counter Register (BBTXCOUNT) Format

Address: 00BDH, 00BCH After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTXCOUNT	0	0	0	0	00	TRNCOUNT10	TRNCOUNT9	TRNCOUNT8

7	6	5	4	3	2	1	0
TRNCOUNT7	TRNCOUNT6	TRNCOUNT5	TRNCOUNT4	TRNCOUNT3	TRNCOUNT2	TRNCOUNT1	TRNCOUNT0

TRNCOUNT10 to TRNCOUNT0	The transmit data counter value upon transmission

Caution “0” is always read for bits 11 to 15.

Downloaded from Arrow.com.

3.4.63 PHY header receive register (BBPHRRX)

This register is used to store the PHY header receive data.

The values of bits 0 to 2, FCSTYPE, and Data Whitening of the PHY header data when receiving the non-mode switch frame are stored. The timing of the storage is the same as the timing when the frame length value is stored.

The reading value is corresponding save bank specified by receive data save bank select bit.

The BBPHRRX register is read by the serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 74 PHY Header Receive Register (BBPHRRX) Format

Address: 00BEH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBPHRRX	0	0	0	DWBIT	FCSTYPE	PHRRX2	PHRRX1	PHRRX0

DWBIT	Data whitening bit
0	Disable
1	Enable

FCSTYPE	FCS type bit
0	32 bits
1	16 bits

PHRRX2	PHR receive bit 2 value

PHRRX1	PHR receive bit 1 value

PHRRX0	PHR receive bit 0 value

Caution “0” is always read for bits 5 to 7.

Downloaded from Arrow.com.

3.4.64 Preamble setting register (BBPABL)

This register is used to optionally set the preamble value. This register consists of 16 bits.

Set following values for each modification.

2FSK/2GFSK: 00AAH

4FSK/4GFSK: 00EEH

BBPABL register is read via serial interface in 8-bit units.

Reset signal generation sets this register to 00AAH.

Figure 3 - 75 Preamble Setting Register (BBPABL) Format

Address: 00C1H, 00C0H After reset: 00AAH R/W

Symbol	15	14	13	12	11	10	9	8
BBPABL	PABL15	PABL14	PABL13	PABL12	PABL11	PABL10	PABL9	PABL8
	7	6	5	4	3	2	1	0
	PABL7	PABL6	PABL5	PABL4	PABL3	PABL2	PABL1	PABL0

PABL15 To PABL0	preamble value

3.4.65 SFD setting register (BBSFD)

This register is used to set the SFD value for FEC disabled frame transmission when MRFSKSFD bit is 0. This register consists of 32 bits.

Set following values for each modification.

2FSK/2GFSK: 00007209H

4FSK/4GFSK: BFAEAAEBH

BBSFD register is read via serial interface in 8-bit units.

Reset signal generation sets this register to 00007209H.

Figure 3 - 76 SFD Setting Register (BBSFD) Format

Address: 00C5H to 00C2H After reset: 00007209H R/W

Symbol	31	30	29	28	27	26	25	24
BBSFD	SFD31	SFD30	SFD29	SFD28	SFD27	SFD26	SFD25	SFD24
	23	22	21	20	19	18	17	16
	SFD23	SFD22	SFD21	SFD20	SFD19	SFD18	SFD17	SFD16
	15	14	13	12	11	10	9	8
	SFD15	SFD14	SFD13	SFD12	SFD11	SFD10	SFD9	SFD8
	7	6	5	4	3	2	1	0
	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0

SFD31 to SFD0	SFD value

Downloaded from Arrow.com.

3.4.66 SHR control register (BBSHRCON)

This register is used to set the number of bytes in the preamble setting register to be used for the repetitive pattern for preamble by using the number-of-preamble setting bit.

0: 1 byte (preamble setting register bits 7 to 0)

1: 2 byte (preamble setting register bits 15 to 0)

This register is used to set the number of bytes in the SFD setting register to be used for the SFD output pattern by using the number-of-SFD setting bit.

00: 1 byte (SFD setting register bits 7 to 0)

01: 2 bytes (SFD setting register bits 15 to 0)

10: Prohibited

11: 4 bytes (SFD setting register bits 31 to 0)

The BBBSHRCON register is set by the serial interface in 8-bit units.

Reset signal generation sets this register to 02H.

Figure 3 - 77 SHR Control Register (BBSHRCON) Format

Address: 00C6H After reset: 02H R/W

Symbol	7	6	5	4	3	2	1	0
BBSHRCON	0	0	0	0	0	SFDBYTE1	SFDBYTE0	PABLBYTE

SFDBYTE1	SFDBYTE0	Number-of-SFD-byte setting bit
0	0	1 byte
0	1	2 byte
1	0	Setting disabled
1	1	4 bytes

PABLBYTE	Number-of-preamble-byte setting bit
0	1 byte
1	2 byte

Caution Be sure to set “0” to bits 3 to 7.

Downloaded from Arrow.com.

3.4.67 ANT0 read register (BBANT0RD)

This register is used to store the RSSI value when the ANTSELOUT0 pin output is at the high level.
The reading value is corresponding save bank specified by receive data save bank select bit.
The value is set as 2's complement. The setting unit is dBm (**ex.** "19EH" is "-98dBm").
BBANT0RD register is set via serial interface in 8-bit units.
Reset signal generation sets this register to 0100H.

Figure 3 - 78 ANT0 Read Register (BBANT0RD) Format

Address: 00C9H, 00C8H After reset: 0100H R

Symbol	15	14	13	12	11	10	9	8
BBANT0RD	0	0	0	0	0	0	0	ANT0RD8
	7	6	5	4	3	2	1	0
	ANT0RD7	ANT0RD6	ANT0RD5	ANT0RD4	ANT0RD3	ANT0RD2	ANT0RD1	ANT0RD0

ANT0RD8 to ANT0RD0	RSSI value when the ANTSELOUT0 pin output is at the high level

Caution "0" is always read for bits 9 to 15.

3.4.68 ANT1 read register (BBANT1RD)

This register is used to store the RSSI value when the ANTSELOUT1 pin output is at the high level.
The reading value is corresponding save bank specified by receive data save bank select bit.
The value is set as 2's complement. The setting unit is dBm (**ex.** "19EH" is "-98dBm").
BBANT1RD register is set via serial interface in 8-bit units.
Reset signal generation sets this register to 0100H.

Figure 3 - 79 ANT1 Read Register (BBANT1RD) Format

Address: 00CBH, 00CAH After reset: 0100H R

Symbol	15	14	13	12	11	10	9	8
BBANT1RD	0	0	0	0	0	0	0	ANT1RD8
	7	6	5	4	3	2	1	0
	ANT1RD7	ANT1RD6	ANT1RD5	ANT1RD4	ANT1RD3	ANT1RD2	ANT1RD1	ANT1RD0

ANT1RD8 to ANT1RD0	RSSI value when the ANTSELOUT1 pin output is at the high level

Caution "0" is always read for bits 9 to 15.

Downloaded from Arrow.com.

3.4.69 Antenna switch time register (BBANTDIVTIM)

This register is used to set the time to switch between high level and low level outputs of the ANTSELOUT0 and ANTSELOUT1 pin outputs when the antenna diversity is enabled. Initial value: 000AH = 10 symbols (Set value: 1H = 1 symbol).

BBANTDIVTIM register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 000AH.

Figure 3 - 80 Antenna Switch Time Register (BBANTDIVTIM) Format

Address: 00CFH, 00CEH After reset: 000AH R/W

Symbol	15	14	13	12	11	10	9	8
BBANTDIVTIM								
	7	6	5	4	3	2	1	0

BBANTDIVTIM	ANTSELOUT0 and ANTSELOUT1 pin output switch time

3.4.70 Receive start timeout setting register (BBANTTIMOUT)

This register is used to set the timeout value when there is no receive start operation after when exceeding the threshold value upon antenna diversity in operation. The operation returns to the antenna select operation after the timeout. Initial value: 0100H= 256 symbols (Set value: 1H = 1 symbol).

BBANTTIMOUT register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 0100H.

Figure 3 - 81 Receive Start Timeout Setting Register (BBANTTIMOUT) Format

Address: 00D1H, 00D0H After reset: 0100H R/W

Symbol	15	14	13	12	11	10	9	8
BBANTTIMOUT								
	7	6	5	4	3	2	1	0

BBANTTIMOUT	Timeout value when there is no receive start operation.

Downloaded from Arrow.com.

3.4.71 Number-of-receive-byte interrupt compare register (BBRCVINTCOMP)

This register is used to generate interrupt depending on the number of received bytes. Generates the interrupt request when receiving the specified number of bytes.

The BBRCVINTCOMP register is set by the serial interface in 8-bit units.

Reset signal generation clears this register to 0010H.

Figure 3 - 82 Number-of-Receive-Byte Interrupt Compare Register (BBRCVINTCOMP) Format

Address: 00D3H, 00D2H After reset: 0010H R/W

Symbol	15	14	13	12	11	10	9	8
BBRCVINTCOMP	0	0	0	0	0	RCVINTCOMP10	RCVINTCOMP9	RCVINTCOMP8

7	6	5	4	3	2	1	0
RCVINTCOMP7	RCVINTCOMP6	RCVINTCOMP5	RCVINTCOMP4	RCVINTCOMP3	RCVINTCOMP2	RCVINTCOMP1	RCVINTCOMP0

RCVINTCOMP10 to RCVINTCOMP0	Number of bytes which generate the number-of-receive-byte interrupt

Caution Be sure to set “0” to bits 11 to 15.

3.4.72 Back off period total number register (BBBOPTOTAL)

This register is used to indicate the total number of count values of the back off period upon CSMA-CA. The maximum value of the count value is FFFFH.

BBBOPTOTAL register is set via serial interface in 8-bit units.

Reset signal generation clears this register to 0000H.

Figure 3 - 83 Back off Period Total Number Register (BBBOPTOTAL) Format

Address: 00D5H, 00D4H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBBOPTOTAL								

7	6	5	4	3	2	1	0

BBBOPTOTAL	Back off period total number

Downloaded from Arrow.com.

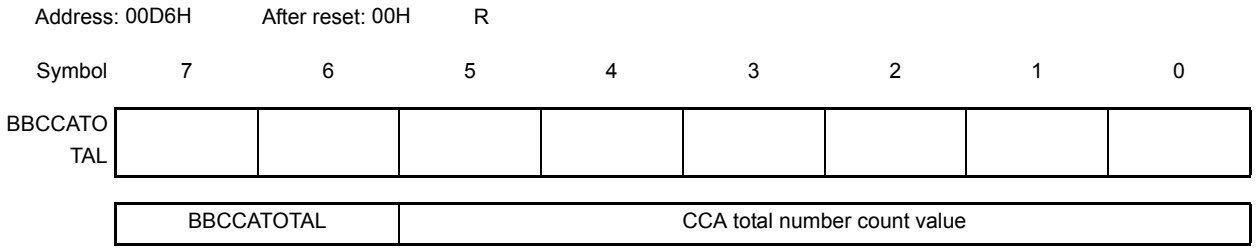
3.4.73 CCA total number register (BBCCATOTAL)

This register is used to indicate the total number of count vales upon CSMA-CA. The maximum value of the count is FFH.

BBCCATOTAL register is set via serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 84 CCA Total Number Register (BBCCATOTAL) Format



Downloaded from Arrow.com.

3.4.74 RF initial setting register 00 to 02 (RFINI00 to RFINI02)

Data read/write area with sub-address is implemented in RF block. These registers are used to set the area. These registers consist of 24 bits.

-Data write

Write RF initial setting register 00 and RF initial setting register 01 continuously.

RF initial setting register 00 (bits 7 to 0): write data

RF initial setting register 01 (bit 7): 0

RF initial setting register 01 (bits 6 to 0): sub-address in RF

-Data read

Write RF initial setting register 00 and RF initial setting register 01 continuously.

RF initial setting register 00 (bits 7 to 0): 00H

RF initial setting register 01 (bit 7): 1

RF initial setting register 01 (bits 6 to 0): sub-address in RF

Read RF initial setting register 02 after writing RF initial setting register 00 and 01.

Caution Two bytes of RF initial setting register 00 and 01 must be written continuously (SEN signal keeps low level).

RF initial setting register 00 to 02 are set via serial interface in 8-bit units.

RF initial setting register 00 and 01 are write only and the read values are undefined.

RF initial setting register 02 is read only and the initial value is undefined.

Figure 3 - 85 RF initial setting register 00 to 02 (RFINI00 to RFINI02) Format

Address: 00D8H After reset: undefined W

Symbol	7	6	5	4	3	2	1	0
RFINI00	RFINI007	RFINI006	RFINI005	RFINI004	RFINI003	RFINI002	RFINI001	RFINI000
	RFINI00		RFINI00 value					

Address: 00D9H After reset: undefined W

Symbol	7	6	5	4	3	2	1	0
RFINI01	RFINI017	RFINI016	RFINI015	RFINI014	RFIN013	RFINI012	RFINI011	RFINI010
	RFINI01		RFINI01 value					

Address: 00DAH After reset: undefined R

Symbol	7	6	5	4	3	2	1	0
RFINI02	RFINI027	RFINI026	RFINI025	RFINI024	RFINI023	RFINI022	RFINI021	RFINI020
	RFINI02		RFINI02 value					

Downloaded from Arrow.com.

3.4.75 RF initial setting register 10 to 12 (RFINI10 to RFINI12)

Data read/write area with sub-address is implemented in RF block. These registers are used to set the area. These registers consist of 24 bits.

-Data write

Write RF initial setting register 10 and RF initial setting register 01 continuously.

RF initial setting register 10 (bits 7 to 0): write data

RF initial setting register 11 (bit 7): 0

RF initial setting register 11 (bits 6 to 0): sub-address in RF

-Data read

Write RF initial setting register 10 and RF initial setting register 11 continuously.

RF initial setting register 10 (bits 7 to 0): 00H

RF initial setting register 11 (bit 7): 1

RF initial setting register 11 (bits 6 to 0): sub-address in RF

Read RF initial setting register 12 after writing RF initial setting register 10 and 11.

Caution Two bytes of RF initial setting register 10 and 11 must be written continuously (SEN signal keeps low level).
RF initial setting register 10 to 12 are set via serial interface in 8-bit units.
RF initial setting register 10 and 11 are write only and the read values are undefined.
RF initial setting register 12 is read only and the initial value is undefined.

Figure 3 - 86 RF initial setting register 10 to 12 (RFINI10 to RFINI12) Format

Address: 00DCH After reset: undefined W

Symbol	7	6	5	4	3	2	1	0
RFINI010	RFINI107	RFINI106	RFINI105	RFINI104	RFINI103	RFINI102	RFINI101	RFINI100
	RFINI10		RFINI 10 value					

Address: 00DDH After reset: undefined W

Symbol	7	6	5	4	3	2	1	0
RFINI11	RFINI117	RFINI116	RFINI115	RFINI114	RFINI113	RFINI112	RFINI111	RFINI110
	RFINI11		RFINI 11 value					

Address: 00DEH After reset: undefined R

Symbol	7	6	5	4	3	2	1	0
RFINI12	RFINI127	RFINI126	RFINI125	RFINI124	RFINI123	RFINI122	RFINI121	RFINI120
	RFINI12		RFINI 12value					

Downloaded from Arrow.com.

3.4.76 PAN identifier register 1 (BBPANID1)

This register is used to set the PAN identifier of second address filter. It consists of 16 bits and is used to detect the match with a received PAN identifier.

BBPANID1 register is set via serial interface in 8-bit units.

Reset signal generation sets this register to FFFFH.

Figure 3 - 87 PAN Identifier Register 1 (BBPANID1) Format

Address: 00E1H, 00E0H After reset:FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBPANID1								
	7	6	5	4	3	2	1	0
	BBPANID1		PAN identifier					

3.4.77 Short address register 1 (BBSHORTAD1)

This register is used to set the short address of second address filter. It consists of 16 bits and is used to detect the match with a received PAN identifier.

BBSHORTAD1 register is set via serial interface in 8-bit units.

Reset signal generation sets this register to FFFFH.

Figure 3 - 88 Short Address Register 1 (BBSHORTAD1) Format

Address: 00E3H, 00E2H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBSHORTAD1								
	7	6	5	4	3	2	1	0
	BBSHORTAD1		Short address					

Downloaded from Arrow.com.

3.4.78 Extended address register 1 (BBEXTENDAD10 to BBEXTENDAD13)

This register is used to set the extended address of second address filter. It consists of 64 bits (16 bit timed by 4) and is used to detect the match with a received extended address.

BBEXTENDAD10 to BBEXTENDAD13 registers are set via serial interface in 8-bit units.

Reset signal generation clears these registers to 0000H.

Figure 3 - 89 Extended Address Register 1 (BBEXTENDAD10 to BBEXTENDAD13) Format

Address: 00EBH, 00EAH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD13								
	7	6	5	4	3	2	1	0

BBEXTENDAD13	Extended address bits 63 to 48

Address: 00E9H, 00E8H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD12								
	7	6	5	4	3	2	1	0

BBEXTENDAD12	Extended address bits 47 to 32

Address: 00E7H, 00E6H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD11								
	7	6	5	4	3	2	1	0

BBEXTENDAD11	Extended address bits 31 to 16

Address: 00E5H, 00E4H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD10								
	7	6	5	4	3	2	1	0

BBEXTENDAD10	Extended address bits 15 to 0

Downloaded from Arrow.com.

3.4.79 Receive timeout register (BBTIMEOUT)

This register is used to set the timeout time when the automatic reception with timeout mode is enabled. This register consists of 12 bits.

BBTIMEOUT register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 07D0H. (07D0H = 2 ms, 1H = 1 µs)

Figure 3 - 90 Receive Timeout Register (BBTIMEOUT) Format

Address: 00EDH, 00ECH After reset: 07D0H R/W

Symbol	15	14	13	12	11	10	9	8
BBTIMEOUT	0	0	0	0				
	7	6	5	4	3	2	1	0

BBTIMEOUT	Timeout time setting value

Caution Be sure to set “0” to bits 12 to 15.

Downloaded from Arrow.com.

3.4.80 ANTSW control register (ANTSWCON)

This register controls the ANTSW signal.

The ANTSW signal can be output from the GPIO4 pin by using the ANTSW output enable bit.

ANTSWCON register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 00H.

Figure 3 - 91 ANTSW Control Register (ANTSWCON) Format

Address: 0080H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ANTSWCON	0	0	0	0	0	0	0	ANTSWEN

ANTSWEN	ANTSW output enable bit
0	Normal port
1	ANTSW output

Caution Be sure to set “0” to bits 1 to 7.

Downloaded from Arrow.com.

3.4.81 Clock output control register (CLKOUTCON)

This register controls the clock output.

The clock can be output from the GPIO0 pin by using the clock output enable bit.

The output clock can be selected between the clock output select bit 0 and the clock output select bit 1.

<R> Do not use clock output function in transmit or receive state.

CLKOUTCON register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 00H.

Figure 3 - 92 Clock Output Control Register (CLKOUTCON) Format

Address: 0081H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CLKOUTCON	0	0	0	0	0	CLKOUTSEL1	CLKOUTSEL0	CLKOUTEN

CLKOUTSEL1	CLKOUTSEL0	Clock output select bit
0	0	8 MHz
0	1	12 MHz
1	0	4 MHz
1	1	Setting prohibited

CLKOUTEN	Clock output enable bit
0	Normal port
1	Clock output enabled

Caution Be sure to set “0” to bits 3 to 7.

Downloaded from Arrow.com.

3.4.82 Port direction register (GPIODIR)

This register is used to set the I/O of the respective ports of GPIO.

GPIODIR register is set via serial interface in 8-bit units.

Reset signal generation clears this register to 00H.

Figure 3 - 93 Port Direction Register (GPIODIR) Format

Address: 0082H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GPIODIR	0	0	0	GPIO4DIR	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR

GPIO4DIR	GPIO4 direction bit
0	Input port
1	Output port

GPIO3DIR	GPIO3 direction bit
0	Input port
1	Output port

GPIO2DIR	GPIO2 direction bit
0	Input port
1	Output port

GPIO1DIR	GPIO1 direction bit
0	Input port
1	Output port

GPIO0DIR	GPIO0 direction bit
0	Input port
1	Output port

Caution Be sure to set “0” to bits 5 to 7.

Downloaded from Arrow.com.

3.4.83 Port data register (GPIODATA)

This register is used to set the output value when the respective ports of GPIO are set to output.
When a GPIO port is set to input, the pin state (H/L) can be read.
GPIODATA register is set via serial interface in 8-bit units.
Reset signal generation clears this register to 00H.

Figure 3 - 94 Port Data Register (GPIODATA) Format

Address: 0083H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GPIODATA	0	0	X	GPIO4 DATA	GPIO3 DATA	GPIO2 DATA	GPIO1 DATA	GPIO0 DATA

GPIO4 DATA	GPIO4 data bit
0	0: Output
1	1: Output

GPIO3 DATA	GPIO3 data bit
0	0: Output
1	1: Output

GPIO2 DATA	GPIO2 data bit
0	0: Output
1	1: Output

GPIO1 DATA	GPIO1 data bit
0	0: Output
1	1: Output

GPIO0 DATA	GPIO0 data bit
0	0: Output
1	1: Output

Caution Be sure to set “0” to bits 5 to 7. Bit 5 becomes x (undefined) when read out.

Downloaded from Arrow.com.

3.4.84 SFD setting register 2 (BBSFD2)

This register is used to set the SFD value for FEC enabled frame transmission/reception when MRFSKSFD bit is 0.

Set the following values for each modulation.

2FSK/2GFSK: 000072F6H

4FSK/4GFSK: BFAEFFBEH

The BBSFD2 register consists of 32 bits. Reset signal generation sets this register to undefined.

BBSFD2 register is set via serial interface in 8-bit units.

Figure 3 - 95 SFD Setting Register 2 (BBSFD2) Format

Address: 0103H-0100H After reset: XXXXXXXXH R/W

Symbol	31	30	29	28	27	26	25	24
BBSFD2	SFD231	SFD230	SFD229	SFD228	SFD227	SFD226	SFD225	SFD224
	23	22	24	20	19	18	17	16
	SFD223	SFD222	SFD221	SFD220	SFD219	SFD218	SFD217	SFD216
	15	14	13	12	11	10	9	8
	SFD215	SFD214	SFD213	SFD212	SFD211	SFD210	SFD209	SFD208
	7	6	5	4	3	2	1	0
	SFD207	SFD206	SFD205	SFD204	SFD203	SFD202	SFD201	SFD200

SFD231-SFD200	SFD2 value

Downloaded from Arrow.com.

3.4.85 SFD setting register 3 (BBSFD3)

This register is used to set the SFD value for FEC disabled frame transmission/reception when MRFSKSFD bit is 1.

Set the following values for each modulation.

2FSK/2GFSK: 0000705EH

4FSK/4GFSK: BFAABBFEH

The BBSFD3 register consists of 32 bits. Reset signal generation sets this register to undefined.

BBSFD3 register is set via serial interface in 8-bit units.

Figure 3 - 96 SFD Setting Register 3 (BBSFD3) Format

Address: 0107H-0104H After reset: XXXXXXXXH R/W

Symbol	31	30	29	28	27	26	25	24
BBSFD3	SFD331	SFD330	SFD329	SFD328	SFD327	SFD326	SFD325	SFD324
	23	22	24	20	19	18	17	16
	SFD323	SFD322	SFD321	SFD320	SFD319	SFD318	SFD317	SFD316
	15	14	13	12	11	10	9	8
	SFD315	SFD314	SFD313	SFD312	SFD311	SFD310	SFD309	SFD308
	7	6	5	4	3	2	1	0
	SFD307	SFD306	SFD305	SFD304	SFD303	SFD302	SFD301	SFD300

SFD331- SFD300	SFD3 value

3.4.86 SFD setting register 4 (BBSFD4)

This register is used to set the SFD value for FEC enabled frame transmission/reception when MRFSKSFD bit is 1.

Set the following values for each modulation.

2FSK/2GFSK: 0000B4C6H

4FSK/4GFSK: EFBAFABEH

The BBSFD4 register consists of 32 bits. Reset signal generation sets this register to undefined.

BBSFD4 register is set via serial interface in 8-bit units.

Figure 3 - 97 SFD Setting Register 4 (BBSFD4) Format

Address: 010BH-0108H After reset: XXXXXXXXH R/W

Symbol	31	30	29	28	27	26	25	24
BBSFD4	SFD431	SFD430	SFD429	SFD428	SFD427	SFD426	SFD425	SFD424
	23	22	24	20	19	18	17	16
	SFD423	SFD422	SFD421	SFD420	SFD419	SFD418	SFD417	SFD416
	15	14	13	12	11	10	9	8
	SFD415	SFD414	SFD413	SFD412	SFD411	SFD410	SFD409	SFD408
	7	6	5	4	3	2	1	0
	SFD407	SFD406	SFD405	SFD404	SFD403	SFD402	SFD401	SFD400

SFD431- SFD400	SFD4 value

Downloaded from Arrow.com.

3.4.87 FEC control register (BBFECCON)

FEC automatic identification enable bit is used to receive with identification of enabled or disabled FEC.
FEC enable bit for transmission is used to set FEC enable or disable of transmission.
FEC control bit for automatic ACK reply must be set to 1 to use automatic ACK reply function.
FEC enable bit for automatic ACK reply is used to set enable or disable of FEC in automatic ACK reply when FEC control bit for automatic ACK reply is set to 1.
FEC control bit for automatic ACK reception is used to switch enable or disable control of FEC for automatic ACK reception is whether depends on FEC control bit for automatic ACK reply.
FEC enable bit for automatic ACK reception is used to set enable or disable of FEC in automatic ACK reception when FEC control bit for automatic ACK reception is set to 1.
MRFSKSFD select bit is used to set value of phyMRFSKSFD bit.
BBFECCON register is set via serial interface in 8-bit units.
Reset signal generation sets this register to 00H.

Downloaded from Arrow.com.

Figure 3 - 98 FEC Control Register (BBFECCON) Format

Address: 010CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBFECCON	x	MRFSKSFD	FECEN ACKRCV	FECCON ACKRCV	FECEN ACKRTN	FECCON ACKRTN	FECENTX	FEC AUTOEN

MRFSKSFD	MRFSKSFD select bit
0	phyMRFSKSFD = 0
1	phyMRFSKSFD = 1

FECEN ACKRCV	FEC enable bit for automatic ACK reception
0	Disable
1	Enable

FECCON ACKRCV	FEC control bit for automatic ACK reception
0	Regardless of FEC enable bit for automatic ACK reception
1	Depend on FEC enable bit for automatic ACK reception

FECEN ACKRTN	FEC enable bit for automatic ACK reply
0	Disable
1	Enable

FECCON ACKRTN	FEC control bit for automatic ACK reply
0	Disables automatic ACK reply
1	Enables automatic ACK reply

FECENTX	FEC enable bit for transmission
0	Disable
1	Enable

FEC AUTOEN	FEC automatic identification enable bit
0	Disable
1	Enable

Caution Be sure to set “0” to bit 7. The bit is read as x (undefined).

Downloaded from Arrow.com.

3.4.88 Address filter extension address control register (BBADFCON)

PAN coordinator 2 bit is used to set whether PAN coordinator on second address filter side.

Frame pending 2 bit is used to set enable or disable of frame pending for ACK reply on second address filter side.

First address filter match monitor bit is used to monitor whether the first address matches. The reading value is corresponding save bank specified by receive data save bank select bit.

Second address filter match monitor bit is used to monitor whether the second address matches. The reading value is corresponding save bank specified by receive data save bank select bit.

When the address filter extension bit is disabled, values of first and second address filter match monitor bits are invalid.

When the address filter extension bit is enabled, values of first and second address filter match monitor bits are invalid under the following conditions.

- Frame version: 00, 01
- Frame type: Beacon frame
- No destination PANID and destination address
- Values of source PANID and PAN identifier register match, or value of PAN identifier register = FFFFH
- PANCORD bit = 0

BBADFCON register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 00H.

Figure 3 - 99 Address Filter Extension Address Control Register (BBADFCON) Format

Address: 010DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBADFCON	0	0	0	0	ADFMONI2	ADFMONI1	FLMPEND2	PANCORD2

ADFMONI2	Second address filter match monitor bit
0	Not match to second address
1	Match to second address

ADFMONI1	First address filter match monitor bit
0	Not match to first address
1	Match to first address

FLMPEND2	Frame pending 2 bit
0	No frame pending
1	With frame pending

PANCORD2	PAN coordinator 2 bit
0	Not a PAN coordinator
1	PAN coordinator

Caution Be sure to clear bits 4 to 7 to “0”. Bits 2,3 are Read Only.

Downloaded from Arrow.com.

3.4.89 Antenna diversity mode register 2 (BBANTDIV2)

ACK reply antenna switch setting bit is used to select ACK reply antenna for automatic ACK reply. This bit is enabled when ANT receive ANTSW setting disable bit is 0.

ACK receive antenna switch setting bit is used to select ACK receive antenna for automatic ACK reception. This bit is enable when ANT reply ANTSW setting disable bit is 0.

Receive antenna monitor bit is used to monitor antenna for reception.The reading value is corresponding save bank specified by receive data save bank select bit.

ACK reply antenna switch invert bit is used to invert to receive antenna output as ACK reply antenna for automatic ACK reply.

BBANTDIV2 register is set via serial interface in 8-bit units.

Reset signal generation sets this register to 00H.

Figure 3 - 100 Antenna Diversity Mode Register 2 (BBANTDIV2) Format

Address: 010EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBANTDIV2	0	0	0	0	ACKRTN RVS	ANTMONI	ANTACK RCVSET	ANTACK RTNSET

ACKRTN RVS	ACK reply antenna switch reverse bit
0	Not reversed
1	Reversed

ANTMONI	Receive antenna monitor bit
0	ANTSELOUT0 = H
1	ANTSELOUT1 = H

ANTACK RCVSET	ACK receive antenna switch setting bit
0	ANTSELOUT0 = H
1	ANTSELOUT1 = H

ANTACK RTNSET	ACK reply antenna switch setting bit
0	ANTSELOUT0 = H
1	ANTSELOUT1 = H

Caution Be sure to clear bits 4 to 7 to "0". Bit 2 is Read Only.

Downloaded from Arrow.com.

3.4.90 Lower limit threshold setting register after SFD detection (PWRLOWTH2)

<R> This register is used to set threshold for detection of no communication state after SFD detection.This register is valid when receive level filter enable bit is 1.

<R> An interrupt request is issued as receive level filter interrupt to return to receive wait state detecting no communication state when the connection is cut during communication or frame length is error detected. When the operation is under noisy environment usually, no communication state is detected correctly adjusting this register. The default is 1 (no communication state is detected when the communication does not formed completely). Set this register to 2 under match noisy environment.

<R> **Figure 3 - 101 Lower limit threshold setting register after SFD detection (PWRLOWTH2) Format**

Address: 050FH After reset: 00H W

Symbol	7	6	5	4	3	2	1	0
PWRLOWTH2								

PWRLOWTH2	Lower limit threshold value after SFD detection (threshold level of receive level filter)

Setting example (at 100 kbps)
Usual use: 01H
Under match noisy environment: 02H

Caution Receive characteristic might be degraded when the setting value is over 02H.

Downloaded from Arrow.com.

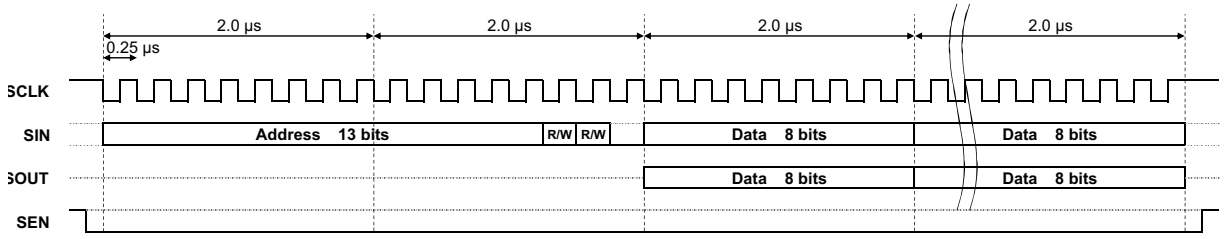
CHAPTER 4 SERIAL INTERFACE

4.1 Communication Format

Data communication is performed in the communication format of 8-bit unit serial communication. The communication timing chart when SCLK is set to 4 MHz is shown in **Figure 4 - 1**.

- Address: 13 bits (AD12 to AD0)
- R/W: 2 bits (When reading: 11b, when writing: 00b)
- Fixed to 0: 1 bit
- Data: 8 bits (DB7 to DB0)

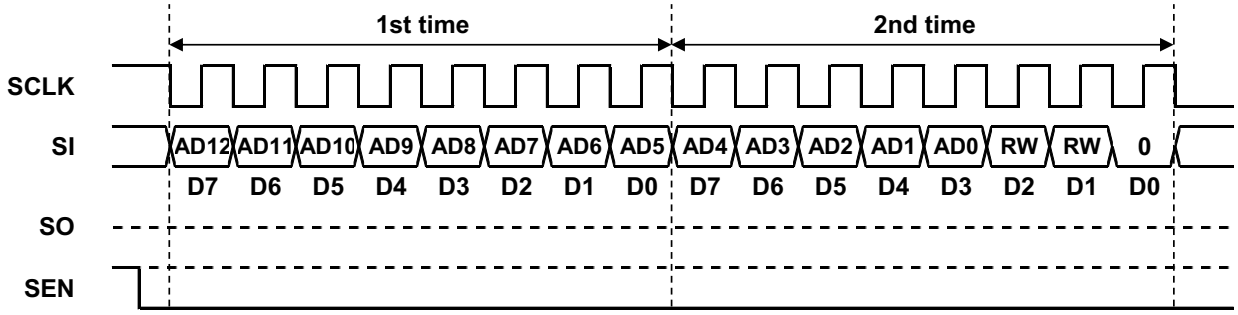
Figure 4 - 1 Serial Interface Communication Timing (Overall)



4.1.1 Address part and R/W part

The 1st and 2nd communication timing chart after the SEN pin is in the low level is shown in **Figure 4 - 2**.
The upper address (AD12 to AD5) and the lower address (AD4 to AD0) are communicated by the first 8-bit serial communication and the next 8-bit serial communication, respectively. Finally, R/W is communicated. Be sure to set "0" to the final one bit of R/W.

Figure 4 - 2 Serial Interface Communication Timing (Address part and R/W part)



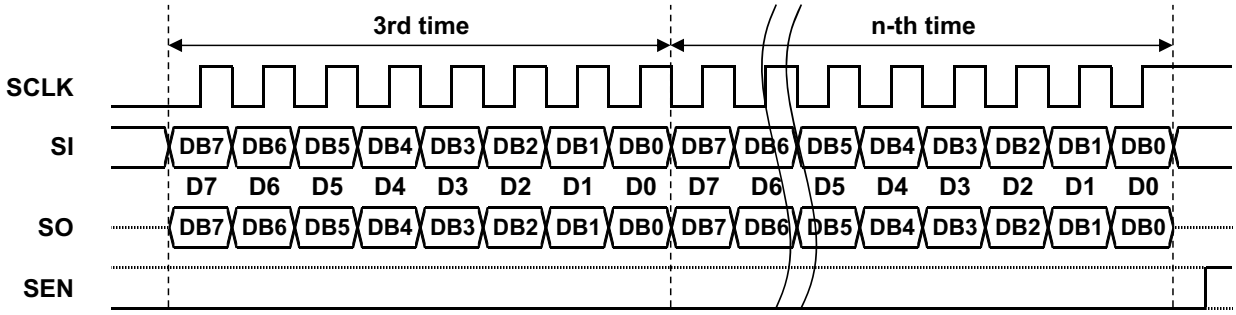
Downloaded from Arrow.com.

4.1.2 Data part

The 3rd and later communication timing chart after the SEN pin is in the low level is shown in **Figure 4 - 3**. In the case R/W is "00," the 8-bit data input from the SIN pin is written into the specified address. In the case R/W is "11," the data which is read from the specified address is output to SOUT.

In addition, performing the fourth and later serial communication with the SEN pin is left in the low level automatically increments the address resulting in enabling the data read and write, accordingly.

Figure 4 - 3 Serial Interface Communication Timing (Data part)



Downloaded from Arrow.com.

CHAPTER 5 STATE TRANSITION

Figure 5 - 1 shows the state transition. The state transition to each state of SLEEP, IDLE, Tx, and Rx is performed according to the setting.
The state returns to IDLE automatically after transmit completion, receive completion or CCA completion.
The following function is provided between Tx and Rx.

- AUTO Rx (ACK reception) function: Changes to the reception state automatically via the IDLE state after data transmission.
- AUTO Tx (ACK transmission) function: Changes to the transmission state automatically via the IDLE state after data reception.

Figure 5 - 1 State Transition

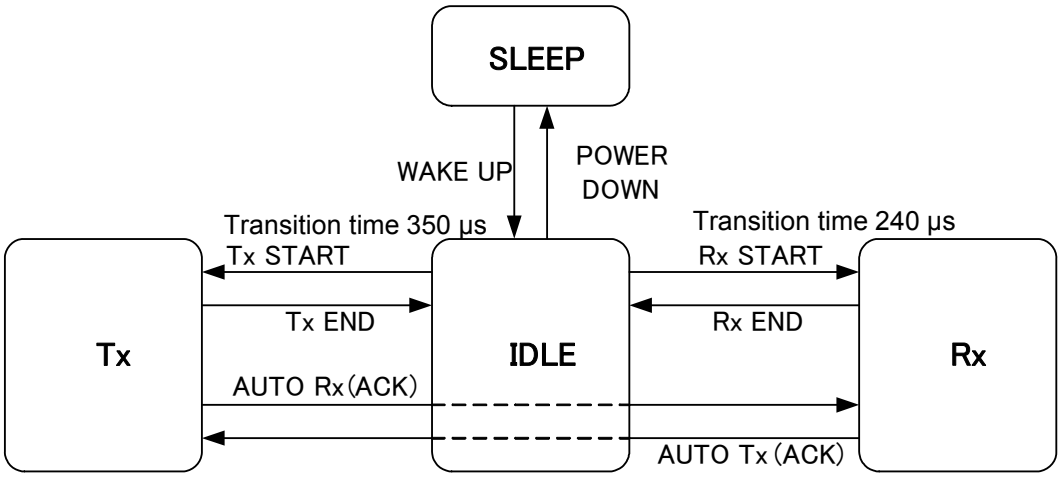


Table 5 - 1 Description of Each Mode

Mode	Description
SLEEP	Turns all the RF transceiver internal circuits to the OFF state. Each register is reset to default value, and setting is also disabled. To change to the IDLE state, Wake Up (startup sequence) must be executed according to the procedures in 5.1.
IDLE	Power supply circuit (DDC/LDO) and 48 MHz crystal oscillator circuit are activated. The settings and data of each register in the RF transceiver are retained. -Returns to IDLE after completion of operation in case of transmission. -Returns to IDLE after completion of operation or setting RFSTOP bit to 1 in case of reception. -Returns to IDLE after completion of operation or setting RFSTOP bit to 1 in case of CCA.
Tx	Indicates the transmission state. Outputs the data written in the data RAM to the RFOUT pin in the specified format.
Rx	Indicates the reception state. Receives the signal input from the RFIP pin.

Downloaded from Arrow.com.

5.1 Wake Up (SLEEP → IDLE)

Figure 5 - 2 shows the Wake Up operation (startup sequence) for the crystal oscillator . While the power is applied externally, set to the high level of STANDBY pin → OSCDRVSEL pin → DON pin → RFRESETB pin in this order. **Figure 5 - 3** shows the startup sequence for the external clock (TCXO, etc.) input. The high level is fixed in the OSCDRVSEL pin. Set to the high level in the STANDBY pin and the DON pin simultaneously. For each state of <1><2><3> and <5>, set to secure the described time or longer. **Table 5 - 3** shows the operation in each state.

Figure 5 - 2 Wake Up Operation 1 (for crystal oscillator)

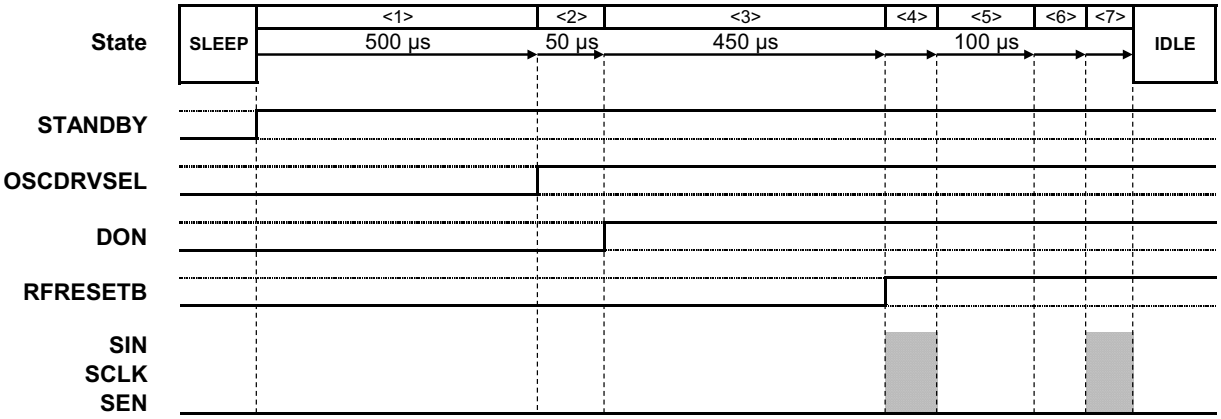


Figure 5 - 3 Wake Up Operation 2 (for external clock input)

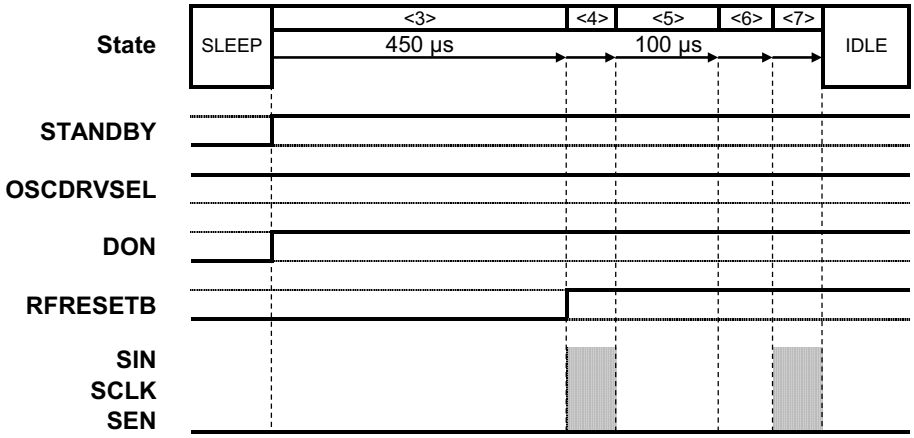


Table 5 - 2 Pin Status

Pin	SLEEP	<1>	<2>	<3>	<4>
SEN	Input	Input	Input	Input	Input
SCLK	Input	Input	Input	Input	Input
SIN	Input	Input	Input	Input	Input
SOUT	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output
INTOUT	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output
GPIO0 to GPIO4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	According to register setting value

Downloaded from Arrow.com.

Table 5 - 3 Operation in Each State in Startup Sequence

State	Operation
<1>	Time taken from startup of crystal oscillator circuit to the oscillation development. When OSCDRVSEL is at the low level, the buffer size (current) of the oscillator circuit becomes larger.
<2>	Time taken from switch of the buffer size of the crystal oscillator circuit to the output stabilization. When OSCDRVSEL is at the high level, the buffer size (current) of the oscillator circuit is smaller.
<3>	Time taken from start of the DCDC converter operation to the output voltage stabilization.
<4>	Cancels the internal circuit reset, and sets interrupt. The calibration starts by setting the calibration register to execute the calibration.
<5>	Executes the calibration for the manufacture variation and reception system IF filter.
<6>	Time taken from detection of the interrupt generation by the INTOUT pin after completion of calibration to start of reading the interrupt flag.
<7>	Sets the processing after completion of calibration by the serial communication. Setting values are the same in cases of crystal oscillation and external clock (TCXO, etc.).

Downloaded from Arrow.com.

Set initial setting registers in Table 5 - 4 and Table 5 - 5 in order from the top in status <7>.
Setting values for initial setting registers are not depend on “Frequency band identifier” in Table 5 - 5.

Caution Refer to the latest application note for setting data in Table 5 - 4 when to use the product.

Table 5 - 4 Initial Setting Registers

Register address (H)	Setting value (H)	Register address (H)	Setting value (H)
000A	8C	0475	32
003A	80	047A	60
0048	04	047B	01
0052	0E	047E	03
0053	01	0481	00
0054	5E	0488	82
0057	50	04EE	00
0058	E6	04F9	03
005A	F0	0501	10
005C	F0	050D	60
0078	E6	050E	01
007C	50	050F	02
007E	E6	0510	00
0086	03	0515	03
008E	73	0583	7F
0092	7B	0587	7F
0094	26	05A5	0A
0096	73	05A6	0A
00A6	0F	05AD	40
0402	04	00D8	04
0430	02	00D9	44
043A	94	00DC	8D
046F	05	00DD	1F
0470	05	00DC	00
0473	F6	00DD	6E

Downloaded from Arrow.com.

5.2 Power Down (IDLE → SLEEP)

Set the STANDBY pin to the low level to enter the SLEEP state. For the crystal oscillator, set the STANDBY pin to the low level, and then set the OSCDRVSEL pin, DON pin, RFRESETB pin to the low level. Otherwise, set all these pins to the low level simultaneously.

For the external clock input, the high level is fixed in the OSCDRVSEL pin. Set the other pin as the same as the crystal oscillator.

Downloaded from Arrow.com.

5.3 Other State Transition

Register setting by the serial communication enables each state transition between IDLE and TX, between IDLE and RX, and between TX and RX. Examples of procedures for transmission and reception are described below.

5.3.1 Example of Procedure for Transmission

(1) Execute the operation described in **5.1 Wake Up (SLEEP → IDLE)**.
(2) Set the transmission frequency in the frequency setting register (BBFREQ).
For details, refer to **6.2 RF frequency setting for transmission**.
(3) Set the transmission output power.
For details, refer to **6.1 Example of Procedure for Transmission Output Power Setting**.
(4) Set the AUTORCV0 bit of the transmission/reception mode register 0 (BBTXRXMODE0) to ”1” when using automatic reception switch mode.
(5) Write in the transmission RAM: Bank 0 (0200H to 027FH address), Bank 1 (0280H to 02FFH address).
(6) Set the transmission frame length in the transmission frame length register (BBTXFLEN).
(7) Set the TRNTRG bit of the transmission/reception control register (BBTXRXCON) to ”1” (transmission start).

After start of transmission, the transmission completion interrupt occurs when the following events occur.
- Transmission completion
- Transmission together with the ACK request with the ACK reception function enabled to complete the ACK reception
- Failure in the ACK reception for a certain period of time after transmission together with the ACK request with the ACK reception function enabled
- Channel busy as the CCA result after transmission with the automatic CSMA-CA enabled

5.3.2 Example of Procedure for Reception

(1) Execute the operation described in **5.1 Wake Up (SLEEP → IDLE)**.
(2) Set the reception frequency in the frequency setting register (BBFREQ).
For details, refer to **6.3 RF frequency setting for reception**.
(3) Set the AUTOACKEN bit, AUTORCV0 bit, and BEACON bit of the transmission/reception mode register 0 (BBTXRXMODE0) to ”1” when using the automatic ACK mode.
(4) Set the PAN identifier in the PAN identifier register 0 (BBPANID0) and PAN identifier register 1 (BBPANID1).
(5) Set the short address register 0 (BBSHORTAD0), short address register 1 (BBSHORTAD1), or short address register 0 (BBEXTENDAD00 to BBEXTENDAD03), short address register 1 (BBEXTENDAD10 to BBEXTENDAD13).
(6) Set the RCVTRG bit of the transmission/reception control register (BBTXRXCON) to ”1” (reception start).
(7) Wait for the reception completion interrupt.
(8) Set the bank selection in the RCVBANKSEL bit of the transmission/reception mode register 3 (BBTXRXMODE3).
(9) Read the reception frame length register (BBRXFLEN).
(10) Check the CRC result by the CRC bit of the transmission/reception status register 0 (BBTXRXST0).
(11) Read the reception RAM data: Bank 0 (0300H to 037FH address), Bank 1 (0380H to 03FFH address).

Downloaded from Arrow.com.

5.3.3 Example of Procedure for CCA

(1) Execute the operation described in **5.1 Wake Up (SLEEP → IDLE)**.
(2) Set the reception frequency in the frequency setting register (BBFREQ).
For details, refer to **6.3 RF frequency setting for reception**.
(3) Set the CCATRG bit of the transmission/reception control register (BBTXRXCON) to ”1” (CCA start).
(4) Wait for the CCA completion interrupt.
(5) Check the CCA result by the CCA bit of the transmission/reception status register 0 (BBTXRXST0).

5.3.4 Example of Procedure for CSMA-CA

(1) Execute the operation described in **5.1 Wake Up (SLEEP → IDLE)**.
(2) Set the reception frequency in the frequency setting register (BBFREQ).
For details, refer to **6.3 RF frequency setting for reception** .
(3) For the beacon mode, set the BEACON bit of the transmission/reception mode register 0 (BBTXRXMODE0) to ”1”.
(4) Set the BOFFPROD0-BOFFPROD7 bit of the back-off period register 2 (BBBOFFPROD2) to the default value. And then, set the BOFFPRODEN bit of the back-off period register (BBBOFFPROD) to “1” (back-off period register automatic random permission).
(5) Set the CSMAST bit of the CSMA control register 0 (BBCSMACON0) to ”1” (Automatic CSMA-CA start). To perform transmission processing after CSMA-CA completion simultaneously, set the CSMATRNST bit of the CSMA control register 0 (BBCSMACON0) to ”1” (transmission processing after CSMA-CA) after completion of CSMA-CA.
(6) Wait for the CSMA-CA completion interrupt.
(7) Check the CSMA-CA result by the CSMA-CA bit of the transmission/reception status register 0 (BBTXRXST0).

5.3.5 Example of Procedure for Calibration

(1) Set 07H to RF start register (BBRFCON).
(2) Set 00H to initial setting register 10 (RFINI10) and 00H to initial setting register 11 (RFINI11) continuously.
(3) Set 01H to Calibration register (BBCAL).
Calibration starts.
(4) Wait for calibration completion interrupt.
(5) Set 03H to RF start register (BBRFCON).

Caution -Required calibration for 5.1 WAKEUP.
-Required calibration in IDLE to change ”Mode” in Table 5 - 7 Each Data Rate List (5.3.6 Setting for Each Data Rate).

Downloaded from Arrow.com.

5.3.6 Setting for Each Data Rate

The list of each data rate is shown in **Table 5 - 5** and the settings required for each data rate is listed in **Table 5 - 6**. Set values to addresses listed in **Table 5 - 6** (1/10) to (10/10) from the left in order according to the desired data rate in IDLE mode.

Caution 1. Calibration must be done after change of "Mode" following 5.3.5 Example of Procedure for Calibration.

Caution 2. Refer to the latest application note for setting data in Table 5 - 6 when to use the product.

Table 5 - 5 Each Data Rate List

Frequency band identifier	PHY	Frequency band	Modulation	Mode	Data rate (kbps)	Modulation index	Channel spacing (kHz)
4	863 MHz (Europe)	863 to 870 MHz	2FSK/2GFSK	001	50	1	200
				002	100		400
			4FSK/4GFSK	003	200	0.33	
5	896 MHz (US)	896 to 901 MHz	2FSK/2GFSK	004	10	0.5	25
				005	20		50
				006	40		100
6	901 MHz (US)	901 to 902 MHz	2FSK/2GFSK	007	10	0.5	25
				008	20		50
				009	40		100
7	915 MHz (US)	902 to 928 MHz	2FSK/2GFSK	010	50	1	200
				011	150	0.5	400
				012	200		
8	917 MHz (Korea)	917 to 923.5 MHz	2FSK/2GFSK	013	50	1	200
				014	150	0.5	400
				015	200		
9	920 MHz (Japan)	920 to 928 MHz	2FSK/2GFSK	016	50	1	200
				000	100		400
				017	200		600
			4FSK/4GFSK	018	400	0.33	
Other		920 to 928 MHz	2GFSK	019	300	0.5	600
		902 to 928 MHz	2GFSK	020	100	0.5	200
		902 to 928 MHz	2GFSK	021	300	0.5	600

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (1/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)								
				000E	00B1	00B2		00AC	00AD	00CC	00CE	
						Diversity: No	Diversity: Yes				Diversity: No	Diversity: Yes
4	863 MHz (Europe)	001	50	A3	42	0C	0C	E0	01	01	0C	0C
		002	100	A3	42	20	11	F0	00	00	20	11
		003	200	A1	83	20	11	F0	00	00	20	11
5	896 MHz (US)	004	10	A3	02	0C	0C	60	09	00	0C	0C
		005	20	A3	02	0C	0C	B0	04	01	0C	0C
		006	40	A3	02	0C	0C	58	02	01	0C	0C
6	901 MHz (US)	007	10	A3	02	0C	0C	60	09	00	0C	0C
		008	20	A3	02	0C	0C	B0	04	00	0C	0C
		009	40	A3	02	0C	0C	58	02	01	0C	0C
7	915 MHz (US)	010	50	A3	42	0C	0C	E0	01	01	0C	0C
		011	150	A2	02	20	10	A0	00	00	20	10
		012	200	A1	02	2E	18	78	00	00	2E	18
8	917 MHz (Korea)	013	50	A3	42	0C	0C	E0	01	01	0C	0C
		014	150	A2	02	20	10	A0	00	00	20	10
		015	200	A1	02	2E	18	78	00	00	2E	18
9	920 MHz (Japan)	016	50	A3	42	0C	0C	E0	01	01	0C	0C
		000	100	A3	42	20	11	F0	00	01	20	11
		017	200	A1	42	2E	18	78	00	02	2E	18
		018	400	A1	83	2E	18	78	00	02	2E	18
Other		019	300	A2	02	3E	2A	50	00	02	3E	2A
		020	100	A3	02	20	11	F0	00	01	20	11
		021	300	A2	02	3E	2A	50	00	02	3E	2A

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (2/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)									
				0044		00C0	00C2	00C3	00C4	00C5	0110		00C6
				FEC: Enable	FEC: Disable						FEC: Enable	FEC: Disable	
4	863 MHz (Europe)	001	50	86	8E	AA	09	72	00	00	86	8E	02
		002	100	8D	95	AA	09	72	00	00	90	98	02
		003	200	8D	95	EE	EB	AA	AE	BF	90	98	06
5	896 MHz (US)	004	10	83	8B	AA	09	72	00	00	83	8B	02
		005	20	87	8F	AA	09	72	00	00	87	8F	02
		006	40	8B	93	AA	09	72	00	00	8B	93	02
6	901 MHz (US)	007	10	83	8B	AA	09	72	00	00	83	8B	02
		008	20	87	8F	AA	09	72	00	00	87	8F	02
		009	40	8B	93	AA	09	72	00	00	8B	93	02
7	915 MHz (US)	010	50	8C	94	AA	09	72	00	00	8C	94	02
		011	150	91	99	AA	09	72	00	00	91	99	02
		012	200	90	98	AA	09	72	00	00	91	99	02
8	917 MHz (Korea)	013	50	8C	94	AA	09	72	00	00	8C	94	02
		014	150	91	99	AA	09	72	00	00	91	99	02
		015	200	90	98	AA	09	72	00	00	91	99	02
9	920 MHz (Japan)	016	50	8C	94	AA	09	72	00	00	8C	94	02
		000	100	8D	95	AA	09	72	00	00	90	98	02
		017	200	92	9A	AA	09	72	00	00	91	99	02
		018	400	8C	94	EE	EB	AA	AE	BF	91	99	06
Other		019	300	94	9C	AA	09	72	00	00	90	98	02
		020	100	8D	95	AA	09	72	00	00	90	98	02
		021	300	94	9C	AA	09	72	00	00	90	98	02

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (3/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)									
				043A	042D		0430	0432	0457		0458		0422
					Diversity: No	Diversity: Yes			FEC: Enable	FEC: Disable	FEC: Enable	FEC: Disable	
4	863 MHz (Europe)	001	50	96	0B	09	0C	18	91	D5	00	01	01
		002	100	96	0A	0A	02	14	6C	A4	01	02	01
		003	200	96	0C	0A	02	0C	E6	46	00	03	09
5	896 MHz (US)	004	10	90	06	0A	08	78	73	B7	00	01	09
		005	20	96	3C	3C	0C	3C	91	21	00	02	09
		006	40	96	1E	1E	0C	1E	E6	40	00	03	09
6	901 MHz (US)	007	10	90	06	0A	08	78	73	B7	00	01	09
		008	20	96	3C	3C	0C	3C	91	21	00	02	09
		009	40	96	1E	1E	0C	1E	E6	40	00	03	09
7	915 MHz (US)	010	50	96	0B	09	0C	18	E6	D5	00	03	01
		011	150	96	08	08	02	08	40	F5	02	08	09
		012	200	96	06	06	02	06	91	D5	00	03	09
8	917 MHz (Korea)	013	50	96	0B	09	0C	18	91	D5	00	03	01
		014	150	96	08	08	02	08	40	F5	02	08	09
		015	200	96	06	06	02	06	91	D5	00	03	09
9	920 MHz (Japan)	016	50	96	0B	09	0C	18	91	D5	00	03	01
		000	100	9E	0A	0A	02	14	6C	A4	01	05	01
		017	200	9E	06	06	02	0D	D5	46	02	0C	01
		018	400	96	06	06	02	09	D5	7D	02	0C	09
Other		019	300	96	04	04	02	0D	A7	DD	05	13	09
		020	100	96	0A	0A	02	0C	6C	A7	01	05	09
		021	300	96	04	04	02	0D	47	DD	0D	13	09

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (4/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)										
				0423	0454	0456	0474	047C	047D	047F	0480	0483	0486	0487
4	863 MHz (Europe)	001	50	01	28	02	A6	1B	0F	34	00	3E	55	05
		002	100	01	28	02	A9	1B	0F	34	20	3F	00	00
		003	200	09	28	02	A6	1B	0F	35	00	3F	33	03
5	896 MHz (US)	004	10	09	28	02	A6	1B	0F	34	00	09	02	00
		005	20	09	28	02	A6	1A	0F	34	00	03	32	00
		006	40	09	28	02	A6	1A	0F	34	00	03	32	00
6	901 MHz (US)	007	10	09	28	02	A6	1B	0F	34	00	09	02	00
		008	20	09	28	02	A6	1A	0F	34	00	03	32	00
		009	40	09	28	02	A6	1A	0F	34	00	03	32	00
7	915 MHz (US)	010	50	01	28	02	A6	1B	0F	34	00	3B	55	05
		011	150	09	28	02	A6	1B	0F	34	01	09	00	00
		012	200	09	28	02	A6	1B	0F	34	00	09	00	00
8	917 MHz (Korea)	013	50	01	28	02	A6	1B	0F	34	00	3F	55	05
		014	150	09	28	02	A6	1B	0F	34	01	09	00	00
		015	200	09	28	02	A6	1B	0F	34	00	09	00	00
9	920 MHz (Japan)	016	50	01	28	02	A6	1B	0F	34	00	3C	55	05
		000	100	01	2E	06	A6	1B	0F	34	20	3D	00	00
		017	200	01	28	02	A6	1B	0F	34	01	3C	00	00
		018	400	09	28	02	A7	1B	0F	34	01	3C	00	00
Other		019	300	09	28	02	A7	19	0D	33	02	19	00	00
		020	100	09	28	02	A7	1B	0F	34	00	3D	00	00
		021	300	09	28	02	A7	19	0D	33	06	19	00	00

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (5/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)										
				048D	048F	0491	0492	0493	0494	0581	0582	058F	059F	05A0
4	863 MHz (Europe)	001	50	46	66	20	55	20	55	12	26	FF	FF	3F
		002	100	57	55	20	55	20	55	15	1C	32	56	03
		003	200	46	66	30	55	30	55	10	24	FF	FF	3F
5	896 MHz (US)	004	10	46	66	20	55	20	55	05	30	FF	FF	3F
		005	20	46	55	20	55	20	55	00	30	FF	FF	3F
		006	40	46	55	20	55	20	55	1C	2B	FF	FF	3F
6	901 MHz (US)	007	10	46	66	20	55	20	55	05	30	FF	FF	3F
		008	20	46	55	20	55	20	55	00	30	FF	FF	3F
		009	40	46	55	20	55	20	55	1C	2B	FF	FF	3F
7	915 MHz (US)	010	50	46	66	20	55	20	55	12	26	FF	FF	3F
		011	150	57	55	20	55	20	55	12	26	FF	FF	3F
		012	200	57	55	20	55	20	55	16	2C	FF	FF	3F
8	917 MHz (Korea)	013	50	46	66	20	55	20	55	12	26	FF	FF	3F
		014	150	57	55	20	55	20	55	12	26	FF	FF	3F
		015	200	57	55	20	55	20	55	16	2C	FF	FF	3F
9	920 MHz (Japan)	016	50	46	66	20	55	20	55	12	26	FF	FF	3F
		000	100	57	55	20	55	20	55	15	1C	32	56	03
		017	200	57	55	20	55	20	55	13	18	FF	FF	3F
		018	400	46	66	30	50	30	50	11	25	FF	FF	3F
Other		019	300	46	55	20	54	20	54	15	21	FF	FF	3F
		020	100	46	55	20	54	20	54	17	33	FF	FF	3F
		021	300	46	55	20	54	20	54	15	21	FF	FF	3F

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (6/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)										
				05A1	05A2	0405	04F6	04F8	0505	0403	0415	04D9	0100	0101
4	863 MHz (Europe)	001	50	FF	3F	10	10	00	48	04	00	36	F6	72
		002	100	56	03	10	10	00	48	04	00	36	F6	72
		003	200	FF	3F	04	10	30	48	0C	F1	2F	BE	FF
5	896 MHz (US)	004	10	FF	3F	10	04	38	48	04	F1	36	F6	72
		005	20	FF	3F	10	04	38	48	04	F1	36	F6	72
		006	40	FF	3F	10	04	38	48	04	F1	36	F6	72
6	901 MHz (US)	007	10	FF	3F	10	04	38	48	04	F1	36	F6	72
		008	20	FF	3F	10	04	38	48	04	F1	36	F6	72
		009	40	FF	3F	10	04	38	48	04	F1	36	F6	72
7	915 MHz (US)	010	50	FF	3F	10	10	00	48	04	00	36	F6	72
		011	150	FF	3F	10	04	38	48	04	F1	36	F6	72
		012	200	FF	3F	10	04	38	48	04	F1	36	F6	72
8	917 MHz (Korea)	013	50	FF	3F	10	10	00	48	04	00	36	F6	72
		014	150	FF	3F	10	04	38	48	04	F1	36	F6	72
		015	200	FF	3F	10	04	38	48	04	F1	36	F6	72
9	920 MHz (Japan)	016	50	FF	3F	10	10	00	48	04	00	36	F6	72
		000	100	56	03	10	10	00	48	04	00	36	F6	72
		017	200	FF	3F	10	10	00	48	04	00	36	F6	72
		018	400	FF	3F	04	10	30	48	0C	F1	2F	BE	FF
Other		019	300	FF	3F	10	04	38	48	04	F1	36	F6	72
		020	100	FF	3F	10	04	38	45	04	F1	36	F6	72
		021	300	FF	3F	10	04	38	48	04	F1	36	F6	72

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (7/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)										
				0102	0103	0104	0105	0106	0107	0108	0109	010A	010B	00DC
4	863 MHz (Europe)	001	50	00	00	5E	70	00	00	C6	B4	00	00	11
		002	100	00	00	5E	70	00	00	C6	B4	00	00	10
		003	200	AE	BF	FE	BB	AA	BF	BE	FA	BA	EF	10
5	896 MHz (US)	004	10	00	00	5E	70	00	00	C6	B4	00	00	10
		005	20	00	00	5E	70	00	00	C6	B4	00	00	11
		006	40	00	00	5E	70	00	00	C6	B4	00	00	11
6	901 MHz (US)	007	10	00	00	5E	70	00	00	C6	B4	00	00	10
		008	20	00	00	5E	70	00	00	C6	B4	00	00	10
		009	40	00	00	5E	70	00	00	C6	B4	00	00	11
7	915 MHz (US)	010	50	00	00	5E	70	00	00	C6	B4	00	00	11
		011	150	00	00	5E	70	00	00	C6	B4	00	00	10
		012	200	00	00	5E	70	00	00	C6	B4	00	00	10
8	917 MHz (Korea)	013	50	00	00	5E	70	00	00	C6	B4	00	00	11
		014	150	00	00	5E	70	00	00	C6	B4	00	00	10
		015	200	00	00	5E	70	00	00	C6	B4	00	00	10
9	920 MHz (Japan)	016	50	00	00	5E	70	00	00	C6	B4	00	00	11
		000	100	00	00	5E	70	00	00	C6	B4	00	00	11
		017	200	00	00	5E	70	00	00	C6	B4	00	00	02
		018	400	AE	BF	FE	BB	AA	BF	BE	FA	BA	EF	02
Other		019	300	00	00	5E	70	00	00	C6	B4	00	00	02
		020	100	00	00	5E	70	00	00	C6	B4	00	00	11
		021	300	00	00	5E	70	00	00	C6	B4	00	00	02

Downloaded from Arrow.com.

Table 5 - 6 Settings Required for Each Data Rate (8/8)

Frequency band identifier	PHY	Mode	Data rate (kbps)	Address (H)										
				00DD	00DC	00DD	00F1	00F2	00F3	00F4	00F5	00FB	00DC	00DD
4	863 MHz (Europe)	001	50	0E	10	23	06	0A	5F	0D	DA	DA	12	63
		002	100	0E	10	23	09	0F	5F	11	DA	DA	12	63
		003	200	0E	10	23	0E	17	5F	0F	DA	DA	12	63
5	896 MHz (US)	004	10	0E	10	23	06	0A	5F	0D	CA	CA	0A	63
		005	20	0E	10	23	06	0A	5F	0D	CA	CA	0A	63
		006	40	0E	10	23	06	0A	5F	0D	CA	CA	0A	63
6	901 MHz (US)	007	10	0E	10	23	06	0A	5F	0D	CA	CA	0A	63
		008	20	0E	10	23	06	0A	5F	0D	CA	CA	0A	63
		009	40	0E	10	23	06	0A	5F	0D	CA	CA	0A	63
7	915 MHz (US)	010	50	0E	10	23	06	0A	5F	0D	BA	BA	0A	63
		011	150	0E	10	23	17	25	5F	0D	BA	BA	0A	63
		012	200	0E	10	23	26	3D	9F	06	BA	BA	0A	63
8	917 MHz (Korea)	013	50	0E	10	23	06	0A	5F	0D	BA	BA	0A	63
		014	150	0E	10	23	17	25	5F	0D	BA	BA	0A	63
		015	200	0E	10	23	26	3D	9F	06	BA	BA	0A	63
9	920 MHz (Japan)	016	50	0E	10	23	06	0A	5F	0D	BA	BA	0A	63
		000	100	0E	10	23	09	0F	5F	11	BA	BA	0A	63
		017	200	0E	40	23	0E	17	5F	0F	BA	BA	0A	63
		018	400	0E	40	23	0E	17	5F	0F	BA	BA	0A	63
Other		019	300	0E	40	23	37	58	5F	04	BA	BA	0A	63
		020	100	0E	10	23	0E	17	5F	0F	BA	BA	0A	63
		021	300	0E	40	23	37	58	5F	04	BA	BA	0A	63

Downloaded from Arrow.com.

CHAPTER 6 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING

6.1 Example of Procedure for Transmission Output Power Setting

Details of "(3) Set the transmission output power." in "5.3.1 Example of Procedure for Transmission" are described below.

(1) See tables according to ”Frequency band identifier” in **Table 5 - 5 Each Data Rate List**.
When it is 9, **Table 6 - 1** to **6 - 4**. When it is 4, see **Table 6 - 5** to **6 - 7**. When it is 5 to 7, see **Table 6 - 8 to 6 - 10**. When it is 8, see **Table 6 - 11** to **6 - 13**.

(2) Set the data [1:0] of 0090H address according to the table. Fix the data [7:2] at ”111101b”.

<R> When setting the data [1:0] of the 0090H address to 1H, set V_{DDRF}[Note] to 2.4 V or higher.

(3) Set the data [4:0] of the 0092H address according to the table. Fix the data [7:5] at "011b".

(4) Set the data [4:0] of 00DCH address according to the table and 19H to address 00DDH. Fix the data [7:5] at ”000b”.

(5) Set the data [4:0] of 00DCH address according to the table and 25H to address 00DDH. Fix the data [7:5] at ”000b”.

(6) Set the data [7:4] of 00DCH address according to the table and 1AH to address 00DDH. Fix the data [3:0] at ”0000b”.

Figure 6 - 1 to **Figure 6 - 4** show the relationship between the transmission output power and gain set.
The values may vary depending on the load conditions and samples. The combination of the coarse control and fine control enables the wider range of the transmission output power.

<R> **Note** Voltage of VCCRF and VCCDDC pins.

Caution Refer to the latest application note for setting values of Figure 6 - 1 to Figure 6 - 4 when to use the product.

Table 6 - 1 Gain Set (Frequency band identifier = 9) (1/4)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
0	3	00	0	00	0
1	3	00	0	1F	6
2	3	01	0	1F	6
3	3	02	0	1F	6
4	3	03	0	1F	6
5	3	04	0	1F	6
6	3	05	0	1F	6
7	3	06	0	1F	6
8	3	07	0	1F	6
9	3	08	0	1F	6
10	3	09	0	1F	6
11	3	0A	0	1F	6
12	3	0B	0	1F	6
13	3	0C	0	1F	6
14	3	0D	0	1F	6

Downloaded from Arrow.com.

Table 6 - 2 Gain Set (Frequency band identifier = 9) (2/4)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
15	3	0E	0	1F	6
16	3	0F	0	1F	6
17	3	10	0	1F	6
18	3	11	0	1F	6
19	3	12	0	1F	6
20	3	13	0	1F	6
21	3	14	0	1F	6
22	2	15	0	1F	6
23	2	16	0	1F	6
24	2	17	0	1F	6
25	2	18	0	1F	6
26	2	19	0	1F	6
27	2	1A	0	1F	6
28	2	1B	0	1F	6
29	2	1C	0	1F	6
30	2	1D	0	1F	6
31	2	1E	0	1F	6
32	2	1F	0	1F	6
33	3	05	1	15	6
34	3	06	1	15	6
35	3	07	1	15	6
36	3	08	1	15	6
37	3	09	1	15	6
38	3	0A	1	15	6
39	3	0B	1	15	6
40	3	0C	1	15	6
41	3	0D	1	15	6
42	3	0E	1	15	6
43	3	0F	1	15	6
44	3	10	1	15	6
45	3	11	1	15	6
46	3	12	1	15	6
47	3	13	1	15	6
48	2	14	1	15	6
49	2	15	1	15	6
50	2	16	1	15	6
51	2	17	1	15	6
52	2	18	1	15	6
53	2	19	1	15	6
54	2	1A	1	15	6
55	2	1B	1	15	6
56	2	1C	1	15	6

Downloaded from Arrow.com.

Table 6 - 3 Gain Set (Frequency band identifier = 9) (3/4)

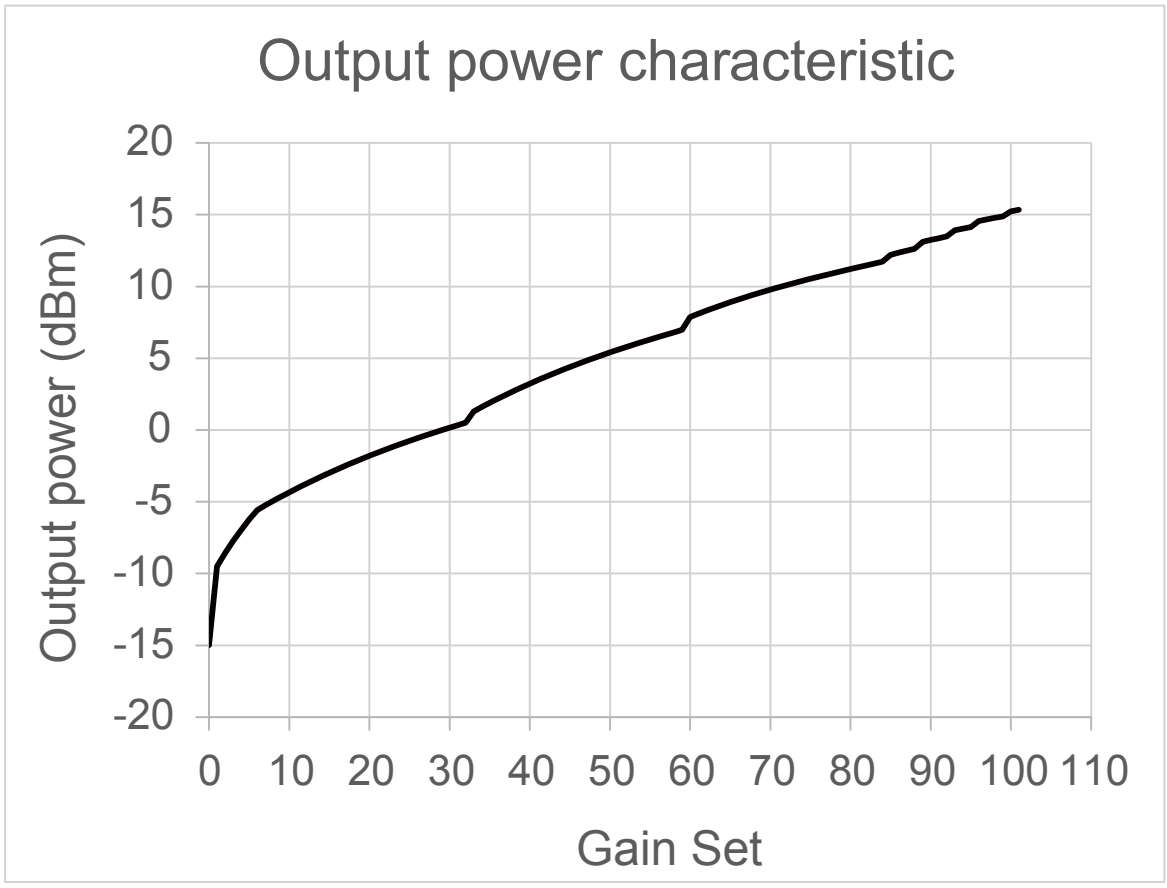
Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
57	2	1D	1	15	6
58	2	1E	1	15	6
59	2	1F	1	15	6
60	3	07	2	1F	6
61	3	08	2	1F	6
62	3	09	2	1F	6
63	3	0A	2	1F	6
64	3	0B	2	1F	6
65	3	0C	2	1F	6
66	3	0D	2	1F	6
67	3	0E	2	1F	6
68	3	0F	2	1F	6
69	3	10	2	1F	6
70	3	11	2	1F	6
71	3	12	2	1F	6
72	3	13	2	1F	6
73	3	14	2	1F	6
74	2	15	2	1F	6
75	2	16	2	1F	6
76	2	17	2	1F	6
77	2	18	2	1F	6
78	2	19	2	1F	6
79	2	1A	2	1F	6
80	2	1B	2	1F	6
81	2	1C	2	1F	6
82	2	1D	2	1F	6
83	2	1E	2	1F	6
84	2	1F	2	1F	6
85	3	11	4	16	6
86	3	12	4	16	6
87	3	13	4	16	6
88	3	14	4	16	6
89	3	11	6	16	6
90	3	12	6	16	6
91	3	13	6	16	6
92	3	14	6	16	6
93	2	15	7	15	6
94	2	16	7	15	6
95	2	17	7	15	6
96	1	1B	7	15	6
97	1	1C	7	15	6
98	1	1D	7	15	6

Downloaded from Arrow.com.

Table 6 - 4 Gain Set (Frequency band identifier = 9) (4/4)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
99	1	1E	7	15	6
100	1	1E	8	11	6
101	1	1F	8	11	6

Figure 6 - 1 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 9)



Downloaded from Arrow.com.

Table 6 - 5 Gain Set (Frequency band identifier = 4) (1/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
0	3	00	0	00	0
1	3	00	0	1F	7
2	3	01	0	1F	7
3	3	02	0	1F	7
4	3	03	0	1F	7
5	3	04	0	1F	7
6	3	05	0	1F	7
7	3	06	0	1F	7
8	3	07	0	1F	7
9	3	08	0	1F	7
10	3	09	0	1F	7
11	3	0A	0	1F	7
12	3	0B	0	1F	7
13	3	0C	0	1F	7
14	3	0D	0	1F	7
15	3	0E	0	1F	7
16	3	0F	0	1F	7
17	3	10	0	1F	7
18	3	11	0	1F	7
19	3	12	0	1F	7
20	3	13	0	1F	7
21	3	14	0	1F	7
22	2	15	0	1F	7
23	2	16	0	1F	7
24	2	17	0	1F	7
25	2	18	0	1F	7
26	2	19	0	1F	7
27	2	1A	0	1F	7
28	2	1B	0	1F	7
29	2	1C	0	1F	7
30	2	1D	0	1F	7
31	2	1E	0	1F	7
32	2	1F	0	1F	7
33	3	06	1	0F	7
34	3	07	1	0F	7
35	3	08	1	0F	7
36	3	09	1	0F	7
37	3	0A	1	0F	7
38	3	0B	1	0F	7
39	3	0C	1	0F	7
40	3	0D	1	0F	7
41	3	0E	1	0F	7

Downloaded from Arrow.com.

Table 6 - 6 Gain Set (Frequency band identifier = 4) (2/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
42	3	0F	1	0F	7
43	3	10	1	0F	7
44	3	11	1	0F	7
45	3	12	1	0F	7
46	3	13	1	0F	7
47	3	14	1	0F	7
48	2	15	1	0F	7
49	2	16	1	0F	7
50	2	17	1	0F	7
51	2	18	1	0F	7
52	2	19	1	0F	7
53	2	1A	1	0F	7
54	2	1B	1	0F	7
55	2	1C	1	0F	7
56	2	1D	1	0F	7
57	2	1E	1	0F	7
58	2	1F	1	0F	7
59	3	05	2	1B	7
60	3	06	2	1B	7
61	3	07	2	1B	7
62	3	08	2	1B	7
63	3	09	2	1B	7
64	3	0A	2	1B	7
65	3	0B	2	1B	7
66	3	0C	2	1B	7
67	3	0D	2	1B	7
68	3	0E	2	1B	7
69	3	0F	2	1B	7
70	3	10	2	1B	7
71	3	11	2	1B	7
72	3	12	2	1B	7
73	3	13	2	1B	7
74	3	14	2	1B	7
75	3	0C	3	1F	7
76	3	0D	3	1F	7
77	3	0E	3	1F	7
78	3	0F	3	1F	7
79	3	10	3	1F	7
80	3	11	3	1F	7
81	3	12	3	1F	7
82	3	13	3	1F	7
83	3	14	3	1F	7

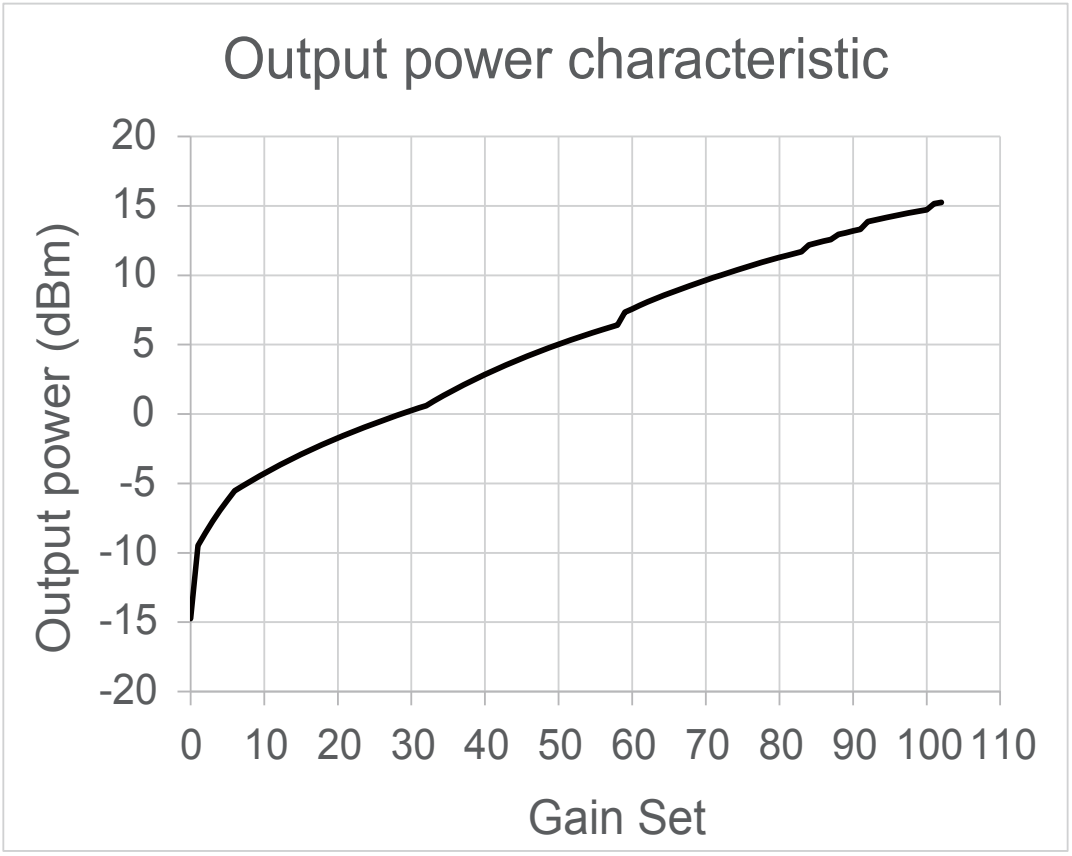
Downloaded from Arrow.com.

Table 6 - 7 Gain Set (Frequency band identifier = 4) (3/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19H)	00DCH address Bit [4:0] (00DDH address is set to 25H)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
84	3	11	4	1B	7
85	3	12	4	1B	7
86	3	13	4	1B	7
87	3	14	4	1B	7
88	3	11	6	1B	7
89	3	12	6	1B	7
90	3	13	6	1B	7
91	3	14	6	1B	7
92	1	14	7	16	7
93	1	15	7	16	7
94	1	16	7	16	7
95	1	17	7	16	7
96	1	18	7	16	7
97	1	19	7	16	7
98	1	1A	7	16	7
99	1	1B	7	16	7
100	1	1C	7	16	7
101	1	1E	8	15	7
102	1	1F	8	15	7

Downloaded from Arrow.com.

Figure 6 - 2 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 4)



Downloaded from Arrow.com.

Table 6 - 8 Gain Set (Frequency band identifier = 5 to 7) (1/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19)	00DCH address Bit [4:0] (00DDH address is set to 25)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
0	3	00	0	00	0
1	3	00	0	1F	6
2	3	01	0	1F	6
3	3	02	0	1F	6
4	3	03	0	1F	6
5	3	04	0	1F	6
6	3	05	0	1F	6
7	3	06	0	1F	6
8	3	07	0	1F	6
9	3	08	0	1F	6
10	3	09	0	1F	6
11	3	0A	0	1F	6
12	3	0B	0	1F	6
13	3	0C	0	1F	6
14	3	0D	0	1F	6
15	3	0E	0	1F	6
16	3	0F	0	1F	6
17	3	10	0	1F	6
18	3	11	0	1F	6
19	3	12	0	1F	6
20	3	13	0	1F	6
21	3	14	0	1F	6
22	2	15	0	1F	6
23	2	16	0	1F	6
24	2	17	0	1F	6
25	2	18	0	1F	6
26	2	19	0	1F	6
27	2	1A	0	1F	6
28	2	1B	0	1F	6
29	2	1C	0	1F	6
30	2	1D	0	1F	6
31	2	1E	0	1F	6
32	2	1F	0	1F	6
33	3	05	1	15	6
34	3	06	1	15	6
35	3	07	1	15	6
36	3	08	1	15	6
37	3	09	1	15	6
38	3	0A	1	15	6
39	3	0B	1	15	6
40	3	0C	1	15	6
41	3	0D	1	15	6

Downloaded from Arrow.com.

Table 6 - 9 Gain Set (Frequency band identifier = 5 to 7) (2/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19)	00DCH address Bit [4:0] (00DDH address is set to 25)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
42	3	0E	1	15	6
43	3	0F	1	15	6
44	3	10	1	15	6
45	3	11	1	15	6
46	3	12	1	15	6
47	3	13	1	15	6
48	3	14	1	15	6
49	2	15	1	15	6
50	2	16	1	15	6
51	2	17	1	15	6
52	2	18	1	15	6
53	2	19	1	15	6
54	2	1A	1	15	6
55	2	1B	1	15	6
56	2	1C	1	15	6
57	2	1D	1	15	6
58	2	1E	1	15	6
59	2	1F	1	15	6
60	3	06	2	1F	6
61	3	07	2	1F	6
62	3	08	2	1F	6
63	3	09	2	1F	6
64	3	0A	2	1F	6
65	3	0B	2	1F	6
66	3	0C	2	1F	6
67	3	0D	2	1F	6
68	3	0E	2	1F	6
69	3	0F	2	1F	6
70	3	10	2	1F	6
71	3	11	2	1F	6
72	3	12	2	1F	6
73	3	13	2	1F	6
74	3	14	2	1F	6
75	2	15	2	1F	6
76	2	16	2	1F	6
77	2	17	2	1F	6
78	2	18	2	1F	6
79	2	19	2	1F	6
80	2	1A	2	1F	6
81	2	1B	2	1F	6
82	2	1C	2	1F	6
83	2	1D	2	1F	6

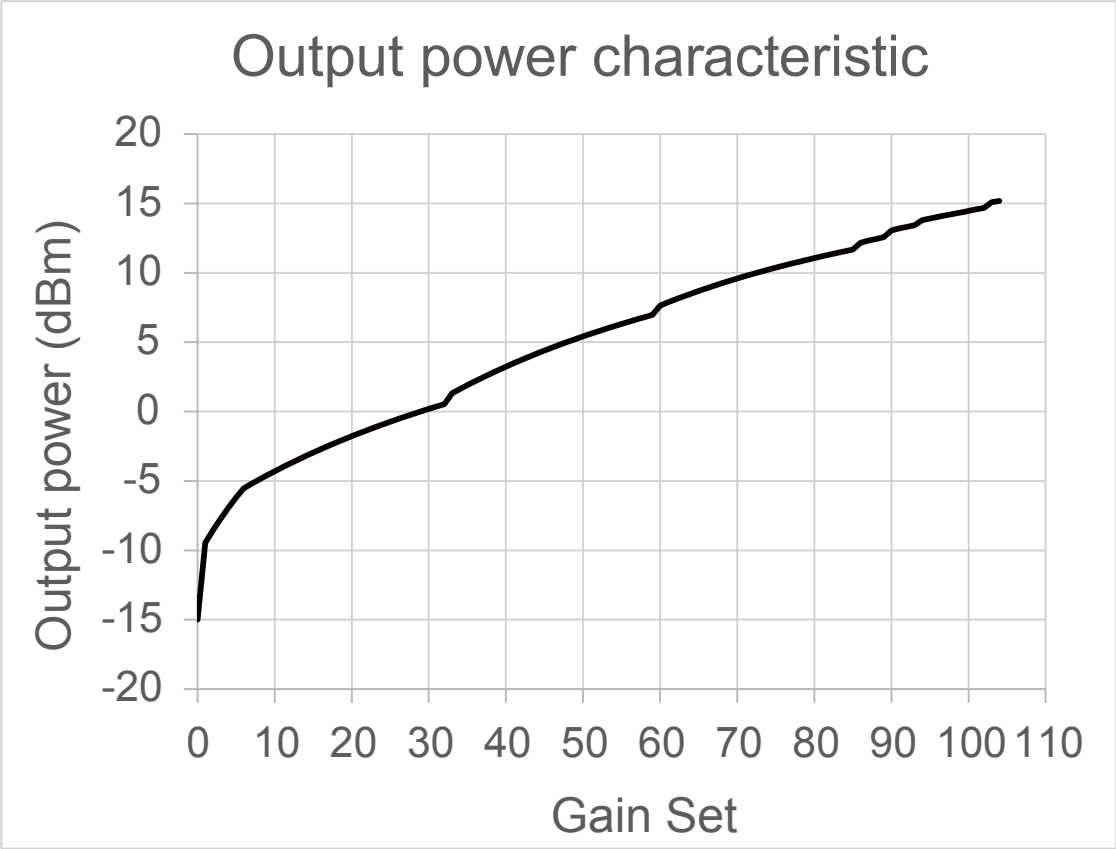
Downloaded from Arrow.com.

Table 6 - 10 Gain Set (Frequency band identifier = 5 to 7) (3/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19)	00DCH address Bit [4:0] (00DDH address is set to 25)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
84	2	1E	2	1F	6
85	2	1F	2	1F	6
86	3	11	4	16	6
87	3	12	4	16	6
88	3	13	4	16	6
89	3	14	4	16	6
90	3	11	6	16	6
91	3	12	6	16	6
92	3	13	6	16	6
93	3	14	6	16	6
94	1	14	7	14	6
95	1	15	7	14	6
96	1	16	7	14	6
97	1	17	7	14	6
98	1	18	7	14	6
99	1	19	7	14	6
100	1	1A	7	14	6
101	1	1B	7	14	6
102	1	1C	7	14	6
103	1	1D	8	11	6
104	1	1E	8	11	6

Downloaded from Arrow.com.

Figure 6 - 3 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 5 to 7)



Downloaded from Arrow.com.

Table 6 - 11 Gain Set (Frequency band identifier = 8) (1/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19)	00DCH address Bit [4:0] (00DDH address is set to 25)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
0	3	00	0	00	0
1	3	00	0	1F	6
2	3	01	0	1F	6
3	3	02	0	1F	6
4	3	03	0	1F	6
5	3	04	0	1F	6
6	3	05	0	1F	6
7	3	06	0	1F	6
8	3	07	0	1F	6
9	3	08	0	1F	6
10	3	09	0	1F	6
11	3	0A	0	1F	6
12	3	0B	0	1F	6
13	3	0C	0	1F	6
14	3	0D	0	1F	6
15	3	0E	0	1F	6
16	3	0F	0	1F	6
17	3	10	0	1F	6
18	3	11	0	1F	6
19	3	12	0	1F	6
20	3	13	0	1F	6
21	3	14	0	1F	6
22	2	15	0	1F	6
23	2	16	0	1F	6
24	2	17	0	1F	6
25	2	18	0	1F	6
26	2	19	0	1F	6
27	2	1A	0	1F	6
28	2	1B	0	1F	6
29	2	1C	0	1F	6
30	2	1D	0	1F	6
31	2	1E	0	1F	6
32	2	1F	0	1F	6
33	3	05	1	15	6
34	3	06	1	15	6
35	3	07	1	15	6
36	3	08	1	15	6
37	3	09	1	15	6
38	3	0A	1	15	6
39	3	0B	1	15	6
40	3	0C	1	15	6
41	3	0D	1	15	6

Downloaded from Arrow.com.

Table 6 - 12 Gain Set (Frequency band identifier = 8) (2/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19)	00DCH address Bit [4:0] (00DDH address is set to 25)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
42	3	0E	1	15	6
43	3	0F	1	15	6
44	3	10	1	15	6
45	3	11	1	15	6
46	3	12	1	15	6
47	3	13	1	15	6
48	3	14	1	15	6
49	2	15	1	15	6
50	2	16	1	15	6
51	2	17	1	15	6
52	2	18	1	15	6
53	2	19	1	15	6
54	2	1A	1	15	6
55	2	1B	1	15	6
56	2	1C	1	15	6
57	2	1D	1	15	6
58	2	1E	1	15	6
59	2	1F	1	15	6
60	3	08	2	1F	6
61	3	09	2	1F	6
62	3	0A	2	1F	6
63	3	0B	2	1F	6
64	3	0C	2	1F	6
65	3	0D	2	1F	6
66	3	0E	2	1F	6
67	3	0F	2	1F	6
68	3	10	2	1F	6
69	3	11	2	1F	6
70	3	12	2	1F	6
71	3	13	2	1F	6
72	3	14	2	1F	6
73	2	15	2	1F	6
74	2	16	2	1F	6
75	2	17	2	1F	6
76	2	18	2	1F	6
77	2	19	2	1F	6
78	2	1A	2	1F	6
79	2	1B	2	1F	6
80	2	1C	2	1F	6
81	2	1D	2	1F	6
82	2	1E	2	1F	6
83	2	1F	2	1F	6

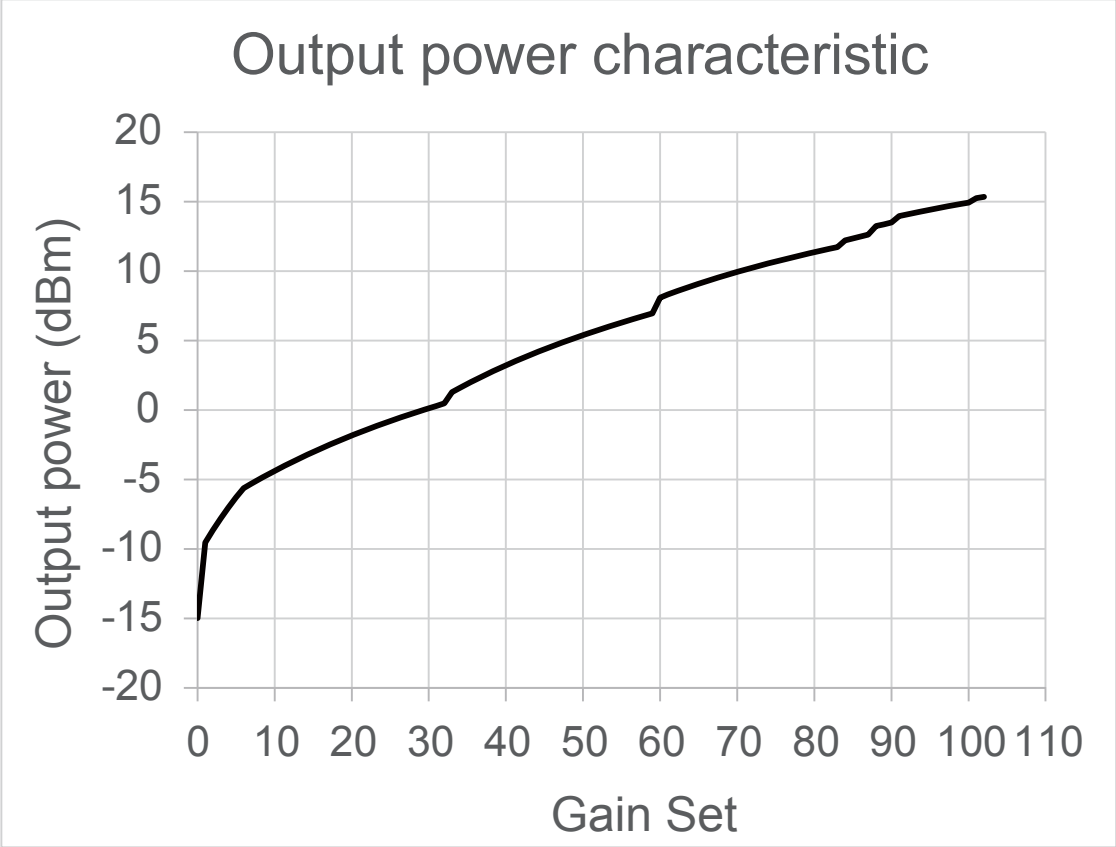
Downloaded from Arrow.com.

Table 6 - 13 Gain Set (Frequency band identifier = 8) (3/3)

Gain set	0090H address Bit [1:0]	0092H address Bit [4:0]	00DCH address Bit [4:0] (00DDH address is set to 19)	00DCH address Bit [4:0] (00DDH address is set to 25)	00DCH address Bit [7:4] (00DDH address is set to 1AH)
84	3	11	4	16	6
85	3	12	4	16	6
86	3	13	4	16	6
87	3	14	4	16	6
88	3	12	6	16	6
89	3	13	6	16	6
90	3	14	6	16	6
91	1	15	7	14	6
92	1	16	7	14	6
93	1	17	7	14	6
94	1	18	7	14	6
95	1	19	7	14	6
96	1	1A	7	14	6
97	1	1B	7	14	6
98	1	1C	7	14	6
99	1	1D	7	14	6
100	1	1E	7	14	6
101	1	1E	8	11	6
102	1	1F	8	11	6

Downloaded from Arrow.com.

Figure 6 - 4 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 8)



6.2 RF frequency setting for transmission

Following descriptions are detail of (2) frequency setting in 5.3.1 Example of Procedure for Transmission.

Set BBFREQ register in 3.4.54 Frequency setting register (BBFREQ).
If the frequency setting is integer times N (864 MHz, 912 MHz) of XIN frequency (48 MHz), the transmission character will degrade. If the frequency matches the following condition, it must be changed to other frequency. N is integer, h is modulation index in 2-level FSK and three times of modulation index in 4-level FSK. R is symbol rate.

48e6 *N - (M2+1.5*R) ≤ Use prohibited transmission frequency [Hz] ≤ 48e6 *N + (M2+1.5*R)
Here, M2 = 3*R*(1+h)

Caution Refer to the latest application note for this setting when to use the product.

Downloaded from Arrow.com.

6.3 RF frequency setting for reception

Following descriptions are detail of (2) frequency setting in 5.3.2 Example of Procedure for Reception.

(1) Set 3.4.54 Frequency setting register (BBFREQ) according to the RF frequency of reception.
(2) Set the data [7:0] of 0095H address following to the **Table 6 - 14** to **Table 6 - 35** according to the RF frequency of reception.
(3) Set data of 0095H address in IDLE mode.
(4) Frequencies 864 MHz ± 400 kHz and 912 MHz ± 400 kHz are use prohibited.
(5) Set the data [7:0] of 0095H address to 08H for the RF frequency of transmission.
Set also data of 0095H address in IDLE mode for the RF frequency of transmission.

Caution Refer to the latest application note for setting values of Table 6 - 5 to Table 6 - 26 when to use the product.

Table 6 - 14 RF Frequency Set (Frequency band identifier = 4, Mode = 001)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	863.0000	863.5875	8H
2	863.6000	864.4000	Prohibited
3	864.4125	865.8500	8H
4	865.8625	866.1375	28H
5	866.1500	867.8500	8H
6	867.8625	868.1375	28H
7	868.1500	869.8500	8H
8	869.8625	870.0000	28H

Table 6 - 15 RF Frequency Set (Frequency band identifier = 4, Mode = 002)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	863.0000	863.5875	8H
2	863.6000	864.4000	Prohibited
3	864.4125	865.7125	8H
4	865.7250	865.9750	48H
5	865.9875	866.2750	28H
6	866.2875	867.7125	8H
7	867.7250	867.9750	48H
8	867.9875	868.2750	28H
9	868.2875	869.7125	8H
10	869.7250	870.0000	28H

Downloaded from Arrow.com.

Table 6 - 16 RF Frequency Set (Frequency band identifier = 4, Mode = 003)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	863.0000	863.5875	8H
2	863.6000	864.4000	Prohibited
3	864.4125	865.7500	8H
4	865.7625	865.9375	48H
5	865.9500	866.2375	28H
6	866.2500	867.7500	8H
7	867.7625	867.9375	48H
8	867.9500	868.2375	28H
9	868.2500	869.7500	8H
10	869.7625	870.0000	28H

Table 6 - 17 RF Frequency Set (Frequency band identifier = 5, Mode = 004)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	896.0000	896.0125	28H
2	896.0250	896.1750	8H
3	896.1875	896.2125	28H
4	896.2250	897.9750	8H
5	897.9875	898.0125	28H
6	898.0250	899.7750	8H
7	899.7875	899.8125	28H
8	899.8250	899.9750	8H
9	899.9875	900.0125	28H
10	900.0250	900.1750	8H
11	900.1875	900.2125	28H
12	900.2250	901.0000	8H

Table 6 - 18 RF Frequency Set (Frequency band identifier = 5, Mode = 005)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	896.0000	896.0375	28H
2	896.0500	896.3500	8H
3	896.3625	896.4375	28H
4	896.4500	897.9500	8H
5	897.9625	898.0375	28H
6	898.0500	899.5500	8H
7	899.5625	899.6375	28H
8	899.6500	899.9500	8H
9	899.9625	900.0375	28H
10	900.0500	900.3500	8H
11	900.3625	900.4375	28H
12	900.4500	901.0000	8H

Downloaded from Arrow.com.

Table 6 - 19 RF Frequency Set (Frequency band identifier = 5, Mode = 006)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	896.0000	896.0625	28H
2	896.0750	896.7250	8H
3	896.7375	896.8625	28H
4	896.8750	897.9250	8H
5	897.9375	897.9500	28H
6	897.9625	898.0625	48H
7	898.0750	899.1250	8H
8	899.1375	899.2625	28H
9	899.2750	899.9250	8H
10	899.9375	900.0375	28H
11	900.0500	900.0625	48H
12	900.0750	900.7250	8H
13	900.7375	900.8375	28H
14	900.8500	901.0000	8H

Table 6 - 20 RF Frequency Set (Frequency band identifier = 6, Mode = 007)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	901.0000	901.9750	8H
2	901.9875	902.0000	28H

Table 6 - 21 RF Frequency Set (Frequency band identifier = 6, Mode = 008)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	901.0000	901.9500	8H
2	901.9625	902.0000	28H

Table 6 - 22 RF Frequency Set (Frequency band identifier = 6, Mode = 009)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	901.0000	901.9250	8H
2	901.9375	902.0000	28H

Downloaded from Arrow.com.

Table 6 - 23 RF Frequency Set (Frequency band identifier = 7, Mode = 010)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	902.0000	902.1375	28H
2	902.1500	903.8500	8H
3	903.8625	904.1375	28H
4	904.1500	905.8500	8H
5	905.8625	906.1375	28H
6	906.1500	907.8500	8H
7	907.8625	908.1375	28H
8	908.1500	909.8500	8H
9	909.8625	910.1375	28H
10	910.1500	911.5875	8H
11	911.6000	912.4000	Prohibited
12	912.4125	913.8500	8H
13	913.8625	914.1375	28H
14	914.1500	915.8500	8H
15	915.8625	916.1375	28H
16	916.1500	917.8500	8H
17	917.8625	918.1375	28H
18	918.1500	919.8500	8H
19	919.8625	920.1375	28H
20	920.1500	921.8500	8H
21	921.8625	922.1375	28H
22	922.1500	923.8500	8H
23	923.8625	924.1375	28H
24	924.1500	925.8500	8H
25	925.8625	926.1375	28H
26	926.1500	927.8500	8H
27	927.8625	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 24 RF Frequency Set (Frequency band identifier = 7, Mode = 011)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	902.0000	902.2625	28H
2	902.2750	903.7250	8H
3	903.7375	904.2625	28H
4	904.2750	905.7250	8H
5	905.7375	906.2625	28H
6	906.2750	907.7250	8H
7	907.7375	908.0375	28H
8	908.0500	908.2625	48H
9	908.2750	909.7250	8H
10	909.7375	910.0375	28H
11	910.0500	910.2625	48H
12	910.2750	911.5875	8H
13	911.6000	912.4000	Prohibited
14	912.4125	913.7250	8H
15	913.7375	913.9500	48H
16	913.9625	914.2625	28H
17	914.2750	915.7250	8H
18	915.7375	915.9500	48H
19	915.9625	916.2625	28H
20	916.2750	917.7250	8H
21	917.7375	918.2625	28H
22	918.2750	919.7250	8H
23	919.7375	920.2625	28H
24	920.2750	921.7250	8H
25	921.7375	922.2625	28H
26	922.2750	923.7250	8H
27	923.7375	924.2625	28H
28	924.2750	925.7250	8H
29	925.7375	926.2625	28H
30	926.2750	927.7250	8H
31	927.7375	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 25 RF Frequency Set (Frequency band identifier = 7, Mode = 012)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	902.0000	902.3500	28H
2	902.3625	903.6375	8H
3	903.6500	904.2625	28H
4	904.2750	904.3500	48H
5	904.3625	905.6375	8H
6	905.6500	906.2625	28H
7	906.2750	906.3500	48H
8	906.3625	907.6375	8H
9	907.6500	907.9500	28H
10	907.9625	908.2125	48H
11	908.2250	908.3500	68H
12	908.3625	909.6375	8H
13	909.6500	909.9500	28H
14	909.9625	910.2125	48H
15	910.2250	911.5875	8H
16	911.6000	912.4000	Prohibited
17	912.4125	913.7750	8H
18	913.7875	914.0375	48H
19	914.0500	914.3500	28H
20	914.3625	915.6375	8H
21	915.6500	915.7750	68H
22	915.7875	916.0375	48H
23	916.0500	916.3500	28H
24	916.3625	917.6375	8H
25	917.6500	917.7250	48H
26	917.7375	918.3500	28H
27	918.3625	919.6375	8H
28	919.6500	919.7250	48H
29	919.7375	920.3500	28H
30	920.3625	921.6375	8H
31	921.6500	922.3500	28H
32	922.3625	923.6375	8H
33	923.6500	924.3500	28H
34	924.3625	925.6375	8H
35	925.6500	926.3500	28H
36	926.3625	927.6375	8H
37	927.6500	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 26 RF Frequency Set Frequency band identifier = 8, Mode = 013)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	917.0000	917.8500	8H
2	917.8625	918.1375	28H
3	918.1500	919.8500	8H
4	919.8625	920.1375	28H
5	920.1500	921.8500	8H
6	921.8625	922.1375	28H
7	922.1500	923.5000	8H

Table 6 - 27 RF Frequency Set (Frequency band identifier = 8, Mode = 014)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	917.0000	917.7250	8H
2	917.7375	918.2625	28H
3	918.2750	919.7250	8H
4	919.7375	920.2625	28H
5	920.2750	921.7250	8H
6	921.7375	922.2625	28H
7	922.2750	923.5000	8H

Table 6 - 28 RF Frequency Set (Frequency band identifier = 8, Mode = 015)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	917.0000	917.6375	8H
2	917.6500	917.7250	48H
3	917.7375	918.3500	28H
4	918.3625	919.6375	8H
5	919.6500	919.7250	48H
6	919.7375	920.3500	28H
7	920.3625	921.6375	8H
8	921.6500	922.3500	28H
9	922.3625	923.5000	8H

Table 6 - 29 RF Frequency Set (Frequency band identifier = 8, Mode = 016)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	920.0000	920.1375	28H
2	920.1500	921.8500	8H
3	921.8625	922.1375	28H
4	922.1500	923.8500	8H
5	923.8625	924.1375	28H
6	924.1500	925.8500	8H
7	925.8625	926.1375	28H
8	926.1500	927.8500	8H
9	927.8625	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 30 RF Frequency Set (Frequency band identifier = 9, Mode = 000)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	920.0000	920.2750	28H
2	920.2875	921.7125	8H
3	921.7250	922.2750	28H
4	922.2875	923.7125	8H
5	923.7250	924.2750	28H
6	924.2875	925.7125	8H
7	925.7250	926.2750	28H
8	926.2875	927.7125	8H
9	927.7250	928.0000	28H

Table 6 - 31 RF Frequency Set (Frequency band identifier = 9, Mode = 017)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	920.0000	920.5375	28H
2	920.5500	921.4500	8H
3	921.4625	921.6125	48H
4	921.6250	922.5250	28H
5	922.5375	923.4500	8H
6	923.4625	923.6125	48H
7	923.6250	924.5250	28H
8	924.5375	924.5375	48H
9	924.5500	925.4500	8H
10	925.4625	926.2125	28H
11	926.2250	926.2500	68H
12	926.2625	926.5375	48H
13	926.5500	927.4500	8H
14	927.4625	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 32 RF Frequency Set (Frequency band identifier = 9, Mode = 018)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	920.0000	920.4750	28H
2	920.4875	921.5125	8H
3	921.5250	921.5500	48H
4	921.5625	922.4750	28H
5	922.4875	923.5125	8H
6	923.5250	923.5500	48H
7	923.5625	924.4750	28H
8	924.4875	925.5125	8H
9	925.5250	926.2750	28H
10	926.2875	926.4750	48H
11	926.4875	927.5125	8H
12	927.5250	928.0000	28H

Table 6 - 33 RF Frequency Set (Frequency band identifier = Other, Mode = 019)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	920.0000	920.5125	28H
2	920.5250	921.4750	8H
3	921.4875	921.5875	48H
4	921.6000	922.5125	28H
5	922.5250	923.4750	8H
6	923.4875	923.5875	48H
7	923.6000	924.5125	28H
8	924.5250	925.4750	8H
9	925.4875	926.2375	28H
10	926.2500	926.5125	48H
11	926.5250	927.4750	8H
12	927.4875	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 34 RF Frequency Set (Frequency band identifier = Other, Mode = 020)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	902.0000	902.1750	28H
2	902.1875	903.8125	8H
3	903.8250	904.1750	28H
4	904.1875	905.8125	8H
5	905.8250	906.1750	28H
6	906.1875	907.8125	8H
7	907.8250	908.1250	28H
8	908.1375	908.1750	48H
9	908.1875	909.8125	8H
10	909.8250	910.1250	28H
11	910.1375	910.1750	48H
12	910.1875	911.5875	8H
13	911.6000	912.4000	Prohibited
14	912.4125	913.8125	8H
15	913.8250	913.8625	48H
16	913.8750	914.1750	28H
17	914.1875	915.8125	8H
18	915.8250	915.8625	48H
19	915.8750	916.1750	28H
20	916.1875	917.8125	8H
21	917.8250	918.1750	28H
22	918.1875	919.8125	8H
23	919.8250	920.1750	28H
24	920.1875	921.8125	8H
25	921.8250	922.1750	28H
26	922.1875	923.8125	8H
27	923.8250	924.1750	28H
28	924.1875	925.8125	8H
29	925.8250	926.1750	28H
30	926.1875	927.8125	8H
31	927.8250	928.0000	28H

Downloaded from Arrow.com.

Table 6 - 35 RF Frequency Set (Frequency band identifier = Other, Mode = 021)

RF frequency set	Lower limit RF frequency [MHz]	Upper limit RF frequency [MHz]	0095H address Bit [7:0]
1	902.0000	902.3875	28H
2	902.4000	902.5250	48H
3	902.5375	903.4625	8H
4	903.4750	904.0875	28H
5	904.1000	904.5250	48H
6	904.5375	905.4625	8H
7	905.4750	906.0875	28H
8	906.1000	906.5250	48H
9	906.5375	907.4625	8H
10	907.4750	907.7750	28H
11	907.7875	908.0375	48H
12	908.0500	908.1500	8H
13	908.1625	908.5250	68H
14	908.5375	909.4625	8H
15	909.4750	909.7750	28H
16	909.7875	910.0375	48H
17	910.0500	911.5875	8H
18	911.6000	912.4000	Prohibited
19	912.4125	913.9500	8H
20	913.9625	914.2125	48H
21	914.2250	914.5250	28H
22	914.5375	915.4625	8H
23	915.4750	915.8375	68H
24	915.8500	915.9500	8H
25	915.9625	916.2125	48H
26	916.2250	916.5250	28H
27	916.5375	917.4625	8H
28	917.4750	917.9000	48H
29	917.9125	918.5250	28H
30	918.5375	919.4625	8H
31	919.4750	919.9000	48H
32	919.9125	920.5250	28H
33	920.5375	921.4625	8H
34	921.4750	921.6000	48H
35	921.6125	922.5250	28H
36	922.5375	923.4625	8H
37	923.4750	923.6000	48H
38	923.6125	924.5250	28H
39	924.5375	925.4625	8H
40	925.4750	926.2375	28H
41	926.2500	926.5250	48H
42	926.5375	927.4625	8H
43	927.4750	928.0000	28H

Downloaded from Arrow.com.

CHAPTER 7 NOTICE FOR USING BASEBAND FUNCTION

7.1 Notice About Transmission

Do not stop transmit operation.

Reset (initialize) by RFRESETB pin after setting RFSTOP bit to 1 for stopping transmission.

Initialize in same way for stopping in continuous transmission mode and special transmission mode.

7.2 Cautions on First and Second Address Filter Match Monitor Bits

(1) When the address filter extension bit is disabled, values of first and second address filter match monitor bits are invalid.

(2) When the address filter extension bit is enabled, values of first and second address filter match monitor bits are invalid under the following conditions.

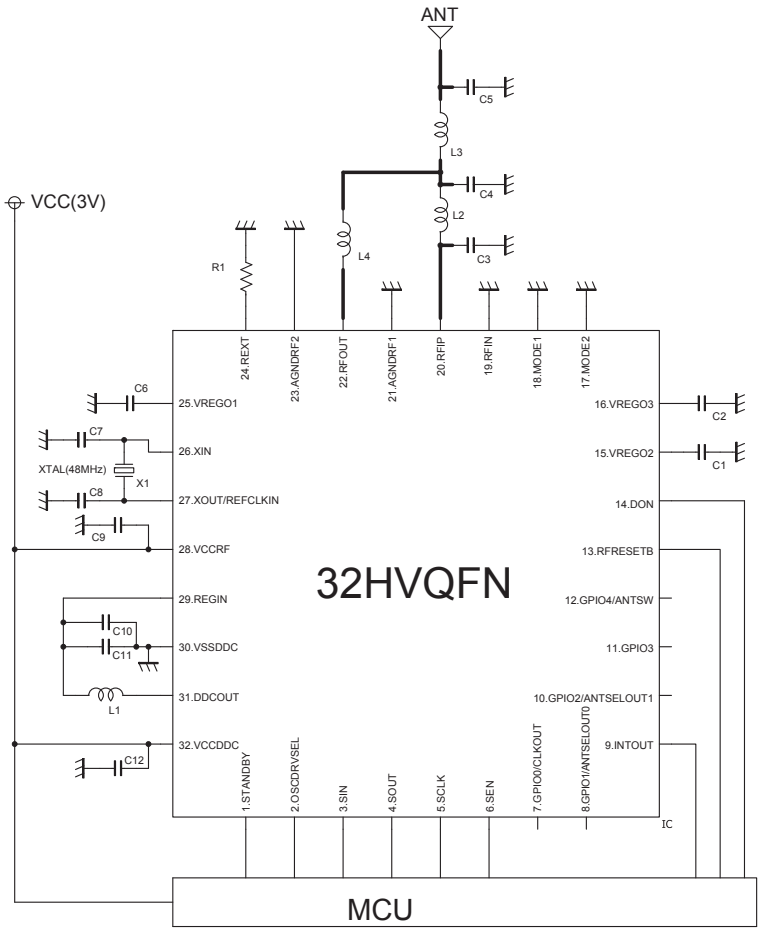
- Frame version: 00, 01
- Frame type: Beacon frame
- No destination PANID and destination address
- Values of source PANID and PAN identifier register match, or value of PAN identifier register = FFFFH
- PANCORD bit = 0

Downloaded from Arrow.com.

CHAPTER 8 PERIPHERAL CIRCUIT CONNECTION DIAGRAM

8.1 RAA604S00 (32-pin)

Figure 8 - 1 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (Without ANTSW)



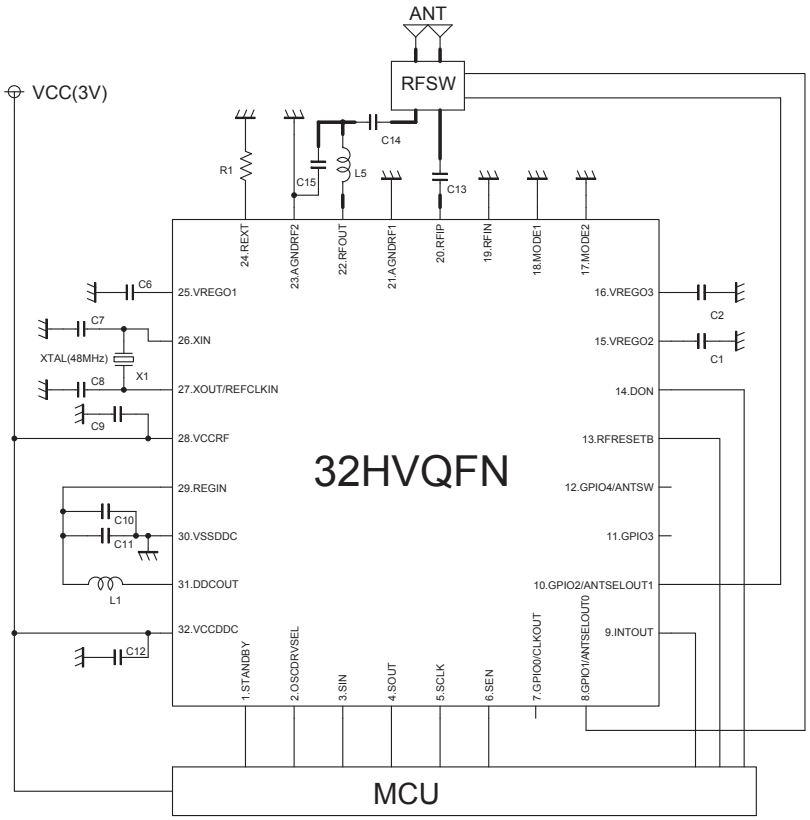
Downloaded from Arrow.com.

Part number	Remarks
C3	Acceptable error: use ±0.25 pF accuracy part
C4	Acceptable error: use ±0.25 pF accuracy part
C5	Acceptable error: use ±0.25 pF accuracy part
R1 (56 kΩ)	Use 1 % accuracy part
L1(10 μH)	MLZ1608M100WT(10.0 μH ±20 %) is comfortable. Required inductor with good DC superposition characteristics. Small loss (DC resistance and AC resistance at operational frequency) is comfortable.
L2, L3, L4	Use chip inductance for high frequency. Required high Q at 1 GHz band, and self-resonance is higher than 1 GHz.

Caution The multiple power supply smoothing capacitors may be connected to a pin depending on the routing of the board wiring, noise, and others.

Downloaded from Arrow.com.

Figure 8 - 2 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (With ANTSW)

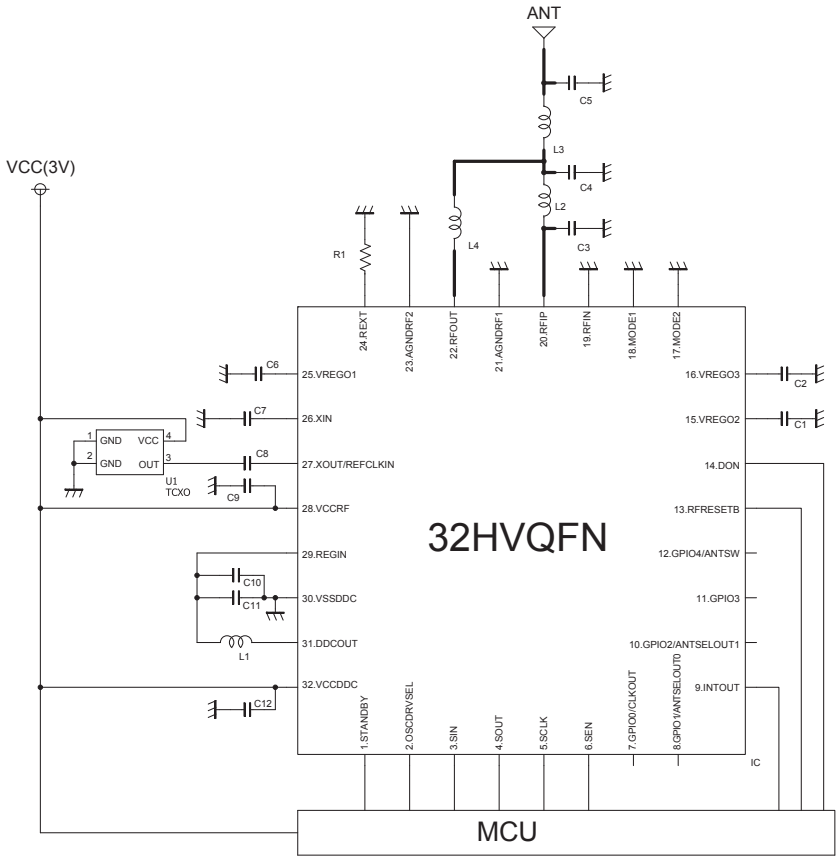


Part number	Remarks
C15	Acceptable error: use ±0.25 pF accuracy part
R1 (56 kΩ)	Use 1 % accuracy part
L1(10 μH)	MLZ1608M100WT(10.0 μH ±20 %) is comfortable. Required inductor with good DC superposition characteristics. Small loss (DC resistance and AC resistance at operational frequency) is comfortable.
L5	Use chip inductance for high frequency. Required high Q at 1 GHz band, and self-resonance is higher than 1 GHz.

Caution The multiple power supply smoothing capacitors may be connected to a pin depending on the routing of the board wiring, noise, and others.

Downloaded from Arrow.com.

<R> **Figure 8 - 3 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (Using TCXO)**



Part number	Remarks
C7	100 pF
C8	100 pF

Caution The multiple power supply smoothing capacitors may be connected to a pin depending on the routing of the board wiring, noise, and others.

Downloaded from Arrow.com.

<R>

CHAPTER 9 ELECTRIC CHARACTERISTICS

9.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
power supply voltage	V_{DDRF}	VCCRF, VCCDDC	–0.3 to +3.8	V
	V_{SSRF}	AGNDRF1, AGNDRF2, VSSDDC, RFIN, DIEGND	–0.3 to +0.3	V
Input voltage	V_{IRF1}	STANDBY, OSCDRVSEL, SIN, SCLK, SEN, GPIO0 to GPIO4, RFRESETB, DON, MODE1, MODE2	–0.3 to +3.8 and –0.3 to V_{DDRF}+0.3	V
	V_{IRF2}	XIN	–0.3 to +1.25	V
	V_{IRF3}	RFIP	–2.0 to +2.0**Note**	V
Output voltage	V_{ORF1}	SOUT, GPIO0 to GPIO4, INTOUT	–0.3 to +3.8 and –0.3 to V_{DDRF}+0.3	V
	V_{ORF2}	XOUT	–0.3 to +1.25	V
	V_{ORF3}	RFOUT	–2.0 to +2.0**Note**	V
RF power supply input voltage	V_{REGIN}	REGIN	–0.3 to +3.8	V
RF power supply output voltage	V_{RFOUT1}	DDCOUT	–0.3 to +3.8	V
	V_{RFOUT2}	VREGO1 to VREGO3	–0.3 to +1.25	V
	V_{RFOUT3}	REXT (reference resistor connection pin)	–0.3 to +1.25	V
High level output current	I_{OHRF}	GPIO0 to GPIO4 (per pin)	–17	mA
Low level output current	I_{OLRF}	GPIO0 to GPIO4 (per pin)	17	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note This value is AC rating. Impression of DC voltage is prohibited to RFIP or RFOUT pins.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Reference voltage is V_{SSRF}.

Downloaded from Arrow.com.

9.2 Recommended Operating Conditions

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power source voltage		1.8	3.0	3.6	V
Operating ambient temperature		-40		85	°C
XIN frequency			48		MHz
Operating frequency		863		928	MHz
Channel interval		12.5/200/400/600			kHz
Data rate	2FSK/GFSK	10/20/40/50/100/150/200/300			kbps
	4FSK/GFSK	200/400			kbps
Modulation index	2FSK/GFSK	0.5/1.0			—
	4FSK/GFSK		0.33		—

9.3 XIN Frequency Deviation

9.3.1 Compatible with IEEE802.15.4g

XIN frequency accuracy is required according to the table below to satisfy the IEEE802.15.4g standard.

Frequency band [MHz]	Maximum frequency [MHz]	Symbol rate [ksymbol/s]	Variable index	MIN.	TYP.	MAX.	Unit	IEEE standard
863	870	50	1	-31.6	—	31.6	ppm	31.6
	870	100	1	-50.0	—	50.0	ppm	50.0
	870	100	0.33	-20.9	—	20.9	ppm	20.9
896	901	10	0.5	-3.1	—	3.1	ppm	3.1
	901	20	0.5	-6.1	—	6.1	ppm	6.1
	901	40	0.5	-12.2	—	12.2	ppm	12.2
901	902	10	0.5	-3.1	—	3.1	ppm	3.1
	902	20	0.5	-6.1	—	6.1	ppm	6.1
	902	40	0.5	-12.2	—	12.2	ppm	12.2
915	928	50	1	-29.6	—	29.6	ppm	29.6
	928	150	0.5	-44.4	—	44.4	ppm	44.4
	928	200	0.5	-50.0	—	50.0	ppm	50.0
917	923.5	50	1	-29.8	—	29.8	ppm	29.8
	923.5	150	0.5	-44.6	—	44.6	ppm	44.6
	923.5	200	0.5	-50.0	—	50.0	ppm	50.0
920	928	50	1	-29.6	—	29.6	ppm	29.6
	928	100	1	-50.0	—	50.0	ppm	50.0
	928	200	1	-50.0	—	50.0	ppm	50.0
	928	200	0.33	-39.1	—	39.1	ppm	39.1

Downloaded from Arrow.com.

9.3.2 Compatible with ARB Standard

XIN frequency accuracy is required according to the table below to satisfy the ARIB standard.

Frequency band [MHz]	Maximum frequency [MHz]	Symbol rate [ksymbol/s]	Variable index	MIN.	TYP.	MAX.	Unit
920	928	50	1	–20	—	+20	ppm
	928	100	1	–20	—	+20	ppm
	928	200	1	–20	—	+20	ppm
	928	200	0.33	–20	—	+20	ppm

Downloaded from Arrow.com.

9.4 DC Characteristics

T_A = 25 °C, V_{DDRF} = 3.0 V, V_{SSRF} = 0 V

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OHRF}	SOUT, GPIO0 to GPIO4, INTOUT (per pin)	1.8V ≤ V_{DDRF} ≤ 3.6 V		–2.0		mA
Low-level output current	I_{OLRF}	SOUT, GPIO0 to GPIO4, INTOUT (per pin)	1.8V ≤ V_{DDRF} ≤ 3.6 V		2.0		mA
High-level input voltage	V_{IHRF}	STANDBY, OSCDRVSEL, SIN, SCLK, SEN, GPIO0 to GPIO4, RFRESETB, DON, MODE1, MODE2		0.85 V_{DDRF}		V_{DDRF}	V
Low-level input voltage	VILRF	STANDBY, OSCDRVSEL, SIN, SCLK, SEN, GPIO0 to GPIO4, RFRESETB, DON, MODE1, MODE2		0		0.1 V_{DDRF}	V
High-level output voltage	V_{OHRF}	I_{OH} = –2.0 mA	GPIO0 to GPIO4, INTOUT, SOUT	V_{DDRF} –0.3			V
Low-level output voltage	V_{OLRF}	I_{OL} = 2.0 mA	GPIO0 to GPIO4, INTOUT, SOUT			0.3	V
High-level input leakage current	I_{LIHRF}	V_I = V_{DDRF}	STANDBY, OSCDRVSEL, SIN, SCLK, SEN, GPIO0 to GPIO4, RFRESETB, DON, MODE1, MODE2			10	µA
Low-level input leakage current	I_{LILRF}	V_I = V_{SSRF}	STANDBY, OSCDRVSEL, SIN, SCLK, SEN, GPIO0 to GPIO4, RFRESETB, DON, MODE1, MODE2			–10	µA

Downloaded from Arrow.com.

9.5 AC Characteristics.

T_A = -40°C to 85 °C, 3.0 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKL cycle time	tsccyc		100			ns
SCLK high-level width	tsch		48			ns
SCLK low-level width	tscl		48			ns
SIN setup time	tsisu		20			ns
SIN hold time	tsihd		60			ns
SOUT output delay time	tsodly				25	ns
SEN setup time	tsesu		200			ns
SEN hold time	tsehd		200			ns
Serial communication interval time **Note**	tscombtw		100			ns

Note Serial communication interval time is required at 100 ns ≤ tsccyc < 250 ns.

T_A = -40°C to 85 °C, 2.4 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKL cycle time	tsccyc		250			ns
SCLK high-level width	tsch		110			ns
SCLK low-level width	tscl		110			ns
SIN setup time	tsisu		90			ns
SIN hold time	tsihd		90			ns
SOUT output delay time	tsodly				40	ns
SEN setup time	tsesu		200			ns
SEN hold time	tsehd		200			ns

T_A = -40°C to 85 °C, 1.8 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKL cycle time	tsccyc		500			ns
SCLK high-level width	tsch		230			ns
SCLK low-level width	tscl		230			ns
SIN setup time	tsisu		140			ns
SIN hold time	tsihd		140			ns
SOUT output delay time	tsodly				90	ns
SEN setup time	tsesu		400			ns
SEN hold time	tsehd		400			ns

Downloaded from Arrow.com.

Figure 9 - 1 Data I/O timing

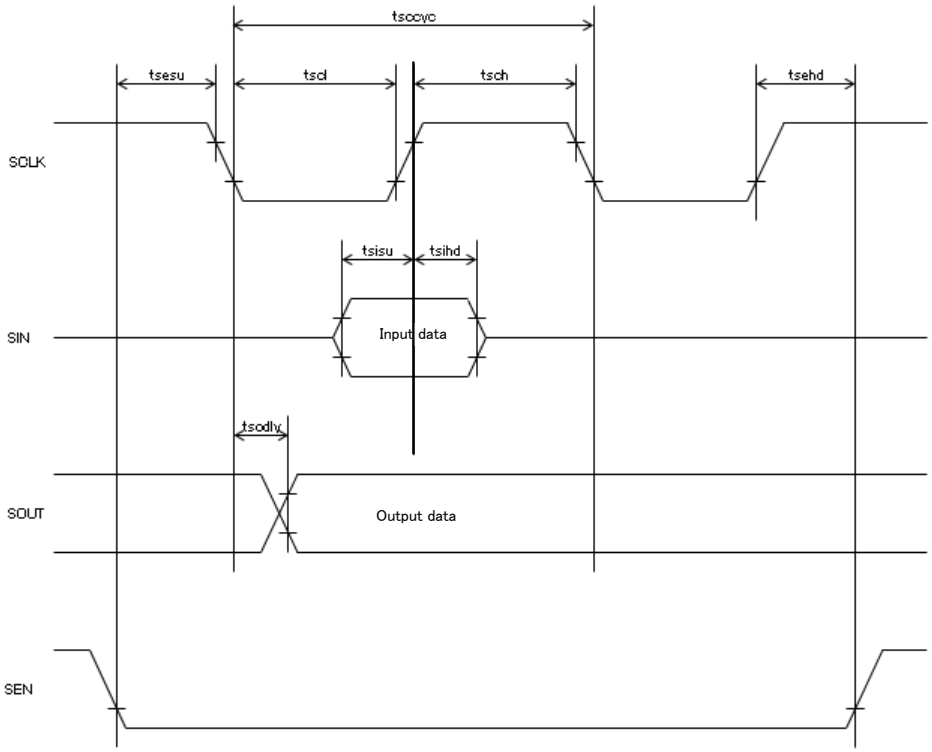
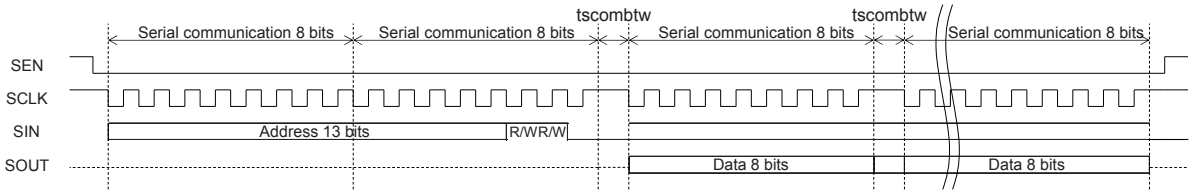


Figure 9 - 2 Data I/O including serial communication interval time



T_A = -40°C to 85 °C, 1.8 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
STANDBY low-level width	tstbyl			10		µs
OSCDRVSEL setup time (to STANDBY↑)	todssu		Crystal resonator	500		µs
DON setup time (to SOCDRVSEL↑)	tdonsu		Crystal resonator	50		µs
RFRESETB setup time (to DON↑)	trfrstsu		Crystal resonator	450		µs
RFRESETB setup time (to STANDBY↑)	trfrstsu2		External clock input	450		µs

Downloaded from Arrow.com.

Figure 9 - 3 Timing Using crystal resonator

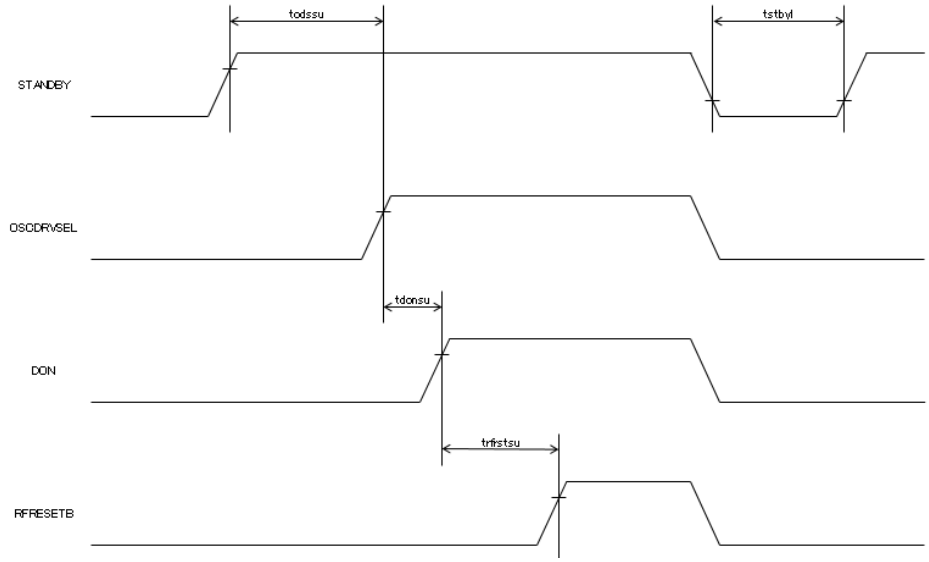
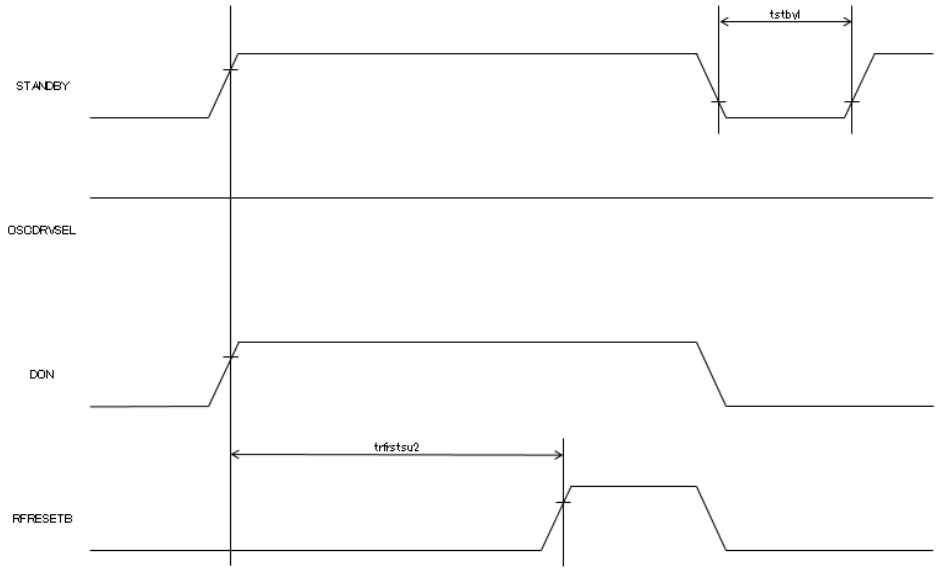


Figure 9 - 4 Timing Using crystal resonator



9.6 Calibration Timing Characteristic

T_A = -40 °C to 85 °C, 1.8 V ≤ V_{DDRF} ≤ 3.6 V, V_{SSRF} = 0 V

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Calibration time				100	µs

Downloaded from Arrow.com.

9.7 Power Supply Current

T_A = 25 °C, V_{DDRF} = 3.0 V, V_{SSRF} = 0 V

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Transmission current (100 kbps, 2GFSK)	+14.5 dBm		53		mA
	+13 dBm		36		mA
	+10 dBm		21		mA
Reception current (100 kbps, 2GFSK)	During receive operation RFIP -95 dBm, CW		6.9		mA
	Waiting signal reception RFIP none		6.3		mA
SLEEP mode			0.1		µA
IDLE mode			1.3		mA

Downloaded from Arrow.com.

9.8 Transceiver Reception Characteristics

T_A = 25 °C , V_{DDRF} = 3.0 V, V_{SSRF} = 0 V

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Reception sensitivity		2GFSK, BT=0.5, BER<0.1%, 10 kbps, m = 0.5	—	–114	–109	dBm
		2GFSK, BT=0.5, BER<0.1%, 20 kbps, m = 0.5	—	–111	–106	dBm
		2GFSK, BT=0.5, BER<0.1%, 40 kbps, m = 0.5	—	–108	–103	dBm
		2GFSK, BT=0.5, BER<0.1%, 50 kbps, m = 1	—	–107	–102	dBm
		2GFSK, BT=0.5, BER<0.1%, 100 kbps, m = 0.5	—	–104	–99	dBm
		2GFSK, BT=0.5, BER<0.1%, 100 kbps, m = 1	—	–105	–100	dBm
		2GFSK, BT=0.5, BER<0.1%, 150 kbps, m = 0.5	—	–102	–97	dBm
		2GFSK, BT=0.5, BER<0.1%, 200 kbps, m = 0.5	—	–101	–96	dBm
		2GFSK, BT=0.5, BER<0.1%, 200 kbps, m = 1	—	–102	–97	dBm
		2GFSK, BT=0.5, BER<0.1%, 300 kbps, m = 0.5	—	–97	–92	dBm
		4GFSK, BT=0.5, BER<0.1%, 200 kbps, m = 0.33	—	–102	–97	dBm
		4GFSK, BT=0.5, BER<0.1%, 400 kbps, m = 0.33	—	–100	–95	dBm
Maximum input level		2GFSK	0	12	—	dBm
Spurious radiation		1 GHz or lower	—	—	–57	dBm
		1 GHz or higher			–47	dBm
ED	Input range	2GFSK, BT = 0.5, 100 kbps, m = 1	–105	—	–5	dBm
	Total accuracy		–5	—	5	dB
RSSI	Input range	2GFSK, BT = 0.5, 100 kbps, m = 1	–100	—	–5	dBm
	Total accuracy		–5	—	5	dB
	Relative accuracy		–2	—	2	dB
Adjacent channel suppression ratio	±200 kHz (50 kbps, m = 1)	2GFSK, BT=0.5, Desired signal 3 dB above the input sensitivity level, CW interferer, BER<0.1%	—	35	—	dB
	±400 kHz (100 kbps, m = 1)		—	40	—	dB
Next-adjacent channel suppression ratio	±400 kHz (50 kbps, m = 1)	2GFSK, BT=0.5, Desired signal 3 dB above the input sensitivity level, CW interferer, BER<0.1%	—	45	—	dB
	±800 kHz (100 kbps, m = 1)		—	50	—	dB
Suppression ratio	±2 MHz	Desired signal 3 dB above the input sensitivity level, CW interferer, BER<0.1%	—	48	—	dB
	±10 MHz		—	60	—	dB
	±60 MHz		—	60	—	dB
Image suppression ratio		Desired signal 3dB above the input sensitivity level, CW interferer, -2*if frequency offset	—	25	—	dB

Downloaded from Arrow.com.

9.9 Transceiver Transmission Characteristics

T_A = 25 °C, V_{DDRF} = 3.0 V, V_{SSRF} = 0 V

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Maximum transmission output power		3.6 V ≥ V_{DDRF} > 2.4 V	14.5	15.3	—	dBm
		2.4 V ≥V_{DDRF} ≥ 1.8 V	—	13.0	—	dBm
Minimum transmission output power			—	–14.0	—	dBm
Variable step size		Within 6 dB from maximum output power (3.6 V ≥ V_{DDRF} > 2.4 V).	—	0.5	—	dB
Transmission output power variation (Power supply voltage variation, temperature variation)		3.6 V ≥ V_{DDRF} ≥ 1.8 V -40 to 85 °C	–1.5	—	+1.5	dB
High frequency	2nd order harmonics	At +13 dBm output	—	—	–33.0	dBm
		At +14.5 dBm output	—	—	–31.5	dBm
	3rd order harmonics	At +13 dBm output	—	—	–33.0	dBm
		At +14.5 dBm output	—	—	–31.5	dBm

Caution Variable step size and transmission output power variation may vary depending on the maximum transmission output voltage power.

Downloaded from Arrow.com.

9.10 IEEE802.15.4g Frequency/Data Rate Table

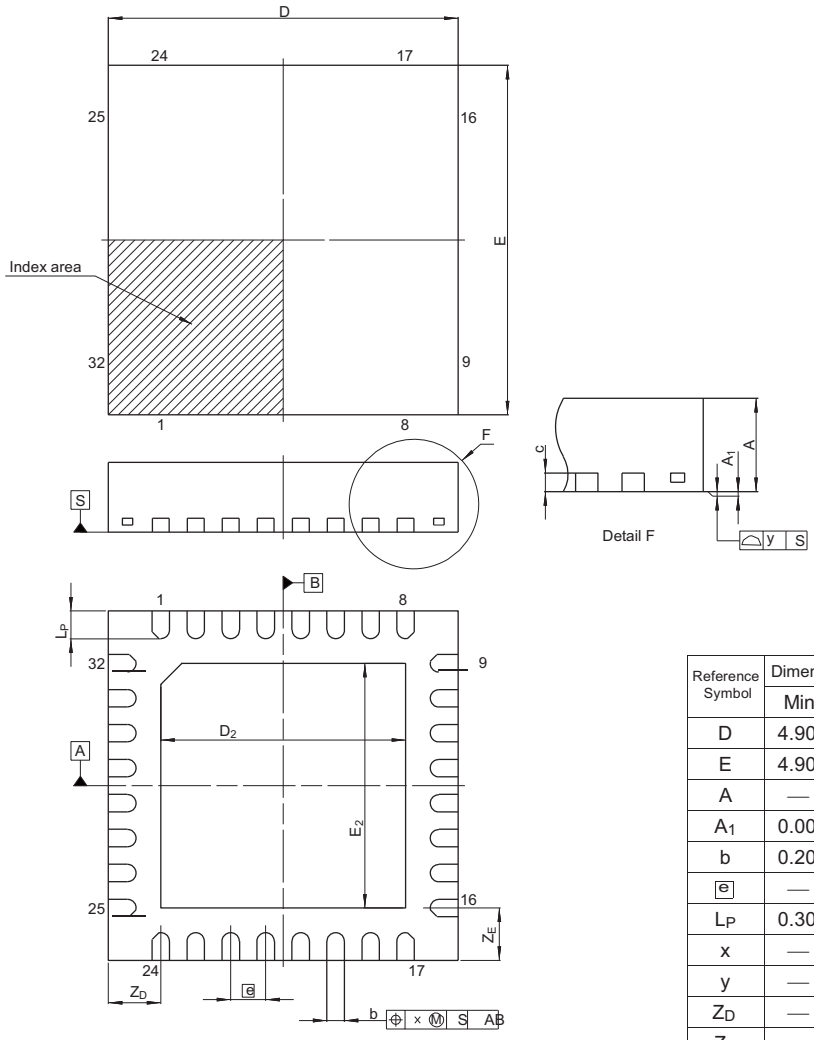
Frequency band identifier	PHY	Frequency band (MHz)	Operating mode	Modulation	Data rate (kbps)	Symbol rate (ksps)	Modulation index	Channel spacing (kHz)	Total number of channels	Channel 0 frequency (MHz)
4	863 MHz (Europe)	863 to 870	#1	2FSK/2GFSK	50	50	1	200	34	863.125
			#2		100	100		400	17	863.225
			#3	4FSK/4GFSK	200	100	0.33			
5	896 MHz (US)	896 to 901	#1	2FSK/2GFSK	10	10	0.5	25	399	896.0125
			#2		20	20		50	397	896.025
			#3		40	40		100	393	896.05
6	901 MHz (US)	901 to 902	#1	2FSK/2GFSK	10	10	0.5	25	79	901.0125
			#2		20	20		50	77	901.025
			#3		40	40		100	73	901.05
7	915 MHz (US)	902 to 928	#1	2FSK/2GFSK	50	50	1	200	129	902.2
			#2		150	150	0.5	400	64	902.4
			#3		200	200				
8	917 MHz (Korea)	917 to 923.5	#1	2FSK/2GFSK	50	50	1	200	32	917.1
			#2		150	150	0.5	400	16	917.3
			#3		200	200				
9	920 MHz (Japan)	920 to 928	#1	2FSK/2GFSK	50	50	1	200	38	920.6
			#2		100	100		400	18	920.9
			#3		200	200		600	12	920.8
			#4	4FSK/4GFSK	400	200	0.33			

Downloaded from Arrow.com.

CHAPTER 10 OUTLINE DRAWING

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HVQFN32-5x5-0.50	PVQN0032KF-A	—	0.05

Unit: mm



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	4.90	5.00	5.10
E	4.90	5.00	5.10
A	—	—	1.00
A_1	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
L_P	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c	—	0.20	—
D_2	—	3.50	—
E_2	—	3.50	—

© 2015 Renesas Electronics Corporation. All rights reserved.

Downloaded from Arrow.com.

APPENDIX A REVISION HISTORY

A.1 Major Revisions in This Edition

Page	Description	Classification
CHAPTER 2 PIN FUNCTIONS		
p.5	Addition of Connection of Unused Pins	(c)
CHAPTER 3 BASEBAND FUNCTION		
p.9	Change of item name in Table 3 - 1 For Normal Receive, Table 3 - 2 For Antenna Diversity Receive	(c)
p.12	Change of Table 3 - 3 Interrupt Sources List and Note 2, Addition of Note 4	(c)
p.49	Change of Figure 3 - 34 Baseband Interrupt Source Register 1 (BBINTREQ1) Format	(a)
p.50	Change of Figure 3 - 35 Baseband Interrupt Source Register 2 (BBINTREQ2) Format	(a)
p.52	Addition of description to 3.4.30 Baseband interrupt enable register 1 (BBINTEN1)	(c)
p.52	Change of Figure 3 - 37 Baseband Interrupt Enable Register 1 (BBINTEN1) Format	(a)
p.53	Deletion of description in 3.4.31 Baseband interrupt enable register 2 (BBINTEN2)	(a)
p.53	Change of Figure 3 - 38 Baseband Interrupt Enable Register 2 (BBINTEN2) Forma	(a)
p.57	Change of Figure 3 - 45 Receive Level Threshold Setting Register (BBLVLVTH) Format	(c)
p.72	Addition of Caution to Figure 3 - 66 Symbol Rate Setting Register (BBSYMBLRATE) Format	(c)
p.74	Addition of Caution 2 to Figure 3 - 68 Modulation Method Setting Register (BBMODSET) Format	(c)
p.92	Addition of description to 3.4.81 Clock output control register (CLKOUTCON)	(b)
p.101	Addition of description to 3.4.90 Lower limit threshold setting register after SFD detection (PWRLOWTH2)	(c)
CHAPTER 6 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING		
p.120	Change of description in CHAPTER 6 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING	(c)
CHAPTER 8 PERIPHERAL CIRCUIT CONNECTION DIAGRAM		
p.151	Change of Figure 8 - 3 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (Using TCXO)	(a)
CHAPTER 9 ELECTRIC CHARACTERISTICS		
Throughout	Change expression of conditions	(c)
p.152	Addition of Caution and Remark to9.1 Absolute Maximum Ratings	(c)
p.162	Change of 9.10 IEEE802.15.4g Frequency/Data Rate Table	(a)

Remark “Classification” in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note,
(d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

Downloaded from Arrow.com.

A.2 Revision History of Preceding Editions

(1/6)

Edition	Description	Chapter
Rev.1.10	Addition of Caution to Figure 3 - 69 CCA Time Register (CCATIME) Format	CHAPTER 3 BASEBAND FUNCTION
	Addition of description to 3.4.88 Address filter extension address control register (BBADFCON)	
	Addition of Caution to 6.1 Example of Procedure for Transmission Output Power Setting, 6.2 RF frequency setting for transmission and 6.3 RF frequency setting for reception	CHAPTER 6 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING
	Addition of 7.2 Cautions on First and Second Address Filter Match Monitor Bits	CHAPTER 7 NOTICE FOR USING BASEBAND FUNCTION
	Addition of table to 9.5 AC Characteristics	CHAPTER 9 ELECTRIC CHARACTERISTICS
	Addition of Figure 9 - 2 Data I/O including serial communication interval	
	Change of 9.8 Transceiver Reception Characteristics	
Rev.1.00	Deletion of expressions preliminary and Under development	Throughout
	Change of Figure 1.3.1 RAA604S00 (32-pin)	CHAPTER 1 OVERVIEW
	Change of description in 1.5 Pin Function Description	
	Change of Table 3 - 1 For Normal Receive	CHAPTER 3 BASEBAND FUNCTION
	Change of Table 3 - 2 For Antenna Diversity Receive	
	Addition of 3.3 Baseband Interrupt	
	Change of Table 3 - 4 Baseband Function Controlling Register	
	Change of description in 3.4.1 RF start register (BBRFCON)	
	Change of Figure Figure 3 - 5 RF Start Register (BBRFCON) Format	
	Change of description in 3.4.2 Transmit/receive reset register (BBTXRXRST)	
	Change of Figure 3 - 6 Transmit/Receive Reset Register (BBTXRXRST) Format	
	Change of description in 3.4.4 Transmit/receive mode register 1 (BBTXRXMODE1)	
	Change of description in 3.4.5 RSSI/CCA result register (BBRSSICCARSLT)	
	Change of Figure 3 - 9 RSSI/CCA Result Register (BBRSSICCARSLT) Format	
	Addition of Table 3 - 5 Register setting for loss of input signal level from antenna	
	Change of description in 3.4.7 Transmit/receive status register 0 (BBTXRXST0)	
	Change of Figure Figure 3 - 11 Transmit/Receive Status Register 0 (BBTXRXST0) Format	
	Change of description in 3.4.8 Transmit/receive mode register 2 (BBTXRXMODE2)	
	Change of description in 3.4.9 Transmit/receive mode register 3 (BBTXRXMODE3)	
	Change of Figure Figure 3 - 13 Transmit/Receive Mode Register 3 (BBTXRXMODE3) Format	
	Change of description in 3.4.10 Transmit/receive status register 1 (BBTXRXST1)	
	Change of Figure 3 - 14 Transmit/Receive Status Register 1 (BBTXRXST1) Format	
	Change of description in 3.4.11 Transmit/receive control register (BBTXRXCON)	
	Addition of description to 3.4.13 CCA level threshold setting register (BBCCAVTH)	
	Change of description in 3.4.18 PAN identifier register 0 (BBPANID0)	
	Change of description in 3.4.19 Short address register 0 (BBSHORTAD0)	
	Change of description in 3.4.20 Extended address register 0 (BBEXTENDAD00 to BBEXTENDAD03)	

(2/6)

Downloaded from Arrow.com.

(2/6)

Edition	Description	Chapter
Rev.1.00	Change of description in 3.4.23 Time stamp registers 0 and 1 (BBTSTAMP0, BBTSTAMP1)	CHAPTER 3 BASEBAND FUNCTION
	Change of description in 3.4.24 Timer control register (BBTIMECON)	
	Change of Figure Figure 3 - 35 Baseband Interrupt Source Register 2 (BBINTREQ2) Format	
	Change of description in 3.4.31 Baseband interrupt enable register 2 (BBINTEN2)	
	Change of Figure Figure 3 - 38 Baseband Interrupt Enable Register 2 (BBINTEN2) Format	
	Change of description in 3.4.36 Receive level threshold setting register (BBLVLVTH)	
	Change of Figure Figure 3 - 47 Count Operation in the Non-BEACON Mode	
	Change of Figure Figure 3 - 49 Automatic Receive Switch Compare Register Count Operation	
	Deletion of Change of 3.4.42 CCA start time register (CCASTATIME)	
	Addition of description to 3.4.42 Communication status register 1 (COMSTATE1)	
	Addition of description to 3.4.43 Communication status register 2 (COMSTATE2)	
	Change of title and description in 3.4.44 Estimate control register (BBEVAREG)	
	Change of description in 3.4.49 ANTSW output timing setting register (BBANTSWTIMG)	
	Change of description in 3.4.50 Receive frame length register (BBRXFLEN)	
	Change of description in 3.4.53 Preamble length setting register (BBPAMBL)	
	Change of description in 3.4.54 Frequency setting register (BBFREQ)	
	Change of description in 3.4.55 Symbol rate setting register (BBSYMBLRATE)	
	Change of description in 3.4.56 SUBG control register (BBSUBGCON)	
	Change of Figure 3 - 68 Modulation Method Setting Register (BBMODSET) Format	
	Change of description in 3.4.58 CCA time register (CCATIME)	
	Change of description in 3.4.59 Antenna diversity mode register (BBANTDIV)	
	Change of Figure 3 - 70 Antenna Diversity Mode Register (BBANTDIV) Format	
	Change of description in 3.4.60 Mode switch frame transmit register (BBTXMODESW)	
	Change of Figure 3 - 71 Mode Switch Frame Transmit Register (BBTXMODESW) Format	
	Change of description in 3.4.61 Mode switch frame receive register (BBRXMODESW)	
	Change of description in 3.4.62 Transmit data counter register (BBTXCOUNT)	
	Change of description in 3.4.63 PHY header receive register (BBPHRRX)	
	Change of description in 3.4.64 Preamble setting register (BBPABL)	
	Change of description in 3.4.65 SFD setting register (BBSFD)	
	Change of description in 3.4.67 ANT0 read register (BBANT0RD)	
	Change of description in 3.4.68 ANT1 read register (BBANT1RD)	
	Change of description in 3.4.69 Antenna switch time register (BBANTDIVTIM)	
	Change of description in 3.4.70 Receive start timeout setting register (BBANTTIMOUT)	
	Change of description in 3.4.72 Back off period total number register (BBBOPTOTAL)	
	Change of description in 3.4.73 CCA total number register (BBCCATOTAL)	
	Deletion of 3.4.73 RF initial setting register (RFINI)	
	Addition of 3.4.74 RF initial setting register 00 to 02 (RFINI00 to RFINI02)	
	Addition of 3.4.75 RF initial setting register 10 to 12 (RFINI10 to RFINI12)	

Downloaded from Arrow.com.

(3/6)

Edition	Description	Chapter
Rev.1.00	Change of description in 3.4.76 PAN identifier register 1 (BBPANID1)	CHAPTER 3 BASEBAND FUNCTION
	Change of description in 3.4.77 Short address register 1 (BBSHORTAD1)	
	Change of description in 3.4.78 Extended address register 1 (BBEXTENDAD10 to BBEXTENDAD13)	
	Change of description in 3.4.79 Receive timeout register (BBTIMEOUT)	
	Deletion of 3.4.78 Transmit CP current select register 1 (TXCPISL1) to 3.4.81 Transmit capacitance and resistance select register 1 (TXCR1)	
	Change of description in 3.4.80 ANTSW control register (ANTSWCON)	
	Change of description in 3.4.81 Clock output control register (CLKOUTCON)	
	Change of description in 3.4.82 Port direction register (GPIODIR)	
	Change of description in 3.4.83 Port data register (GPIODATA)	
	Deletion of 3.4.86 Upon-transmission power supply setting register 0 (TXCON0)	
	Change of description in 3.4.84 SFD setting register 2 (BBSFD2)	
	Change of description in 3.4.85 SFD setting register 3 (BBSFD3)	
	Change of description in 3.4.86 SFD setting register 4 (BBSFD4)	
	Addition of description to 3.4.87 FEC control register (BBFECCON)	
	Addition of caution to Figure 3 - 98 FEC Control Register (BBFECCON) Format	
	Change of description in 3.4.88 Address filter extension address control register (BBADFCON)	
	Change of Figure 3 - 99 Address Filter Extension Address Control Register (BBADFCON) Format	
	Change of description in 3.4.89 Antenna diversity mode register 2 (BBANTDIV2)	
	Change of Figure 3 - 100 Antenna Diversity Mode Register 2 (BBANTDIV2) Format and caution	
	Addition of description to 3.4.90 Lower limit threshold setting register after SFD detection (PWRLOWTH2)	
	Change of description in the top	CHAPTER 5 STATE TRANSITION
	Change of Figure 5 - 1 State Transition	
	Change of Table 5 - 1 Description of Each Mode	
	Change of title of Figure 5 - 2 Wake Up Operation 1 (for crystal oscillator)	
	Change of Table 5 - 3 Operation in Each State in Startup Sequence	
	Change of description and addition of Caution to 5.1 Wake Up (SLEEP → IDLE)	
	Change of Table 5 - 4 Initial Setting	
	Deletion of description in 5.3.2 Example of Procedure for Reception	
	Change of title of 5.3.4 Example of Procedure for CSMA-CA	
	Change of description and caution in 5.3.5 Example of Procedure for Calibration	
	Addition of caution in 5.3.6 Setting for Each Data Rate	
	Change of Table 5 - 5 Each Data Rate List	
	Change of Table 5 - 6 Settings Required for Each Data Rate	
	Change of description in 6.1 Example of Procedure for Transmission Output Power Setting	CHAPTER 6 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING
	Change of Table 6 - 1 to Gain Set (Frequency band identifier = 9) to Figure 6 - 4 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 8)	

Downloaded from Arrow.com.

(4/6)

Edition	Description	Chapter
Rev.1.00	Change of Table 6 - 14 RF Frequency Set (Frequency band identifier = 4, Mode = 001) to Table 6 - 35 Frequency Set (Frequency band identifier = Other, Mode = 021)	CHAPTER 6 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING
	Addition of the chapter	CHAPTER 7 NOTICE FOR USING BASEBAND FUNCTION
	Change of Figure 8 - 1 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (Without ANTSW)	CHAPTER 8 PERIPHERAL CIRCUIT CONNECTION DIAGRAM
	Change of Figure 8 - 2 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (With ANTSW)	
	Addition of Figure 8 - 3 RAA604S00 (32-pin) Peripheral Circuit Connection Diagram (Using TCXO)	
	Change of the title	CHAPTER 9 ELECTRIC CHARACTERISTICS
	Change of 9.1 Absolute Maximum Ratings	
	Addition of 9.3.2 Compatible with ARB Standard	
	Change of 9.7 Power Supply Current	
	Change of 9.8 Transceiver Reception Characteristics	
	Change of 9.9 Transceiver Transmission Characteristics	
	Change of 9.10 IEEE802.15.4g Frequency/Data Rate Table	
Rev.0.60	Change of description in 1.1 Features	CHAPTER 1 OVERVIEW
	Change of figure and description in 1.3.1 RAA604S00 (32-pin)	
	Change of figures in 1.4.1 RAA604S00 (32-pin)	
	Change of Table 1 - 1 RAA604S00 (32-pin) Pin Function List	
	Change of title in Figure 2 - 1 Block Diagram for STANBY, OSCDRVSEL, SIN, SCLK, SEN, RFRESETB, DON, MODE1, MODE2	CHAPTER 2 PIN FUNCTIONS
	Change of description in 3.1 Communication Format	CHAPTER 3 SERIAL INTERFACE
	Change of description in 3.1.2 Data part	
	Change of description in 4.1 Wake Up (SLEEP → IDLE)	CHAPTER 4 STATE TRANSITION
	Change of Figure 4 - 2 Wake Up Operation 2 (for crystal oscillator)	
	Change of Figure 4 - 3 Wake Up Operation 2 (for external clock Input), deletion in the description	
	Addition of Table 4 - 2 Pin Status	
	Addition of description in 4.1 Wake Up (SLEEP → IDLE)	
	Change of title and description in 4.3.1 Example of Procedure for Transmission	
	Change of title and description in 4.3.2 Example of Procedure for Reception	
	Change of title and description in 4.3.3 Example of Procedure for CCA	
	Change of title and description in 4.3.4 Example of Procedure for CSMA	
	Addition of 4.3.5 Example of Procedure for Calibration	
	Change of description and addition of caution in 4.3.6 Setting for Each Data Rate	
	Change of Table 4 - 6 to 4 - 12 Settings Required for Each Data Rate	
	Change of Figure 5 - 1 Baseband Block Diagram	CHAPTER 5 BASEBAND FUNCTION
	Change of the title and description in 5.2.2 Preamble value	
	Change of Table 5 - 3 Baseband Function Controlling Register	
	Change of description in 5.3.4 Transmit/receive mode register 1 (BBTXRXMODE1)	
	Change of description in 5.3.9 Transmit/receive mode register 3 (BBTXRXMODE3)	

Downloaded from Arrow.com.

(5/6)

Edition	Description	Chapter
Rev.0.60	Change of Figure 5 - 13 Transmit/Receive Mode Register 3 (BBTXRXMODE3) Format and the caution	CHAPTER 5 BASEBAND FUNCTION
	Deletion of description in 5.3.10 Transmit/receive status register 1 (BBTXRXST1), addition of caution	
	Change of Figure 5 - 14 Transmit/Receive Status Register 1 (BBTXRXST1) Format	
	Change of description in 5.3.11 Transmit/receive control register (BBTXRXCON)	
	Change of description in 5.3.12 CSMA control register 0 (BBCSMACON0)	
	Change of caution in Figure 5 - 16 CSMA Control Register 0 (BBCSMACON0) Format	
	Change of description in 5.3.15 Transmit/receive mode register 4 (BBTXRXMODE4)	
	Change of caution in Figure 5 - 19 Transmit/Receive Mode Register 4 (BBTXRXMODE4) Format	
	Change of Figure 5 - 34 Baseband Interrupt Source Register 1 (BBINTREQ1) Format, addition of caution	
	Change of caution and Figure 5 - 35 Baseband Interrupt Source Register 2 (BBINTREQ2) Format	
	Change of Figure 5 - 37 Baseband Interrupt Enable Register 1 (BBINTEN1) Format, addition of caution	
	Change of Figure 5 - 38 Baseband Interrupt Enable Register 2 (BBINTEN2) Format and the caution	
	Addition of description to 5.3.32 CSMA control register 3 (BBCSMACON3)	
	Change of description in 5.3.36 Receive level threshold setting register (BBLVLVTH)	
	Deletion of 5.3.43 CCA data read register (CCADATARD)	
	Change of description in 5.3.43 Estimate control register 1 (BBEVAREG)	
	Change of description in 5.3.48 ANTSW output timing setting register (BBANTSWTIMG)	
	Change of Figure 5 - 59 ANTSW Output Timing Setting Register (BBANTSWTIMG) Format	
	Change of description in 5.3.55 SUBG control register (BBSUBGCON)	
	Change of Figure 5 - 66 SUBG Control Register (BBSUBGCON) Format, addition of caution	
	Change of Figure 5 - 67 Modulation Method Setting Register (BBMODSET) Format and the caution	
	Change of description in 5.3.58 Antenna diversity mode register (BBANTDIV)	
	Change of Figure 5 - 69 Antenna Diversity Mode Register (BBANTDIV) Format	
	Change of description in 5.3.61 Transmit data counter register (BBTXCOUNT)	
	Change of description in 5.3.64 SFD setting register (BBSFD)	
	Change of description in 5.3.69 Receive start timeout setting register (BBANTTIMOUT)	
	Deletion of 5.3.74 RF serial 2 control registers 0 to 2 (RFSER2REG0 to RFSER2REG2)	
	Addition of 5.3.73 RF initial setting register (RFINI)	
	Change of description in 5.3.82 ANTSW control register (ANTSWCON)	
	Change of description in 5.3.85 Port data register (GPIODATA)	
	Change of Figure 5 - 96 Port Data Register (GPIODATA) Format	

Downloaded from Arrow.com.

(6/6)

Edition	Description	Chapter
Rev.0.60	Addition of 5.3.87 SFD setting register 2 (BBSFD2) to 5.3.92 Antenna diversity mode register 2 (BBANTDIV2)	CHAPTER 5 BASEBAND FUNCTION
	Change of figures in 6.1 RAA604S00 (32-pin)	CHAPTER 6 PERIPHERAL CIRCUIT CONNECTION DIAGRAM
	Change of description in 7.1 Example of Procedure for Transmission Output Power Setting	CHAPTER 7 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING
	Change of Table 7 - 1 to Table 7 - 6 Gain set (Frequency band identifier = 9)	
	Change of Figure 7 - 1 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 9)	
	Change of figures in 6.1 RAA604S00 (32-pin)	CHAPTER 6 PERIPHERAL CIRCUIT CONNECTION DIAGRAM
	Change of description in 7.1 Example of Procedure for Transmission Output Power Setting	CHAPTER 7 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING
	Change of Table 7 - 1 to Table 7 - 6 Gain set (Frequency band identifier = 9)	
	Change of Figure 7 - 1 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 9)	
	Addition of Table 7 - 7 Gain set (Frequency band identifier = 9) to Figure 7 - 4 Relationship between Transmission Output Power and Gain Set (Frequency band identifier = 8)	CHAPTER 7 EXAMPLE OF PROCEDURE FOR FUNCTION SETTING
	Addition of 7.2 RF frequency setting for transmission	
	Addition of 7.3 RF frequency setting for reception	
	Change of description in 8.1 Absolute Maximum Ratings	CHAPTER 8 ELECTRIC CHARACTERISTICS (TARGET)
	Addition of description in 8.3 XIN Frequency Deviation (Compatible with IEEE802.15.4g)	
	Change of 8.4 DC Characteristics	
	Addition of 8.5 AC Characteristics	
	Addition of 8.6 Calibration Timing Characteristic	
	Change of description and deletion of note in 8.7 Power Supply Current	
	Change of description in 8.8 Transceiver Reception Characteristics	
	Change of description and deletion of note1 in 8.9 Transceiver Transmission Characteristics	
Rev.0.50	First Edition issued.	Throughout

Downloaded from Arrow.com.

SubGHz Transceiver (RAA604S00) User's Manual: Hardware

Publication Date: Rev. 0.50 Mar 16, 2015
Rev. 1.20 Nov 30, 2016

Published by: Renesas Electronics Corporation

Downloaded from Arrow.com.

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

© 2016 Renesas Electronics Corporation. All rights reserved.

Colophon 4.0

Downloaded from Arrow.com.

SubGHz Transceiver (RAA604S00)

Renesas Electronics Corporation

R01UH0567EJ0120

Downloaded from Arrow.com.