



# 74HCT241-Q100

Octal buffer/line driver; 3-state

Rev. 2 — 5 August 2024

Product data sheet

## 1. General description

The 74HCT241-Q100 is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1OE and 2OE), each controlling four of the 3-state outputs. A HIGH on 1OE or LOW on 2OE causes the associated outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

The 74HCT241-Q100 device features reduced input threshold levels to allow interfacing to TTL logic levels.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

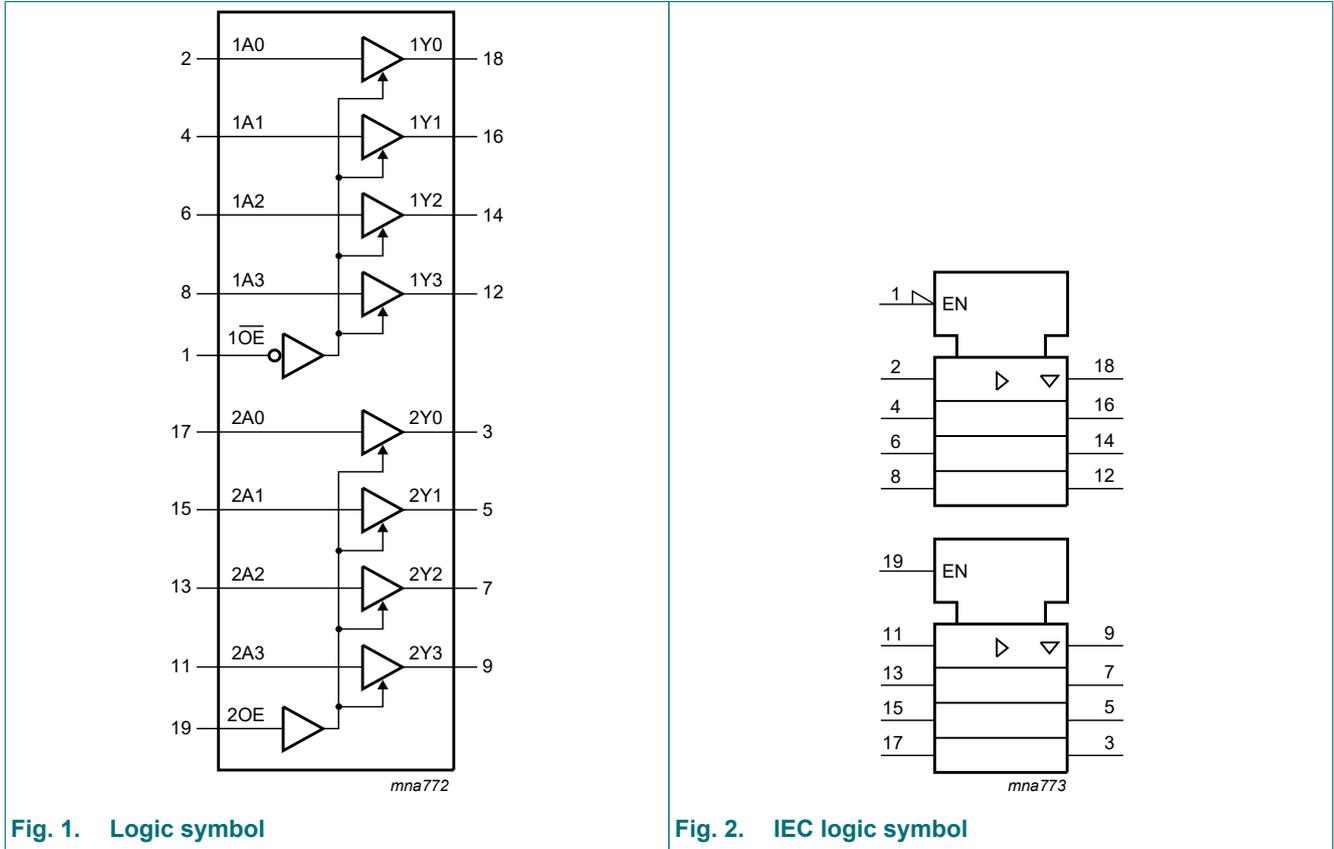
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 4.5 V to 5.5 V
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels at TTL level
- Octal bus interface
- Non-inverting 3-state outputs
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

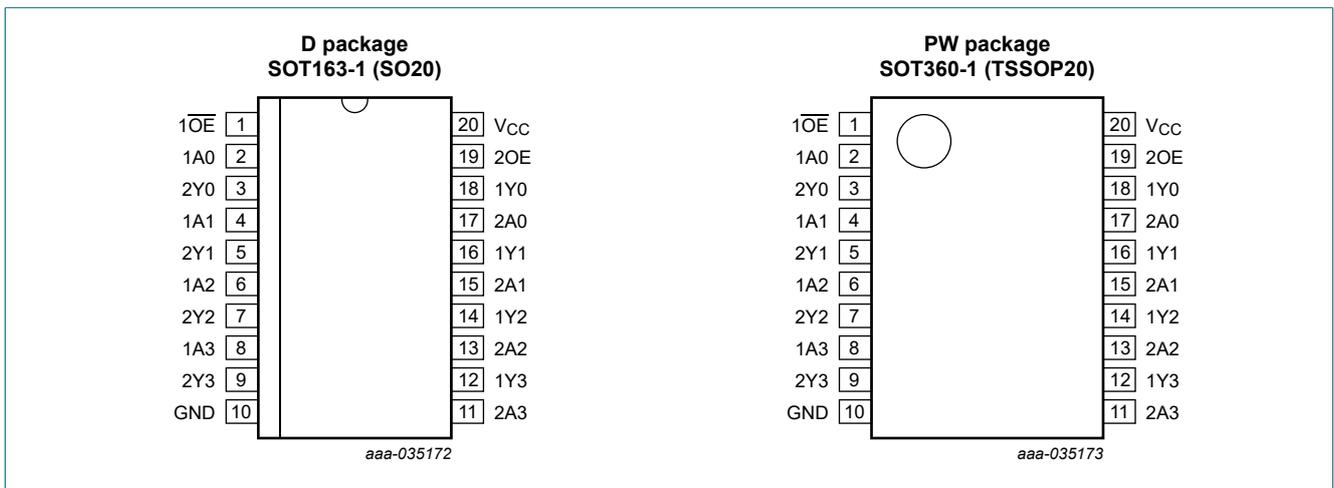
Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74HCT241D-Q100</a>	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	<a href="#">SOT163-1</a>
<a href="#">74HCT241PW-Q100</a>	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	<a href="#">SOT360-1</a>

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
GND	10	ground (0 V)
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
2OE	19	output enable input (active HIGH)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = High impedance "OFF" state

Inputs		Outputs	Inputs		Outputs
1OE	1An	1Yn	2OE	2An	2Yn
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±35	mA
I <sub>CC</sub>	supply current		-	70	mA
I <sub>GND</sub>	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	[1]	-	500	mW

- [1] For SOT163-1 (SO20) package: P<sub>tot</sub> derates linearly with 12.3 mW/K above 109 °C.  
For SOT360-1 (TSSOP20) package: P<sub>tot</sub> derates linearly with 10.0 mW/K above 100 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5\text{ V}$								
		$I_O = -20\ \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6\text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5\text{ V}$								
		$I_O = 20\ \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0\text{ mA}$	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5\text{ V}$ ; $V_O = V_{CC}$ or GND	-	-	$\pm 0.5$	-	$\pm 5.0$	-	$\pm 10$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$ ; $I_O = 0\text{ A}$	-	-	8.0	-	80	-	160	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; $V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or GND; $I_O = 0\text{ A}$								
		nAn; $\overline{1OE}$	-	70	252	-	315	-	343	$\mu\text{A}$
		2OE	-	150	540	-	675	-	735	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

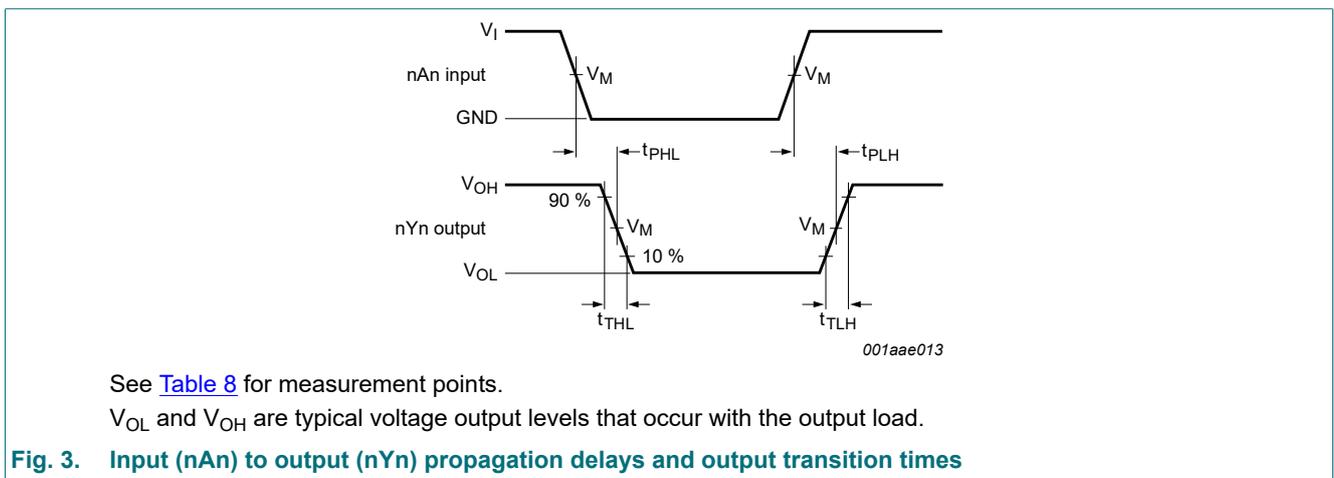
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

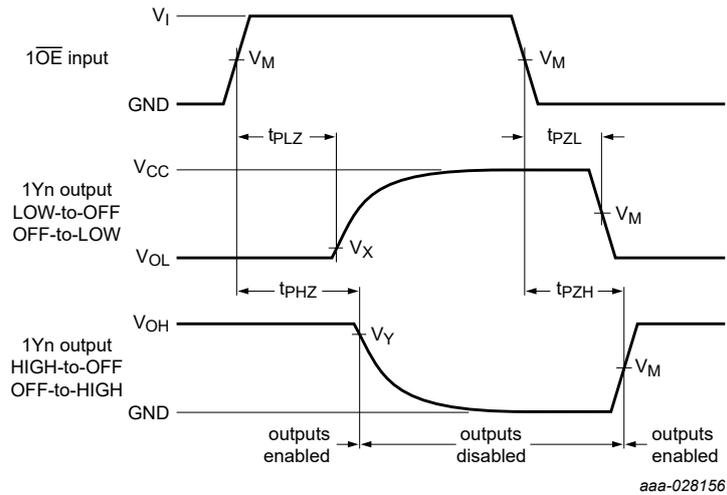
Symbol	Parameter	Conditions	+25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nYn; see Fig. 3 [1]								
		V <sub>CC</sub> = 4.5 V	-	13	22	-	28	-	33	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	-	-	ns
t <sub>en</sub>	enable time	1OE to 1Yn; see Fig. 4; [2] 2OE to 2Yn; see Fig. 5; V <sub>CC</sub> = 4.5 V	-	15	30	-	38	-	45	ns
t <sub>dis</sub>	disable time	1OE to 1Yn; see Fig. 4; [3] 2OE to 2Yn; see Fig. 5; V <sub>CC</sub> = 4.5 V	-	18	30	-	38	-	45	ns
t <sub>t</sub>	transition time	V <sub>CC</sub> = 4.5 V; see Fig. 3 [4]	-	5	12	-	15	-	18	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [5]	-	30	-	-	-	-	-	pF

- [1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
- [2] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.
- [3] t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.
- [4] t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

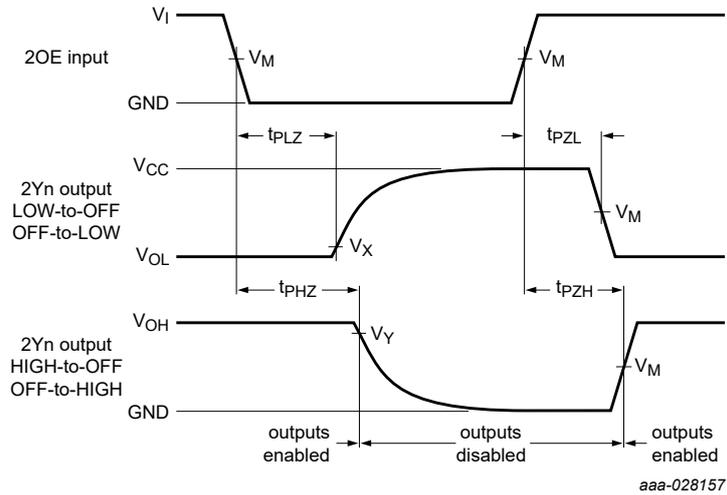
### 10.1. Waveforms and test circuit





See [Table 8](#) for measurement points.  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 4. 3-state output (10E to 1Yn) enable and disable times**



See [Table 8](#) for measurement points.  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 5. 3-state output (2OE to 2Yn) enable and disable times**

**Table 8. Measurement points**

Type	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
74HCT241-Q100	GND to 3 V	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

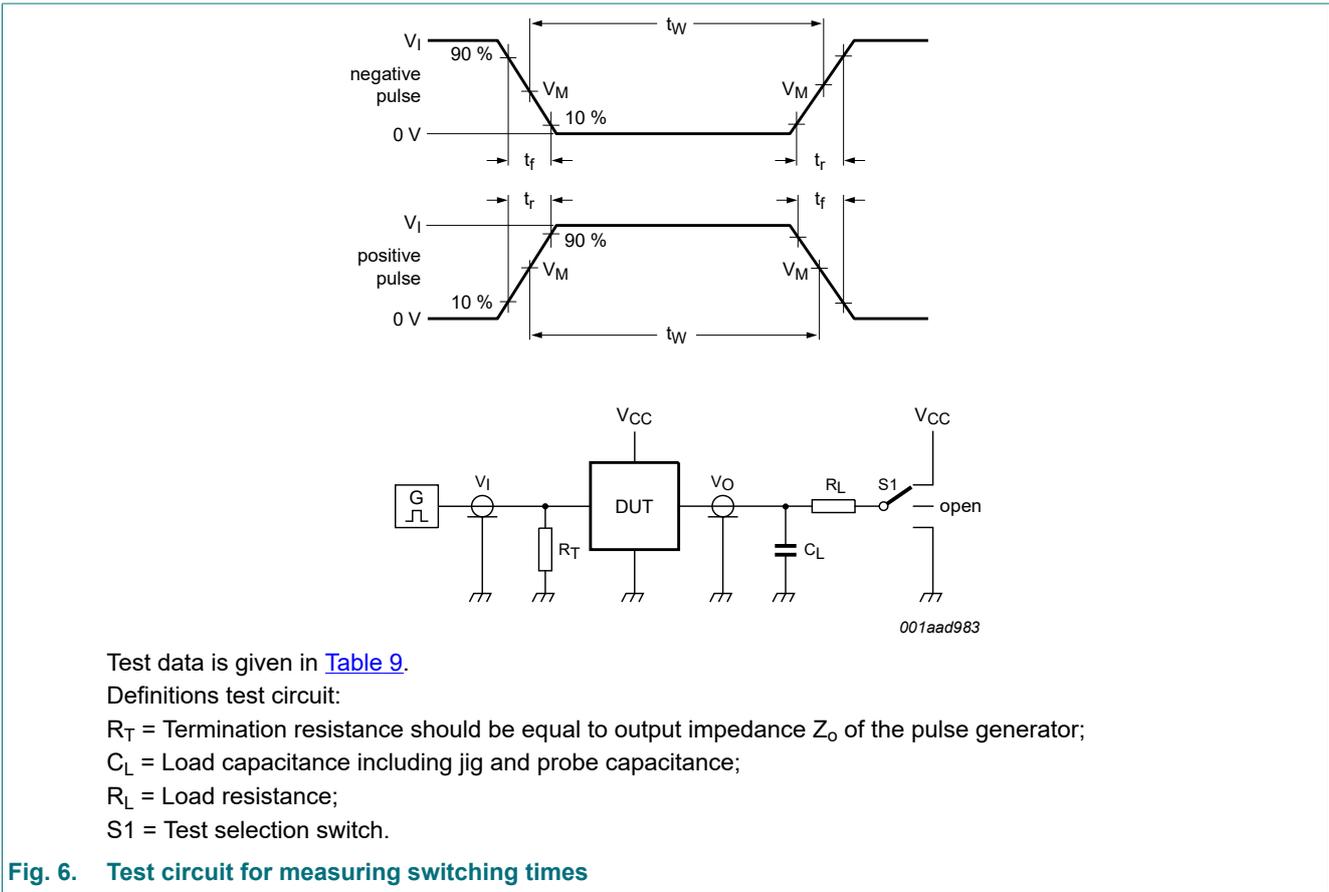


Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HCT241-Q100	GND to 3 V	6 ns	50 pF	1 kΩ	open	GND	$V_{CC}$

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

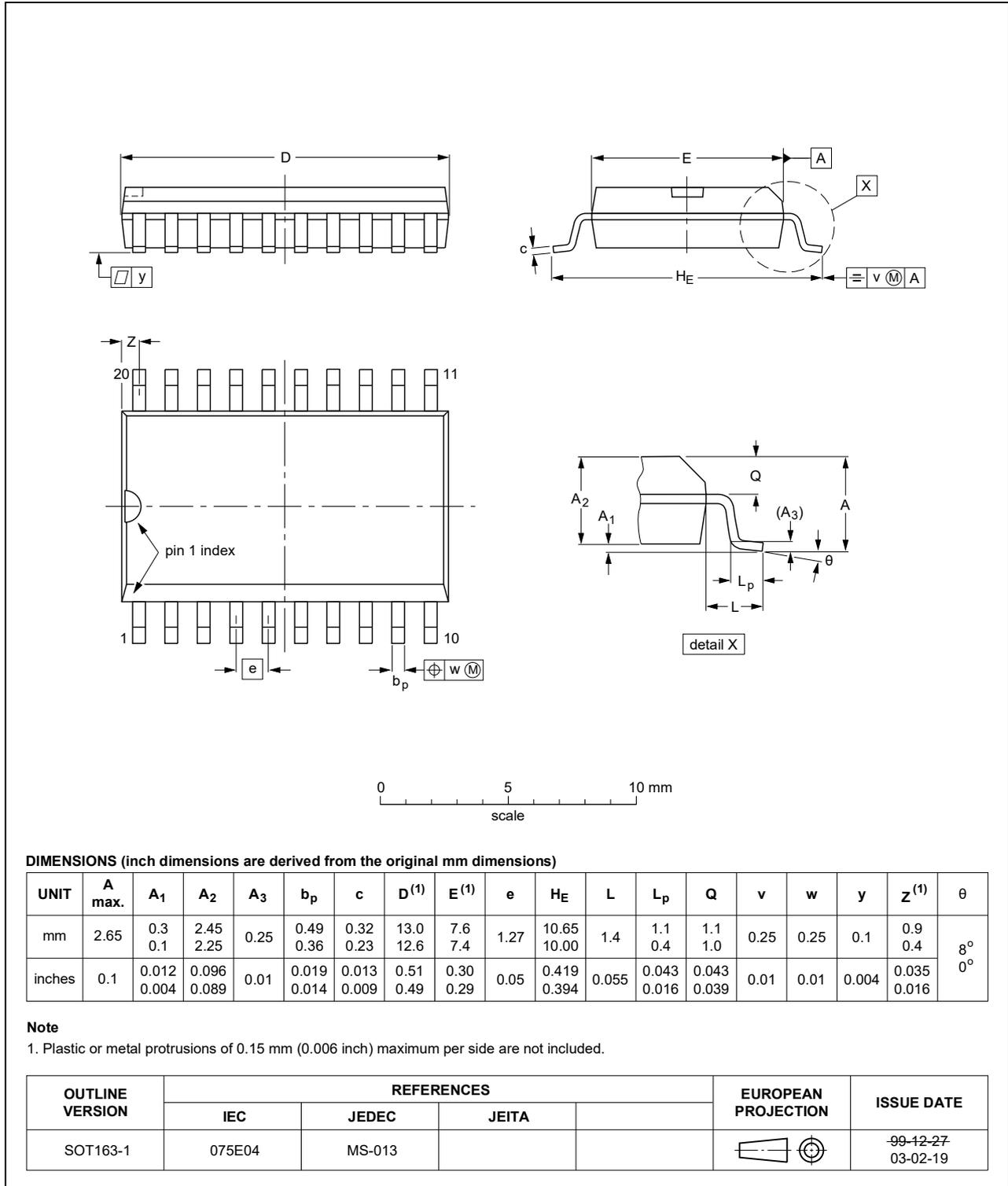


Fig. 7. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

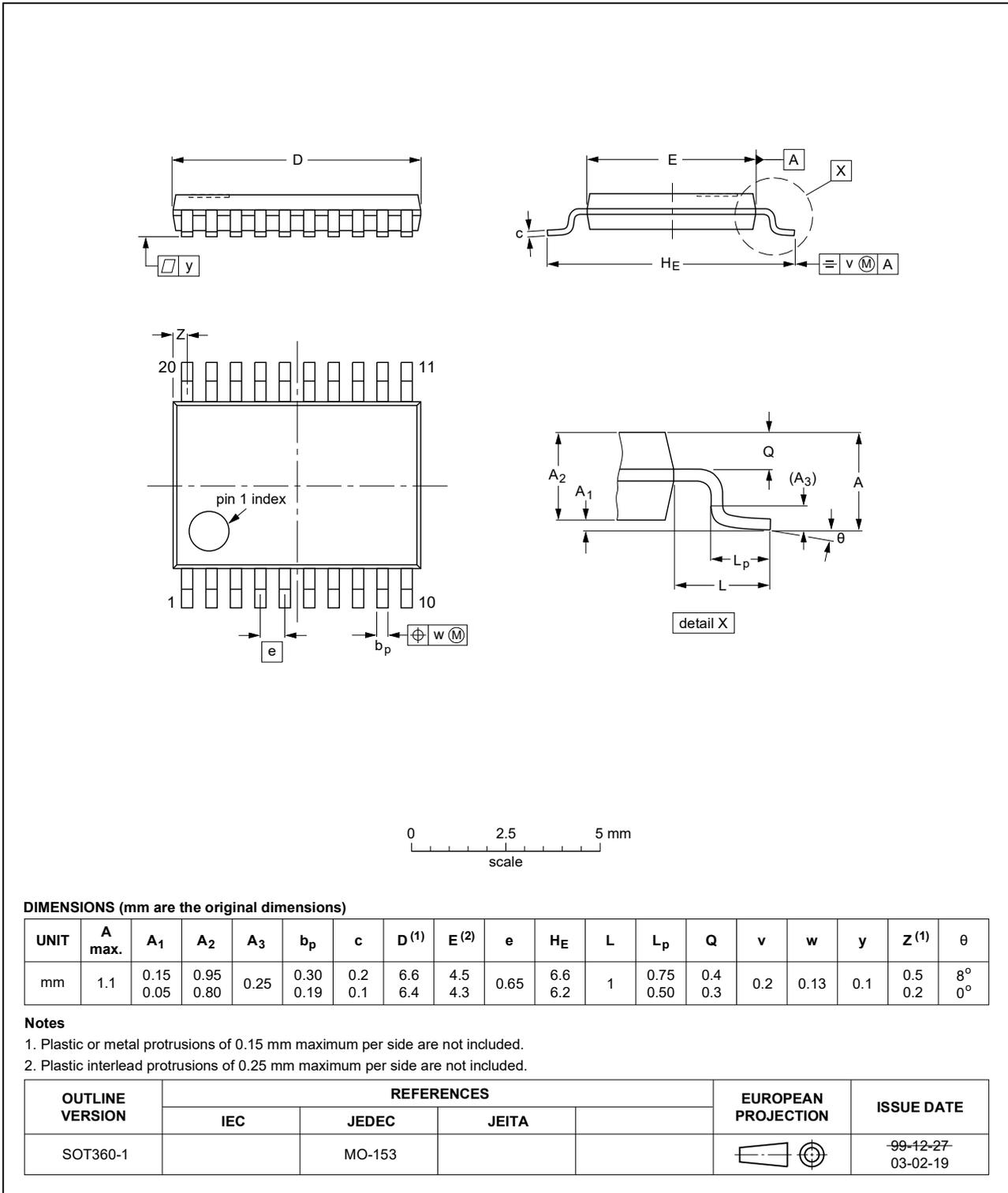


Fig. 8. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCT241_Q100 v.2	20240805	Product data sheet	-	74HCT241_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74HCT241_Q100 v.1	20231025	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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## Contents

- 1. General description..... 1
- 2. Features and benefits..... 1
- 3. Ordering information..... 1
- 4. Functional diagram..... 2
- 5. Pinning information..... 2
  - 5.1. Pinning..... 2
  - 5.2. Pin description..... 3
- 6. Functional description..... 3
- 7. Limiting values..... 3
- 8. Recommended operating conditions..... 4
- 9. Static characteristics..... 4
- 10. Dynamic characteristics..... 5
  - 10.1. Waveforms and test circuit..... 5
- 11. Package outline..... 8
- 12. Abbreviations..... 10
- 13. Revision history..... 10
- 14. Legal information..... 11

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