CY14MB064J
CY14ME064J

64-Kbit (8 K × 8) Serial (I^2C) nvSRAM

Features

- 64-Kbit nonvolatile static random access memory (nvSRAM)
  - Internally organized as 8 K × 8
  - STORE to QuantumTrap nonvolatile elements initiated automatically on power-down (AutoStore) or by using I^2C command (Software STORE) or $\overline{HSB}$ pin (Hardware STORE)
  - RECALL to SRAM initiated on power-up (Power-Up RECALL) or by I^2C command (Software RECALL)
  - Automatic STORE on power-down with a small capacitor (except for CY14MX064J1)
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years at 85 °C
- High speed I^2C interface [1]
  - Industry standard 100 kHz and 400 kHz speed
  - Fast-mode Plus: 1 MHz speed
  - High speed: 3.4 MHz
  - Zero cycle delay reads and writes
- Write protection
  - Hardware protection using Write Protect (WP) pin
  - Software block protection for 1/4, 1/2, or entire array
- I^2C access to special functions
  - Nonvolatile STORE/RECALL
  - 8 byte serial number
  - Manufacturer ID and Product ID
  - Sleep mode
- Low power consumption
  - Average active current of 1 mA at 3.4 MHz operation
  - Average standby mode current of 150 µA
  - Sleep mode current of 8 µA
- Industry standard configurations
  - Operating voltages:
    - CY14MB064J: V_{CC} = 2.7 V to 3.6 V
    - CY14ME064J: V_{CC} = 4.5 V to 5.5 V
  - Industrial temperature
  - 8- and 16-pin small outline integrated circuit (SOIC) package
  - Restriction of hazardous substances (RoHS) compliant

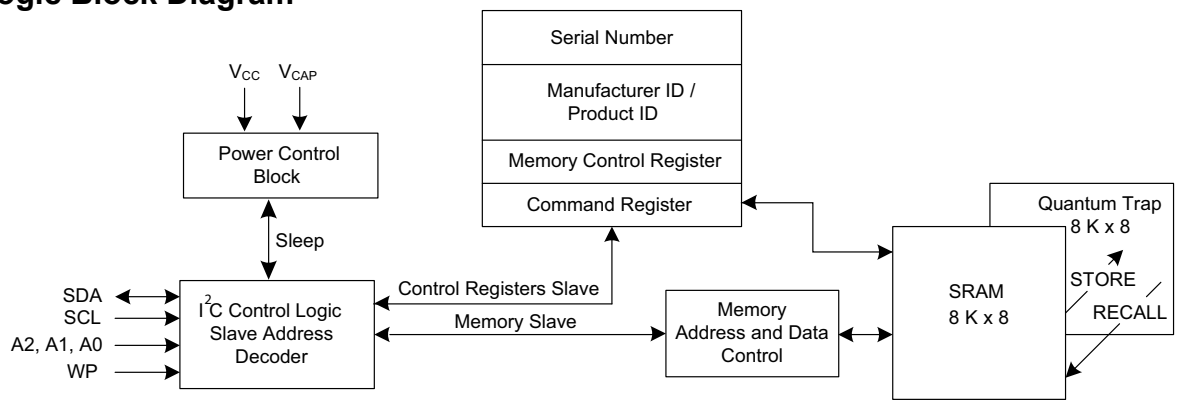
Overview

The Cypress CY14MB064J/CY14ME064J combines a 64-Kbit nvSRAM[2] with a nonvolatile element in each memory cell. The memory is organized as 8 K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cells provide highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power-down (except for CY14MX064J1). On power-up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). The STORE and RECALL operations can also be initiated by the user through I^2C commands.

Configuration

Feature	CY14MX064J1	CY14MX064J2	CY14MX064J3
AutoStore	No	Yes	Yes
Software STORE	Yes	Yes	Yes
Hardware STORE	No	No	Yes
Slave Address pins	A2, A1, A0	A2, A1	A2, A1, A0

Logic Block Diagram



Notes
1. The I^2C nvSRAM is a single solution which is usable for all four speed modes of operation. As a result, some I/O parameters are slightly different than those on chips which support only one mode of operation. Refer to AN87209 for more details.
2. Serial (I^2C) nvSRAM is referred to as nvSRAM throughout the datasheet.

Not Recommended for New Designs

Downloaded from Arrow.com.

Contents

Pinouts **3**
Pin Definitions **3**
I2C Interface **4**
Protocol Overview **4**
I2C Protocol – Data Transfer 4
Data Validity 5
START Condition (S) 5
STOP Condition (P) 5
Repeated START (Sr) 5
Byte Format 5
Acknowledge / No-acknowledge 5
High Speed Mode (Hs-mode) 6
Slave Device Address 7
Write Protection (WP) 9
AutoStore Operation 9
Hardware STORE and HSB pin Operation 9
Hardware RECALL (Power-Up) 9
Write Operation 10
Read Operation 10
Memory Slave Access 10
Control Registers Slave 14
Serial Number **16**
Serial Number Write 16
Serial Number Lock 16
Serial Number Read 16
Device ID **17**
Executing Commands Using Command Register 17
Maximum Ratings **18**
Operating Range **18**
DC Electrical Characteristics **18**
Data Retention and Endurance **19**
Thermal Resistance **19**
AC Test Loads and Waveforms **20**
AC Test Conditions **20**
AC Switching Characteristics **21**
Switching Waveforms **21**
nvSRAM Specifications **22**
Switching Waveforms **22**
Software Controlled STORE/RECALL Cycles **23**
Switching Waveforms **23**
Hardware STORE Cycle **24**
Switching Waveforms **24**
Ordering Information **25**
Ordering Code Definitions 25
Package Diagrams **26**
Acronyms **28**
Document Conventions **28**
Units of Measure 28
Document History Page **29**
Sales, Solutions, and Legal Information **31**
Worldwide Sales and Design Support 31
Products 31
PSoC® Solutions 31
Cypress Developer Community 31
Technical Support 31

Not Recommended for New Designs

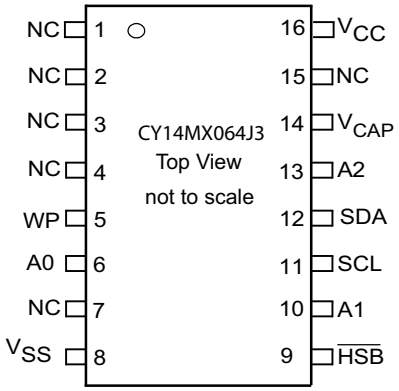
Downloaded from Arrow.com.

Pinouts

Figure 1. 8-pin SOIC pinout



Figure 2. 16-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
SCL	Input	Clock. Runs at speeds up to a maximum of f_{SCL}.
SDA	Input/Output	I/O. Input/Output of data through I^2C interface. Output: Is open-drain and requires an external pull-up resistor.
WP	Input	Write Protect. Protects the memory from all writes. This pin is internally pulled LOW and hence can be left open if not connected.
A2–A0 [3]	Input	Slave Address. Defines the slave address for I^2C. This pin is internally pulled LOW and hence can be left open if not connected.
$\overline{HSB}$	Input/Output	Hardware STORE Busy: Output: Indicates busy status of nvSRAM when LOW. After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (External pull up resistor connection optional). Input: Hardware STORE implemented by pulling this pin LOW externally.
V_{CAP}	Power supply	AutoStore Capacitor. Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If not required, AutoStore must be disabled and this pin left as no connect. It must never be connected to ground.
NC	No connect	No Connect. This pin is not connected to the die.
V_{SS}	Power supply	Ground
V_{CC}	Power supply	Power supply

Note
3. A0 pin is not available in CY14MX064J2.

Not Recommended for New Designs

Downloaded from Arrow.com.

I²C Interface

I²C bus consists of two lines – serial clock line (SCL) and serial data line (SDA) that carry information between multiple devices on the bus. I²C supports multi-master and multi-slave configurations. The data is transmitted from the transmitter to the receiver on the SDA line and is synchronized with the clock SCL generated by the master.

The SCL and SDA lines are open-drain lines and are pulled up to V_{CC} using resistors. The choice of pull-up resistor on the system depends on the bus capacitance and the intended speed of operation. The master generates the clock and all the data I/Os are transmitted in synchronization with this clock. The CY14MX064J supports up to 3.4 MHz clock speed on SCL line.

Protocol Overview

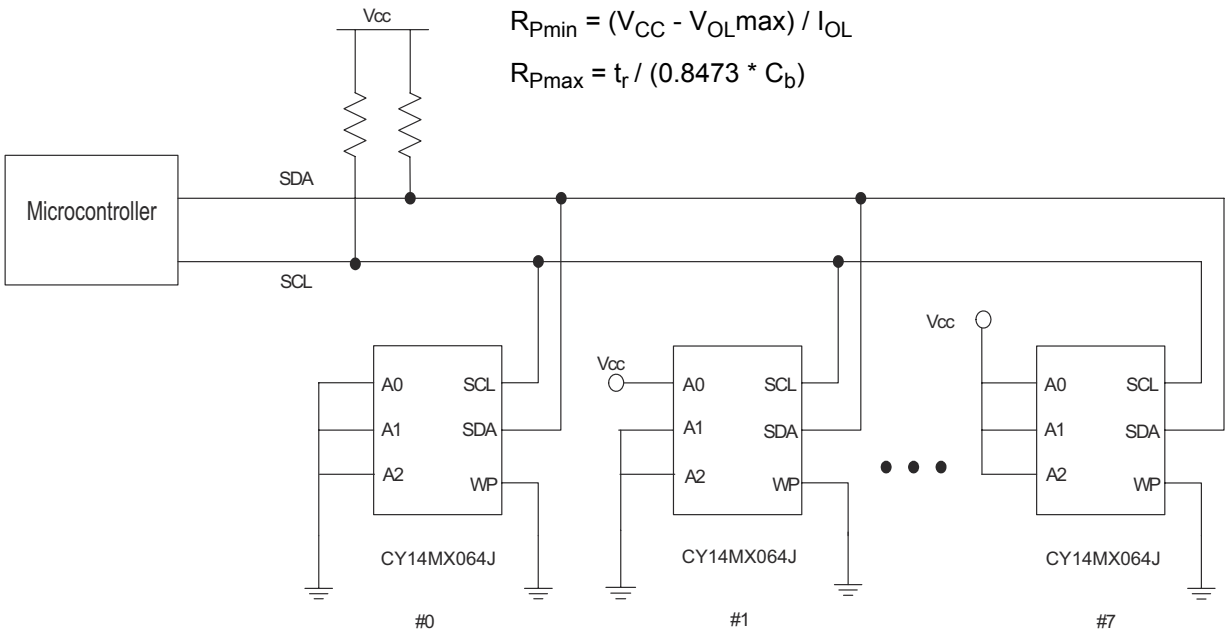
This device supports only a 7-bit addressable scheme. The master generates a START condition to initiate the communication followed by broadcasting a slave select byte. The slave select byte consists of a seven bit address of the slave that the master intends to communicate with and R/W bit indicating a read or a write operation. The selected slave responds to this with an acknowledgement (ACK). After a slave is selected, the remaining part of the communication takes place between the master and the selected slave device. The other devices on the bus ignore the signals on the SDA line till a STOP or Repeated START condition is detected. The data transfer is done between the master and the selected slave device through the SDA pin synchronized with the SCL clock generated by the master.

I²C Protocol – Data Transfer

Each transaction in I²C protocol starts with the master generating a START condition on the bus, followed by a seven bit slave address and eighth bit (R/$\overline{W}$) indicating a read (1) or a write (0) operation. All signals are transmitted on the open-drain SDA line and are synchronized with the clock on SCL line. Each byte of data transmitted on the I²C bus is acknowledged by the receiver by holding the SDA line LOW on the ninth clock pulse. The request for write by the master is followed by the memory address and data bytes on the SDA line. The writes can be performed in burst-mode by sending multiple bytes of data. The memory address increments automatically after receiving /transmitting of each byte on the falling edge of 9th clock cycle. The new address is latched just prior to sending/receiving the acknowledgment bit. This allows the next sequential byte to be accessed with no additional addressing. On reaching the last memory location, the address rolls back to 0x0000 and writes continue. The slave responds to each byte sent by the master during a write operation with an ACK. A write sequence can be terminated by the master generating a STOP or Repeated START condition.

A read request is performed at the current address location (address next to the last location accessed for read or write). The memory slave device responds to a read request by transmitting the data on the current address location to the master. A random address read may also be performed by first sending a write request with the intended address of read. The master must abort the write immediately after the last address byte and issue a Repeated START or STOP signal to prevent any write operation. The following read operation starts from this address. The master acknowledges the receipt of one byte of data by holding the SDA pin LOW for the ninth clock pulse. The reads can be terminated by the master sending a no-acknowledge (NACK) signal on the SDA line after the last data byte. The no-acknowledge signal causes the CY14MX064J to release the SDA line and the master can then generate a STOP or a Repeated START condition to initiate a new operation.

Figure 3. System Configuration using Serial (I²C) nvSRAM



Not Recommended for New Designs

Downloaded from Arrow.com.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The state of the data line can only change when the clock on the SCL line is LOW for the data to be valid. There are only two conditions under which the SDA line may change state with SCL line held HIGH, that is, START and STOP condition. The START and STOP conditions are generated by the master to signal the beginning and end of a communication sequence on the I^2C bus.

START Condition (S)

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. Every transaction in I^2C begins with the master generating a START condition.

STOP Condition (P)

A LOW to HIGH transition on the SDA line while SCL is HIGH indicates a STOP condition. This condition indicates the end of the ongoing transaction.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again after the STOP condition.

Repeated START (Sr)

If an Repeated START condition is generated instead of a STOP condition the bus continues to be busy. The ongoing transaction on the I^2C lines is stopped and the bus waits for the master to send a slave ID for communication to restart.

Figure 4. START and STOP Conditions

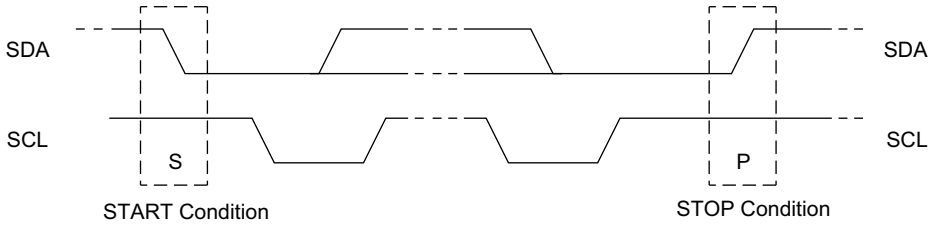
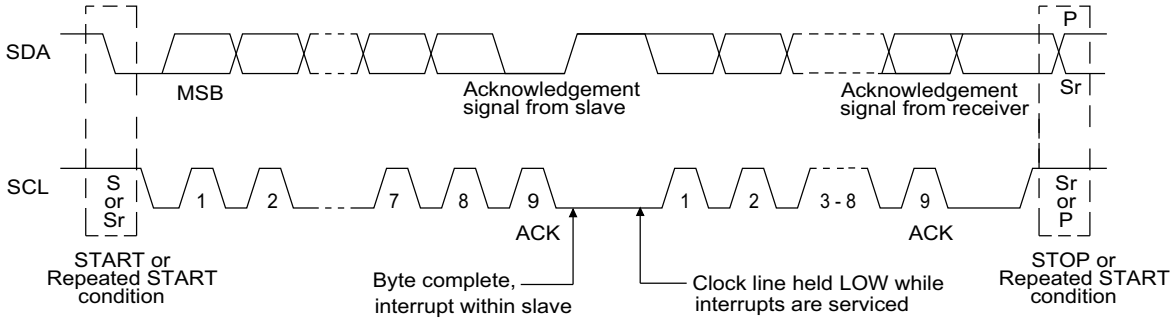


Figure 5. Data Transfer on the I^2C Bus



Byte Format

Each operation in I^2C is done using 8 bit words. The bits are sent in MSB first format on SDA line and each byte is followed by an ACK signal by the receiver.

An operation continues till a NACK is sent by the receiver or STOP or Repeated START condition is generated by the master The SDA line must remain stable when the clock (SCL) is HIGH except for a START or STOP condition.

Acknowledge / No-acknowledge

After transmitting one byte of data or address, the transmitter releases the SDA line. The receiver pulls the SDA line LOW to acknowledge the receipt of the byte. Every byte of data transferred on the I^2C bus needs to be responded with an ACK signal by the receiver to continue the operation. Failing to do so is considered as a NACK state. NACK is the state where receiver does not acknowledge the receipt of data and the operation is aborted.

NACK can be generated by master during a READ operation in following cases:

- The master did not receive valid data due to noise
- The master generates a NACK to abort the READ sequence. After a NACK is issued by the master, nvSRAM slave releases control of the SDA pin and the master is free to generate a Repeated START or STOP condition.

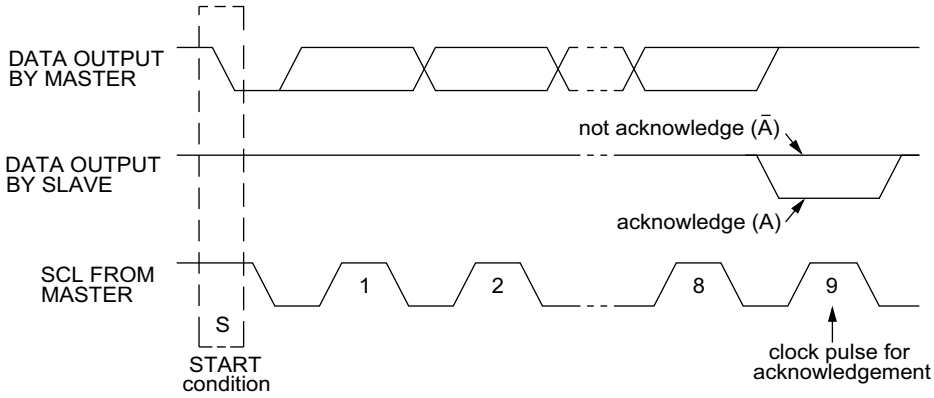
NACK can be generated by nvSRAM slave during a WRITE operation in following cases:

- nvSRAM did not receive valid data due to noise.
- The master tries to access write protected locations on the nvSRAM. Master must restart the communication by generating a STOP or Repeated START condition.

Not Recommended for New Designs

Downloaded from Arrow.com.

Figure 6. Acknowledge on the I²C Bus



High Speed Mode (Hs-mode)

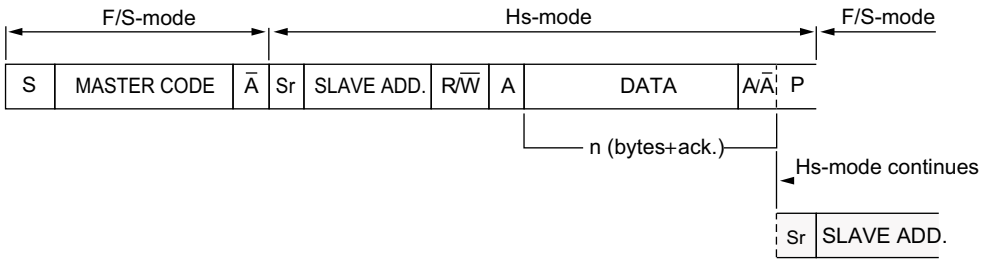
In Hs-mode, nvSRAM can transfer data at bit rates of up to 3.4 Mbit/s. A master code (0000 1XXXb) must be issued to place the device into high speed mode. This enables master/slave communication for speed upto 3.4 MHz. A stop condition exits Hs-mode.

Serial Data Format in Hs-mode

Serial data transfer format in Hs-mode meets the standard-mode I²C-bus specification. Hs-mode can only commence after the following conditions (all of which are in F/S-modes):

1. START condition (S)
2. 8-bit master code (0000 1XXXb)
3. No-acknowledge bit (Ā)

Figure 7. Data transfer format in Hs-mode



Single and multiple-byte reads and writes are supported. After the device enters into Hs-mode, data transfer continues in Hs-mode until stop condition is sent by master device. The slave switches back to F/S-mode after a STOP condition (P). To continue data transfer in Hs-mode, the master sends Repeated START (Sr).

See Figure 13 on page 11 and Figure 16 on page 12 for Hs-mode timings for read and write operation.

Not Recommended for New Designs

Downloaded from Arrow.com.

Slave Device Address

Every slave device on an I^2C bus has a device select address. The first byte after START condition contains the slave device address with which the master intends to communicate. The seven MSBs are the device address and the LSB (R/$\overline{W}$ bit) is used for indicating Read or Write operation. The CY14MX064J reserves two sets of upper 4 MSBs [7:4] in the slave device address field for accessing Memory and Control Registers. The accessing mechanism is described in Memory Slave Device on page 7.

The nvSRAM product provides two different functionalities: Memory and Control Registers functions (such as serial number and product ID). The two functions of the device are accessed through different slave device addresses. The first four most significant bits [7:4] in the device address register are used to select between the nvSRAM functions.

Table 1. Slave device Addressing

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	nvSRAM Function Select
1	0	1	0	Device Select ID			R/$\overline{W}$	Selects Memory
0	0	1	1	Device Select ID			R/$\overline{W}$	Selects Control Registers

CY14MX064J Slave Devices

Memory, 8 K × 8

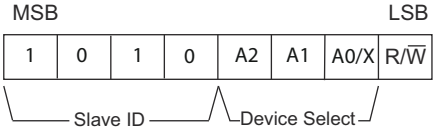
Control Registers
- Memory Control Register, 1 × 8
- Serial Number, 8 × 8
- Device ID, 4 × 8
- Command Register, 1 × 8

Memory Slave Device

The nvSRAM device is selected for Read/Write if the master issues the slave address as 1010b followed by two/three bits of device select. For CY14MX064J1/J3 device select is 3 bits and for CY14MX064J2 it is two bits with third bit don't care. If slave address sent by the master matches with the Memory Slave device address then depending on the R/$\overline{W}$ bit of the slave address, data is either read from (R/$\overline{W}$ = '1') or written to (R/$\overline{W}$ = '0') the nvSRAM.

The address length for CY14MX064J is 13 bits and thus it requires 2 address bytes to map the entire memory address location. The dedicated two address bytes represent bit A0 to A12. However, since the address is only 13-bits, it implies that the first three MSB bits that is fed in is ignored by the device. Although these bits are 'don't care', Cypress recommends that this bit is treated as 0 to enable seamless transition to higher memory densities.

Figure 8. Memory Slave Device Address

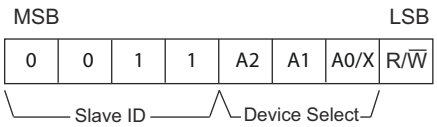


Control Registers Slave Device

The Control Registers Slave device includes the Serial Number, Product ID, Memory Control and Command Register.

The nvSRAM Control Register Slave device is selected for Read/Write if the master issues the Slave address as 0011b followed by two/three bits of device select. For CY14MX064J1/J3 device select is 3 bits and for CY14MX064J2 it is two bits with third bit don't care. If the slave address sent by the master matches with the Memory Slave device address then depending on the R/$\overline{W}$ bit of the slave address, data is either read from (R/$\overline{W}$ = '1') or written to (R/$\overline{W}$ = '0') the nvSRAM.

Figure 9. Control Registers Slave Device Address



Not Recommended for New Designs

Downloaded from Arrow.com.

Table 2. Control Registers map

Address	Description	Read/Write	Details
0x00	Memory Control Register	Read/Write	Contains Block Protect Bits and Serial Number Lock bit
0x01	Serial Number 8 Bytes	Read/Write (Read only when SNL is set)	Programmable Serial Number. Locked by setting the Serial Number lock bit in the Memory Control Register to '1'.
0x02			
0x03			
0x04			
0x05			
0x06			
0x07			
0x08			
0x09	Device ID	Read only	Device ID is factory programmed
0x0A			
0x0B			
0x0C			
0x0D	Reserved	Reserved	Reserved
0xAA	Command Register	Write only	Allows commands for STORE, RECALL, AutoStore Enable/Disable, SLEEP Mode

Memory Control Register

The Memory Control Register contains the following bits:

Table 3. Memory Control Register Bits

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SNL (0)	0	0	BP1 (0)	BP0 (0)	0	0

- **BP1:BP0**: Block Protect bits are used to protect 1/4, 1/2 or full memory array. These bits can be written through a write instruction to the 0x00 location of the Control Register Slave device. However, any STORE cycle causes transfer of SRAM data into a nonvolatile cell regardless of whether or not the block is protected. The default value shipped from the factory for BP0 and BP1 is '0'.

Table 4. Block Protection

Level	BP1:BP0	Block Protection
0	00	None
1/4	01	0x1800–0x1FFF
1/2	10	0x1000–0x1FFF
1	11	0x0000–0x1FFF

SNL (S/N Lock) Bit: Serial Number Lock bit (SNL) is used to lock the serial number. Once the bit is set to '1', the serial number registers are locked and no modification is allowed. This bit cannot be cleared to '0'. The serial number is secured on the next STORE operation (Software STORE or AutoStore). If AutoStore is not enabled, user must perform the Software STORE operation to secure the lock bit status. If a STORE was not performed, the serial number lock bit will not survive the power cycle. The default value shipped from the factory for SNL is '0'.

Command Register

The Command Register resides at address "AA" of the Control Registers Slave device. This is a write only register. The byte written to this register initiates a STORE, RECALL, AutoStore Enable, AutoStore Disable and sleep mode operation as listed in Table 5. Refer to Serial Number on page 16 for details on how to execute a command register byte.

Table 5. Command Register bytes

Data Byte [7:0]	Command	Description
0011 1100	STORE	STORE SRAM data to nonvolatile memory
0110 0000	RECALL	RECALL data from nonvolatile memory to SRAM
0101 1001	ASENB	Enable AutoStore
0001 1001	ASDISB	Disable AutoStore
1011 1001	SLEEP	Enter Sleep Mode for low power consumption

- **STORE**: Initiates nvSRAM Software STORE. The nvSRAM cannot be accessed for t_{STORE} time after this instruction has been executed. When initiated, the device performs a STORE operation regardless of whether a write has been performed since the last NV operation. After the t_{STORE} cycle time is completed, the SRAM is activated again for read/write operations.
- **RECALL**: Initiates nvSRAM Software RECALL. The nvSRAM cannot be accessed for t_{RECALL} time after this instruction has been executed. The RECALL operation does not alter the data in the nonvolatile elements. A RECALL may be initiated in two ways: Hardware RECALL, initiated on power-up; and Software RECALL, initiated by a I^2C RECALL instruction.
- **ASENB**: Enables nvSRAM AutoStore. The nvSRAM cannot be accessed for t_{SS} time after this instruction has been executed. This setting is not nonvolatile and needs to be followed by a manual STORE sequence if this is desired to survive power cycle. The part comes from the factory with AutoStore Enabled and 0x00 written in all cells.
- **ASDISB**: Disables nvSRAM AutoStore. The nvSRAM cannot be accessed for t_{SS} time after this instruction has been executed. This setting is not nonvolatile and needs to be followed by a manual STORE sequence if this is desired to survive the power cycle.

Note If AutoStore is disabled and V_{CAP} is not required, it is required that the V_{CAP} pin is left open. V_{CAP} pin must never be connected to ground. Power-Up RECALL operation cannot be disabled in any case.

- **SLEEP**: SLEEP instruction puts the nvSRAM in a sleep mode. When the SLEEP instruction is registered, the nvSRAM takes t_{SS} time to process the SLEEP request. Once the SLEEP command is successfully registered and processed, the nvSRAM toggles HSB LOW, performs a STORE operation to secure the data to nonvolatile memory and then enters into SLEEP mode. Whenever nvSRAM enters into sleep mode, it initiates non volatile STORE cycle which results in losing an endurance cycle per sleep command execution. A STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle.

Not Recommended for New Designs

Downloaded from Arrow.com.

The nvSRAM enters into sleep mode as follows:

1. The Master sends a START command
2. The Master sends Control Registers Slave device ID with I^2C Write bit set (R/$\overline{W}$ = '0')
3. The Slave (nvSRAM) sends an ACK back to the Master
4. The Master sends Command Register address (0xAA)
5. The Slave (nvSRAM) sends an ACK back to the Master
6. The Master sends Command Register byte for entering into Sleep mode
7. The Slave (nvSRAM) sends an ACK back to the Master
8. The Master generates a STOP condition.

Once in Sleep mode the device starts consuming I_{ZZ} current t_{SLEEP} time after SLEEP instruction is registered. The device is not accessible for normal operations until it is out of sleep mode. The nvSRAM wakes up after t_{WAKE} duration after the device slave address is transmitted by the master.

Transmitting any of the two slave addresses wakes the nvSRAM from Sleep mode. The nvSRAM device is not accessible during t_{SLEEP} and t_{WAKE} interval, and any attempt to access the nvSRAM device by the master is ignored and nvSRAM sends NACK to the master. As an alternative method of determining when the device is ready, the master can send read or write commands and look for an ACK.

Write Protection (WP)

The WP pin is an active high pin and protects entire memory and all registers from write operations. To inhibit all the write operations, this pin must be held high. When this pin is high, all memory and register writes are prohibited and address counter is not incremented. This pin is internally pulled LOW and hence can be left open if not used.

AutoStore Operation

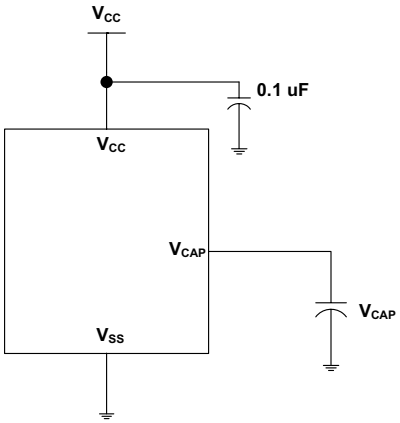
The AutoStore operation is a unique feature of nvSRAM which automatically stores the SRAM data to QuantumTrap cells during power-down. This STORE makes use of an external capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. When the voltage on the V_{CC} pin drops below V_{SWITCH} during power-down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the V_{CAP} capacitor. The AutoStore operation is not initiated if no write cycle has been performed since the last STORE or RECALL.

Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled by issuing the AutoStore Disable instruction specified in Command Register on page 8. If AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This will corrupt the data stored in nvSRAM as well as the serial number and it will unlock the SNL bit.

Figure 10 shows the proper connection of the storage capacitor (V_{CAP}) for AutoStore operation. Refer to DC Electrical Characteristics on page 18 for the size of the V_{CAP}.

Figure 10. AutoStore Mode



Hardware STORE and $\overline{HSB}$ pin Operation

The $\overline{HSB}$ pin in CY14MX064J is used to control and acknowledge STORE operations. If no STORE or RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, device conditionally initiates a STORE operation after t_{DELAY} duration. An actual STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle. Reads and Writes to the memory are inhibited for t_{STORE} duration or as long as $\overline{HSB}$ pin is LOW.

The $\overline{HSB}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

Note For successful last data byte STORE, a hardware STORE should be initiated at least one clock cycle after the last data bit D0 is received.

Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ pin unconnected if not used.

Hardware RECALL (Power-Up)

During power-up, when V_{CC} crosses V_{SWITCH}, an automatic RECALL sequence is initiated which transfers the content of nonvolatile memory on to the SRAM. The data would previously have been stored on the nonvolatile memory through a STORE sequence.

A Power-Up RECALL cycle takes t_{FA} time to complete and the memory access is disabled during this time. $\overline{HSB}$ pin can be used to detect the Ready status of the device.

Not Recommended for New Designs

Downloaded from Arrow.com.

Write Operation

The last bit of the slave device address indicates a read or a write operation. In case of a write operation, the slave device address is followed by the memory or register address and data. A write operation continues as long as a STOP or Repeated START condition is generated by the master or if a NACK is issued by the nvSRAM.

A NACK is issued from the nvSRAM under the following conditions:

1. A valid Device ID is not received.
2. A write (burst write) access to a protected memory block address returns a NACK from nvSRAM after the data byte is received. However, the address counter is set to this address and the following current read operation starts from this address.
3. A write/random read access to an invalid or out-of-bound memory address returns a NACK from the nvSRAM after the address is received. The address counter remains unchanged in such a case.

After a NACK is sent out from the nvSRAM, the write operation is terminated and any data on the SDA line is ignored till a STOP or a Repeated START condition is generated by the master.

For example, consider a case where the burst write access is performed on Control Register Slave address 0x01 for writing the serial number and continued to the address 0x09, which is a read only register. The device returns a NACK and address counter will not be incremented. A following read operation will be started from the address 0x09. Further, any write operation which starts from a write protected address (say, 0x09) will be responded by the nvSRAM with a NACK after the data byte is sent and set the address counter to this address. A following read operation will start from the address 0x09 in this case also.

Note In case the user tries to read/write access an address that does not exist (for example 0x0D in Control Register Slave), nvSRAM responds with a NACK immediately after the out-of-bound address is transmitted. The address counter remains unchanged and holds the previous successful read or write operation address.

A write operation is performed internally with no delay after the eighth bit of data is transmitted. If a write operation is not intended, the master must terminate the write operation before the eighth clock cycle by generating a STOP or Repeated START condition.

More details on write instruction are provided in the section Memory Slave Access on page 10.

Read Operation

If the last bit of the slave device address is ‘1’, a read operation is assumed and the nvSRAM takes control of the SDA line immediately after the slave device address byte is sent out by the master. The read operation starts from the current address location (the location following the previous successful write or read operation). When the last address is reached, the address counter loops back to the first address.

In case of the Control Register Slave, whenever a burst read is performed such that it flows to a non-existent address, the reads operation will loop back to 0x00. This is applicable, in particular for the Command Register.

There are the following ways to end a read operation:

1. The Master issues a NACK on the 9th clock cycle followed by a STOP or a Repeated START condition on the 10th clock cycle.
2. Master generates a STOP or Repeated START condition on the 9th clock cycle.

More details on write instruction are provided in the section Memory Slave Access on page 10.

Memory Slave Access

The following sections describe the data transfer sequence required to perform Read or Write operations from nvSRAM.

Write nvSRAM

Each write operation consists of a slave address being transmitted after the start condition. The last bit of slave address must be set as ‘0’ to indicate a Write operation. The master may write one byte of data or continue writing multiple consecutive address locations while the internal address counter keeps incrementing automatically. The address register is reset to 0x0000 after the last address in memory is accessed. The write operation continues till a STOP or Repeated START condition is generated by the master or a NACK is issued by the nvSRAM.

A write operation is executed only after all the 8 data bits have been received by the nvSRAM. The nvSRAM sends an ACK signal after a successful write operation. A write operation may be terminated by the master by generating a STOP condition or a Repeated START operation. If the master desires to abort the current write operation without altering the memory contents, this should be done using a START/STOP condition prior to the 8th data bit.

If the master tries to access a write protected memory address on the nvSRAM, a NACK is returned after the data byte intended to write the protected address is transmitted and address counter will not be incremented. Similarly, in a burst mode write operation, a NACK is returned when the data byte that attempts to write a protected memory location and address counter will not be incremented.

Not Recommended for New Designs

Downloaded from Arrow.com.

Figure 11. Single-Byte Write into nvSRAM (except Hs-mode)

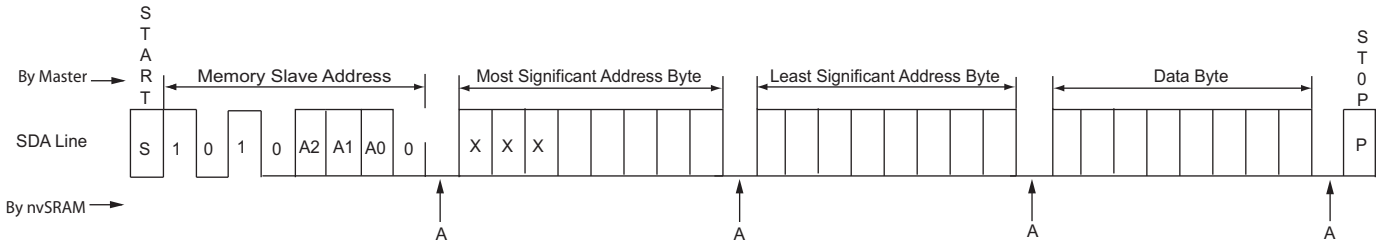


Figure 12. Multi-Byte Write into nvSRAM (except Hs-mode)

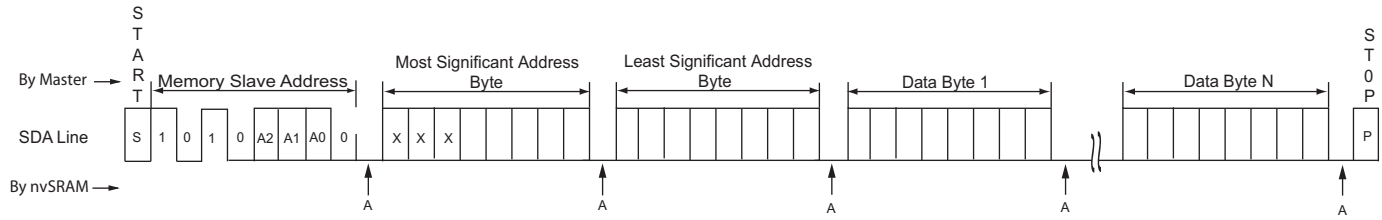


Figure 13. Single-Byte Write into nvSRAM (Hs-mode)

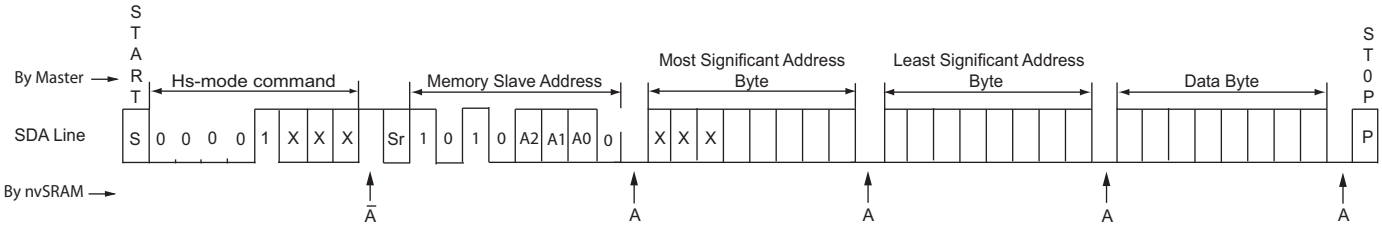
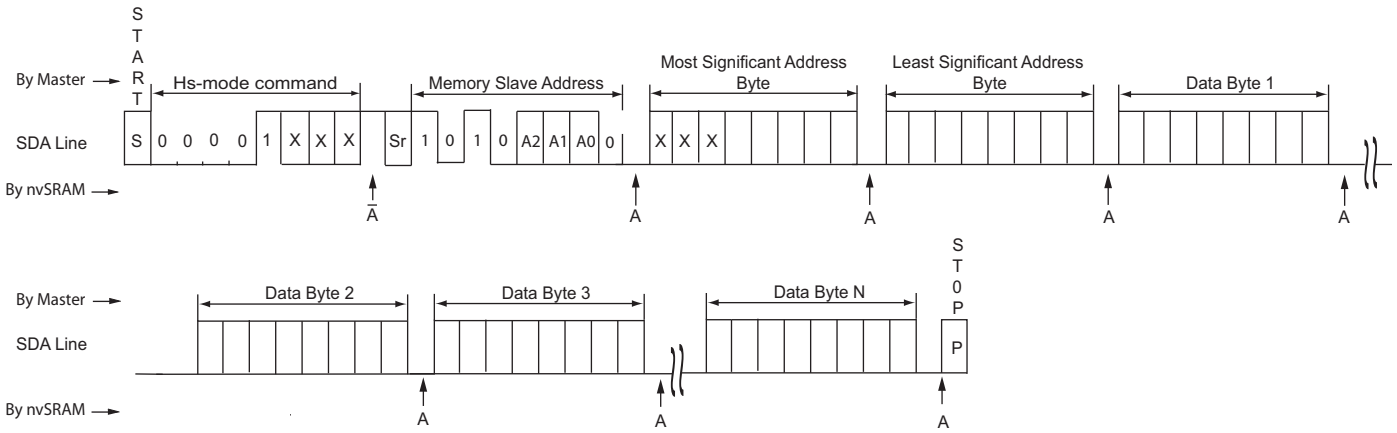


Figure 14. Multi-Byte Write into nvSRAM (Hs-mode)



Not Recommended for New Designs

Downloaded from Arrow.com.

Current nvSRAM Read

Each read operation starts with the master transmitting the nvSRAM slave address with the LSB set to '1' to indicate "Read". The reads start from the address on the address counter. The address counter is set to the address location next to the last accessed with a "Write" or "Read" operation. The master may terminate a read operation after reading 1 byte or continue reading addresses sequentially till the last address in the memory after which the address counter rolls back to the address 0x0000. The valid methods of terminating read access are described in Section Read Operation on page 10.

Figure 15. Current Location Single-Byte nvSRAM Read (except Hs-mode)

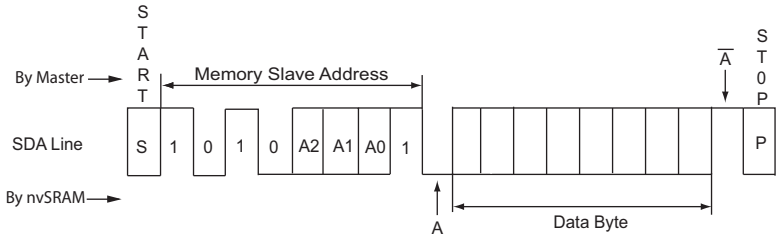


Figure 16. Current Location Multi-Byte nvSRAM Read (except Hs-mode)

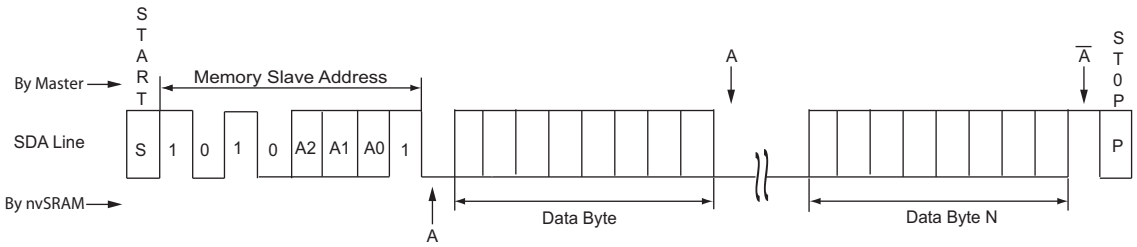


Figure 17. Current Location Single-Byte nvSRAM Read (Hs-mode)

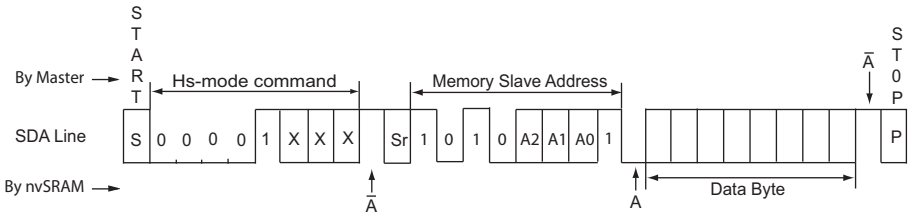
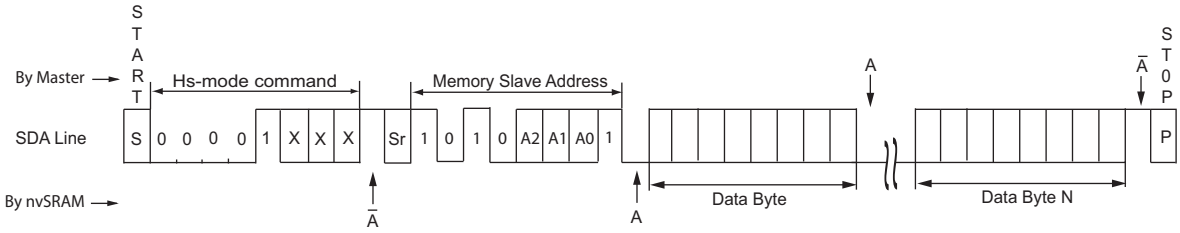


Figure 18. Current Location Multi-Byte nvSRAM Read (Hs-mode)



Not Recommended for New Designs

Downloaded from Arrow.com.

Random Address Read

A random address read is performed by first initiating a write operation and generating a Repeated START immediately after the last address byte is acknowledged. The address counter is set to this address and the next read access to this slave will initiate read operation from here. The master may terminate a read operation after reading 1 byte or continue reading addresses sequentially till the last address in the memory after which the address counter rolls back to the start address 0x0000.

Figure 19. Random Address Single-Byte Read (except Hs-mode)

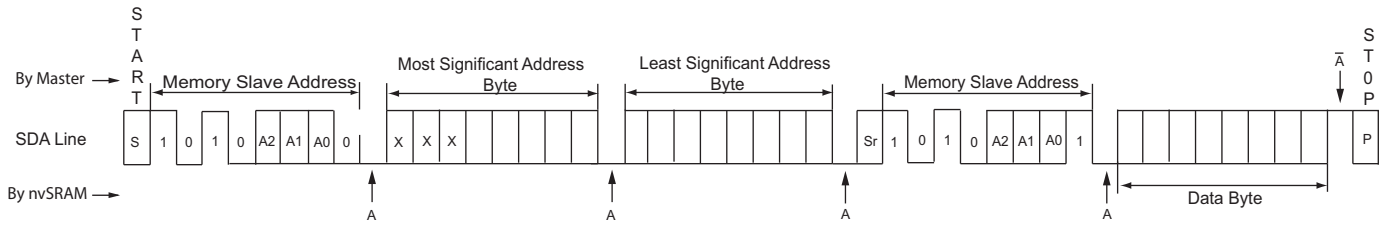


Figure 20. Random Address Multi-Byte Read (except Hs-mode)

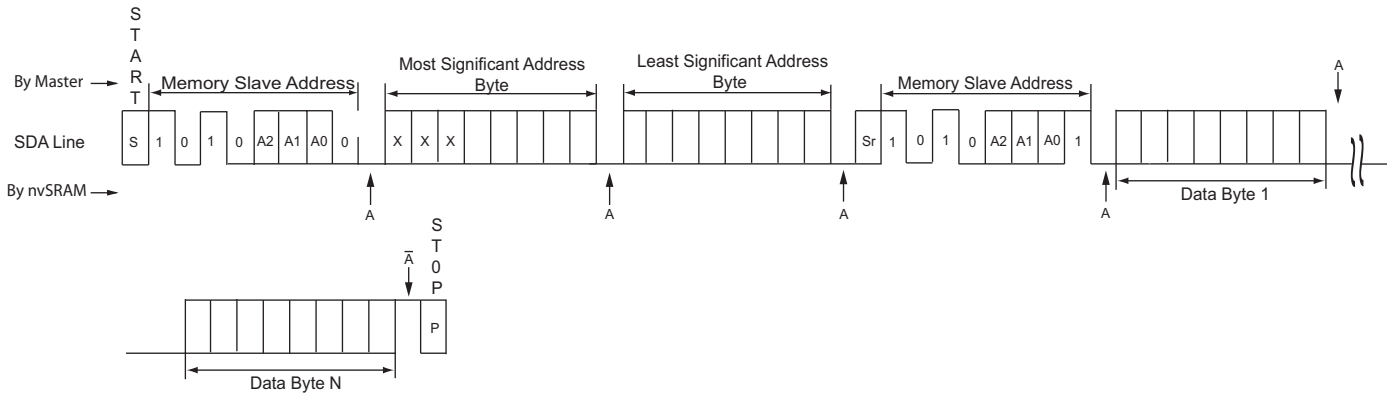
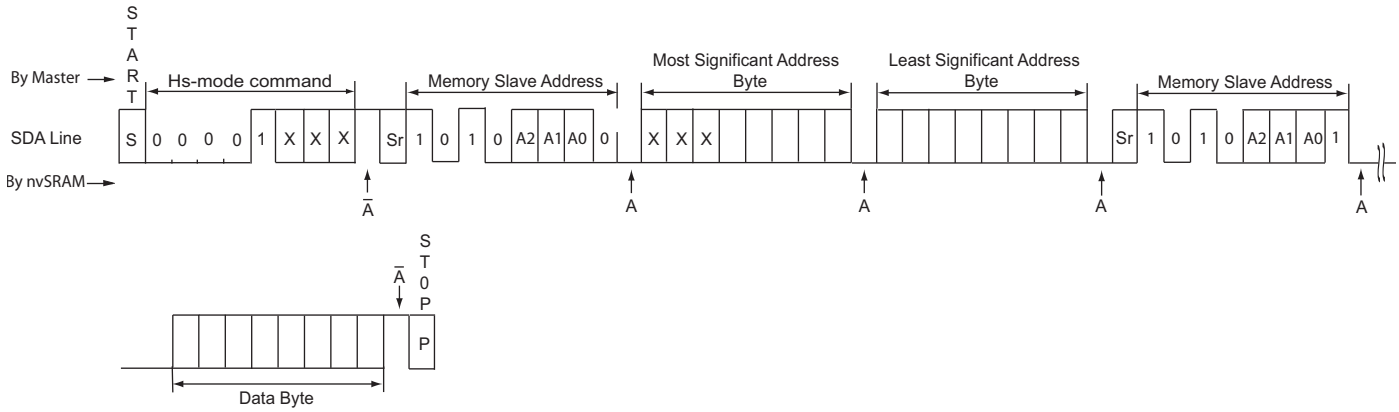


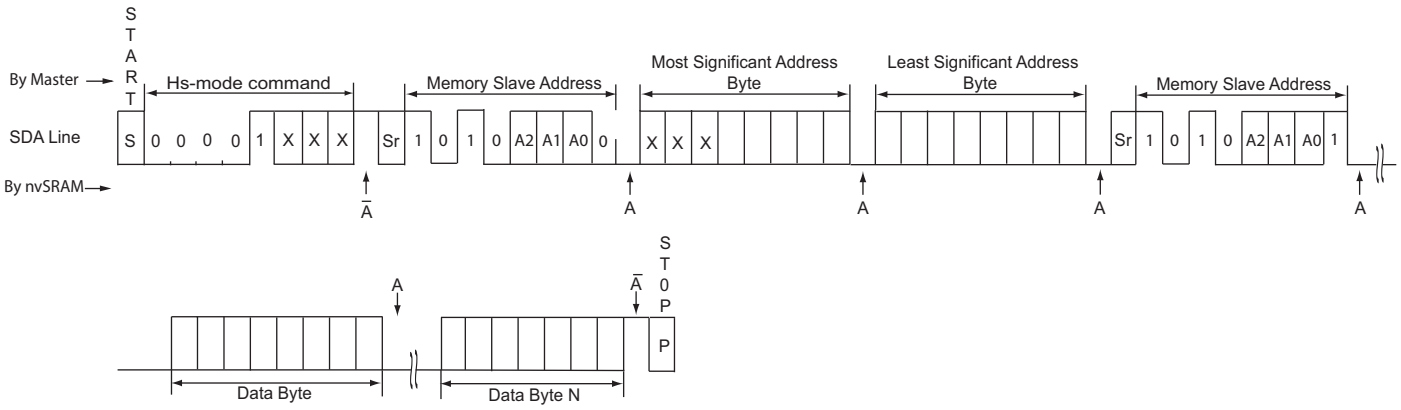
Figure 21. Random Address Single-Byte Read (Hs-mode)



Not Recommended for New Designs

Downloaded from Arrow.com.

Figure 22. Random Address Multi-Byte Read (Hs-mode)



Control Registers Slave

The following sections describes the data transfer sequence required to perform Read or Write operations from Control Registers Slave.

Write Control Registers

To write the Control Registers Slave, the master transmits the Control Registers Slave address after generating the START condition. The write sequence continues from the address location specified by the master till the master generates a STOP condition or the last writable address location.

If a non writable address location is accessed for write operation during a normal write or a burst, the slave generates a NACK after the data byte is sent and the write sequence terminates. Any following data bytes are ignored and the address counter is not incremented.

If a write operation is performed on the Command Register (0xAA), the following current read operation also begins from the first address (0x00) as in this case, the current address is an out-of-bound address. The address is not incremented and the next current read operation begins from this address location. If a write operation is attempted on an out-of-bound address location, the nvSRAM sends a NACK immediately after the address byte is sent.

Further, if the serial number is locked, only two addresses (0xAA or Command Register, and 0x00 or Memory Control Register) are writable in the Control Registers Slave. On a write operation to any other address location, the device will acknowledge command byte and address bytes but it returns a NACK from the Control Registers Slave for data bytes. In this case, the address will not be incremented and a current read will happen from the last acknowledged address.

The nvSRAM Control Registers Slave sends a NACK when an out of bound memory address is accessed for write operation, by the master. In such a case, a following current read operation begins from the last acknowledged address.

Figure 23. Single-Byte Write into Control Registers

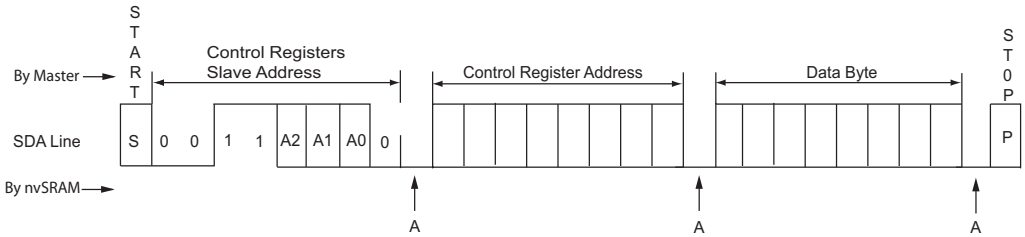
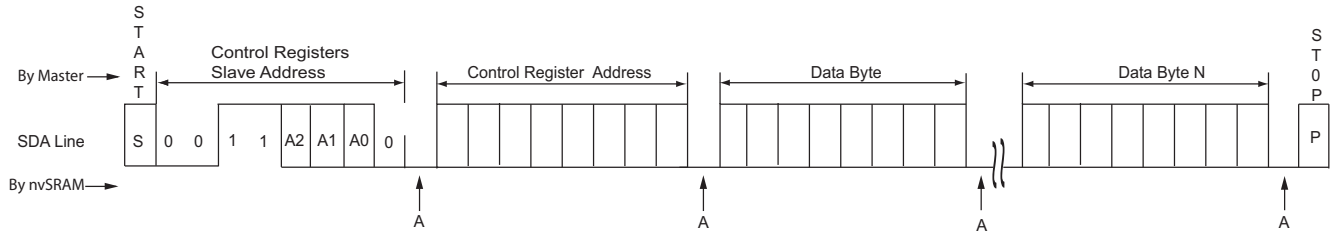


Figure 24. Multi-Byte Write into Control Registers



Not Recommended for New Designs

Downloaded from Arrow.com.

Current Control Registers Read

A read of Control Registers Slave is started with master sending the Control Registers Slave address after the START condition with the LSB set to '1'. The reads begin from the current address which is the next address to the last accessed location. The reads to Control Registers Slave continues till the last readable address location and loops back to the first location (0x00). Note that the Command Register is a write only register and is not accessible through the sequential read operations. If a burst read operation begins from the Command Register (0xAA), the address counter wraps around to the first address in the register map (0x00).

Figure 25. Control Registers Single-Byte Read

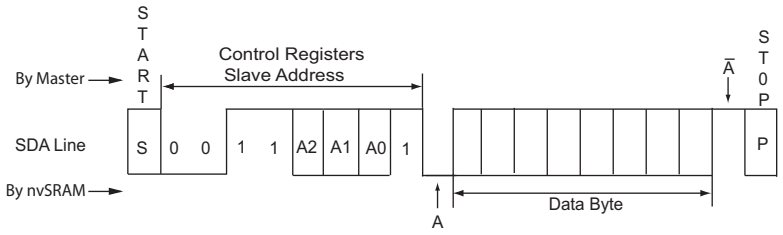
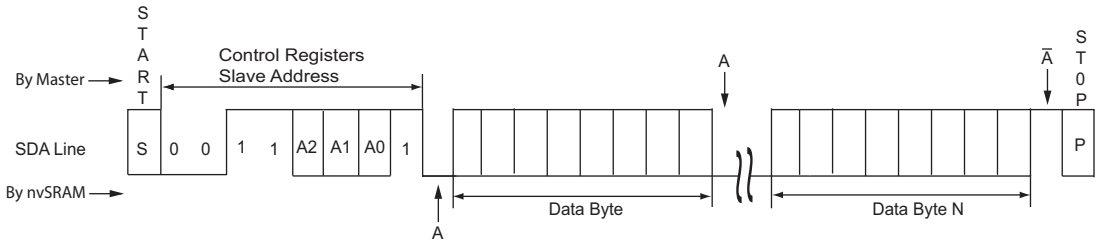


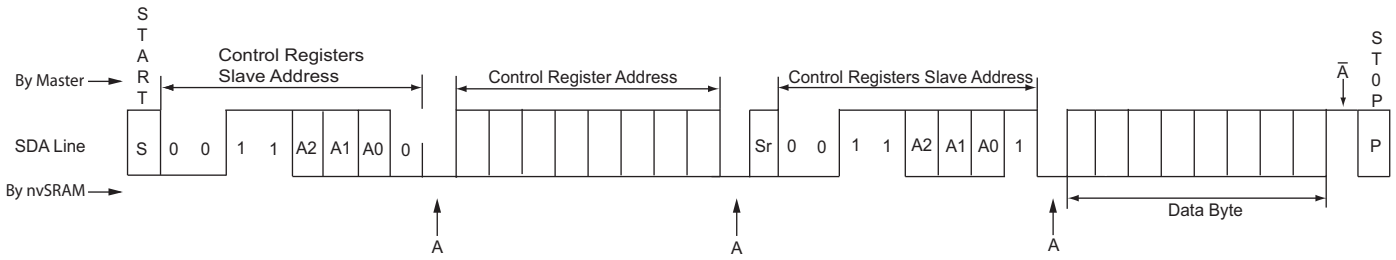
Figure 26. Current Control Registers Multi-Byte Read



Random Control Registers Read

A read of random address may be performed by initiating a write operation to the intended location of read and immediately following with a Repeated START operation. The reads to Control Registers Slave continues till the last readable address location and loops back to the first location (0x00). Note that the Command Register is a write only register and is not accessible through the sequential read operations. A random read starting at the Command Register (0xAA) loops back to the first address in the Control Registers map (0x00). If a random read operation is initiated from an out-of-bound memory address, the nvSRAM sends a NACK after the address byte is sent.

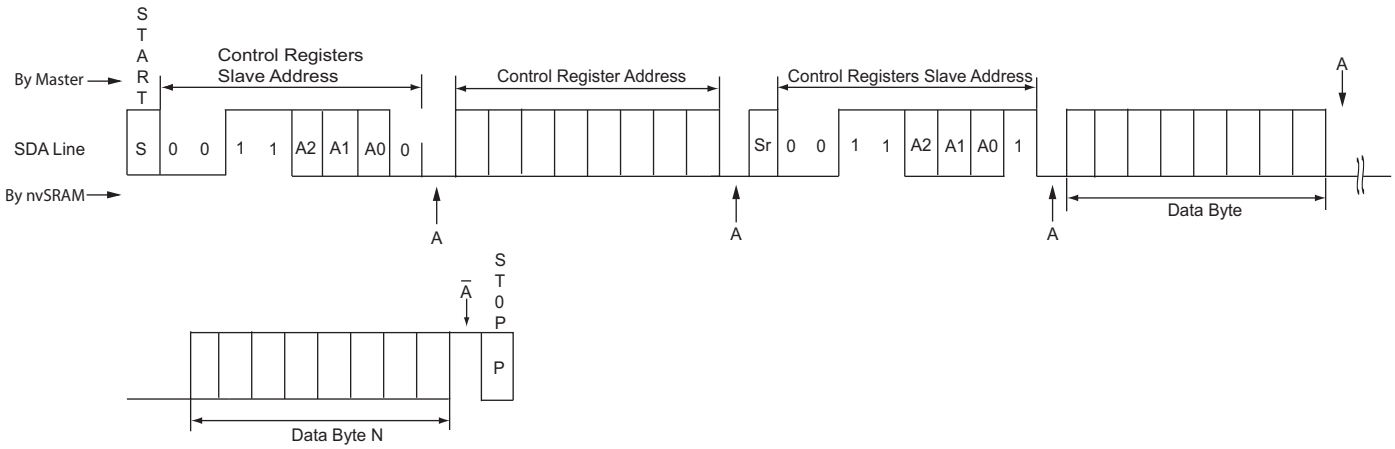
Figure 27. Random Control Registers Single-Byte Read



Not Recommended for New Designs

Downloaded from Arrow.com.

Figure 28. Random Control Registers Multi-Byte Read



Serial Number

Serial number is an 8 byte memory space provided to the user to uniquely identify this device. It typically consists of a two byte customer ID, followed by five bytes of unique serial number and one byte of CRC check. However, nvSRAM does not calculate the CRC and it is up to the user to utilize the eight byte memory space in the desired format. The default values for the eight byte locations are set to ‘0x00’.

Serial Number Write

The serial number can be accessed through the Control Registers Slave Device. To write the serial number, master transmits the Control Registers Slave address after the START condition and writes to the address location from 0x01 to 0x08. The content of Serial Number registers is secured to nonvolatile memory on the next STORE operation. If AutoStore is enabled, nvSRAM automatically stores the Serial number in the nonvolatile memory on power-down. However, if AutoStore is disabled, user must perform a STORE operation to secure the contents of Serial Number registers.

Note If the serial number lock (SNL) bit is not set, the serial number registers can be re-written regardless of whether or not a STORE has happened. Once the serial number lock bit is set, no writes to the serial number registers are allowed. If the master tries to perform a write operation to the serial number registers when the lock bit is set, a NACK is returned and write will not be performed.

Serial Number Lock

After writes to Serial Number registers is complete, master is responsible for locking the serial number by setting the serial number lock bit to ‘1’ in the Memory Control Register (0x00). The content of Memory Control Register and serial number are secured on the next STORE operation (STORE or AutoStore). If AutoStore is not enabled, user must perform STORE operation to secure the lock bit status.

If a STORE was not performed, the serial number lock bit will not survive power cycle. The serial number lock bit and 8-byte serial number is defaults to ‘0’ at power-up.

Serial Number Read

Serial number can be read back by a read operation of the intended address of the Control Registers Slave. The Control Registers Device loops back from the last address (excluding the Command Register) to 0x00 address location while performing burst read operation. The serial number resides in the locations from 0x01 to 0x08. Even if the serial number is not locked, a serial number read operation will return the current values written to the serial number registers. Master may perform a serial number read operation to confirm if the correct serial number is written to the registers before setting the lock bit.

Not Recommended for New Designs

Downloaded from Arrow.com.

Device ID

Device ID is a 4 byte code consisting of JEDEC assigned manufacturer ID, product ID, density ID, and die revision. These registers are set in factory and are read only registers for the user.

Table 6. Device ID

Device	Device ID (4 bytes)	Device ID Description			
		31–21 (11 bits)	20–7 (14 bits)	6–3 (4 bits)	2–0 (3 bits)
		Manufacture ID	Product ID	Density ID	Die Rev
CY14MB064J1	0x06812888	00000110100	00001001010001	0001	000
CY14MB064J2	0x0681A888	00000110100	00001101010001	0001	000
CY14MB064J3	0x0681AA88	00000110100	00001101010101	0001	000
CY14ME064J1	0x06813088	00000110100	00001001100001	0001	000
CY14ME064J2	0x0681B088	00000110100	00001101100001	0001	000
CY14ME064J3	0x0681B288	00000110100	00001101100101	0001	000

The device ID is divided into four parts as shown in Table 6:

1. Manufacturer ID (11 bits)

This is the JEDEC assigned manufacturer ID for Cypress. JEDEC assigns the manufacturer ID in different banks. The first three bits of the manufacturer ID represent the bank in which ID is assigned. The next eight bits represent the manufacturer ID.

Cypress manufacturer ID is 0x34 in bank 0. Therefore the manufacturer ID for all Cypress nvSRAM products is given as:

Cypress ID - 000_0011_0100

2. Product ID (14 bits)

The product ID for device is shown in the Table 6.

3. Density ID (4 bits)

The 4-bit density ID is used as shown in Table 6 for indicating the 64-Kb density of the product.

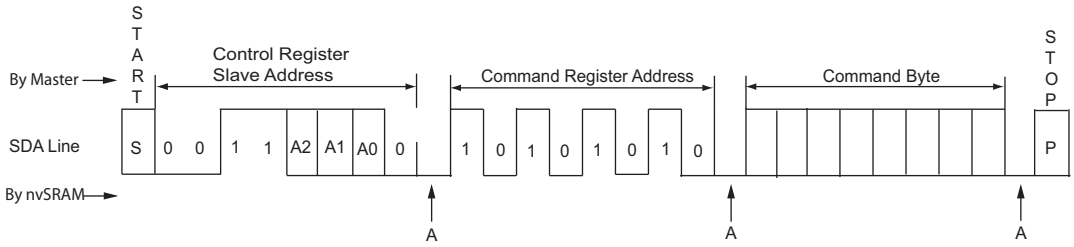
4. Die Rev (3 bits)

This is used to represent any major change in the design of the product. The initial setting of this is always 0x0.

Executing Commands Using Command Register

The Control Registers Slave allows different commands to be executed by writing the specific command byte in the Command Register (0xAA). The command byte codes for each command are specified in Table 5 on page 8. During the execution of these commands the device is not accessible and returns a NACK if any of the three slave devices is selected. If an invalid command is sent by the master, the nvSRAM responds with an ACK indicating that the command has been acknowledged with NOP (No Operation). The address will rollover to 0x00 location.

Figure 29. Command Execution using Command Register



Not Recommended for New Designs

Downloaded from Arrow.com.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS}

CY14MB064J: .....–0.5 V to +4.1 V

CY14ME064J: .....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z state .....–0.5 V to V_{CC} + 0.5 V

Input voltage .....–0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential .....–2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1 s duration). ... 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 140 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}
CY14MB064J	Industrial	–40 °C to +85 °C	2.7 V to 3.6 V
CY14ME064J			4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [4]	Max	Unit
V_{CC}	Power supply		CY14MB064J	2.7	3.0	3.6	V
			CY14ME064J	4.5	5.0	5.5	V
I_{CC1}	Average V_{CC} current	f_{SCL} = 3.4 MHz; Values obtained without output loads (I_{OUT} = 0 mA)		–	–	1	mA
		f_{SCL} = 1 MHz; Values obtained without output loads (I_{OUT} = 0 mA)	CY14MB064J	–	–	400	µA
			CY14ME064J	–	–	450	µA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}		–	–	3	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	3	mA
I_{SB}	V_{CC} standby current	SCL ≥ (V_{CC} – 0.2 V). V_{IN} ≤ 0.2 V or ≥ (V_{CC} – 0.2 V). Standby current level after nonvolatile cycle is complete. Inputs are static. f_{SCL} = 0 MHz.		–	–	150	µA
I_{ZZ}	Sleep mode current	t_{SLEEP} time after SLEEP Instruction is Issued. All inputs are static and configured at CMOS logic level.		–	–	8	µA
I_{IX} [5]	Input current in each I/O pin (except HSB)	0.1 V_{CC} < V_i < 0.9 $V_{CC(max)}$		–1	–	+1	µA
	Input current in each I/O pin (for HSB)			–100	–	+1	µA
I_{OZ}	Output leakage current			–1	–	+1	µA
C_i	Capacitance for each I/O pin	Capacitance measured across all input and output signal pin and V_{SS}.		–	–	7	pF

Note

4. Typical values are at 25 °C, V_{CC} = $V_{CC(typ)}$. Not 100% tested.
5. Not applicable to WP, A2, A1 and A0 pins.

Not Recommended for New Designs

Downloaded from Arrow.com.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [4]	Max	Unit
V_{IH}	Input HIGH voltage			0.7 × Vcc	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage			– 0.5	–	0.3 × Vcc	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		0	–	0.4	V
		I_{OL} = 6 mA		0	–	0.6	V
R_{in} [6]	Input resistance (WP, A2, A1, A0)	For $V_{IN} = V_{IL\ (max)}$		50	–	–	kΩ
		For $V_{IN} = V_{IH\ (min)}$		1	–	–	MΩ
V_{hys}	Hysteresis of Schmitt trigger inputs			0.05 × V_{CC}	–	–	V
V_{CAP} [7]	Storage capacitor	Between V_{CAP} pin and V_{SS}		42	47	180	µF
V_{VCAP} [8, 9]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = Max	CY14MB064J	–	–	V_{CC}	V
			CY14ME064J	–	–	V_{CC}– 0.5	

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

Thermal Resistance

Parameter [9]	Description	Test Conditions	8-pin SOIC	16-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	101.08	56.68	°C/W
Θ_{JC}	Thermal resistance (junction to case)		37.86	32.11	°C/W

Notes

6. The input pull-down circuit is stronger (50 KΩ) when the input voltage is below V_{IL} and weak (1 MΩ) when the input voltage is above V_{IH}.
7. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on V_{CAP} options.
8. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
9. These parameters are guaranteed by design and are not tested.

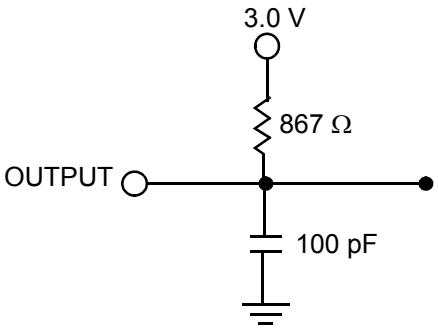
Not Recommended for New Designs

Downloaded from Arrow.com.

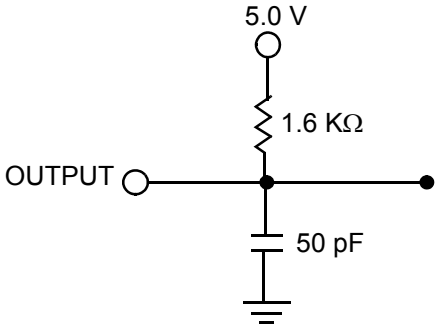
AC Test Loads and Waveforms

Figure 30. AC Test Loads and Waveforms

For 3.0 V (CY14MB064J)



For 5.0 V (CY14ME064J)



AC Test Conditions

Description	CY14MB064J	CY14ME064J
Input pulse levels	0 V to 3 V	0 V to 5 V
Input rise and fall times (10%–90%)	10 ns	10 ns
Input and output timing reference levels	1.5 V	2.5 V

Not Recommended for New Designs

Downloaded from Arrow.com.

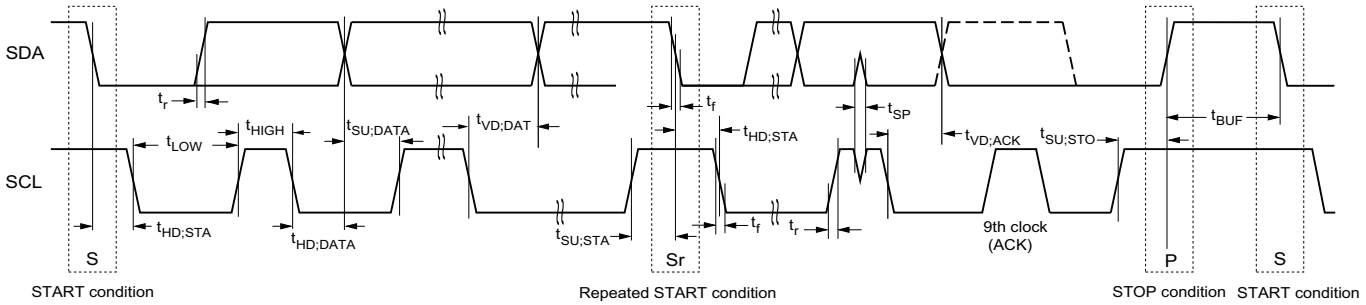
AC Switching Characteristics

Over the Operating Range

Parameter[10]	Description	3.4 MHz [11]		1 MHz [11]		400 kHz [11]		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL	–	3400	–	1000	–	400	kHz
$t_{SU;\ STA}$	Setup time for Repeated START condition	160	–	250	–	600	–	ns
$t_{HD;STA}$	Hold time for START condition	160	–	250	–	600	–	ns
t_{LOW}	LOW period of the SCL	160	–	500	–	1300	–	ns
t_{HIGH}	HIGH period of the SCL	60	–	260	–	600	–	ns
$t_{SU;DATA}$	Data in setup time	10	–	100	–	100	–	ns
$t_{HD;DATA}$	Data hold time (In/Out)	0	–	0	–	0	–	ns
t_{DH}	Data out hold time	0	–	0	–	0	–	ns
t_r[12]	Rise time of SDA and SCL	–	80	–	120	–	300	ns
t_f[12]	Fall time of SDA and SCL	–	80	–	120	–	300	ns
$t_{SU;STO}$	Setup time for STOP condition	160	–	250	–	600	–	ns
$t_{VD;DATA}$	Data output valid time	–	130	–	400	–	900	ns
$t_{VD;ACK}$	ACK output valid time	–	130	–	400	–	900	ns
t_{OF}[12]	Output fall time from V_{IH} min to V_{IL} max	–	80	–	120	–	250	ns
t_{BUF}	Bus free time between STOP and next START condition	0.3	–	0.5	–	1.3	–	µs
t_{SP}	Pulse width of spikes that must be suppressed by input filter	–	10	–	50	–	50	ns

Switching Waveforms

Figure 31. Timing Diagram



Notes
10. Test conditions assume signal transition time of 10 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL} and load capacitance shown in Figure 30 on page 20.
11. Bus Load (Cb) considerations; Cb < 500 pF for I^2C clock frequency (SCL) 100/400 KHz; Cb < 550 pF for SCL at 1000 kHz; Cb < 100 pF for SCL at 3.4 MHz.
12. These parameters are guaranteed by design and are not tested.

Not Recommended for New Designs

Downloaded from Arrow.com.

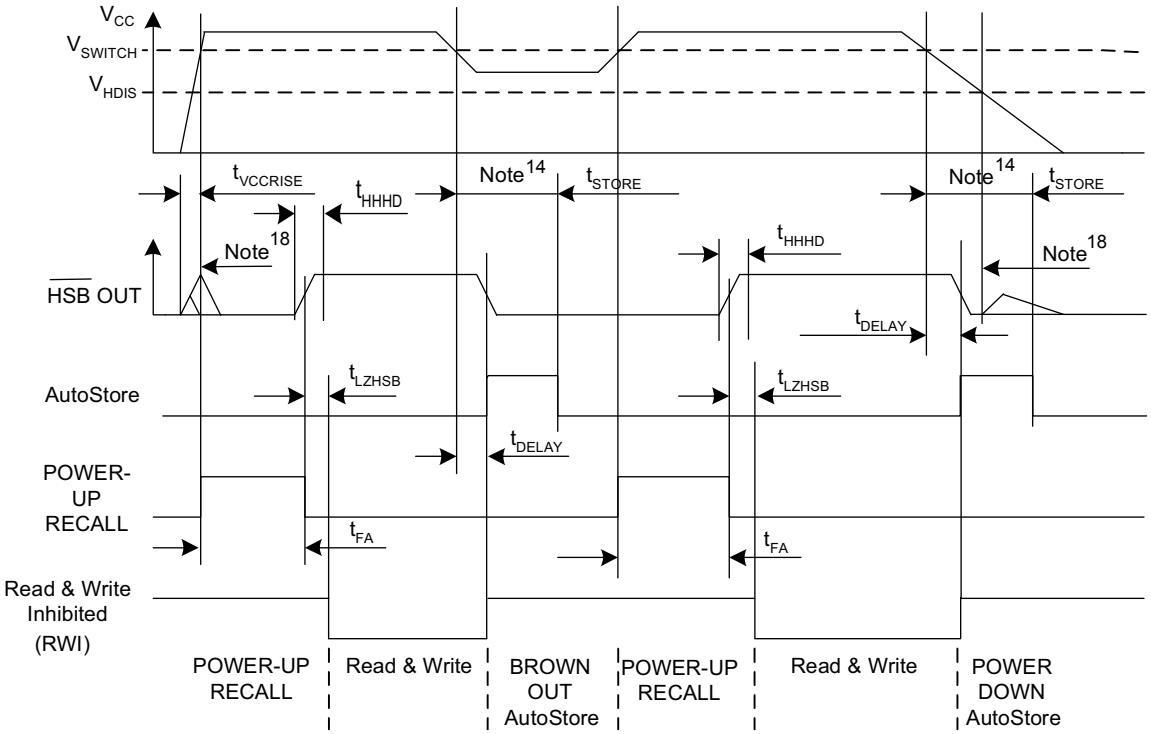
nvSRAM Specifications

Over the Operating Range

Parameters	Description		Min	Max	Unit
t_{FA} [13]	Power-Up RECALL duration		–	20	ms
t_{STORE} [14]	STORE cycle duration		–	8	ms
t_{DELAY} [15]	Time allowed to complete SRAM write cycle		–	25	ns
$t_{VCCRISE}$ [16]	V_{CC} rise time		150	–	µs
V_{SWITCH}	Low voltage trigger level	CY14MB064J	–	2.65	V
		CY14ME064J	–	4.40	V
t_{LZHSB} [16]	$\overline{HSB}$ high to nvSRAM active time		–	5	µs
V_{HDIS} [16]	$\overline{HSB}$ output disable voltage		–	1.9	V
t_{HHHD} [16]	$\overline{HSB}$ HIGH active time		–	500	ns
t_{WAKE}	Time for nvSRAM to wake up from SLEEP mode		–	20	ms
t_{SLEEP}	Time to enter low power mode after issuing SLEEP instruction		–	8	ms
t_{SB} [16]	Time to enter into standby mode after issuing STOP condition		–	100	µs

Switching Waveforms

Figure 32. AutoStore or Power-Up RECALL [17]



Notes
13. t_{FA} starts from the time V_{CC} rises above V_{SWITCH}.
14. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
15. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
16. These parameters are guaranteed by design and are not tested.
17. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
18. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Not Recommended for New Designs

Downloaded from Arrow.com.

Software Controlled STORE/RECALL Cycles

Over the Operating Range

Parameter	Description	CY14MX064J		Unit
		Min	Max	
t_{RECALL}	RECALL duration	–	600	µs
t_{SS}[19, 20]	Software sequence processing time	–	500	µs

Switching Waveforms

Figure 33. Software STORE/RECALL Cycle

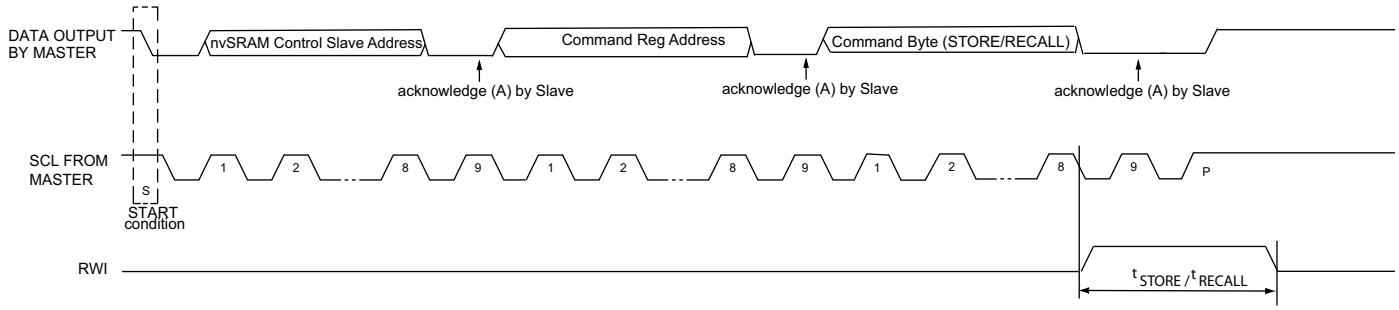
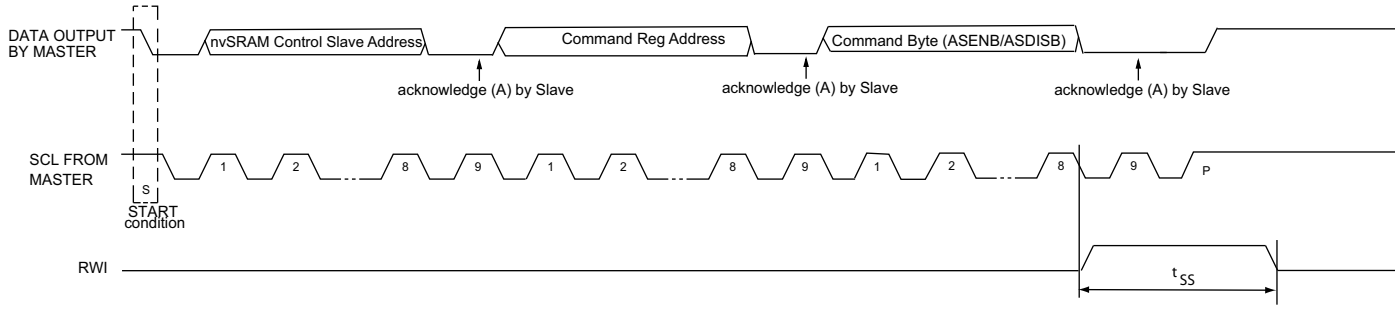


Figure 34. AutoStore Enable/Disable Cycle



Not Recommended for New Designs

Notes
19. This is the amount of time it takes to take action on a soft sequence command. V_{CC} power must remain HIGH to effectively register command.
20. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

Downloaded from Arrow.com.

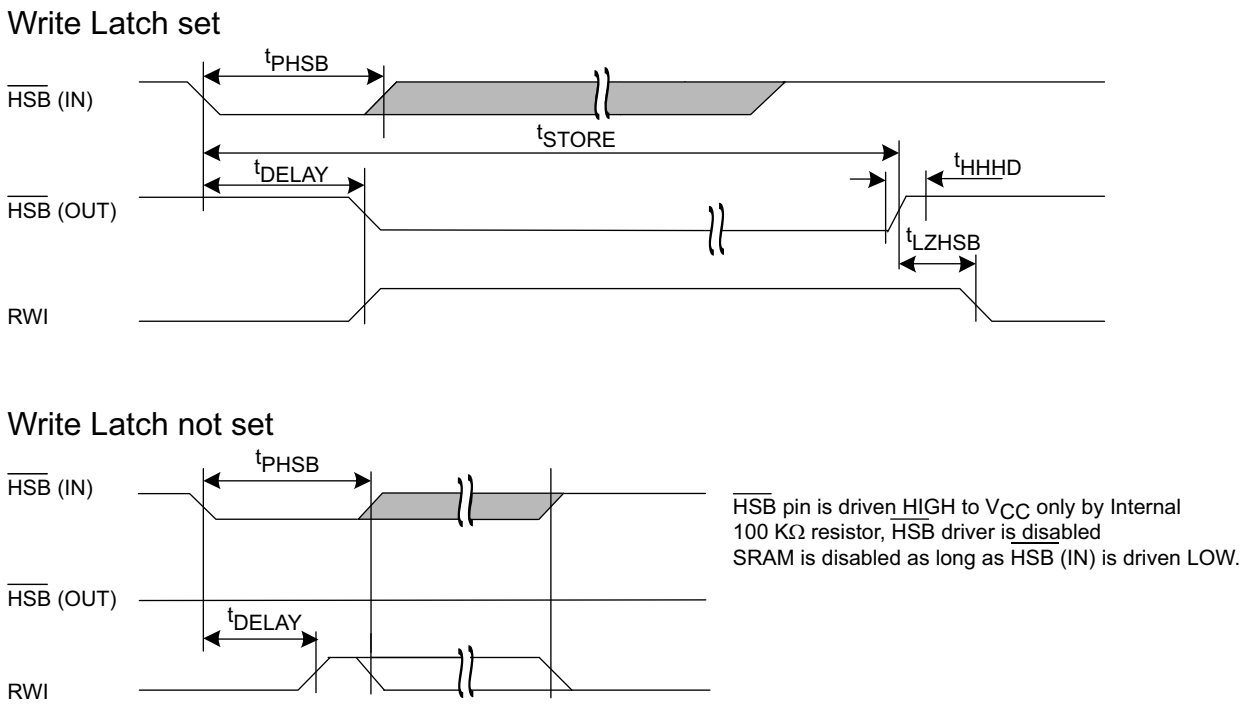
Hardware STORE Cycle

Over the Operating Range

Parameter	Description	CY14MX064J		Unit
		Min	Max	
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Switching Waveforms

Figure 35. Hardware STORE Cycle [21]



Not Recommended for New Designs

Note
21. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware STORE is not initiated.

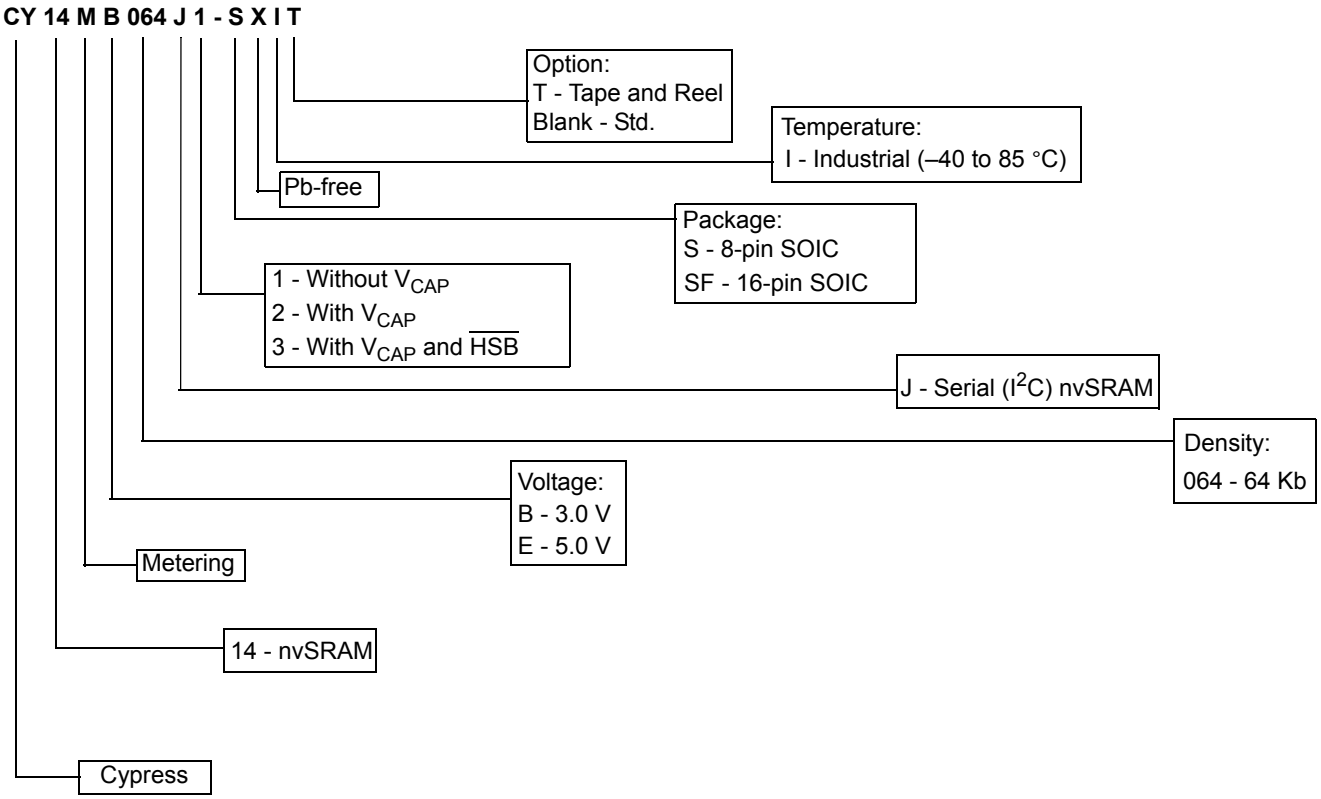
Downloaded from Arrow.com.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14MB064J1-SXIT	51-85066	8-pin SOIC (without V_{CAP})	Industrial
CY14MB064J1-SXI		8-pin SOIC (without V_{CAP})	
CY14MB064J2-SXIT		8-pin SOIC (with V_{CAP})	
CY14MB064J2-SXI		8-pin SOIC (with V_{CAP})	
CY14ME064J1-SXIT		8-pin SOIC (without V_{CAP})	
CY14ME064J1-SXI		8-pin SOIC (without V_{CAP})	
CY14ME064J2-SXIT		8-pin SOIC (with V_{CAP})	
CY14ME064J2-SXI		8-pin SOIC (with V_{CAP})	

All these parts are Pb-free. This table contains Final information. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

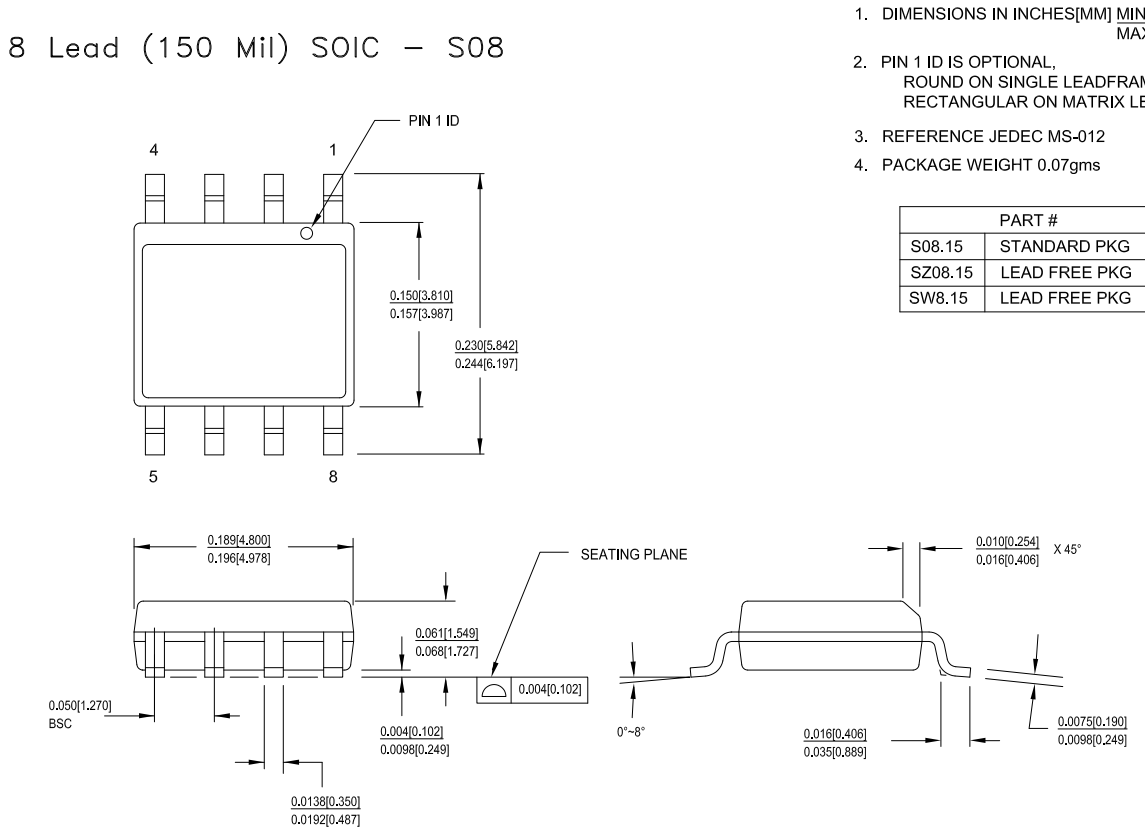


Not Recommended for New Designs

Downloaded from Arrow.com.

Package Diagrams

Figure 36. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

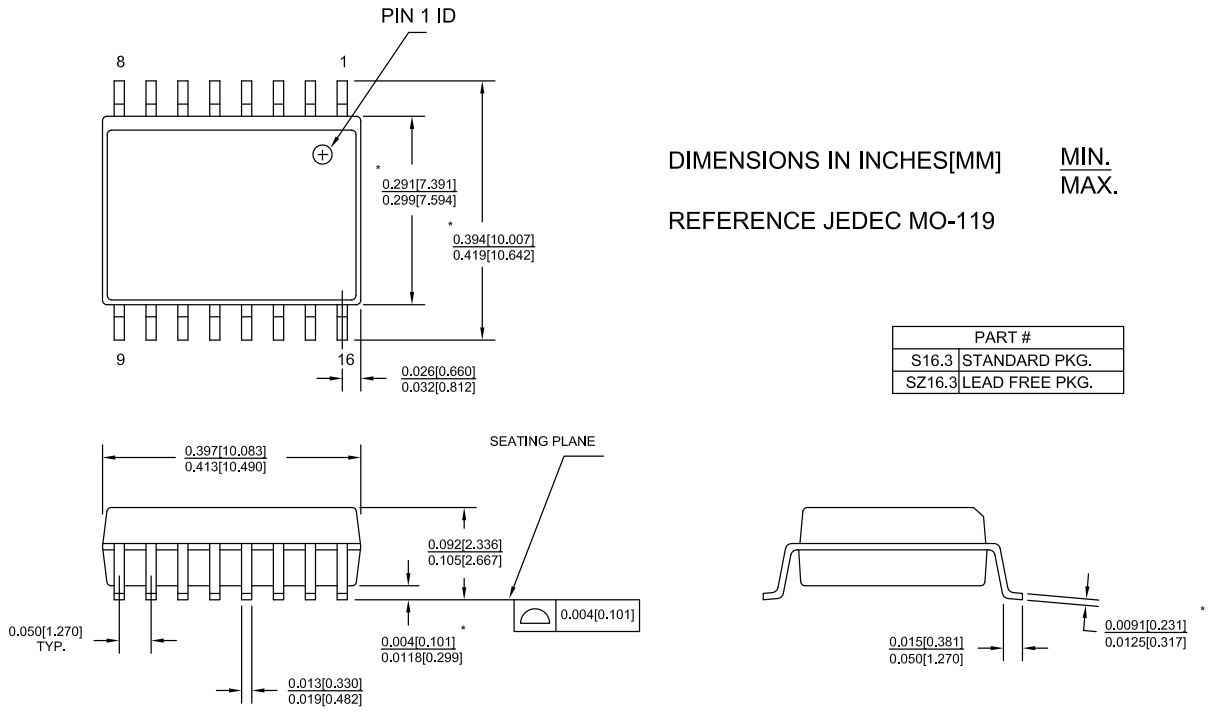
51-85066 *F

Not Recommended for New Designs

Downloaded from Arrow.com.

Package Diagrams (continued)

Figure 37. 16-pin SOIC (0.413 × 0.299 × 0.0932 Inches) Package Outline, 51-85022



Not Recommended for New Designs

Downloaded from Arrow.com.

Acronyms

Acronym	Description
ACK	Acknowledge
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
EIA	Electronic Industries Alliance
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
nvSRAM	Non-volatile Static Random Access Memory
NACK	No Acknowledge
RoHS	Restriction of Hazardous Substances
R/$\overline{W}$	Read/Write
RWI	Read and Write Inhibit
SCL	Serial Clock Line
SDA	Serial Data Access
SNL	Serial Number Lock
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
WP	Write Protect

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Not Recommended for New Designs

Downloaded from Arrow.com.

Document History Page

Document Title: CY14MB064J, CY14ME064J, 64-Kbit (8 K × 8) Serial (I^2C) nvSRAM Document Number: 001-65051				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3088565	11/17/2010	GVCH	New datasheet
*A	3201457	03/17/2011	GVCH	Updated Configuration (Added Slave Address information). Updated Pin Definitions (Added Note 3). Updated AutoStore Operation (description). Updated Hardware STORE and HSB pin Operation. (Added more clarity on HSB pin operation). Updated Table 6 (Product ID column). Updated DC Electrical Characteristics (Added Note 5). Updated nvSRAM Specifications (description of t_{LZHSB} parameter). Fixed typo error in Figure 32. Updated Ordering Code Definitions Updated in new template.
*B	3248609	05/06/2011	GVCH	Datasheet status changed from “Preliminary to “Final” Updated Ordering Information
*C	3400749	10/10/2011	GVCH	Updated Pin Definitions (SDA pin description). Updated Command Register (SLEEP description on page 8). Updated Device ID (Added device ID (4 bytes) column in Table 6). Updated Executing Commands Using Command Register (description). Updated DC Electrical Characteristics (Added I_{CC1} parameter value of 400 µA for 1 MHz frequency, changed maximum value of I_{CC2} parameter from 2 mA to 3 mA, removed I_{CC3} parameter, added Note 7 and referred the note in the V_{CAP} parameter). Updated AC Switching Characteristics (Added Note 10 and referred the note in the Parameter column, and updated maximum value of t_{SP} parameter from 5 ns to 10 ns for 3.4 MHz). Updated Software Controlled STORE/RECALL Cycles (Updated Figure 33 and Figure 34). Updated Package Diagrams.
*D	3468905	12/20/2011	GVCH	Updated DC Electrical Characteristics (Added I_{CC1} parameter value of 450 µA for CY14ME064J).
*E	3680853	07/25/2012	GVCH	Updated DC Electrical Characteristics (Added V_{VCAP} parameter and its details, added Note 8 and referred the same note in V_{VCAP} parameter, also referred Note 9 in V_{VCAP} parameter).
*F	3757952	09/27/2012	GVCH	Updated Maximum Ratings (Removed “Ambient temperature with power applied” and included “Maximum junction temperature”).
*G	3909884	02/21/2013	GVCH	Updated Features: Added Note 1 and referred the same note in “High speed I^2C interface”.
*H	3985389	04/29/2013	GVCH	Updated Features: Updated Note 1. Updated DC Electrical Characteristics: Added one more condition “I_{OL} = 6 mA” for V_{OL} parameter and added respective values. Updated AC Switching Characteristics: Updated Note 11. Changed value of t_{OF} parameter from 300 ns to 250 ns for 400 kHz frequency. Updated Package Diagrams: spec 51-85066 – Changed revision from *E to *F. spec 51-85022 – Changed revision from *D to *E.

Not Recommended for New Designs

Downloaded from Arrow.com.

Document History Page (continued)

Document Title: CY14MB064J, CY14ME064J, 64-Kbit (8 K × 8) Serial (I^2C) nvSRAM Document Number: 001-65051				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*I	4188206	11/11/2013	GVCH	Added watermark as “Not Recommended for New Designs.” Updated in new template. Completing Sunset Review.

Not Recommended for New Designs

Downloaded from Arrow.com.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

Not Recommended for New Designs

© Cypress Semiconductor Corporation, 2010-2013. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

All products and company names mentioned in this document may be the trademarks of their respective holders.

Downloaded from Arrow.com.