

FEATURES

- 650 V enhancement mode power transistor
- Bottom-cooled, 8x8 mm PDFN package
- $R_{DS(on)}(Typ) = 50\text{ m}\Omega$
- $I_{DS(max)} = 30\text{ A}$
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- High switching frequency (> 1 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Source Sense (SS) pin for optimized gate drive
- ROHS Compliant
- Halogen-free

KEY PERFORMANCE PARAMETERS

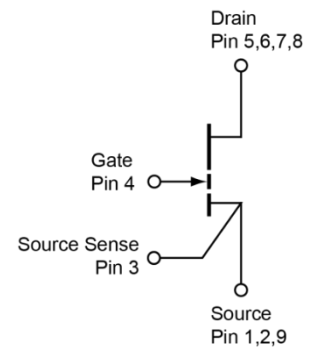
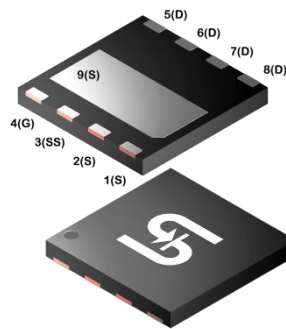
PARAMETER		VALUE	UNIT
V_{DS}		650	V
$R_{DS(on)}$ (max)	$V_{GS} = 6\text{ V}$	68	m Ω
Q_g		6.7	nC



APPLICATIONS

- Bridgeless Totem Pole PFC
- Consumer, Industrial and Datacenter High Density Power Supply
- High Power Adapters
- LED Lighting Drivers
- Solar Inverter
- Uninterruptable Power Supplies
- Appliance and Industrial Motor Drives
- Laser Drivers
- Wireless Power Transfer

PDFN88



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (Note 1)	$V_{DS(transient)}$	850	V
Gate-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	30	A
	$T_C = 100^\circ\text{C}$	20	
Pulse Drain Current (Pulse width 10 μs , $V_{GS} = 6\text{ V}$) (Note 2)	$I_{DS\text{ Pulse}}$	60	
Operating Junction Temperature	T_J	-55 to +150	$^\circ\text{C}$
Storage Temperature Range	T_S	-55 to +150	$^\circ\text{C}$

Notes:

1. For $\leq 100\text{ }\mu\text{s}$.
2. Defined by product design and characterization.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.5	$^{\circ}\text{C/W}$
Junction to Ambient Thermal Resistance(Note 3)	$R_{\theta JA}$	35	$^{\circ}\text{C/W}$

Notes:

- Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm² each. The PCB is mounted in horizontal position without air stream cooling

Electrical Characteristics (Typical values at $T_J = 25^{\circ}\text{C}$, $V_{GS} = 6\text{ V}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Drain-to-Source Blocking Voltage	$V_{GS} = 0\text{ V}$, $I_{DSS} \leq 58\text{ }\mu\text{A}$	$V_{(BL)DSS}$	650	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 7.5\text{ mA}$	$V_{GS(TH)}$	1.1	1.7	2.6	V
Gate-to-Source Current	$V_{GS} = 6\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GS}	--	182	--	μA
Drain-Source Leakage Current	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$ $T_J = 25^{\circ}\text{C}$	I_{DSS}	--	2	58	μA
	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$ $T_J = 150^{\circ}\text{C}$		--	70	--	
Drain-Source On-State Resistance	$V_{GS} = 6\text{ V}$, $T_J = 25^{\circ}\text{C}$ $I_{DS} = 5.5\text{ A}$	$R_{DS(on)}$	--	50	68	m Ω
	$V_{GS} = 6\text{ V}$, $T_J = 150^{\circ}\text{C}$ $I_{DS} = 5.5\text{ A}$		--	127	--	
Total Gate Charge	$V_{GS} = 0\text{ to }6\text{ V}$ $V_{DS} = 400\text{ V}$	Q_g	--	6.7	--	nC
Gate-Source Charge		Q_{gs}	--	1.9	--	
Gate-Drain Charge		Q_{gd}	--	2	--	
Output Charge		Q_{OSS}	--	61	--	
Gate Plateau Voltage	$V_{DS} = 400\text{ V}$, $I_{DS} = 30\text{ A}$	V_{plat}	--	3.5	--	V
Internal Gate Resistance	$f = 5\text{ MHz}$, open drain	R_G		1.3		Ω
Input Capacitance	$V_{DS} = 400\text{ V}$	C_{iss}	--	235	--	pF
Output Capacitance	$V_{GS} = 0\text{ V}$	C_{oss}	--	60	--	
Reverse Transfer Capacitance	$f = 100\text{ kHz}$	C_{rss}	--	0.6	--	
Effective Output Capacitance Energy Related (Note 4)	$V_{GS} = 0\text{ V}$	$C_{O(ER)}$	--	96	--	
Effective Output Capacitance Time Related (Note 5)	$V_{DS} = 0\text{ to }400\text{ V}$	$C_{O(TR)}$	--	150	--	
Reverse Recovery Charge		Q_{rr}	--	0	--	nC

Notes:

- $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated V_{DS} .
- $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated V_{DS} .

Electrical Characteristics cont'd (Typical values at $T_J = 25\text{ }^{\circ}\text{C}$, $V_{GS} = 6\text{ V}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Turn-On Delay	$V_{DD} = 400\text{ V}$, $V_{GS} = +6/-3\text{ V}$, $I_{DS} = 15\text{ A}$, $R_{G(on)} = 15\text{ }\Omega$, $R_{G(off)} = 2\text{ }\Omega$, $L = 90\text{ }\mu\text{H}$, $L_P = 12\text{ nH}$ (Notes 6, 7, 8)	$t_{D(on)}$	--	8.2	--	nS
Rise Time		t_R	--	6.3	--	
Turn-Off Delay		$t_{D(off)}$	--	10.8	--	
Turn-Off Fall Time		t_F	--	5.7	--	
Switching Energy during turn-on		E_{on}	--	50	--	μJ
Switching Energy during turn-off		E_{off}	--	10	--	
Output Capacitance Stored Energy	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$, $f = 100\text{ kHz}$	E_{OSS}	--	8	--	

Notes:

6. See Figure 16 for switching test circuit diagram.
7. See Figure 17 for switching time definition waveforms.
8. L_P = parasitic inductance

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSG65N068CE RVG	PDFN88	3,000pcs / 13" Reel

Electrical Performance Graphs

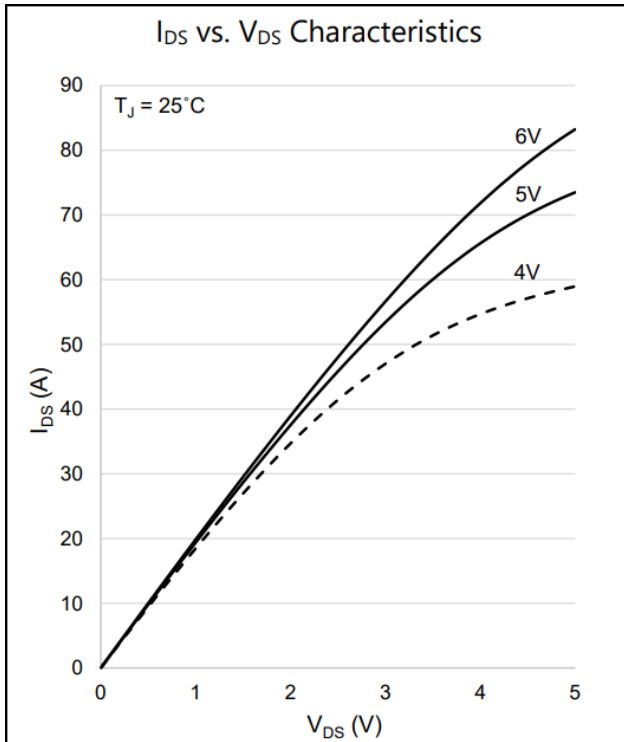


Figure 1: Typical I_{DS} vs. V_{DS} @ $T_J = 25^\circ\text{C}$

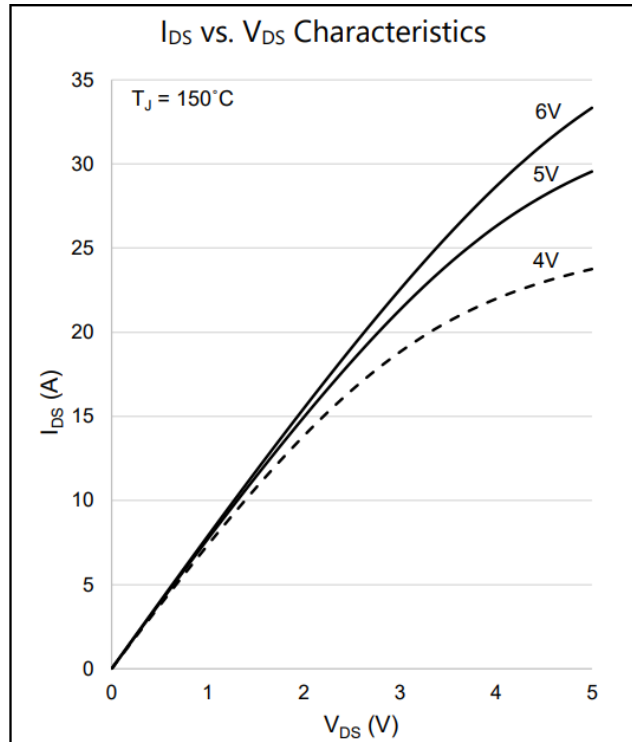


Figure 2: Typical I_{DS} vs. V_{DS} @ $T_J = 150^\circ\text{C}$

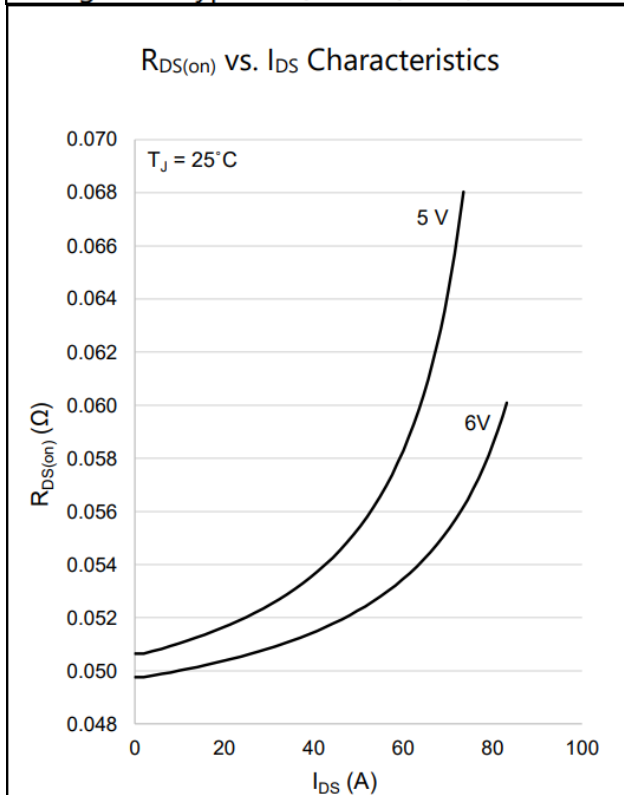


Figure 3: $R_{DS(on)}$ vs. I_{DS} at $T_J = 25^\circ\text{C}$

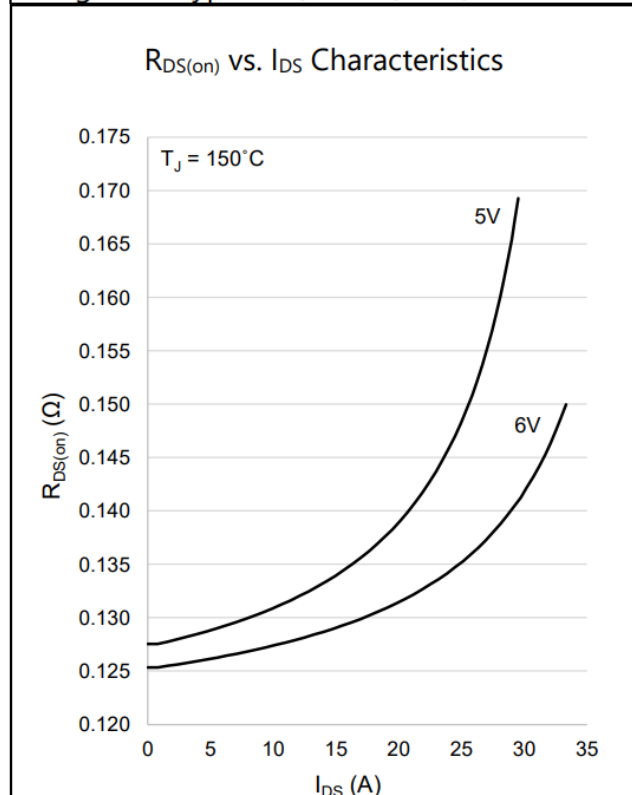


Figure 4: $R_{DS(on)}$ vs. I_{DS} at $T_J = 150^\circ\text{C}$

Electrical Performance Graphs

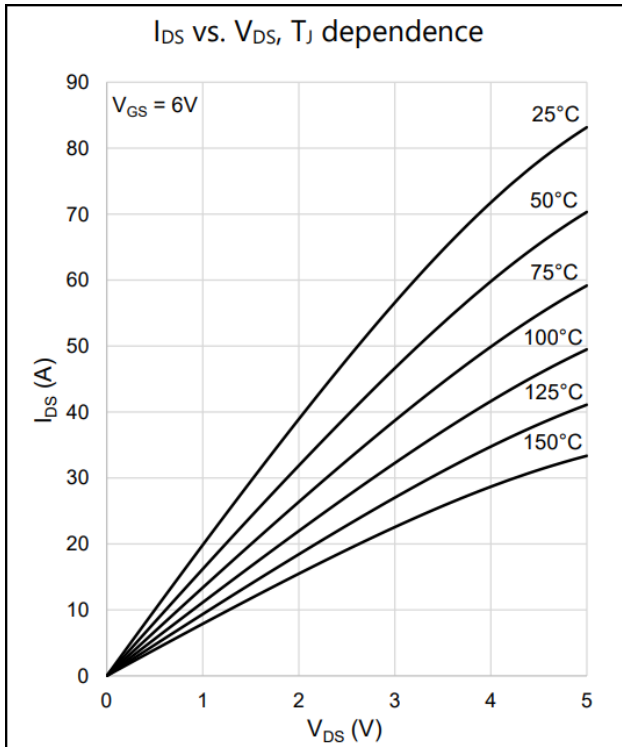


Figure 5: Typical I_{DS} vs. V_{DS} @ $V_{GS} = 6V$

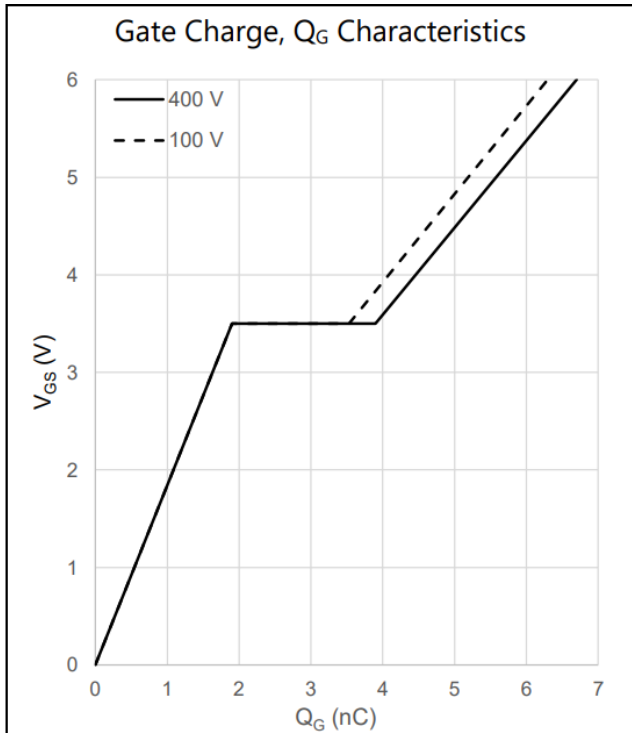


Figure 6: Typical V_{GS} vs. Q_G @ $V_{DS} = 100, 400V$

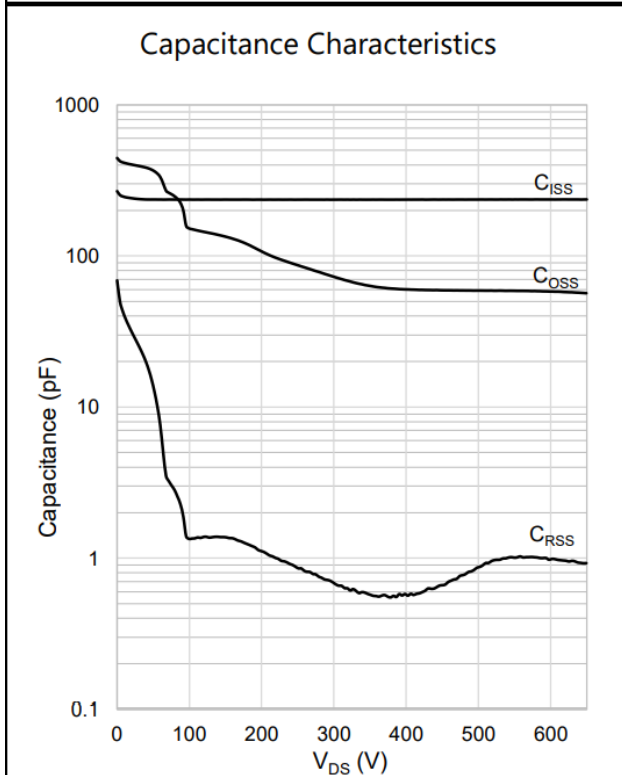


Figure 7: Typical C_{ISS} , C_{OSS} , C_{RSS} vs. V_{DS}

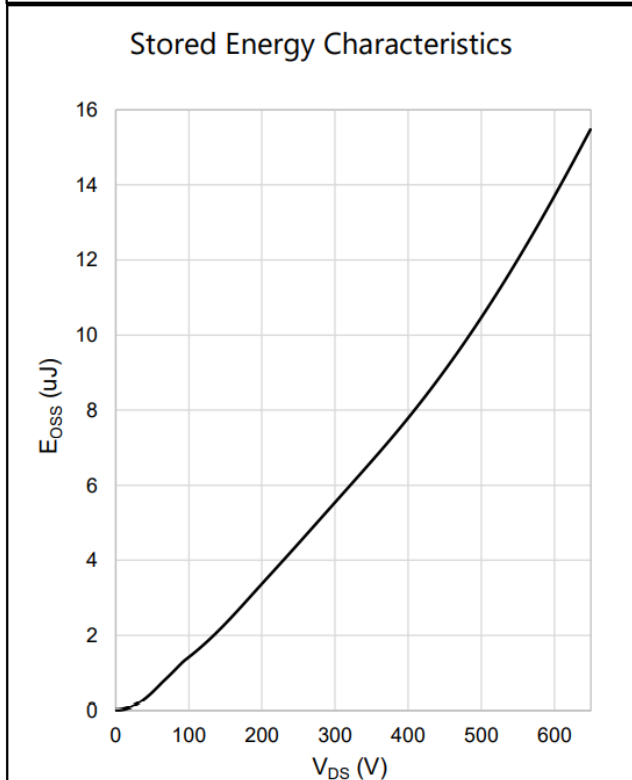


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

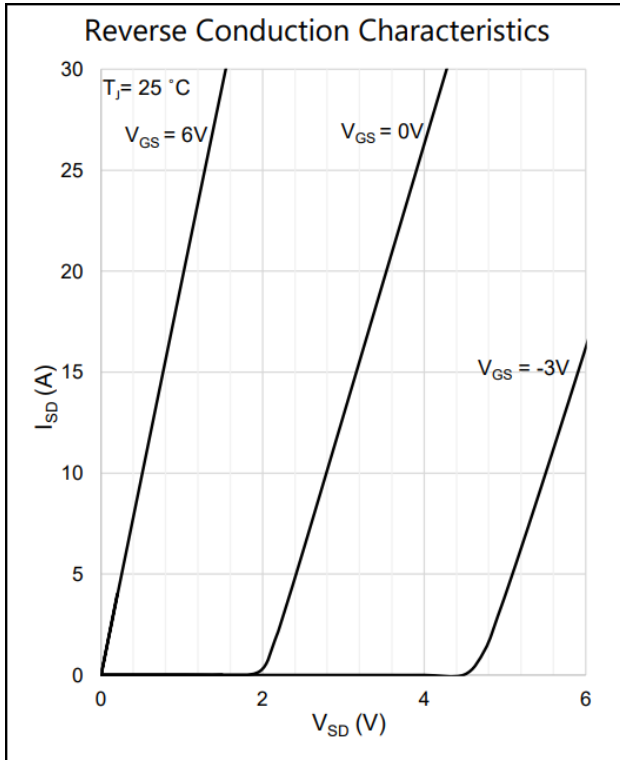


Figure 9: Typical I_{SD} vs. V_{SD} @ $T_J = 25\text{ }^{\circ}\text{C}$

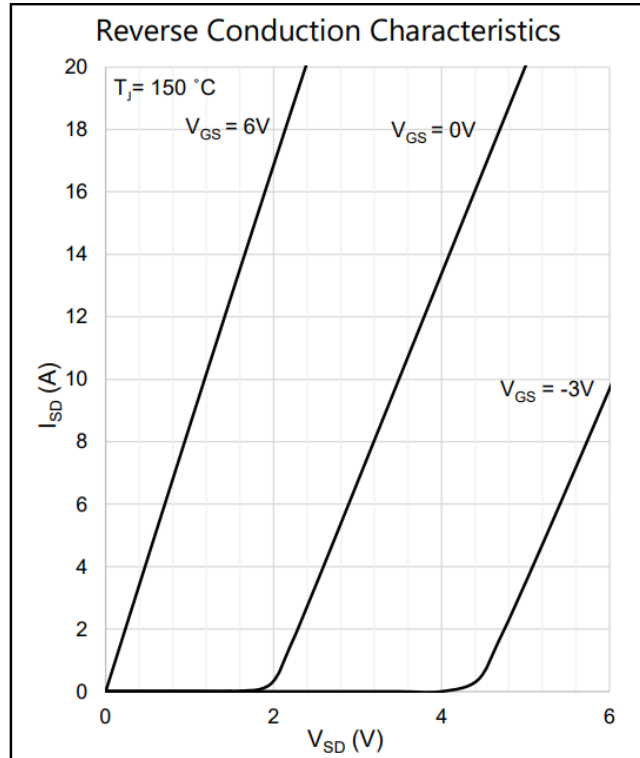


Figure 10: Typical I_{SD} vs. V_{SD} @ $T_J = 150\text{ }^{\circ}\text{C}$

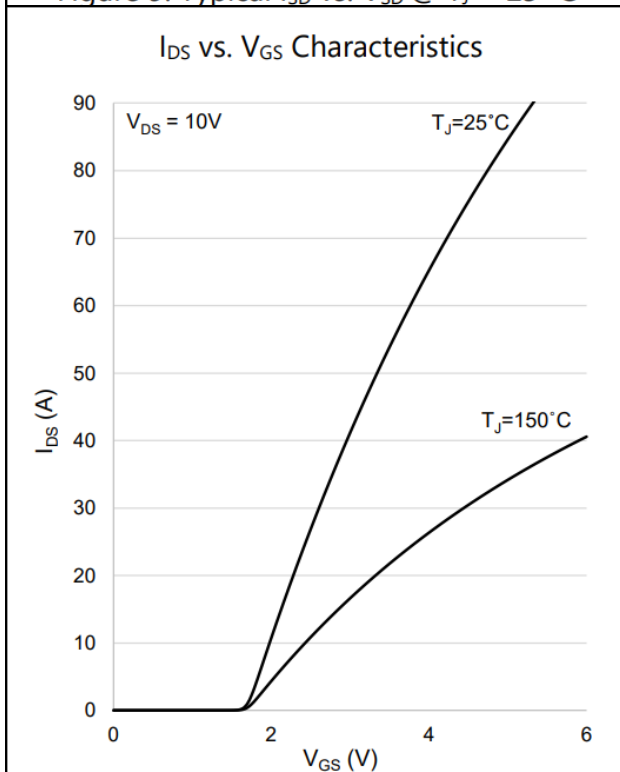


Figure 11: Typical I_{DS} vs. V_{GS}

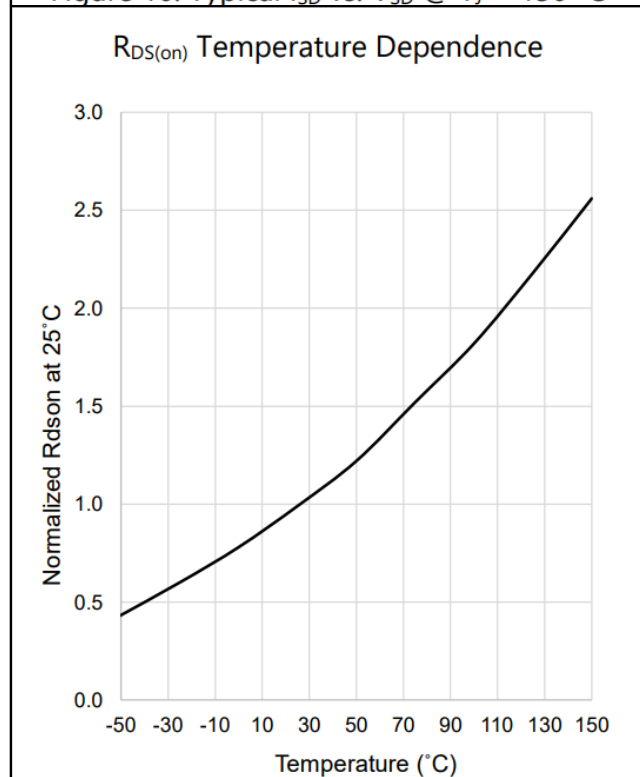
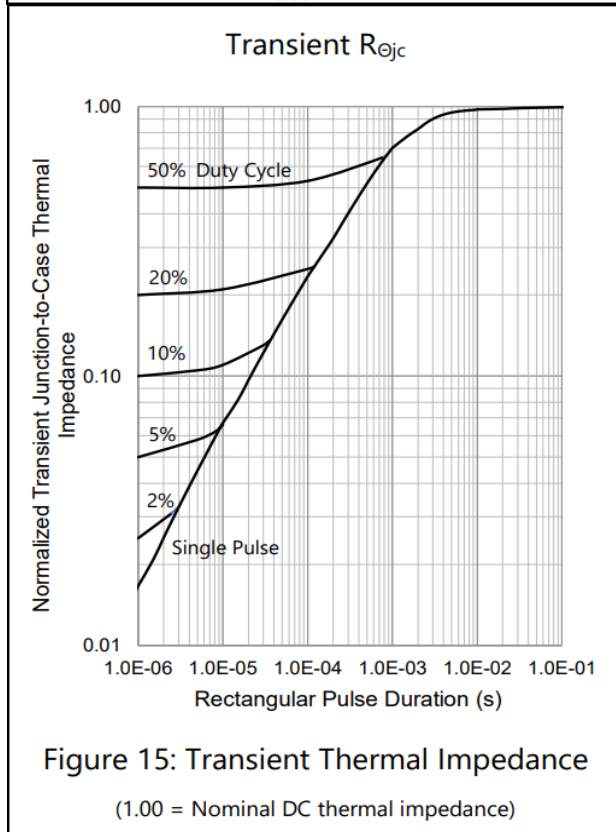
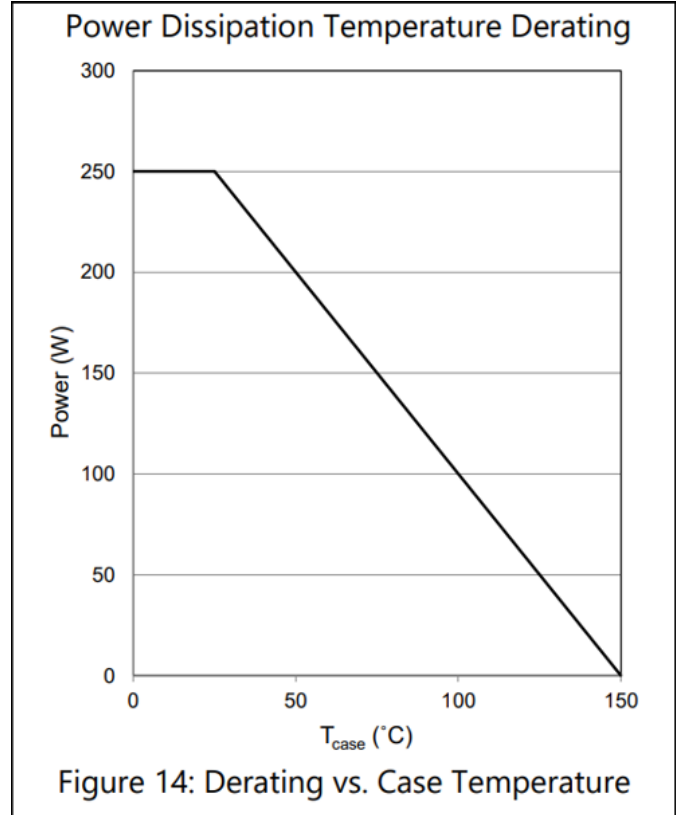
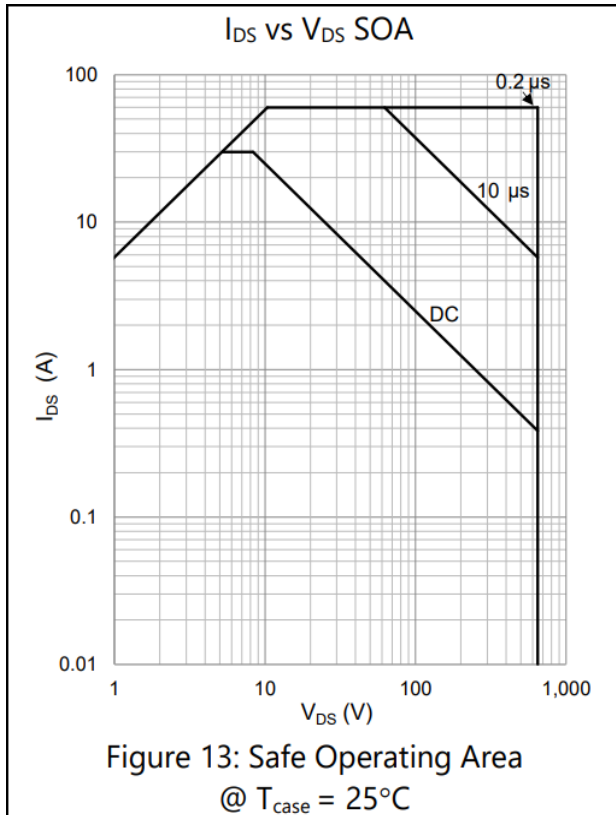


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs



Test Circuits

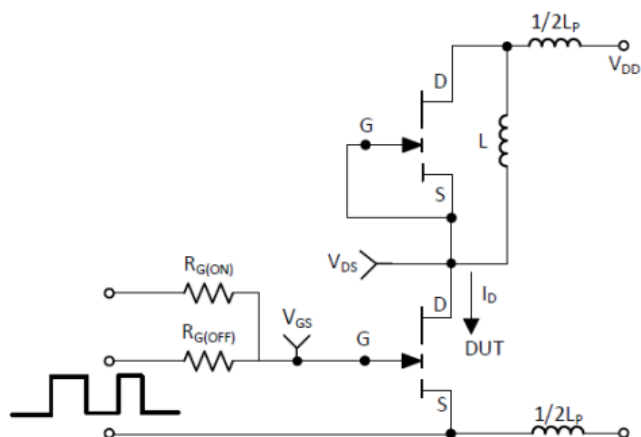
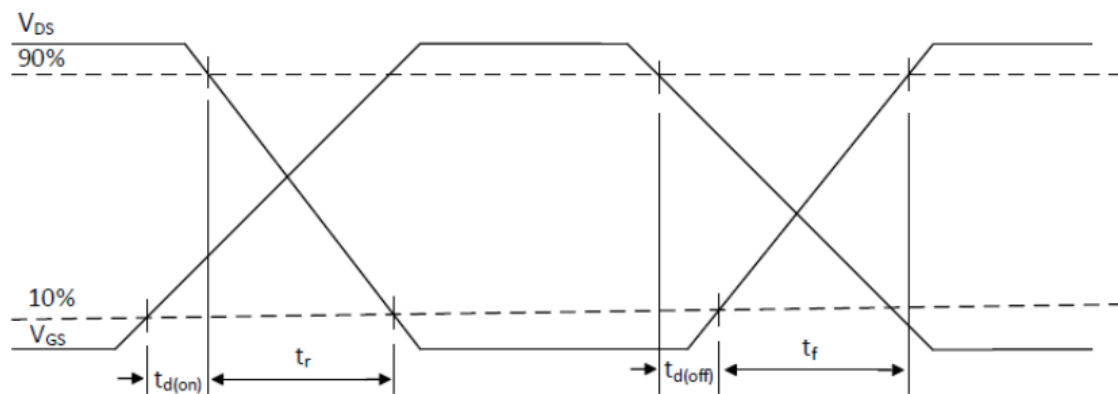
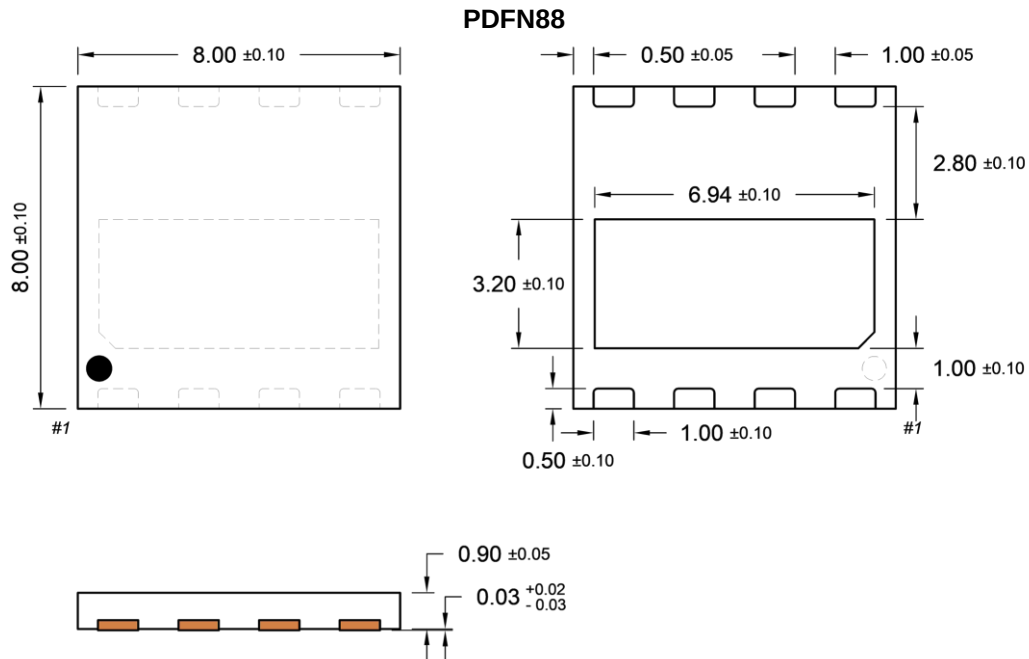


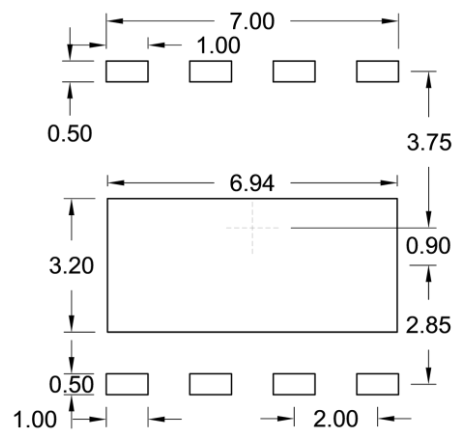
Figure 16: Switching Test Circuit



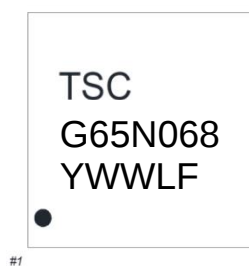
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



Recommended PCB Footprint



MARKING DIAGRAM



Y = Year Code
WW = Week Code (01~52)
L = Lot Code (1~9,A~Z)
F = Factory Code

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