Low Inductance Capacitors

Introduction

The signal integrity characteristics of a Power Delivery
Network (PDN) are becoming critical aspects of board level
and semiconductor package designs due to higher operating
frequencies, larger power demands, and the ever shrinking
lower and upper voltage limits around low operating voltages.
These power system challenges are coming from mainstream
designs with operating frequencies of 300MHz or greater,
modest ICs with power demand of 15 watts or more, and
operating voltages below 3 volts.

The classic PDN topology is comprised of a series of
capacitor stages. Figure 1 is an example of this architecture
with multiple capacitor stages.

An ideal capacitor can transfer all its stored energy to a load
instantly. A real capacitor has parasitics that prevent
instantaneous transfer of a capacitor’s stored energy. The
true nature of a capacitor can be modeled as an RLC
equivalent circuit. For most simulation purposes, it is possible
to model the characteristics of a real capacitor with one
capacitor, one resistor, and one inductor. The RLC values in
this model are commonly referred to as equivalent series
capacitance (ESC), equivalent series resistance (ESR), and
equivalent series inductance (ESL).

The ESL of a capacitor determines the speed of energy
transfer to a load. The lower the ESL of a capacitor, the faster
that energy can be transferred to a load. Historically, there
has been a tradeoff between energy storage (capacitance)
and inductance (speed of energy delivery). Low ESL devices
typically have low capacitance. Likewise, higher capacitance
devices typically have higher ESLs. This tradeoff between
ESL (speed of energy delivery) and capacitance (energy
storage) drives the PDN design topology that places the
fastest low ESL capacitors as close to the load as possible.
Low Inductance MLCCs are found on semiconductor
packages and on boards as close as possible to the load.

LOW INDUCTANCE CHIP CAPACITORS

The key physical characteristic determining equivalent series
inductance (ESL) of a capacitor is the size of the current loop
it creates. The smaller the current loop, the lower the ESL. A
standard surface mount MLCC is rectangular in shape with
electrical terminations on its shorter sides. A Low Inductance
Chip Capacitor (LICC) sometimes referred to as Reverse
Geometry Capacitor (RGC) has its terminations on the longer
side of its rectangular shape.

When the distance between terminations is reduced, the size
of the current loop is reduced. Since the size of the current
loop is the primary driver of inductance, an 0306 with a
smaller current loop has significantly lower ESL than an 0603.
The reduction in ESL varies by EIA size; however, ESL is
typically reduced 60% or more with an LICC versus a
standard MLCC.

INTERDIGITATED CAPACITORS

The size of a current loop has the greatest impact on the ESL
characteristics of a surface mount capacitor. There is a
secondary method for decreasing the ESL of a capacitor.
This secondary method uses adjacent opposing current
loops to reduce ESL. The InterDigitated Capacitor (IDC)
utilizes both primary and secondary methods of reducing
inductance. The IDC architecture shrinks the distance
between terminations to minimize the current loop size, then
further reduces inductance by creating adjacent opposing
current loops.

An IDC is one single capacitor with an internal structure that
has been optimized for low ESL. Similar to standard MLCC
versus LICCs, the reduction in ESL varies by EIA case size.
Typically, for the same EIA size, an IDC delivers an ESL that
is at least 80% lower than an MLCC.
Low Inductance Capacitors

Introduction

LAND GRID ARRAY (LGA) CAPACITORS
Land Grid Array (LGA) capacitors are based on the first Low ESL MLCC technology created to specifically address the design needs of current day Power Delivery Networks (PDNs). This is the 3rd low inductance capacitor technology developed by AVX. LGA technology provides engineers with new options. The LGA internal structure and manufacturing technology eliminates the historic need for a device to be physically small to create small current loops to minimize inductance.

The first family of LGA products are 2 terminal devices. A 2 terminal 0306 LGA delivers ESL performance that is equal to or better than an 0306 8 terminal IDC. The 2 terminal 0805 LGA delivers ESL performance that approaches the 0508 8 terminal IDC. New designs that would have used 8 terminal IDCs are moving to 2 terminal LGAs because the layout is easier for a 2 terminal device and manufacturing yield is better for a 2 terminal LGA versus an 8 terminal IDC.

LGA technology is also used in a 4 terminal family of products that AVX is sampling and will formerly introduce in 2008. Beyond 2008, there are new multi-terminal LGA product families that will provide even more attractive options for PDN designers.

LOW INDUCTANCE CHIP ARRAYS (LICA®)
The LICA® product family is the result of a joint development effort between AVX and IBM to develop a high performance MLCC family of decoupling capacitors. LICA was introduced in the 1980s and remains the leading choice of designers in high performance semiconductor packages and high reliability board level decoupling applications.

LICA® products are used in 99.999% uptime semiconductor package applications on both ceramic and organic substrates. The C4 solder ball termination option is the perfect complement to flip-chip packaging technology. Mainframe class CPUs, ultimate performance multi-chip modules, and communications systems that must have the reliability of 5 9's use LICA®.

LICA® products with either Sn/Pb or Pb-free solder balls are used for decoupling in high reliability military and aerospace applications. These LICA® devices are used for decoupling of large pin count FPGAs, ASICs, CPUs, and other high power ICs with low operating voltages.

When high reliability decoupling applications require the very lowest ESL capacitors, LICA® products are the best option.

470 nF 0306 Impedance Comparison

Figure 2 MLCC, LICC, IDC, and LGA technologies deliver different levels of equivalent series inductance (ESL).
Low Inductance Capacitors (SnPb)

0612/0508/0306/0204 Tin Lead Termination “B”

GENERAL DESCRIPTION
The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL.

A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer sides of its rectangular shape. The image on the right shows the termination differences between an MLCC and an LICC.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL than an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC versus a standard MLCC.

AVX LICC products are available with a lead termination for high reliability military and aerospace applications that must avoid tin whisker reliability issues.

PERFORMANCE CHARACTERISTICS

<table>
<thead>
<tr>
<th>Capacitance Tolerances</th>
<th>K = ±10%; M = ±20%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>X7R = -55°C to +125°C</td>
</tr>
<tr>
<td></td>
<td>X5R = -55°C to +85°C</td>
</tr>
<tr>
<td></td>
<td>X7S = -55°C to +125°C</td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td>X7R, X5R = ±15%; X7S = ±22%</td>
</tr>
<tr>
<td>Voltage Ratings</td>
<td>4, 6.3, 10, 16, 25 VDC</td>
</tr>
<tr>
<td>Dissipation Factor</td>
<td>4V, 6.3V = 6.5% max; 10V = 5.0% max; 16V = 3.5% max; 25V = 3.0% max</td>
</tr>
<tr>
<td>Insulation Resistance</td>
<td>100,000MΩ min, or 1,000MΩ per μF min., whichever is less</td>
</tr>
</tbody>
</table>

HOW TO ORDER

<table>
<thead>
<tr>
<th>Size</th>
<th>Voltage</th>
<th>Dielectric</th>
<th>Capacitance Code (In pF)</th>
<th>Capacitance Code</th>
<th>Capacitance Tolerance</th>
<th>Failure Rate</th>
<th>Terminations</th>
<th>Packaging</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD18</td>
<td>Z</td>
<td>D</td>
<td>105</td>
<td>M</td>
<td>A</td>
<td>B</td>
<td>2</td>
<td>A*</td>
<td></td>
</tr>
<tr>
<td>LD15 = 0204</td>
<td>4 = 4V</td>
<td>C = X7R</td>
<td>2 Sig. Digits + Number of Zeros</td>
<td>K = ±10%</td>
<td>A = N/A</td>
<td>5% min lead</td>
<td>7” Reel</td>
<td>mm (in)</td>
<td></td>
</tr>
<tr>
<td>LD16 = 0306</td>
<td>6 = 6.3V</td>
<td>D = X5R</td>
<td></td>
<td>M = ±20%</td>
<td></td>
<td></td>
<td>13” Reel</td>
<td>0.35 (0.014)</td>
<td></td>
</tr>
<tr>
<td>LD17 = 0508</td>
<td>Z = 10V</td>
<td>W = X6S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.56 (0.022)</td>
<td></td>
</tr>
<tr>
<td>LD18 = 0612</td>
<td>3 = 25V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.61 (0.024)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5 = 50V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.76 (0.030)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.02 (0.040)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.27 (0.050)</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers.

TYPICAL IMPEDANCE CHARACTERISTICS

![Typical Impedance Characteristics Graph](image-url)
### Low Inductance Capacitors (SnPb)

**0612/0508/0306/0204 Tin Lead Termination “B”**

**PREFERRED SIZES ARE SHADED**

<table>
<thead>
<tr>
<th>SIZE</th>
<th>LD15</th>
<th>LD16</th>
<th>LD17</th>
<th>LD18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soldering</td>
<td>Reflow Only</td>
<td>Reflow Only</td>
<td>Reflow/Wave</td>
<td></td>
</tr>
<tr>
<td>Packaging</td>
<td>All Paper</td>
<td>All Paper</td>
<td>Paper/Embossed</td>
<td></td>
</tr>
<tr>
<td>(L) Length</td>
<td>0.50 ± 0.05 (0.020 ± 0.002)</td>
<td>0.81 ± 0.15 (0.032 ± 0.006)</td>
<td>1.27 ± 0.25 (0.050 ± 0.013)</td>
<td>1.60 ± 0.25 (0.063 ± 0.013)</td>
</tr>
<tr>
<td>(W) Width</td>
<td>1.00 ± 0.05 (0.040 ± 0.002)</td>
<td>1.60 ± 0.15 (0.063 ± 0.006)</td>
<td>2.00 ± 0.25 (0.080 ± 0.010)</td>
<td>3.20 ± 0.25 (0.126 ± 0.010)</td>
</tr>
</tbody>
</table>

**PHYSICAL DIMENSIONS AND PAD LAYOUT**

**PHYSICAL CHIP DIMENSIONS mm (in.)**

<table>
<thead>
<tr>
<th>0612</th>
<th>0508</th>
<th>0306</th>
<th>0204</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>1.60 ± 0.25 (0.063 ± 0.010)</td>
<td>3.20 ± 0.25 (0.126 ± 0.010)</td>
<td>0.13 min. (0.005 min.)</td>
</tr>
<tr>
<td>W</td>
<td>0.81 ± 0.15 (0.032 ± 0.006)</td>
<td>1.60 ± 0.15 (0.063 ± 0.006)</td>
<td>0.13 min. (0.005 min.)</td>
</tr>
<tr>
<td>t</td>
<td>0.50 ± 0.05 (0.020 ± 0.002)</td>
<td>1.00 ± 0.05 (0.040 ± 0.002)</td>
<td>0.18 ± 0.08 (0.007 ± 0.003)</td>
</tr>
</tbody>
</table>

**PAD LAYOUT DIMENSIONS mm (in.)**

<table>
<thead>
<tr>
<th>0612</th>
<th>0508</th>
<th>0306</th>
<th>0204</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.61 (0.024)</td>
<td>0.61 (0.024)</td>
<td>0.61 (0.024)</td>
</tr>
<tr>
<td>B</td>
<td>0.76 (0.030)</td>
<td>0.76 (0.030)</td>
<td>0.76 (0.030)</td>
</tr>
<tr>
<td>C</td>
<td>1.02 (0.040)</td>
<td>1.02 (0.040)</td>
<td>1.02 (0.040)</td>
</tr>
</tbody>
</table>

**T** - See Range Chart for Thickness and Codes