TPS23753A IEEE 802.3 PoE Interface and Converter Controller with Enhanced ESD Immunity

1 Features

- Enhanced ESD ride-through capability
- Optimized for isolated converters
- Complete PoE interface
- Adapter ORing support
- 12-V adapter support
- Programmable frequency with synchronization
- Robust 100-V, 0.7-Ω hotswap MOSFET
- Small 14-Pin TSSOP package
- 15-kV and 8-kV system level ESD capable
- –40°C to 125°C junction temperature range
- Design procedure application note – SLVA305
- Adapter oring application note – SLVA306

2 Applications

- IEEE 802.3at compliant powered devices
- VoIP telephones
- Access points
- Security cameras

3 Description

The TPS23753A is a combined Power over Ethernet (PoE) powered device (PD) interface and current-mode DC-DC controller optimized specifically for isolated converter designs. The PoE implementation supports the IEEE 802.3at standard as a 13-W, type 1 PD. The requirements for an IEEE 802.3at type 1 device are a superset of IEEE 802.3-2008 (originally IEEE 802.3af).

The TPS23753A supports a number of input-voltage ORing options including highest voltage, external adapter preference, and PoE preference.

The PoE interface features an external detection signature pin that can also be used to disable the internal hotswap MOSFET. This allows the PoE function to be turned off. Classification can be programmed to any of the defined types with a single resistor.

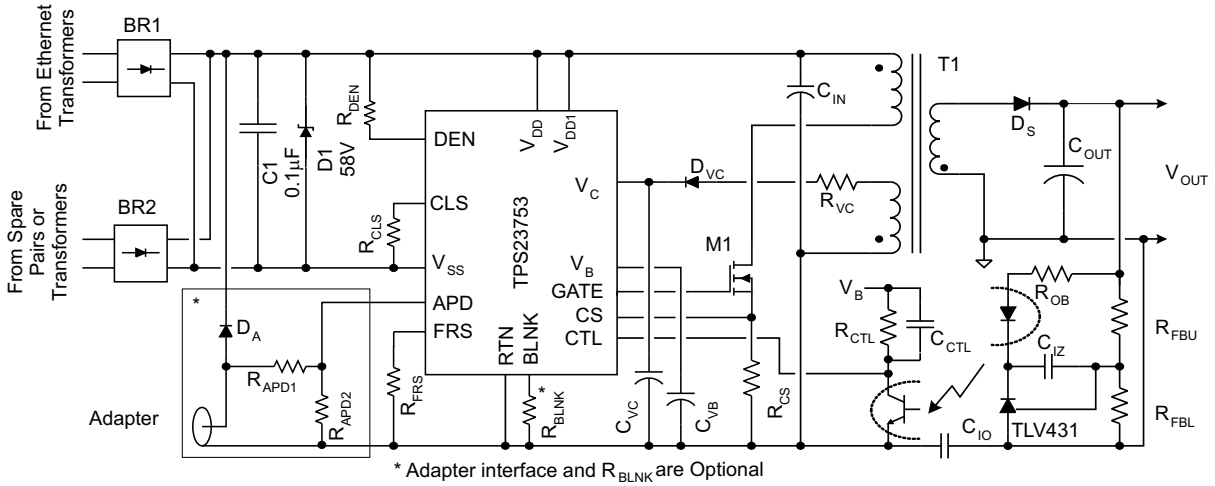
The DC-DC controller features a bootstrap start-up mechanism with an internal, switched current source. This provides the advantages of cycling overload fault protection without the constant power loss of a pullup resistor.

The programmable oscillator may be synchronized to a higher-frequency external timing reference. The TPS23753A features improvements for uninterrupted device operation through an ESD event.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS23753A	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Basic TPS23753A Implementation

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2016) to Revision D (December 2020) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document....1
- Changed Start-up time unit from "V" to "ms" in *Electrical Characteristics: Controller Section Only* table.... 5

Changes from Revision B (January 2010) to Revision C (April 2016) **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.... 1
- Deleted *Dissipation Ratings* 6

Changes from Revision A (September 2009) to Revision B (January 2010) **Page**

- Changed From: IEEE 802.3-2005 To: IEEE 802.3at throughout the data sheet.... 1
- Changed the text in paragraph one of the DESCRIPTION....1
- Changed the Thermal resistance note in the DISSIPATION RATINGS table to include additional information... 6
- Changed text in the second paragraph of Classic PoE Overdrive From: The PD may return the default 12.95 W (often referred to as 13 W) current-encoded class, or one of four other choices. To: The PD may return the default 13-W current-encoded class, or one of four other choices.... 14
- Changed Table 8-1 - Notes for the Class 4 row....16

Changes from Revision * (July 2009) to Revision A (September 2009) **Page**

- Changed the ESDS statement....1

5 Product Information

DEVICE	DUTY CYCLE	POE UVLO ON / HYST.	DC-DC UVLO ON / HYST.
TPS23753A	0 – 78%	35/4.5	9/3.5

6 Pin Configuration and Functions

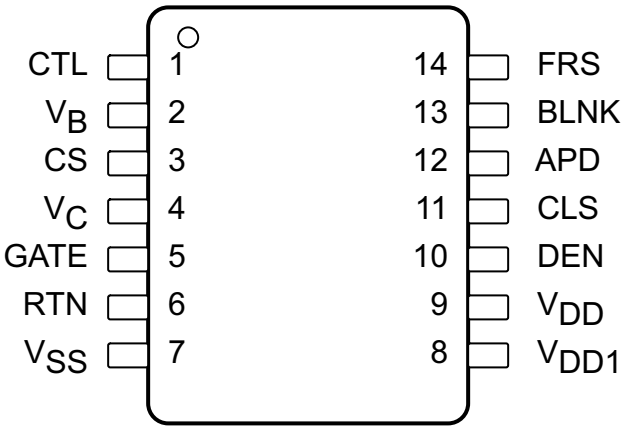


Figure 6-1. PW Package 14-Pin TSSOP Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CTL	I	The control loop input to the PWM (pulse width modulator). Use V_B as a pullup for CTL.
2	V_B	O	5-V bias rail for DC-DC control circuits. Apply a 0.1-µF ceramic capacitor to RTN. V_B may be used to bias an external optocoupler for feedback.
3	CS	I	DC-DC converter switching MOSFET current-sense input. Connect CS to the high side of R_{CS}.
4	V_C	I/O	DC-DC converter bias voltage. The internal start-up current source and converter bias winding output power this pin. Connect a 0.22-µF minimum ceramic capacitor to RTN, and a larger capacitor to facilitate start-up.
5	GATE	O	Gate drive output for the DC-DC converter switching MOSFET.
6	RTN	—	RTN is the negative rail input to the DC-DC converter and output of the PoE hotswap.
7	V_{SS}	—	Negative power rail derived from the PoE source.
8	V_{DD1}	—	Source of DC-DC converter start-up current. Connect to V_{DD} for most applications.
9	V_{DD}	—	Positive input power rail for PoE interface circuit. Derived from the PoE source.
10	DEN	I/O	Connect a 24.9-kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. Pulling this pin to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off.
11	CLS	O	Connect a resistor from CLS to V_{SS} to program the classification current.
12	APD	I	Pull APD above 1.5 V to disable the internal PD hotswap switch, forcing power to come from an external adapter. Connect to the adapter through a resistor divider.
13	BLNK	I/O	Connect to RTN to use the internally set blanking period or connect through a resistor to RTN to program the blanking period.
14	FRS	I/O	Connect a resistor from FRS to RTN to program the converter switching frequency.

7 Specifications

7.1 Absolute Maximum Ratings

Voltage are with respect to V_{SS} (unless otherwise noted)(1) per Figure 9-1 per Table 8-1

			MIN	MAX	UNIT
V_I	Input voltage	V_{DD}, V_{DD1}, DEN, RTN(2)	–0.3	100	V
		V_{DD1} to RTN	–0.3	100	
		CLS(3)	–0.3	6.5	
		[APD, BLNK(3), CTL, FRS(3), V_B (3)] to RTN	–0.3	6.5	
		CS to RTN	–0.3	V_B	
		V_C to RTN	–0.3	19	
		GATE(3) to RTN	–0.3	V_C + 0.3	
	Sourcing current	V_B	Internally limited		mA
	Average sourcing or sinking current	GATE		25	mA_{RMS}
T_J	Operating junction temperature		–40 to Internally Limited		°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{RTN} = 0 for V_{RTN} > 80 V.
(3) Do not apply voltage to these pins.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2 contact discharge(3)	±8000	
		IEC 61000-4-2 air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Surges per EN61000-4-2, 1999 applied between RJ-45 and output ground and between adapter input and output ground of the TPS23753AEVM-001 (HPA304-001) evaluation module (documentation available on the web). These were the test levels, not the failure threshold.

7.3 Recommended Operating Conditions

Voltage with respect to V_{SS} (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage, V_{DD}, V_{DD1}, RTN	0		57	V
	Input voltage, V_C to RTN	0		18	
	Input voltage, APD, CTL to RTN	0		V_B	
	Input voltage, CS to RTN	0		2	
	RTN current (T_J ≤ 125°C)			350	mA
	V_B sourcing current	0	2.5	5	mA
	V_B capacitance	0.08	0.1		µF
R_{BLNK}		0		350	kΩ
	Synchronization pulse width input (when used)	25			ns
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS23753A PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: Controller Section Only

Unless otherwise noted: CS = APD = CTL = RTN, GATE open, R_{FRS} = 60.4 kΩ, R_{BLNK} = 249 kΩ, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, $V_{VDD-VSS}$ = 48 V, $V_{VDD1-RTN}$ = 48 V, 8.5 V ≤ V_{VC-RTN} ≤ 18 V, –40°C ≤ T_J ≤ 125°C [V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to RTN. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C						
UVLO_1	Undervoltage lockout	V_C rising	8.65	9	9.3	V
UVLO_H		Hysteresis(1)	3.3	3.5	3.7	
	Operating current	V_C = 12 V, CTL = V_B	0.4	0.58	0.85	mA
t_{ST}	Start-up time, C_{VC} = 22 µF	V_{DD1} = 10.2 V, V_{VC}(0) = 0 V	50	85	175	ms
		V_{DD1} = 35 V, V_{VC}(0) = 0 V	30	48	85	
	Start-up current source - I_{VC}	V_{DD1} = 10.2 V, V_{VC} = 8.6 V	0.44	1.06	1.8	mA
		V_{DD1} = 48 V, V_{VC} = 0 V	2.5	4.3	6	
V_B						
	Voltage	6.5 V ≤ V_C ≤ 18 V, 0 ≤ I_{VB} ≤ 5 mA	4.75	5.1	5.25	V
FRS						
	Switching frequency	CTL= V_B, Measure GATE	223	248	273	kHz
		R_{FRS} = 60.4 kΩ				
D_{MAX}	Duty cycle	CTL= V_B, Measure GATE	76%	78.5%	81%	
V_{SYNC}	Synchronization	Input threshold	2	2.2	2.4	V
CTL						
V_{ZDC}	0% duty cycle threshold	V_{CTL} ↓ until GATE stops	1.3	1.5	1.7	V
	Soft-start period	Interval from switching start to V_{CSMAX}	400	800		µs
	Input resistance		70	100	145	kΩ
BLNK						
	Blanking delay	In addition to t1	35	52	75	ns
		BLNK = RTN				
		R_{BLNK} = 49.9 kΩ	41	52	63	
CS						
V_{CSMAX}	Maximum threshold voltage	V_{CTL} = V_B, V_{CS} ↑ until GATE duty cycle drops	0.5	0.55	0.6	V
t_1	Turnoff delay	V_{CS} = 0.65 V	25	41	60	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referred to CS	90	118	142	mV
I_{SL_EX}	Peak slope compensation current	V_{CTL} = V_B, I_{CS} at maximum duty cycle (ac component)	30	42	54	µA

Unless otherwise noted: CS = APD = CTL = RTN, GATE open, R_{FRS} = 60.4 kΩ, R_{BLNK} = 249 kΩ, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, $V_{VDD-VSS}$ = 48 V, $V_{VDD1-RTN}$ = 48 V, 8.5 V ≤ V_{VC-RTN} ≤ 18 V, –40°C ≤ T_J ≤ 125°C [V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to RTN. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Bias current (sourcing)	Gate high, DC component of CS current	2	3	4.2	µA
GATE						
	Source current	V_{CTL} = V_B, V_C = 12 V, GATE high, Pulsed measurement	0.3	0.46	0.6	A
	Sink current	V_{CTL} = V_B, V_C = 12 V, GATE low, Pulsed measurement	0.5	0.79	1.1	A
APD						
V_{APDEN}	Threshold voltage	V_{APD}↑	1.42	1.5	1.58	V
V_{APDH}		Hysteresis(1)	0.28	0.3	0.32	
THERMAL SHUTDOWN						
	Turnoff temperature		135	145	155	°C
	Hysteresis(2)			20		°C

(1) The hysteresis tolerance tracks the rising threshold for a given device.
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.6 Electrical Characteristics: PoE and Control

Unless otherwise noted: CS = APD = CTL = RTN, GATE open, R_{FRS} = 60.4 kΩ, R_{BLNK} = 249 kΩ, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, $V_{VDD-VSS}$ = 48 V, $V_{VDD1-RTN}$ = 48 V, 8.5 V ≤ V_{VC-RTN} ≤ 18 V, –40°C ≤ T_J ≤ 125°C [V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to RTN. [V_{DD} = V_{DD1}] or [V_{DD1} = RTN], V_{VC-RTN} = 0 V, all voltages referred to V_{SS}. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEN (DETECTION) (V_{DD} = V_{DD1} = RTN = V_{SUPPLY} POSITIVE)						
	Detection current	Measure I_{SUPPLY}				
		V_{DD} = 1.6 V	62	64.3	66.5	µA
		V_{DD} = 10 V	399	406	413	
	Detection bias current	V_{DD} = 10 V, DEN open, Measure I_{SUPPLY}		5.2	12	µA
V_{PD_DIS}	Hotswap disable threshold		3	4	5	V
I_{lkg}	DEN leakage current	V_{DEN} = V_{DD} = 57 V, Float V_{DD1} and RTN, Measure I_{DEN}		0.1	5	µA
CLS (CLASSIFICATION) (V_{DD} = V_{DD1} = RTN = V_{SUPPLY} POSITIVE)						
I_{CLS}	Classification current	13 V ≤ V_{DD} ≤ 21 V, Measure I_{SUPPLY}	1.8	2.14	2.4	mA
		R_{CLS} = 1270 Ω	1.8	2.14	2.4	
		R_{CLS} = 243 Ω	9.9	10.6	11.3	
		R_{CLS} = 137 Ω	17.6	18.6	19.4	
		R_{CLS} = 90.9 Ω	26.5	27.9	29.3	
		R_{CLS} = 63.4 Ω	38	39.9	42	
V_{CL_ON}	Classification regulator lower threshold	Regulator turns on, V_{DD} rising	10	11.7	13	V
V_{CL_HYS}		Hysteresis(1)	1.9	2.05	2.2	
V_{CU_OFF}	Classification regulator upper threshold	Regulator turns off, V_{DD} rising	21	22	23	V
V_{CU_HYS}		Hysteresis(1)	0.5	0.77	1	
I_{lkg}	Leakage current	V_{DD} = 57 V, V_{CLS} = 0 V, DEN = V_{SS}, Measure I_{CLS}			1	µA
RTN (PASS DEVICE) (V_{DD1} = RTN)						
	ON-resistance			0.7	1.2	Ω
	Current limit	V_{RTN} = 1.5 V, V_{DD} = 48 V, Pulsed Measurement	405	450	505	mA
	Inrush limit	V_{RTN} = 2 V, V_{DD}: 0 V → 48 V, Pulsed Measurement	100	140	180	mA
	Foldback voltage threshold	V_{DD} rising	11	12.3	13.6	V
I_{lkg}	Leakage current	V_{DD} = V_{RTN} = 100 V, DEN = V_{SS}			40	µA

Unless otherwise noted: CS = APD = CTL = RTN, GATE open, R_{FRS} = 60.4 kΩ, R_{BLNK} = 249 kΩ, C_{VB} = C_{VC} = 0.1 µF, R_{DEN} = 24.9 kΩ, R_{CLS} open, $V_{VDD-VSS}$ = 48 V, $V_{VDD1-RTN}$ = 48 V, 8.5 V ≤ V_{VC-RTN} ≤ 18 V, –40°C ≤ T_J ≤ 125°C [V_{SS} = RTN and V_{DD} = V_{DD1}] or [V_{SS} = RTN = V_{DD}], all voltages referred to RTN. [V_{DD} = V_{DD1}] or [V_{DD1} = RTN], V_{VC-RTN} = 0 V, all voltages referred to V_{SS}. Typical specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
UVLO_R	Undervoltage lockout threshold	V_{DD} rising	33.9	35	36.1	V
UVLO_H		Hysteresis (1)	4.4	4.55	4.7	V
THERMAL SHUTDOWN						
	Turnoff temperature		135	145	155	°C
	Hysteresis(2)			20		°C

(1) The hysteresis tolerance tracks the rising threshold for a given device.
(2) These parameters are provided for reference only.

7.7 Typical Characteristics

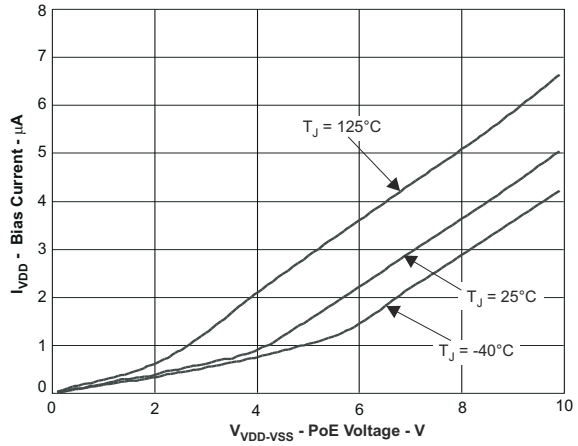


Figure 7-1. Detection Bias Current vs Voltage

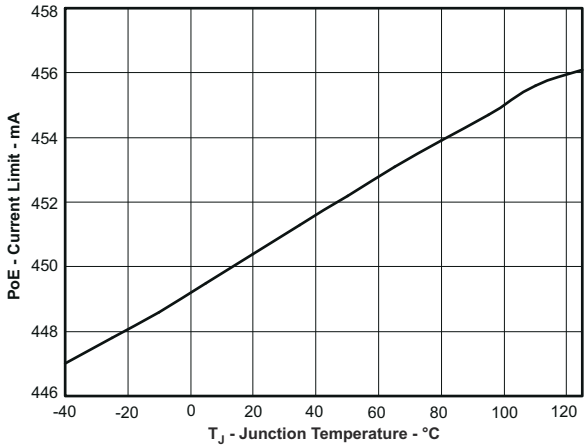


Figure 7-2. PoE Current Limit vs Temperature

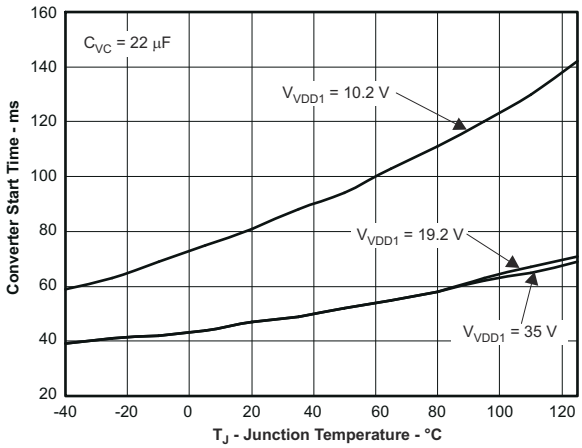


Figure 7-3. Converter Start Time vs Temperature

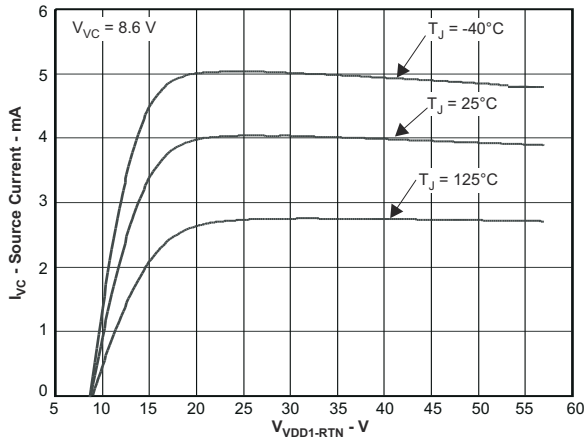


Figure 7-4. Converter Start-Up Source Current vs VVDD1

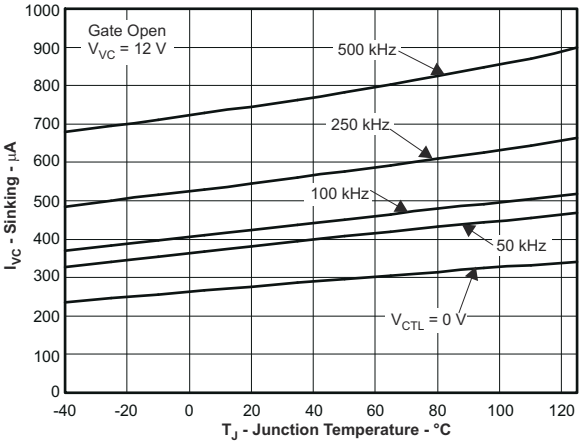


Figure 7-5. Controller Bias Current vs Temperature

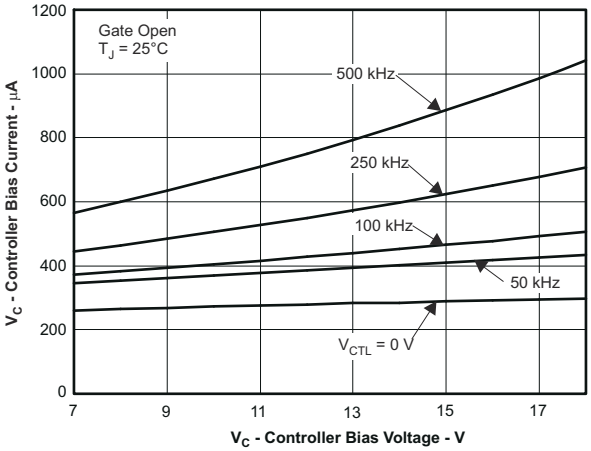


Figure 7-6. Controller Bias Current vs Voltage

7.7 Typical Characteristics (continued)

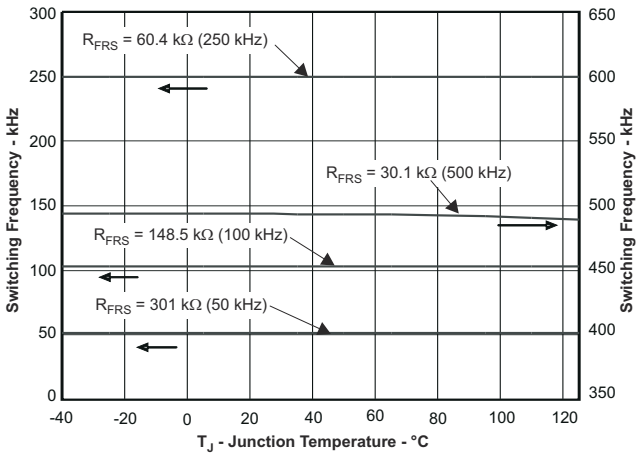


Figure 7-7. Switching Frequency vs Temperature

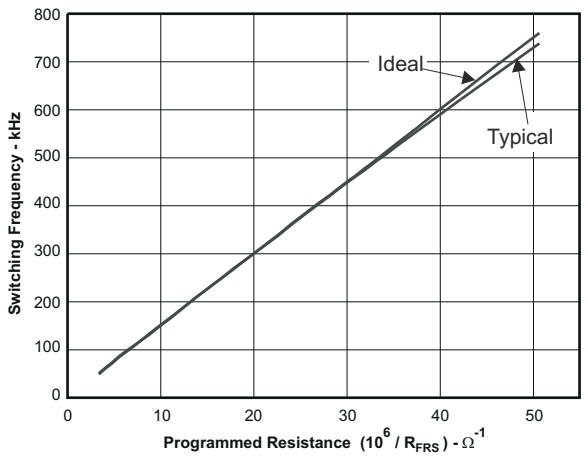


Figure 7-8. Switching Frequency vs Programmed Resistance

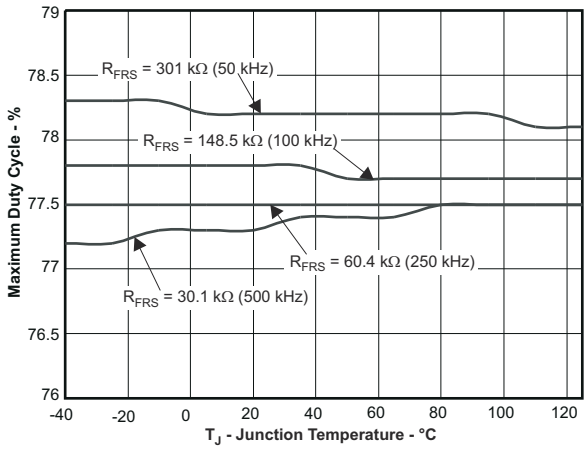


Figure 7-9. Maximum Duty Cycle vs Temperature

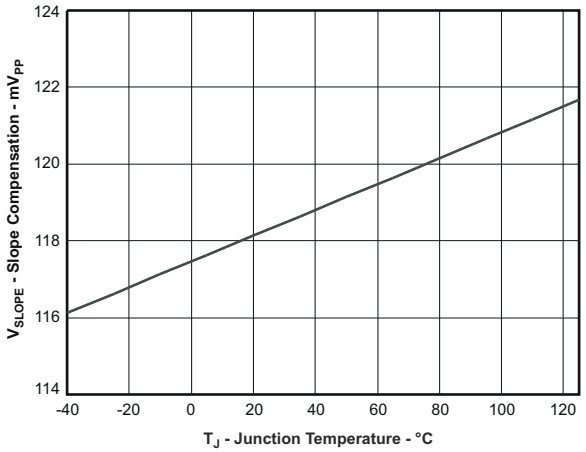


Figure 7-10. Current Slope Compensation Voltage vs Temperature

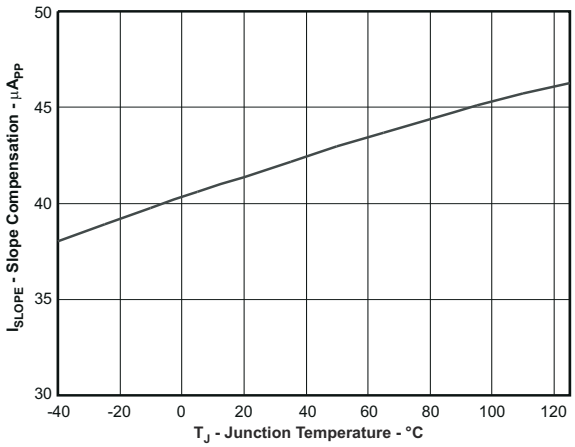


Figure 7-11. Current Slope Compensation Current vs Temperature

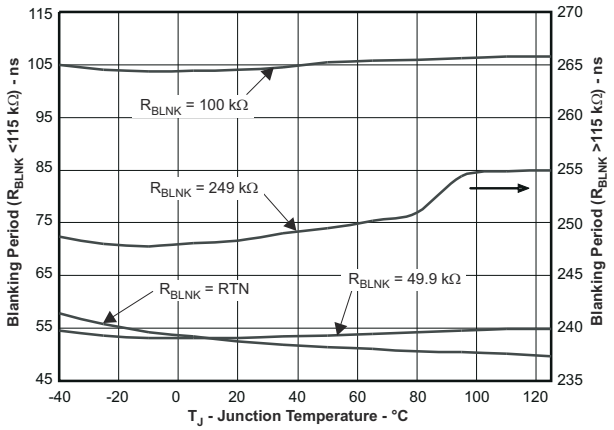


Figure 7-12. Blanking Period vs Temperature

7.7 Typical Characteristics (continued)

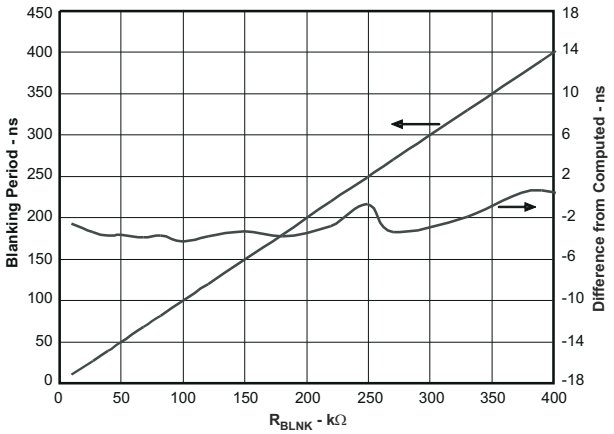


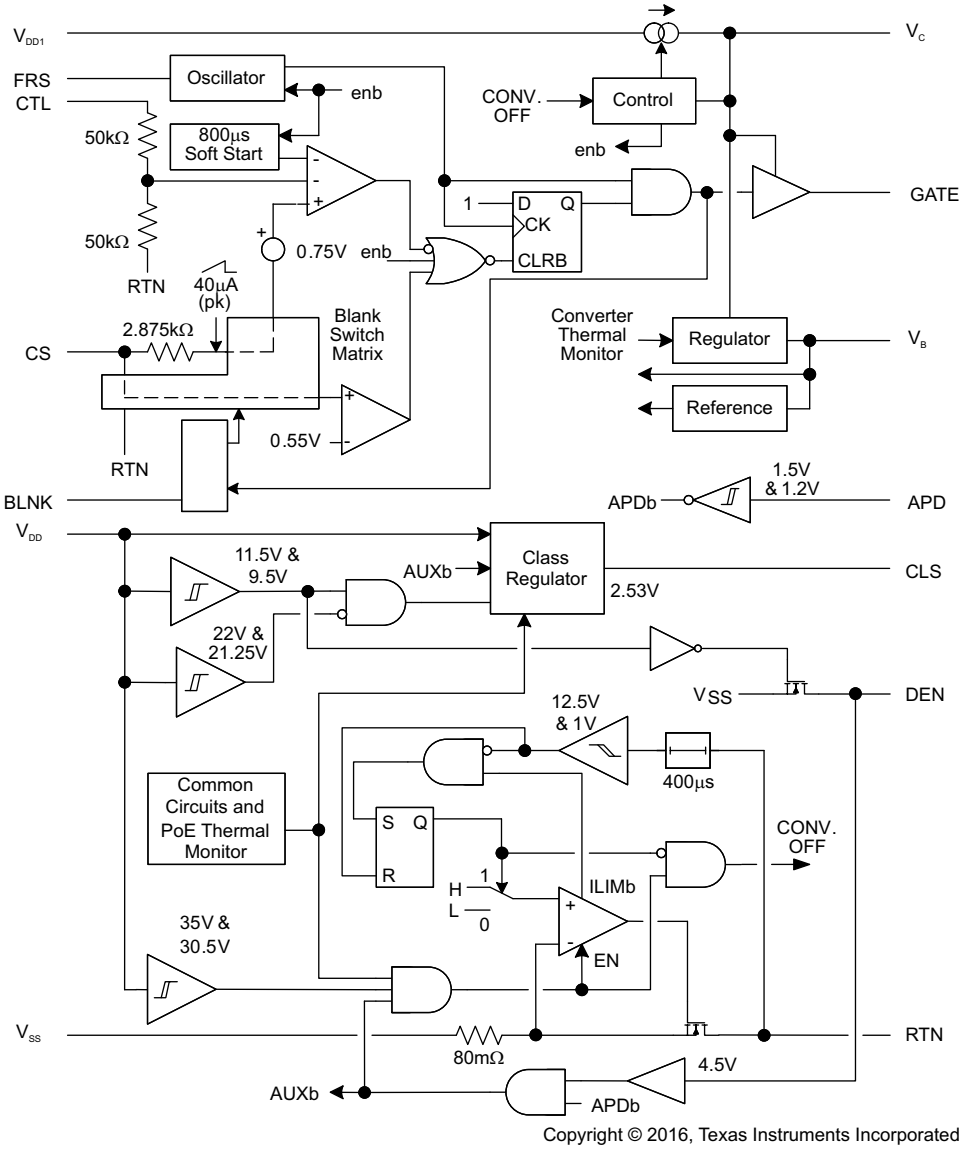
Figure 7-13. Blanking Period vs RBLNK

8 Detailed Description

8.1 Overview

The TPS23753A device has a PoE that contains all of the features needed to implement an IEEE802.3at Type 1 powered device (PD) such as detection, classification, and 140-mA inrush current mode DC-DC controller optimized specifically for isolated converters. The TPS23753A device integrates a low 0.7-Ω internal switch to allow for up to 405 mA of continuous current through the PD during normal operation. The TPS23753A device contains several protection features such as thermal shutdown, current limit foldback, and a robust 100-V internal switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pin Description

See Figure 9-1 for component reference designators (R_{CS} for example), and *Electrical Characteristics: Controller Section Only* for values denoted by reference (V_{CSMAX} for example). Electrical Characteristic values take precedence over any numerical values used in the following sections.

8.3.1.1 APD

APD forces power to come from an external adapter connected from V_{DD1} to RTN by opening the hotswap switch. TI recommends using a resistor divider. The divider provides ESD protection, leakage discharge for the adapter ORing diode, and input voltage qualification. Voltage qualification assures the adapter can support the PD before the PoE current is cut off.

Select the APD divider resistors per Equation 1 and Equation 2, where $V_{ADPTR-ON}$ is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1} = R_{APD2} \; x \; \left(V_{ADPTR\_ON} - V_{APDEN}\right) / V_{APDEN} \tag{1}$$

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \; x \; \left(V_{APDEN} - V_{APDH}\right) \tag{2}$$

The CLS output is disabled when a voltage above V_{APDEN} is applied to the APD pin.

Place the APD pulldown resistor adjacent to the APD pin.

APD must be tied to RTN when not used.

8.3.1.2 BLNK

Blanking provides an interval between the gate drive going high and the current comparator on CS actively monitoring the input. This delay allows the normal turnon current transient (spike) to subside before the comparator is active, preventing undesired short duty cycles and premature current limiting.

Connect BLNK to RTN to obtain the internally set blanking period. Connect a resistor from BLNK to RTN for a programmable blanking period. The relationship between the desired blanking period and the programming resistor is defined by Equation 3.

$$R_{BLNK}\left(k\Omega\right) = t_{BLNK}\left(ns\right) \tag{3}$$

Place the resistor adjacent to the BLNK pin when it is used.

8.3.1.3 CLS

Connect a resistor from CLS to V_{SS} to program the classification current per IEEE 802.3-at. The PD power ranges and corresponding resistor values are listed in Table 8-1. The power assigned must correspond to the maximum average power drawn by the PD during operation. The TPS23753A supports class 0 – 3 power levels.

8.3.1.4 CS

The current-sense input for the DC-DC converter should be connected to the high side of the current-sense resistor of the switching MOSFET. The current-limit threshold, V_{CSMAX}, defines the voltage on CS above which the GATE ON-time are terminated regardless of the voltage on CTL.

The TPS23753A provides internal slope compensation to stabilize the current mode control loop. If the provided slope is not sufficient, the effective slope may be increased by addition of R_S per Figure 8-8.

Routing between the current-sense resistor and the CS pin must be short to minimize cross-talk from noisy traces such as the gate drive signal.

8.3.1.5 CTL

CTL is the voltage control loop input to the PWM (pulse width modulator). Pulling V_{CTL} below V_{ZDC} causes GATE to stop switching. Increasing V_{CTL} above V_{ZDC} raises the switching MOSFET programmed peak current. The maximum (peak) current is requested at approximately V_{ZDC} + (2 × V_{CSMAX}). The AC gain from CTL to the PWM comparator is 0.5.

Use V_B as a pullup source for CTL.

8.3.1.6 DEN

Connect a 24.9-kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. DEN goes to a high impedance state when not in the detection voltage range. Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET and class regulator to turn off.

8.3.1.7 FRS

Connect a resistor from FRS to RTN to program the converter switching frequency. Select the resistor using Equation 4.

$$R_{FRS}(k\Omega) = \frac{15000}{f_{SW}(kHz)} \quad (4)$$

The converter may be synchronized to a frequency above its maximum free-running frequency by applying short AC-coupled pulses into the FRS pin. More information is provided in *Application and Implementation*.

The FRS pin is high impedance. Keep the connections short and apart from potential noise sources.

8.3.1.8 GATE

Gate drive output for the DC-DC converter switching MOSFET.

8.3.1.9 RTN

RTN is internally connected to the drain of the PoE hotswap MOSFET, and the DC-DC controller return. RTN must be treated as a local reference plane (ground plane) for the DC-DC controller and converter primary to maintain signal integrity.

8.3.1.10 V_B

V_B is an internal 5-V control rail that must be bypassed by a 0.1-µF capacitor to RTN. V_B should be used to bias the feedback optocoupler.

8.3.1.11 V_C

V_C is the bias supply for the DC-DC controller. The MOSFET gate driver runs directly from V_C. V_B is regulated down from V_C, and is the bias voltage for the rest of the converter control. A start-up current source from V_{DD1} to V_C is controlled by a comparator with hysteresis to implement a bootstrap start-up of the converter. V_C must be connected to a bias source, such as a converter auxiliary output, during normal operation.

A minimum 0.22-µF capacitor, located adjacent to the V_C pin, must be connected from V_C to RTN to bypass the gate driver. A larger total capacitance is required for start-up.

8.3.1.12 V_{DD}

Positive input power rail for PoE control that is derived from the PoE. V_{DD} should be bypassed to V_{SS} with a 0.1-µF (X7R,10%) capacitor as required by the standard. A transient suppressor (Zener) diode, must be connected from V_{DD} to V_{SS} to protect against overvoltage transients.

8.3.1.13 V_{DD1}

Source of DC-DC converter start-up current. Connect to V_{DD} for most applications. V_{DD1} may be isolated by a diode from V_{DD} to support PoE-priority operation.

8.3.1.14 V_{SS}

V_{SS} is the PoE input-power return side. It is the reference for the PoE interface circuits, and has a current-limited hotswap switch that connects it to RTN. V_{SS} is clamped to a diode drop above RTN by the hotswap switch. A local V_{SS} reference plane should be used to connect the input components and the V_{SS} pin.

8.4 Device Functional Modes

The following text is intended as an aid in understanding the operation of the TPS23753A, but it is not a substitute for the actual IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification.

Generally speaking, a device compliant to IEEE 802.3-2008 is referred to as a type 1 device, and devices with high power or enhanced classification is referred to as type 2 devices. The TPS23753A is intended to power type 1 devices (up to 13 W), and is fully compliant to IEEE 802.3at for hardware classes 0 - 3. Standards change and must always be referenced when making design decisions.

The IEEE 802.3at standard defines a method of safely powering a PD (powered device) over a cable, and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this is referred to as (hardware) classification. Only Type 2 PSEs are required to do hardware classification. The PD may return the default 13-W current-encoded class, or one of four other choices. The PSE may then power the PD if it has adequate capacity. Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 8-1 shows the operational states as a function of PD input voltage.

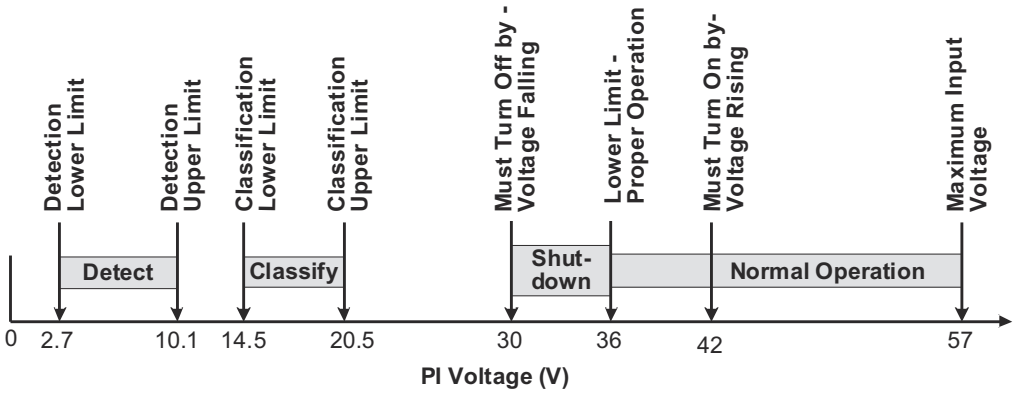


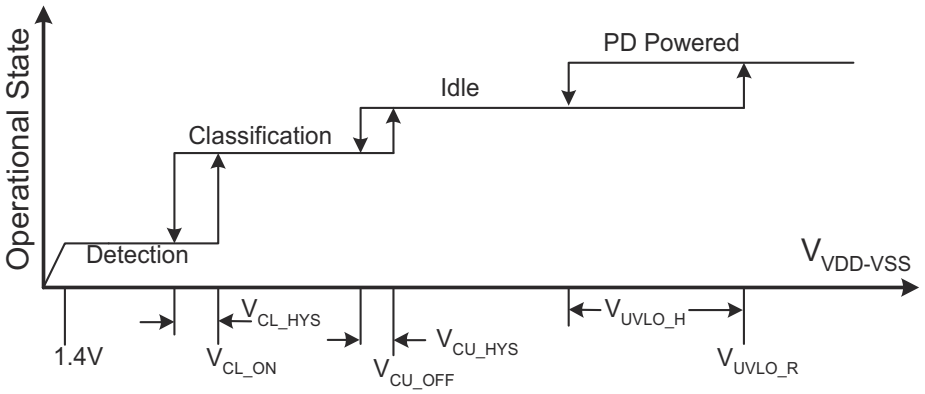
Figure 8-1. IEEE 802.3-2005 (Type 1) Operational States

The PD input is typically an RJ-45 eight-lead connector which is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops in the cable and operating margin. The IEEE 802.3at standard uses a cable resistance of 20 Ω for type 1 devices to derive the voltage limits at the PD based on the PSE output voltage requirements. Although the standard specifies an output power of 15.4 W at the PSE, only 13 W is available at the PI due to the worst-case power loss in the cable. The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6 for 10baseT or 100baseT), or between the two spare pairs (4–5 and 7–8). The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS23753A specifications.

The PSE is permitted to disconnect a PD if it draws more than its maximum class power over a one second interval. A Type 1 PSE compliant to IEEE 802.3at is required to limit current to between 400 mA and 450 mA during powered operation, and it must disconnect the PD if it draws this current for more than 75 ms. Class 0 and 3 PDs may draw up to 400-mA peak currents for up to 50 ms. The PSE may set lower output current limits based on the declared power requirements of the PD.

8.4.1 Threshold Voltages

The TPS23753A has a number of internal comparators with hysteresis for stable switching between the various states as shown in Figure 8-1. Figure 8-2 relates the parameters in *Electrical Characteristics: Controller Section Only* and *Electrical Characterisics: PoE and Control* to the PoE states. The mode labeled idle between classification and operation implies that the DEN, CLS, and RTN pins are all high impedance.



Note: Variable names refer to Electrical Characteristic Table parameters

Figure 8-2. Threshold Voltages

8.4.2 PoE Start-Up Sequence

The waveforms of Figure 8-3 demonstrate detection, classification, and start-up from a Type 1 PSE. The key waveforms shown are $V_{VDD-VSS}$, $V_{RTN-VSS}$, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels; however, four levels are shown in this example. Four levels guard against misdetection of a device when plugged in during the detection sequence.

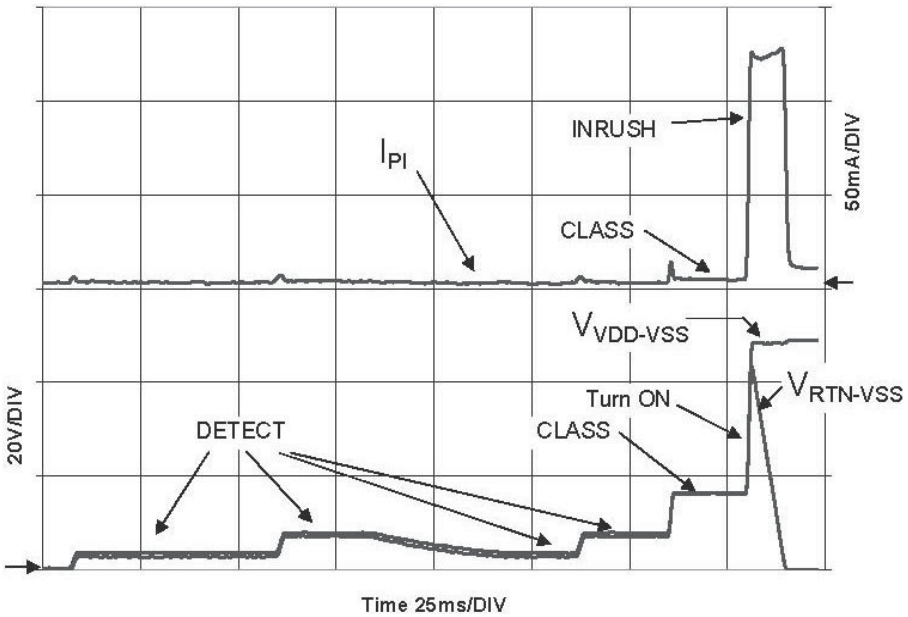


Figure 8-3. PoE Start-Up Sequence

8.4.3 Detection

The TPS23753A is in detection mode whenever $V_{VDD-V\ SS}$ is below the lower classification threshold. When the input voltage rises above V_{CL_ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, almost all the internal circuits are disabled, and the DEN pin is pulled to V_{SS}.

An R_{DEN} of 24.9 kΩ (1%), presents the correct signature. It may be a small, low-power resistor because it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance between 23.75 kΩ and 26.25 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and the TPS23753A bias loading. The incremental resistance of the input diode bridge may be hundreds of ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially cancelled by the effective resistance of the TPS23753A during detection.

8.4.4 Hardware Classification

Hardware classification allows a PSE to determine the power requirements of a PD before starting, and helps with power management once power is applied. The maximum power entries in Table 8-1 determine the class the PD must advertise. A Type 1 PD may not advertise Class 4. The PSE may disconnect a PD if it draws more than its stated Class power. The standard permits the PD to draw limited current peaks; however, the average power requirement always applies.

Voltage from 14.5 V to 20.5 V is applied to the PD for up to 75 ms during hardware classification. A fixed output voltage is sourced by the CLS pin, causing a fixed current to be drawn from V_{DD} through R_{CLS}. The total current drawn from the PSE during classification is the sum of bias and R_{CLS} currents. PD current is measured and decoded by the PSE to determine which of the five available classes is advertised (see Table 8-1). The TPS23753A disables classification above V_{CU_OFF} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limit or when APD or DEN are active. The CLS output is inherently current-limited, but should not be shorted to V_{SS} for long periods of time.

Table 8-1. Class Resistor Selection

CLASS	POWER AT PD PI		CLASS CURRENT REQUIREMENT		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)	MINIMUM (mA)	MAXIMUM (mA)		
0	0.44	12.95	0	4	1270	
1	0.44	3.84	9	12	243	
2	3.84	6.49	17	20	137	
3	6.49	12.95	26	30	90.9	
4	12.95	25.5	36	44	63.4	Only permitted for type 2 devices

8.4.5 Maintain Power Signature (MPS)

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum DC current of 10 mA (at a duty cycle of at least 75 ms on every 225 ms) and an AC impedance lower than 26.25 kΩ in parallel with 0.05 µF. The AC impedance is usually accomplished by the minimum C_{IN} requirement of 5 µF. When APD or DEN are used to force the hotswap switch off, the DC MPS is not met. A PSE that monitors the DC MPS will remove power from the PD when this occurs. A PSE that monitors only the AC MPS may remove power from the PD.

8.4.6 TPS23753A Operation

8.4.6.1 Start-Up and Converter Operation

The internal PoE undervoltage lockout (UVLO) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits discharges C_{IN}, C_{VC}, and C_{VB} while the PD is unpowered. Thus $V_{RTN-VDD}$ will be a small voltage just after full voltage is applied to the PD, as seen in Figure 8-3.

The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{DD} rises above the UVLO turnon threshold (V_{UVLO-R}, approximately 35 V) with RTN high, the TPS23753A enables the hotswap MOSFET with an approximately 140-mA (inrush) current limit. See the waveforms of Figure 8-4 for an example. Converter switching is disabled while C_{IN} charges and V_{RTN} falls from V_{DD} to nearly V_{SS}; however, the converter start-up circuit is allowed to charge C_{VC}. Once the inrush current falls about 10% below the inrush

current limit, the PD control switches to the operational level (approximately 450 mA) and converter switching is permitted.

Converter switching is allowed if the PD is not in inrush and the V_C UVLO circuit permits it. Continuing the start-up sequence shown in Figure 8-4, V_{VC} rises as the start-up current source charges C_{VC} and M1 switching is inhibited by the status of the V_C UVLO. The V_B regulator powers the internal converter circuits as V_{VC} rises. Start-up current is turned off, converter switching is enabled, and a soft-start cycle starts when V_{VC} exceeds $UVLO_1$ (approximately 9 V). V_{VC} falls as it powers both the internal circuits and the switching MOSFET gate. If the converter control-bias output rises to support V_{VC} before it falls to $UVLO_1 – UVLO_{1H}$ (approximately 5.5 V), a successful start-up occurs. Figure 8-4 shows a small droop in V_{VC} while the output voltage rises smoothly and a successful start-up occurs.

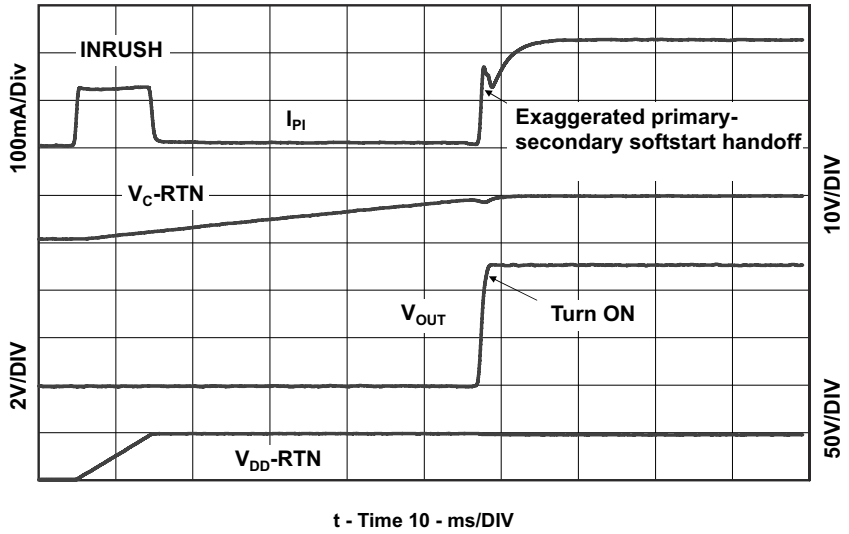


Figure 8-4. Power Up and Start

If $V_{VDD-VSS}$ drops below the lower PoE UVLO ($UVLO_R – UVLO_H$, approximately 30.5 V), the hotswap MOSFET is turned off, but the converter still runs. The converter stops if V_{VC} falls below the converter UVLO ($UVLO_1 – UVLO_H$, approximately 5.5 V), the hotswap is in inrush current limit, or 0% duty cycle is demanded by V_{CTL} ($V_{CTL} < V_{ZDC}$, approximately 1.5 V), or the converter is in thermal shutdown.

8.4.6.2 PD Self-Protection

The PD section has the following self-protection functions.

- Hotswap switch current limit
- Hotswap switch foldback
- Hotswap thermal protection

The internal hotswap MOSFET is protected against output faults with a current limit and deglitched foldback. The PSE output cannot be relied on to protect the PD MOSFET against transient conditions, requiring the PD to provide fault protection. High stress conditions include converter output shorts, shorts from V_{DD1} to RTN, or transients on the input line. An overload on the pass MOSFET engages the current limit, with $V_{RTN-VSS}$ rising as a result. If V_{RTN} rises above approximately 12 V for longer than approximately 400 µs, the current limit reverts to the inrush limit, and turns the converter off. The 400-µs deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 8-5 shows an example of recovery from a 15-V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to 420-mA, full-current limit, and charges the input capacitor while the converter continues to run. The MOSFET did not go into foldback because $V_{RTN-VSS}$ was below 12 V after the 400-µs deglitch.

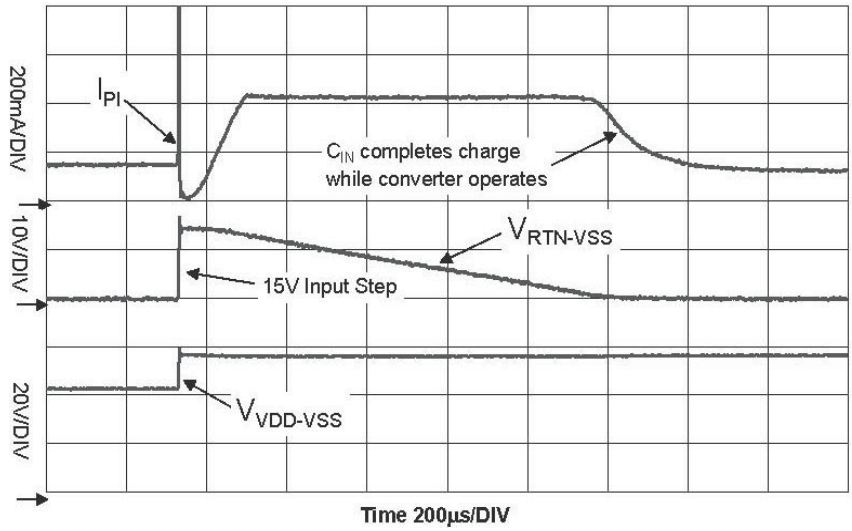


Figure 8-5. Response to PSE Step Voltage

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like start-up or operation into a V_{DD} to RTN short cause high power dissipation in the MOSFET. An overtemperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The PD restarts in inrush current limit when exiting from a PD overtemperature event.

Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with secondary-side adapter ORing to achieve adapter priority. Take care with synchronous converter topologies that can deliver power in both directions.

The hotswap switch is forced off under the following conditions:

- V_{APD} above V_{APDEN} (approximately 1.5 V)
- $V_{DE\ N} \leq V_{PD\_DIS}$ when $V_{VDD-VSS}$ is in the operational range
- PD over temperature
- $V_{VDD-VSS}$ < PoE UVLO (approximately 30.5 V)

8.4.6.3 Converter Controller Features

The TPS23753A DC-DC controller implements a typical current-mode control as shown in Figure 8-6. Features include oscillator, overcurrent and PWM comparators, current-sense blanker, soft start, and gate driver. In addition, an internal current-compensation ramp generator, frequency synchronization logic, thermal shutdown, and start-up current source with control are provided.

The TPS23753A is optimized for isolated converters, and does not provide an internal error amplifier. Instead, the optocoupler feedback is directly fed to the CTL pin which serves as a current-demand control for the PWM and converter. There is an offset of V_{ZDC} (approximately 1.5 V) and 2:1 resistor divider between the CTL pin and the PWM. A V_{CTL} below V_{ZDC} stops converter switching, while voltages above (V_{ZDC} + 2 × V_{CSMAX}) does not increase the requested peak current in the switching MOSFET. Optocoupler biasing design is eased by this limited control range.

The internal start-up current source and control logic implement a bootstrap-type start-up. The start-up current source charges C_{VC} from V_{DD1} when the converter is disabled (either by the PD control or the V_C control), while operational power must come from a converter (bias winding) output. Loading on V_C and V_B must be minimal while C_{VC} charges, otherwise the converter may never start. The optocoupler does not load V_B when the converter is off. The converter shuts off when V_C falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the output voltages fall including the one that powers V_C. The control circuit discharges V_C until it hits the lower UVLO and turns off. A restart initiates as described in *Start-Up and Converter Operation* if the converter turns off and there

is sufficient V_{DD1} voltage. This type of operation is sometimes referred to as *hiccup mode*, which provides robust output short protection by providing time-average heating reduction of the output rectifier.

Take care in the design of the transformer and V_C bias circuit to obtain hiccup overload protection. Leading-edge voltage overshoot on the bias winding may cause V_C to peak-charge, preventing the expected tracking with output voltage. R_{VC} (Figure 9-1) is often required slow the peak charging. Good transformer bias-to-output-winding coupling results in reduced overshoot and better voltage tracking.

The start-up current source transitions to a resistance as (V_{DD1} – V_C) falls below 7 V, but starts the converter from 12-V adapters within t_{ST} (V_{DD1} ≥ 10.2, t_{ST} approximately 85 ms). The converter starts from lower voltages, limited by the case when charge current equals the device bias current at voltage below the upper V_C UVLO. The bootstrap source provides reliable start-up from widely varying input voltages, and eliminates the continual power loss of external resistors. The start-up current source does not charge above the maximum recommended V_{VC} if the converter is disabled and there is sufficient V_{DD1} to charge higher.

The peak current limit does not have duty cycle dependency unless R_S is used as shown in Figure 8-8 to increase slope compensation. This makes it easier to design the current limit to a fixed value.

The TPS23753A blanker timing is precise enough that the traditional R-C filters on CS can be eliminated. This avoids current-sense waveform distortion, which tends to get worse at light output loads. While the internally set blanking period is relatively precise, almost all converters require their own blanking period. The TPS23753A provides the BLNK pin to allow this programming. There may be some situations or designers that prefer an R-C approach. The TPS23753A provides a pulldown on CS during the GATE OFF-time to improve sensing when an R-C filter must be used. The CS input signal must be protected from nearby noisy signals like GATE drive and the MOSFET drain.

Converters require a soft start on the voltage error amplifier to prevent output overshoot on start-up. Figure 8-6 shows a common implementation of a secondary-side soft start that works with the typical TL431 error amplifier shown in Figure 9-1. This secondary-side error amplifier does not become active until there is sufficient voltage on the secondary. The TPS23753A provides a primary-side soft start, which persists long enough (approximately 800 µs) for secondary side voltage-loop soft start to take over; however, the actual start-up is typically shorter than this. The primary-side current-loop soft-start controls the switching MOSFET peak current by applying a slowly rising ramp voltage to a second PWM control input. The lower of the CTL and soft-start ramps controls the PWM comparator. Figure 8-4 shows an exaggerated handoff between the primary and secondary-side soft start that is most easily seen in the I_{PI} waveform. The output voltage rises in a smooth monotonic fashion with no overshoot. The soft-start handoff in this example could have been optimized by decreasing the secondary-side soft-start period.

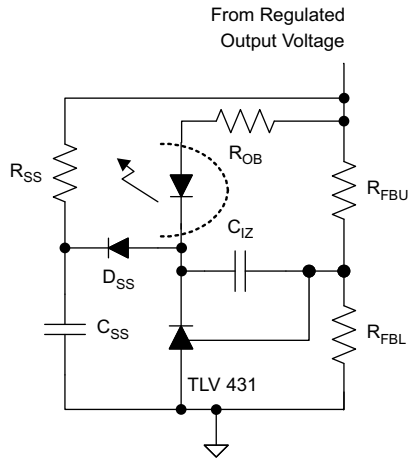


Figure 8-6. Example of Soft-Start Circuit Added to Error Amplifier

The DC-DC controller has an OTSD that can be triggered by heat sources including the V_B regulator, GATE driver, bootstrap current source, and bias currents. The controller OTSD turns off V_B, the GATE driver, resets the soft-start generator, and forces the V_C control into an undervoltage state.

8.4.7 Special Switching MOSFET Considerations

Take special care in selecting the converter switching MOSFET. The TPS23753A converter section has minimum V_C operating voltage of approximately 5.5 V, which is reflected in the applied gate voltage. This occurs during an output overload, or towards the end of a (failed) bootstrap start-up. The MOSFET must be able to carry the anticipated peak fault current at this gate voltage.

8.4.8 Thermal Considerations

Sources of nearby local PCB heating must be considered during the thermal design. Typical calculations assume that the TPS23753A is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS23753A device to experience an OTSD event if it is excessively heated by a nearby device.

8.4.9 FRS and Synchronization

The FRS pin programs the (free-running) oscillator frequency, and may also be used to synchronize the TPS23753A converter to a higher frequency. The internal oscillator sets the maximum duty cycle and controls the current-compensation ramp circuit, making the ramp height independent of frequency. R_{FRS} must be selected per Equation 5.

$$R_{FRS}(k\Omega) = \frac{15000}{f_{SW}(kHz)} \tag{5}$$

The TPS23753A may be synchronized to an external clock to eliminate beat frequencies from a sampled system, or to place emission spectrum away from an RF input frequency. Synchronization may be accomplished by applying a short pulse (> 25 ns) of magnitude V_{SYNC} to FRS as shown in Figure 8-7. R_{FRS} must be chosen so that the maximum free-running frequency is just below the desired synchronization frequency. The synchronization pulse terminates the potential ON-time period, and the OFF-time period does not begin until the pulse terminates. A short pulse is preferred to avoid reducing the potential ON-time.

Figure 8-7 shows examples of nonisolated and transformer-coupled synchronization circuits RT reduces noise susceptibility for the isolation transformer implementation. The FRS node must be protected from noise because it is high impedance.

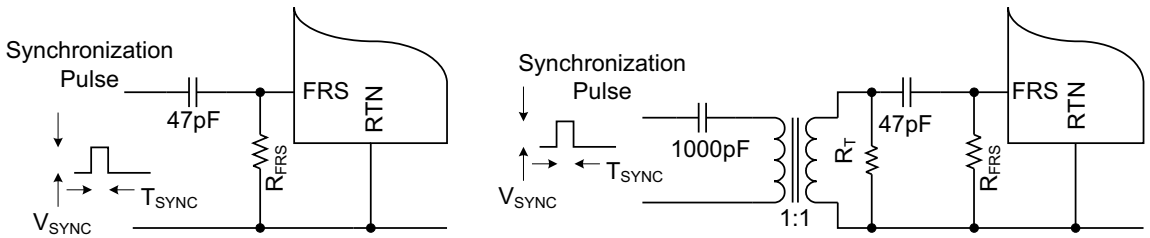


Figure 8-7. Synchronization

8.4.10 Blanking – R_{BLNK}

The TPS23753A BLNK feature permits programming of the blanking period with specified tolerance. Selection of the blanking period is often empirical because it is affected by parasitics and thermal effects of every device between the gate-driver and output capacitors.

There is a critical range of blanking period that is bounded on the short side by erratic operation, and on the long side by potentially harmful switching-MOSFET and output rectifier currents during a short circuit. The minimum blanking period prevents the current limit and PWM comparators from being falsely triggered by the inherent current *spike* that occurs when the switching MOSFET turns on. The maximum blanking period is bounded by the ability of the output rectifier to withstand the currents experienced during a converter output short.

The TPS23753A provides a choice between internal fixed and programmable blanking periods. The blanking period is specified as an increase in the minimum GATE on time over the inherent gate driver and comparator delays. The default period (see *Electrical Characteristics: Controller Section Only* and *Electrical Characterisics: PoE and Control*) is selected by connecting BLNK to RTN, and the programmable period is set with a resistor from BLNK to RTN using Equation 6.

$$R_{BLNK}\left(k\Omega\right) = t_{BLNK}\left(ns\right) \tag{6}$$

For example, a 100-ns period is programmed by a 100-kΩ resistor. For a brand-new design, TI recommends designing an initial blanking period of 125 ns. This period must be turned when the converter is operational.

8.4.11 Current Slope Compensation

Current-mode control requires addition of a compensation ramp to the sensed inductor (flyback transformer) current for stability at duty cycles near and over 50%. The TPS23753A has a maximum duty cycle limit of 78%, permitting the design of wide input-range flyback converters with a lower voltage stress on the output rectifiers. While the maximum duty cycle is 78%, converters may be designed that run at duty cycles well below this for a narrower, 36-V to 57-V range. The TPS23753A provides a fixed internal compensation ramp that suffices for most applications. R_S (see Figure 8-8) may be used if the internally provided slope compensation is not enough. It works with ramp current (I_{PK} = I_{SL-EX}, approximately 40 µA) that flows out of the CS pin when the MOSFET is on. The I_{PK} specification does not include the approximately 3-µA fixed current that flows out of the CS pin.

Most current-mode control papers and application notes define the slope values in terms of V_{PP}/T_S (peak ramp voltage / switching period); however, *Electrical Characteristics: Controller Section Only* specifies the slope peak (V_{SLOPE}) based on the maximum duty cycle. Assuming that the desired slope, $V_{SLOPE-D}$ (in mV/period), is based on the full period, compute R_S per Equation 7 where V_{SLOPE}, D_{MAX}, and I_{SL-EX} are from *Electrical Characteristics: Controller Section Only* with voltages in mV, current in µA, and the duty cycle is unitless (for example, D_{MAX} = 0.78).

$$R_S(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(V_{SLOPE}(mV) / D_{MAX}\right)\right]}{I_{SL\_EX}(\mu A)} \cdot 1000 \tag{7}$$

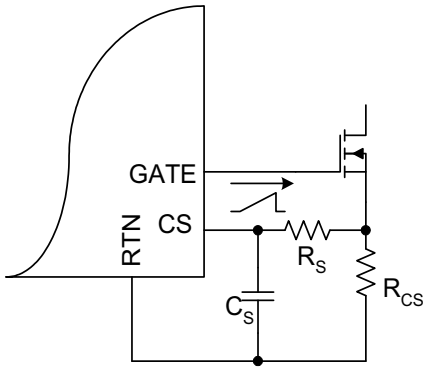


Figure 8-8. Additional Slope Compensation

C_S may be required if the presence of R_S causes increased noise, due to adjacent signals like the gate drive, to appear at the C_S pin. The TPS23753A has an internal pulldown on C_S (approximately 400 Ω maximum) while the MOSFET is OFF to reduce cycle-to-cycle carry-over voltage on C_S.

8.4.12 Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the

TPS23753A supports forced operation from either of the power sources. Figure 8-9 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS23753A PoE input, option 2 applies power between the TPS23753A PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. A detailed discussion of the TPS23753A and ORing solutions is covered in application note *Advanced Adapter ORing Solutions using the TPS23753*, (SLVA306).

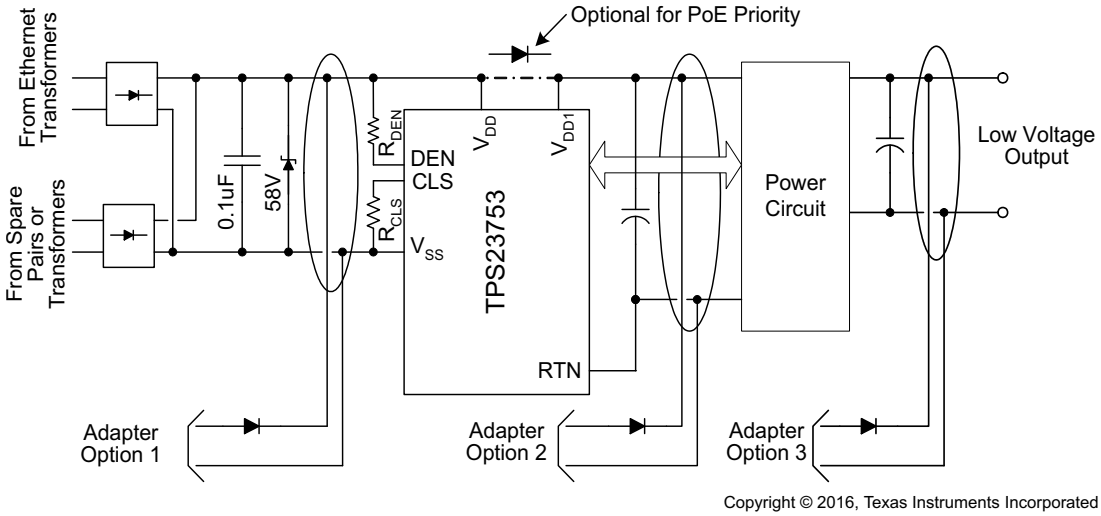


Figure 8-9. ORing Configurations

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors contributing to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, PD inrush, and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult if not impossible for many of the combinations. However, the TPS23753A offers several built-in features that simplify some combinations.

Several examples demonstrate the limitations inherent in ORing solutions. Diode ORing a 48-V adapter with PoE (option 1) presents the problem that either source might be higher. A blocking switch would be required to assure which source was active. A second example is combining a 12-V adapter with PoE using option 2. The converter draws approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while C_{IN} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example is use of a 12-V adapter with ORing option 1. The PD hotswap would have to handle four times the current, and have 1/16 the resistance (be 16 times larger) to dissipate equal power. A fourth example is that MPS is lost when running from the adapter, causing the PSE to remove power from the PD. If adapter power is then lost, the PD stops operating until the PSE detects and powers the PD.

The most popular preferential ORing scheme is option 2 with adapter priority. The hotswap MOSFET is disabled when the adapter is used to pull APD high, blocking the PoE source from powering the output. This solution works well with a wide range of adapter voltages, is simple, and requires few external parts. When the AC power fails, or the adapter is removed, the hotswap switch is enabled. In the simplest implementation, the PD momentarily loses power until the PSE completes its start-up cycle.

The DEN pin can be used to disable the PoE input when ORing with option 3. This is an adapter priority implementation. Pulling DEN low, while creating an invalid detection signature, disables the hotswap MOSFET, and prevents the PD from redetecting. This would typically be accomplished with an optocoupler that is driven from the secondary side of the converter.

The least popular technique is PoE priority. It is implemented by placing a diode between the PD supply voltage, V_{DD}, and the DC-DC controller bias voltage, V_{DD1}. The diode prevents reverse biasing of the PoE input diode bridges when option 2 adapter ORing is used. The PSE may then detect, classify, and provide power to the PD

while a live adapter is connected. As long as the PoE voltage is greater than the adapter voltage, the PSE powers the load. The APD function is not used in this technique.

The IEEE standards require that the PI conductors be electrically isolated from ground and all other system potentials not part of the PI interface. The adapter must meet a minimum 1500-Vac dielectric withstand test between the output and all other connections for options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse-voltage adapter, a short on the adapter input pins, and damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

8.4.13 Protection

A TVS across the rectified PoE voltage per Figure 9-1 must be used. For general indoor applications, TI recommends an SMAJ58A or a part with equal to or better performance. If an adapter is connected from V_{DD1} to RTN, as in ORing option 2 above, voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to be within the *Absolute Maximum Ratings*. Configurations that use D_{VDD} as in Figure 8-10 may require additional protection against ESD transients that would turn D_{VDD} off and force all the voltage to appear across the internal hotswap MOSFET. C_{VDD} and D_{RTN} per Figure 8-10 provide this additional protection.

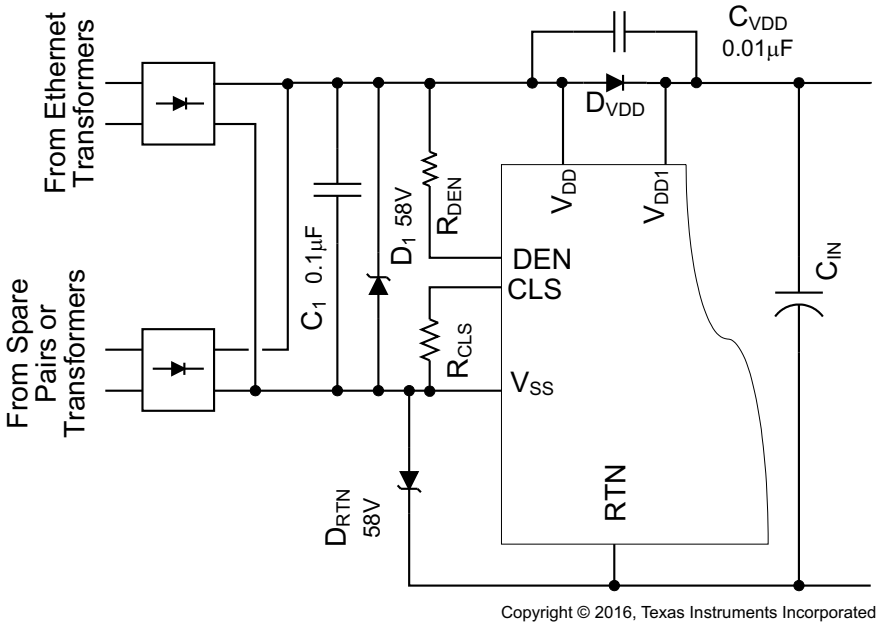


Figure 8-10. Additional Protection Against ESD

Outdoor applications require more extensive protection to lightning standards.

8.4.14 Frequency Dithering for Conducted Emissions Control

The international standard CISPR 22 (and adopted versions) is often used as a requirement for conducted emissions. Ethernet cables are covered as a telecommunication port under section 5.2 for conducted emissions. Meeting EMI requirements is often a challenge, with the lower limits of Class B being especially hard. Circuit board layout, filtering, and snubbing various nodes in the power circuit are the first layer of control techniques. A more detailed discussion of EMI control is presented in *Practical Guidelines to Designing an EMI Compliant PoE Powered Device With Isolated Flyback*, SLUA469. Additionally, IEEE 802.3at sections 33.3 and 33.4 have requirements for noise injected onto the Ethernet cable based on compatibility with data transmission.

Occasionally, a technique referred to as frequency dithering is used to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider

bandwidth, thus lowering peak measurements. The circuit of Figure 8-11 modulates the switching frequency by feeding a small AC signal into the FRS pin. These values may be adapted to suit individual needs.

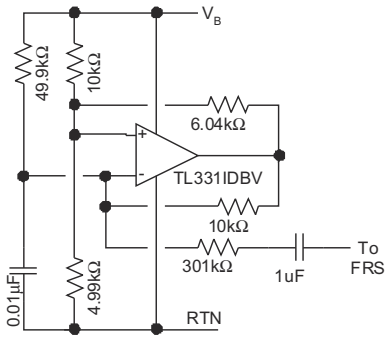


Figure 8-11. Frequency Dithering

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS23753A supports power supply topologies that require a single PWM gate drive with current-mode control. Figure 9-1 provides an example of a simple diode rectified flyback converter.

9.2 Typical Application

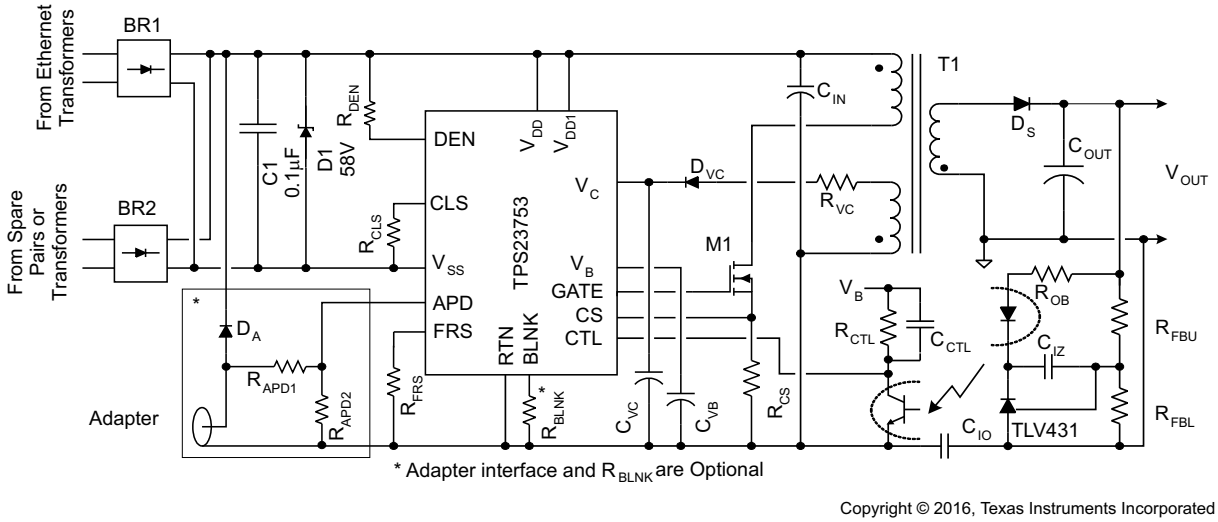


Figure 9-1. Basic TPS23753A Implementation

9.2.1 Design Requirements

Selecting a converter topology along with a design procedure is beyond the scope of this applications section.

For more specific converter design examples refer to the following application notes:

- *Advanced Adapter ORing Solutions using the TPS23753*, SLVA306
- *Implementing a Buck Converter with the TPS23753A*, SLVA440
- *Using the TPS23753A with an External Error Amplifier*, SLVA433

9.2.2 Detailed Design Procedure

A detailed design procedure for PDs using the TPS23753A is covered in *Designing with the TPS23753 Powered Device and Power Supply Controller*, SLVA305. Several designs with data are provided in the evaluation module documentation SLVU314 and SLVU315.

9.2.3 Application Curves

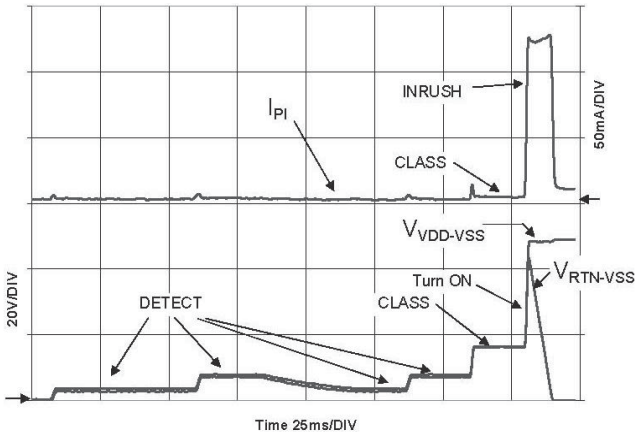


Figure 9-2. PoE Start-Up Sequence

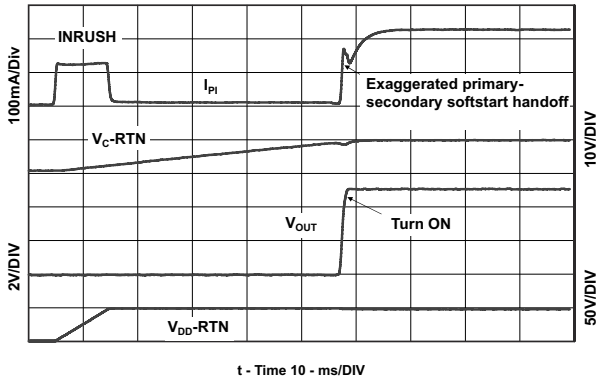


Figure 9-3. Power Up and Start

10 Power Supply Recommendations

The TPS23753A converter must be designed such that the input voltage of the converter is capable of operating within the IEEE802.3at-recommended input voltage as shown in Figure 8-1 and the minimum operating voltage of the adapter if applicable.

11 Layout

11.1 Layout Guidelines

Printed-circuit board layout recommendations are provided in the evaluation module (EVM) documentation available for these devices.

11.2 Layout Example

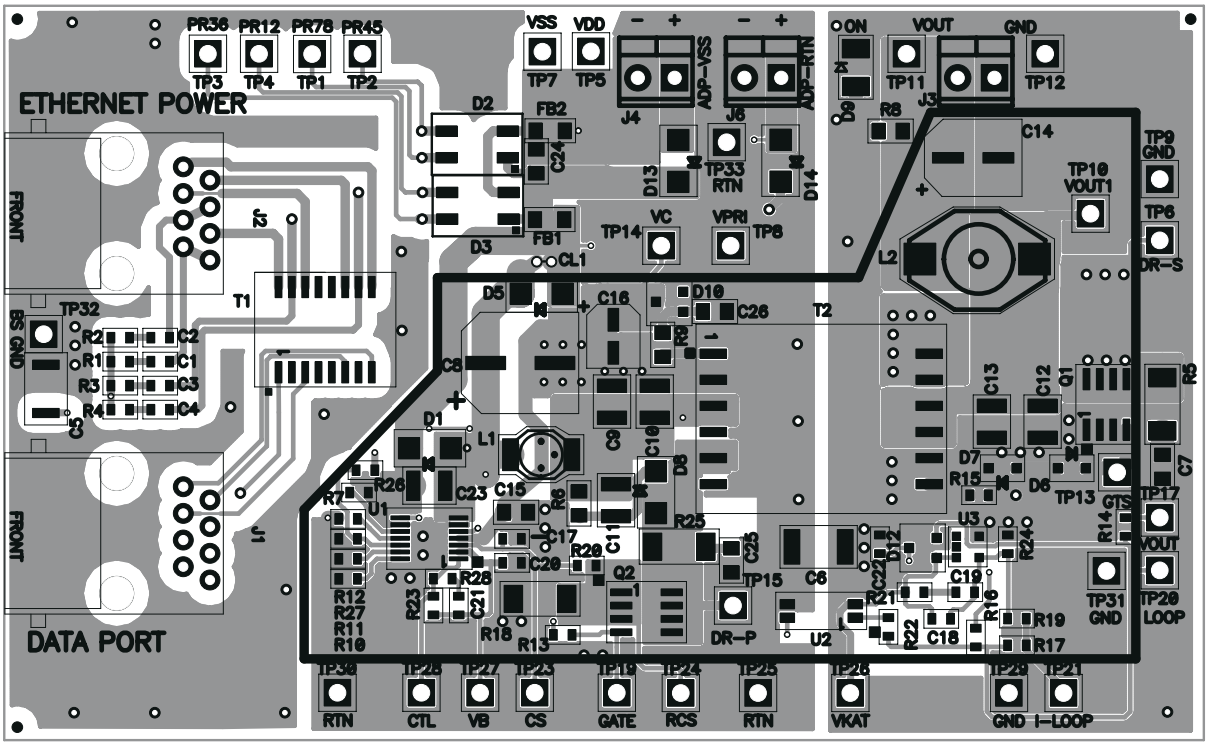


Figure 11-1. Top-Side Placement

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *IEEE Standard for Information Technology … Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications*, IEEE Computer Society, IEEE 802.3™at (Clause 33)
- *Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement*, International Electrotechnical Commission, CISPR 22 Edition 5.2, 2006-03
- *Designing with the TPS23753 Powered Device and Power Supply Controller*, Eric Wright, TI, SLVA305
- *Advanced Adapter ORing Solutions using the TPS23753*, Eric Wright, TI, SLVA306
- *Practical Guidelines to Designing an EMI-Compliant PoE Powered Device With Isolated Flyback*, Donald V. Comiskey, TI, SLUA469
- *TPS23753AEVM-004: Evaluation Module for TPS23753A*, SLVU314
- *TPS23753AEVM-0041 Evaluation Module for TPS23753A*, SLVU315
- *Implementing a Buck Converter with the TPS23753A*, SLVA440
- *Using the TPS23753A with an External Error Amplifier*, SLVA433

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS23753APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23753A	Samples
TPS23753APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23753A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

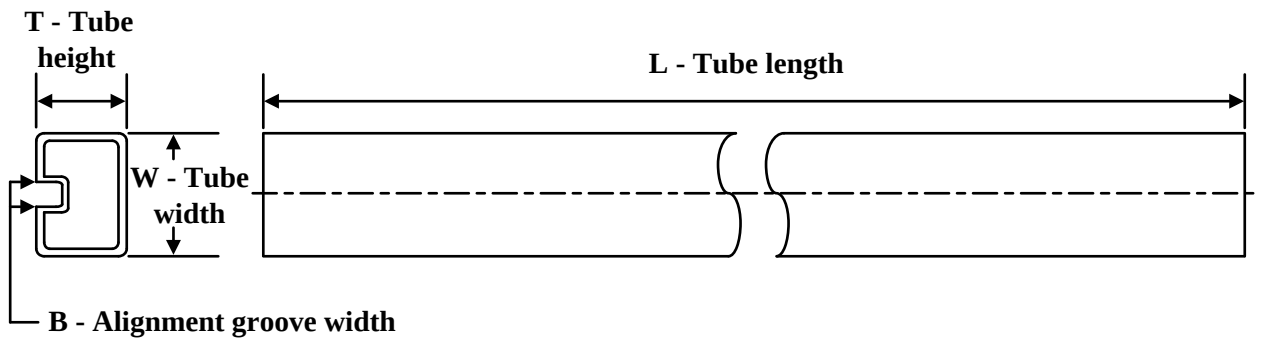
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

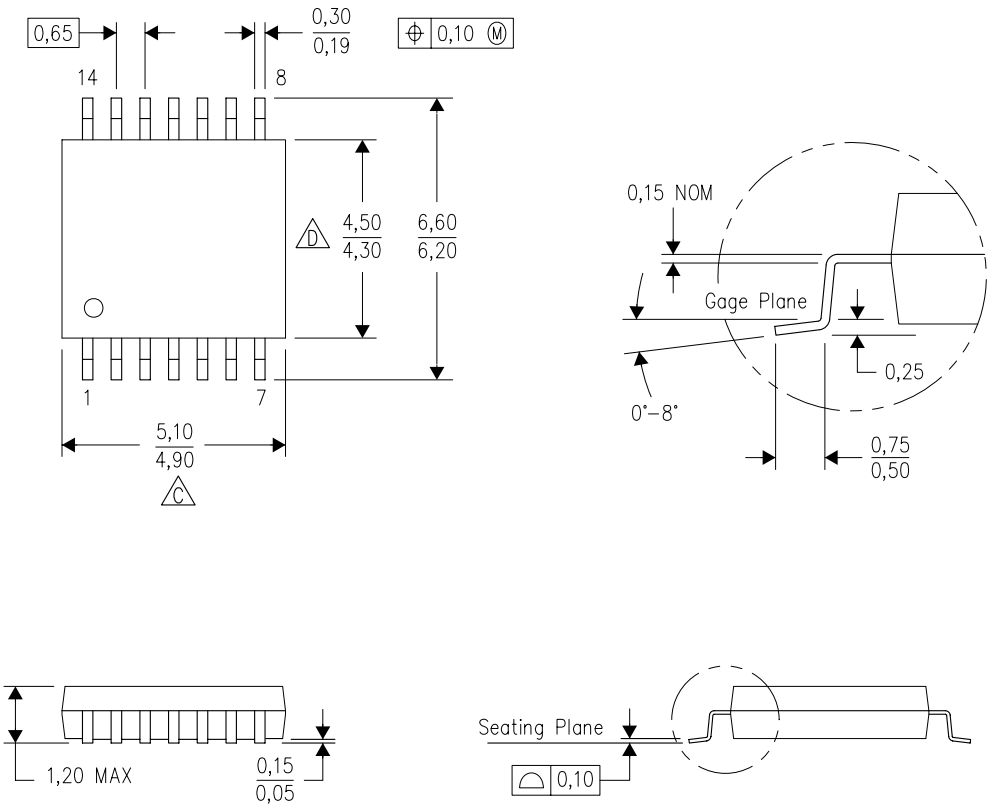
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS23753APW	PW	TSSOP	14	90	530	10.2	3600	3.5

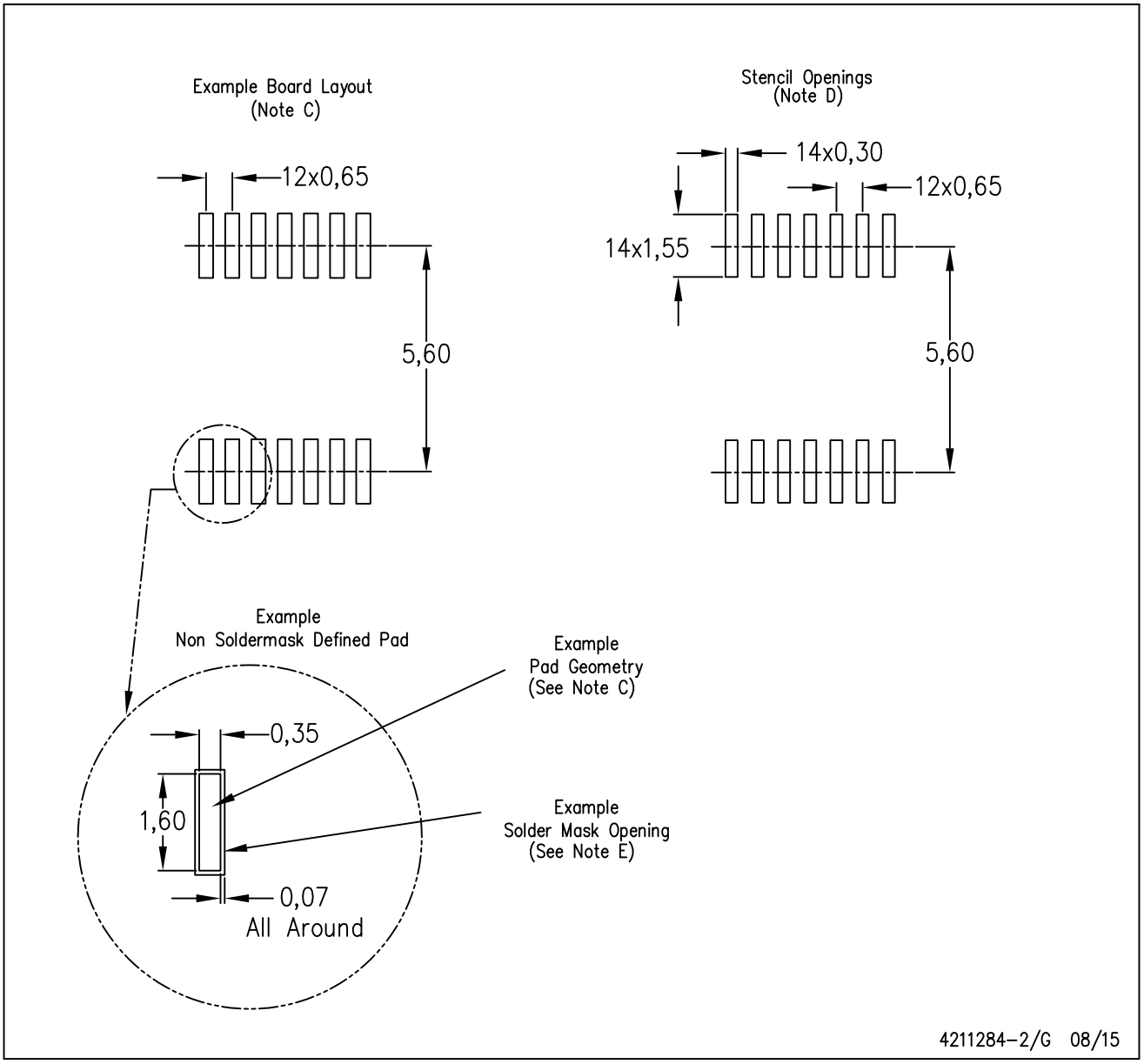
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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