LM4898 Boomer® Audio Power Amplifier Series 1 Watt Fully Differential Audio Power Amplifier With Shutdown Select

Check for Samples: LM4898, LM4898MMBD

FEATURES

- **Fully Differential Amplification**
- **Available in Space-Saving Packages DSBGA, VSSOP, and WSON**
- **Ultra Low Current Shutdown Mode**
- **Can Drive Capacitive Loads up to 500pF**
- **Improved Pop and Click Circuitry Eliminates Noises During Turn-On and Turn-Off Transitions**
- **2.4 - 5.5V Operation**
- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**
- **Shutdown High or Low Selectivity**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **Improved PSRR at 217Hz: 83 dB(typ)**
- **Power Output at 5.0V, 1% THD: 1.0 W(typ)**
- **Power Output at 3.3V, 1% THD: 400 mW(typ)**
- **Shutdown Current: 0.1µA(typ)**

DESCRIPTION

The LM4898 is a fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4898 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4898 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown select pin to be driven in a likewise manner to enable Shutdown. Additionally, the LM4898 features an internal thermal shutdown protection mechanism.

The LM4898 contains advanced pop and click circuitry which virtually eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Connection Diagrams

Top View

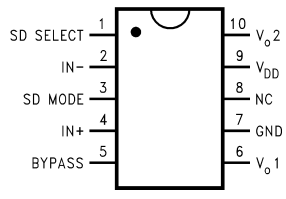

Figure 1. VSSOP Package
See Package Number DGS0010A

Top View

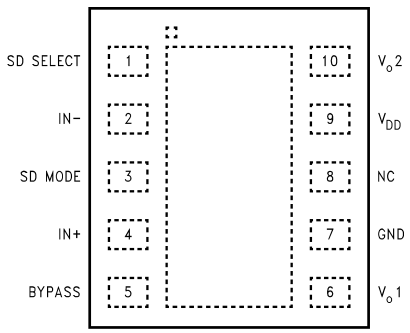

Figure 2. WSON Package
See Package Number NGZ0010B

Top View

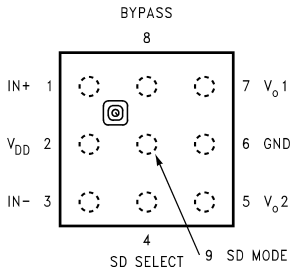

Figure 3. 9 Bump DSBGA Package
See Package Number YZR0009AAA

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Typical Application

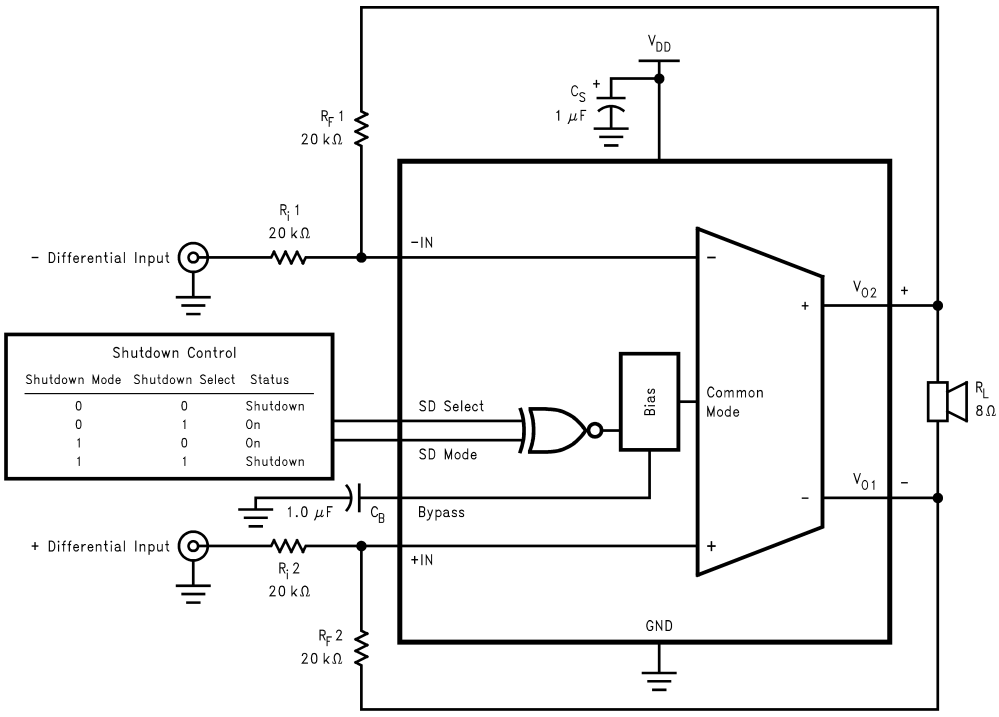


Figure 4. Typical Audio Amplifier Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation (3)		Internally Limited
ESD Susceptibility (4)		2000V
ESD Susceptibility (5)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (WSON)	12°C/W
	θ_{JA} (WSON)	63°C/W
	θ_{JA} (DSBGA)	220°C/W
	θ_{JC} (VSSOP)	56°C/W
	θ_{JA} (VSSOP)	190°C/W
For Soldering Information, see AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009).		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics VDD = 3V state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

(4) Human body model, 100pF discharged through a 1.5kΩ resistor.

(5) Machine Model, 220pF–240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage		$2.4V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (1) (2) (3)

The following specifications apply for V_{DD} = 5V, 8Ω load, and A_V = 1V/V, unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4898		Units (Limits)
			Typ(4)	Limit(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load	3	6	mA (max)
		V_{IN} = 0V, R_L = 8 Ω	5	10	
I_{SD}	Shutdown Current	V_{SDMODE} = $V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
P_o	Output Power	THD = 1% (max); f = 1 kHz			
		LM4898LD, R_L= 4Ω(6)	1.4		W (min)
		LM4898, R_L= 8Ω	1	0.9	
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4 Wrms; f = 1kHz	0.05		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p			
		f = 217Hz (7)	83		dB (min)
		f = 1kHz (7)	90		
		f = 217Hz (8)	83	71	
		f = 1kHz (8)	83	71	
CMRR	Common_Mode Rejection Ratio	f = 217Hz V_{CM} = 200mV_{DD}	50		dB
V_{OS}	Output Offset	V_{IN} = 0V	2		mV
V_{SDIH}	Shutdown Voltage Input High	SD Mode = GND	0.9		V
V_{SDIL}	Shutdown Voltage Input Low	SD Mode = GND	0.7		V
V_{SDIH}	Shutdown Voltage Input High	SD Mode = V_{DD}	0.9		V
V_{SDIL}	Shutdown Voltage Input Low	SD Mode = V_{DD}	0.7		V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics VDD = 3V state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) When driving 4Ω loads from a 5V supply, the LM4898LD must be mounted to a circuit board with the exposed-DAP area soldered down to a 1sq. in plane of 1oz. copper.
(7) Unterminated input.
(8) 10Ω terminated input.

Electrical Characteristics V_{DD} = 3V(1) (2) (3)

The following specifications apply for V_{DD} = 3V, 8Ω load and A_V = 1V/V, unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM4898		Units (Limits)
			Typ(4)	Limit(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, no load	2.5	5 .5	mA (max)
		V_{IN} = 0V, R_L = 8 Ω	4	9	
I_{SD}	Shutdown Current	V_{SDMODE} = $V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
P_o	Output Power	THD = 1% (max); f = 1kHz LM4898, RL = 8Ω	0.35		W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.25Wrms; f = 1kHz	0.03		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p			
		f = 217Hz (6)	83		dB
		f = 1kHz (6)	84		
		f = 217Hz (7)	83		
		f = 1kHz (7)	83		
CMRR	Common-Mode Rejection Ratio	f = 217Hz V_{CM} = 200mV_{PP}	50		dB
V_{OS}	Output Offset	V_{IN} = 0V	2		mV
V_{SDIH}	Shutdown Voltage Input High	SD Mode = GND	0.8		V
V_{SDIL}	Shutdown Voltage Input Low	SD Mode = GND	0.6		V
V_{SDIH}	Shutdown Voltage Input High	SD Mode = V_{DD}	0.8		V
V_{SDIL}	Shutdown Voltage Input Low	SD Mode = V_{DD}	0.6		V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics VDD = 3V state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.
(4) Typicals are measured at 25°C and represent the parametric norm.
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Unterminated input.
(7) 10Ω terminated input.

External Components Description

(See Figure 4)

Components		Functional Description
1.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
2.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B.
3.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f.
4.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.

Typical Performance Characteristics
NGZ0010B Specific Characteristics

THD+N vs Output Power
V_{DD} = 5V, R_L = 4Ω

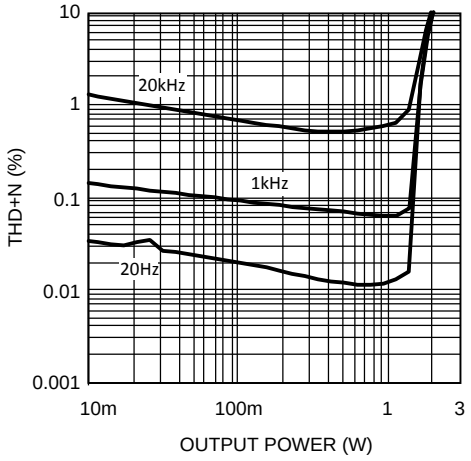


Figure 5.

THD+N vs Frequency
V_{DD} = 5V, R_L = 4Ω, P_O = 1W

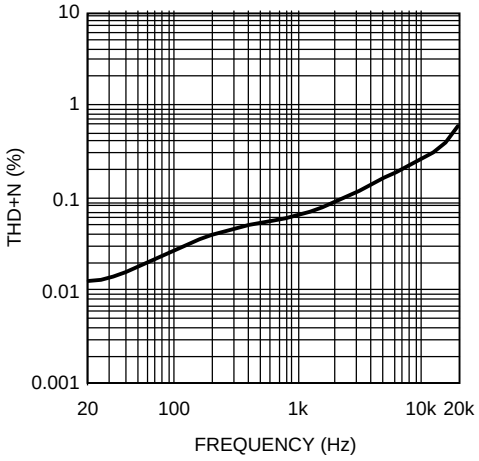


Figure 6.

LM4898
Power Dissipation vs Output Power

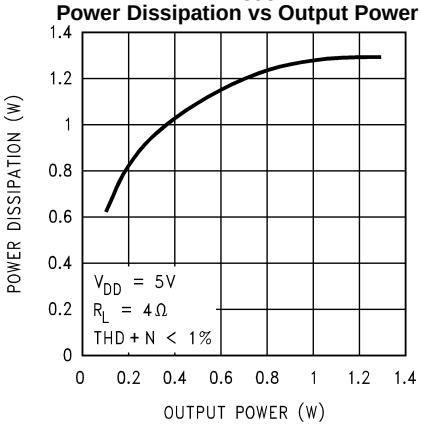


Figure 7.

LM4898
Power Derating Curve

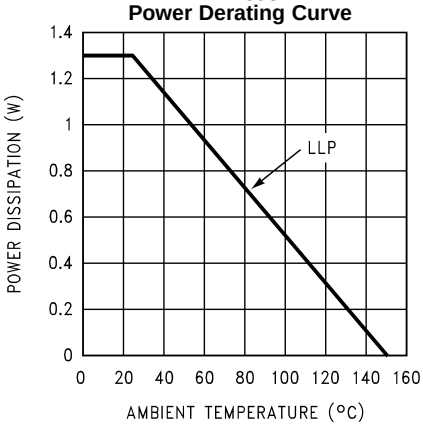


Figure 8.

Typical Performance Characteristics
Non-NGZ0010B Specific Characteristics

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 400mW

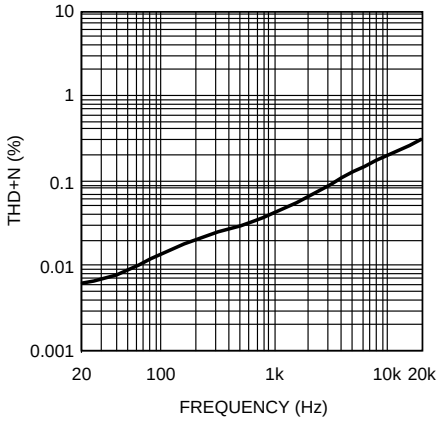


Figure 9.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, P_O = 275mW

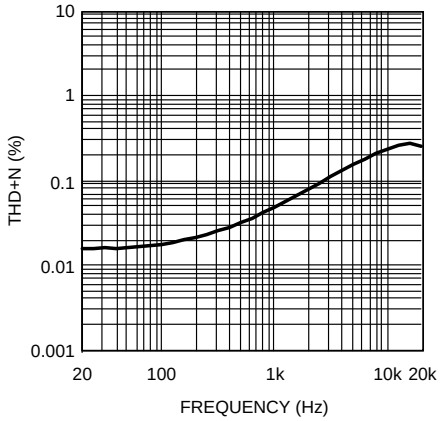


Figure 10.

THD+N vs Frequency
V_{DD} = 3V, R_L = 4Ω, P_O = 225mW

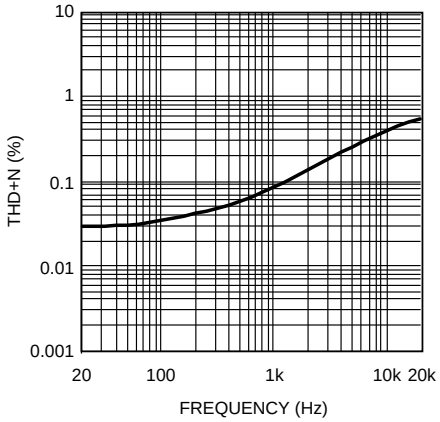


Figure 11.

THD+N vs Frequency
V_{DD} = 2.6V, R_L = 8Ω, P_O = 150mW

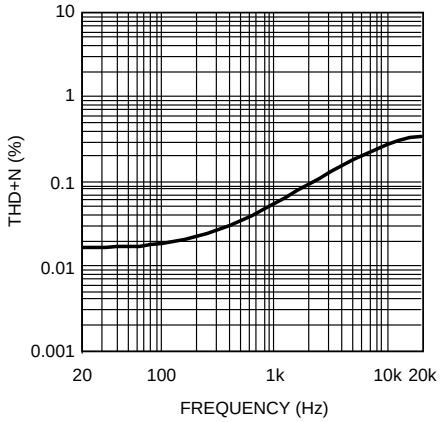


Figure 12.

THD+N vs Frequency
V_{DD} = 2.6V, R_L = 4Ω, P_O = 150mW

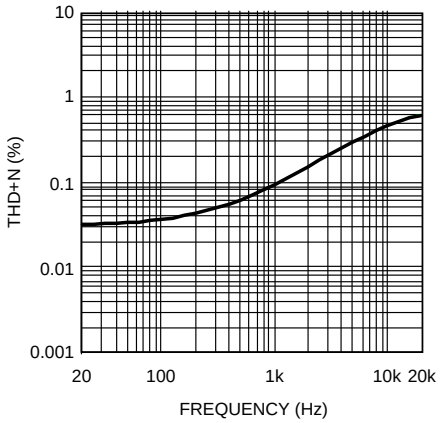


Figure 13.

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω

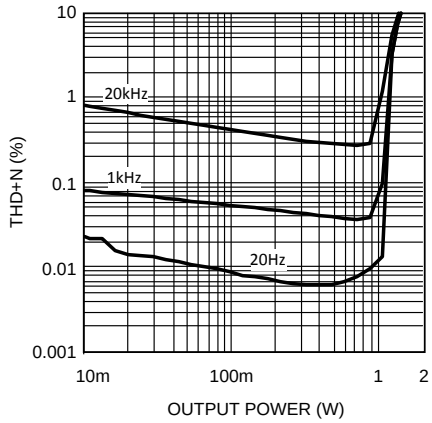


Figure 14.

Typical Performance Characteristics
Non-NGZ0010B Specific Characteristics (continued)

THD+N vs Output Power
V_{DD} = 3V, R_L = 8Ω

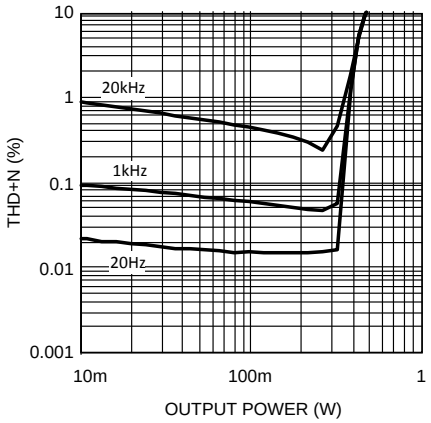


Figure 15.

THD+N vs Output Power
V_{DD} = 3V, R_L = 4Ω

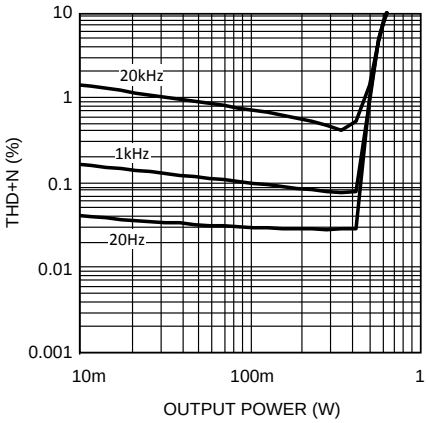


Figure 16.

THD+N vs Output Power
V_{DD} = 2.6V, R_L = 8Ω

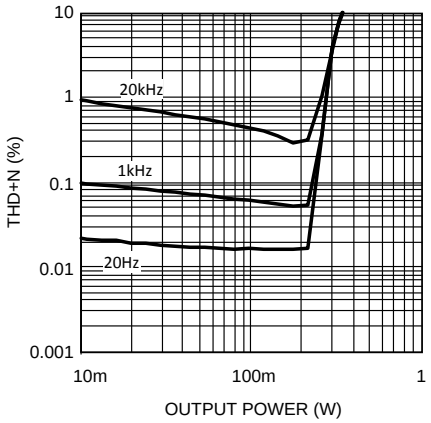


Figure 17.

THD+N vs Output Power
V_{DD} = 2.6V, R_L = 4Ω

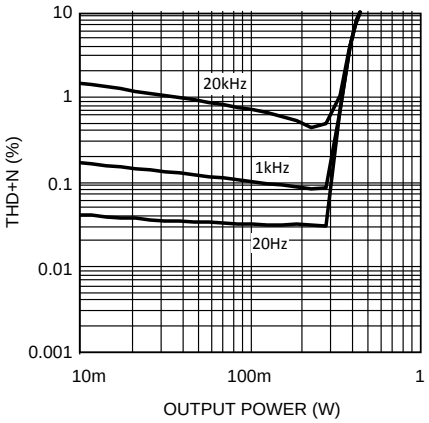


Figure 18.

PSRR vs Frequency
V_{DD} = 5V, R_L = 8Ω, Input 10Ω Terminated

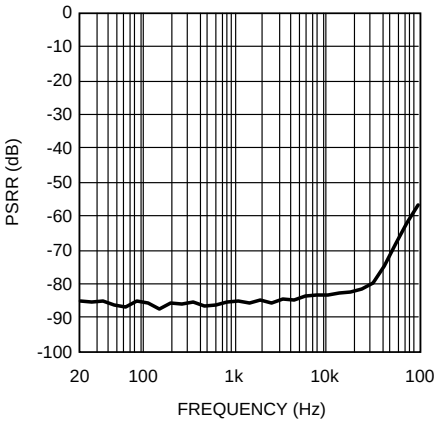


Figure 19.

PSRR vs Frequency
V_{DD} = 3V, R_L = 8Ω, Input 10Ω Terminated

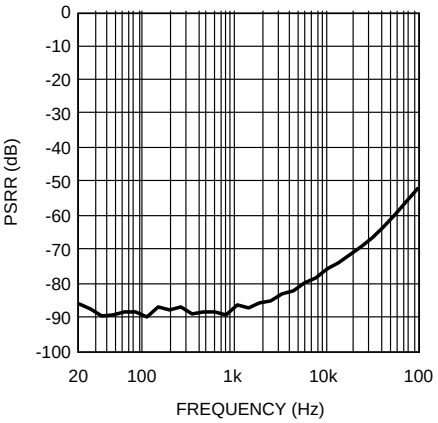


Figure 20.

Typical Performance Characteristics

Non-NGZ0010B Specific Characteristics (continued)

Output Power vs Supply Voltage
R_L = 8Ω

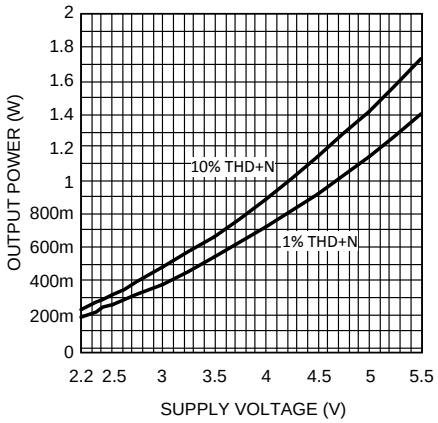


Figure 21.

Output Power vs Supply Voltage
R_L = 4Ω

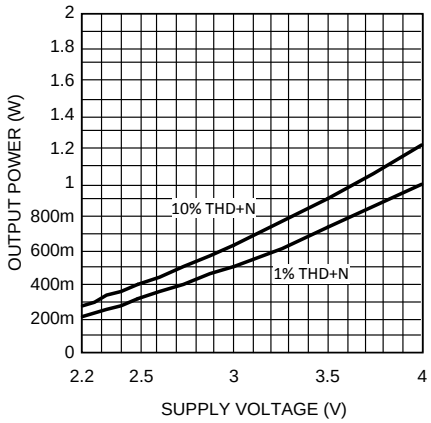


Figure 22.

Power Dissipation vs Output Power

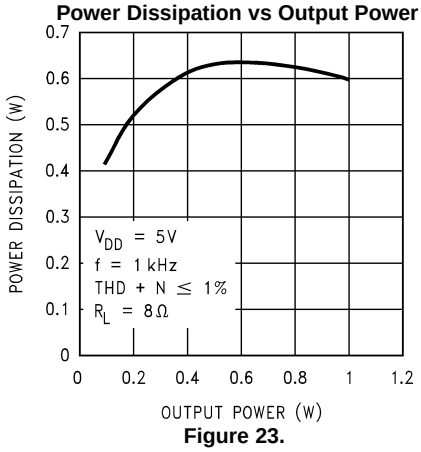


Figure 23.

Power Dissipation vs Output Power

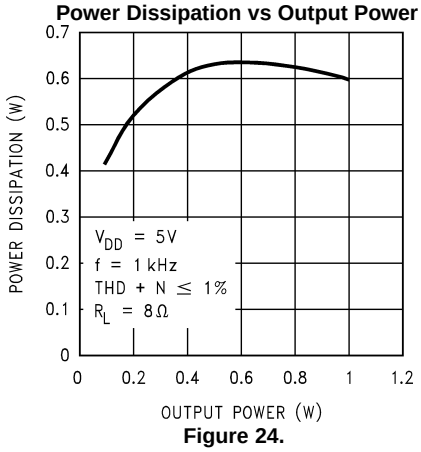


Figure 24.

Power Dissipation vs Output Power

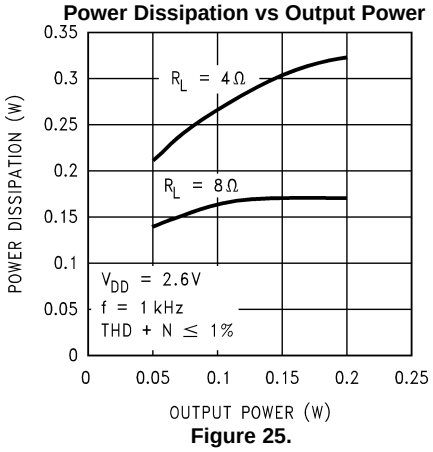


Figure 25.

Output Power vs Load Resistance

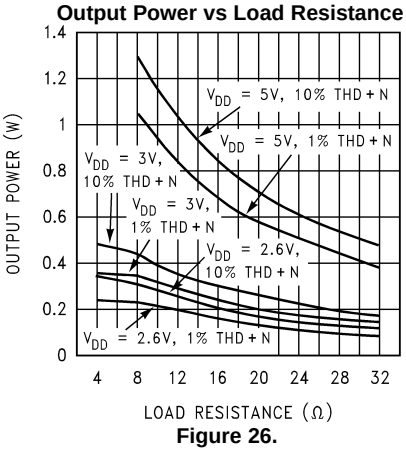


Figure 26.

Typical Performance Characteristics

Non-NGZ0010B Specific Characteristics (continued)

Supply Current vs Shutdown Voltage Shutdown Low

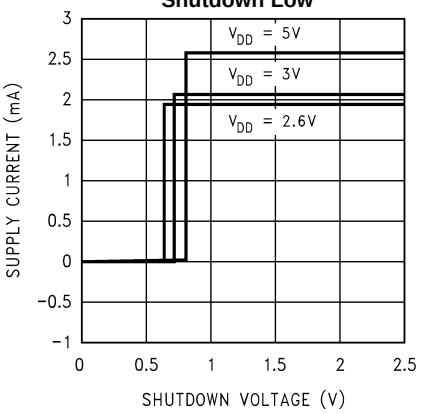


Figure 27.

Supply Current vs Shutdown Voltage Shutdown High

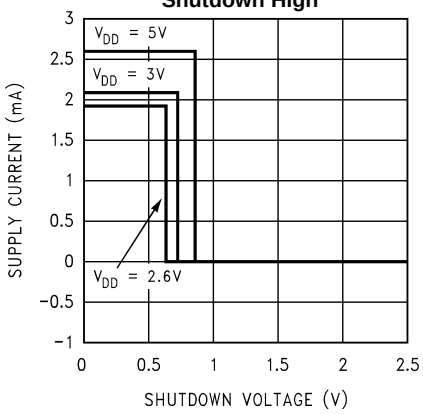


Figure 28.

Clipping (Dropout) Voltage vs Supply Voltage

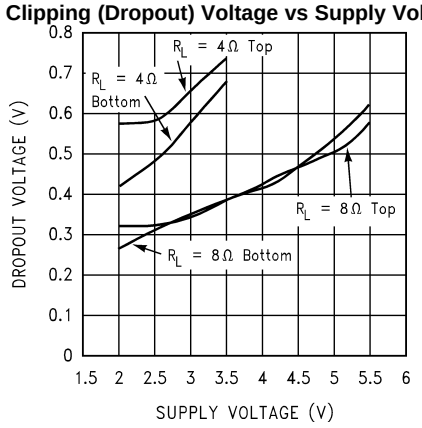


Figure 29.

Open Loop Frequency Response

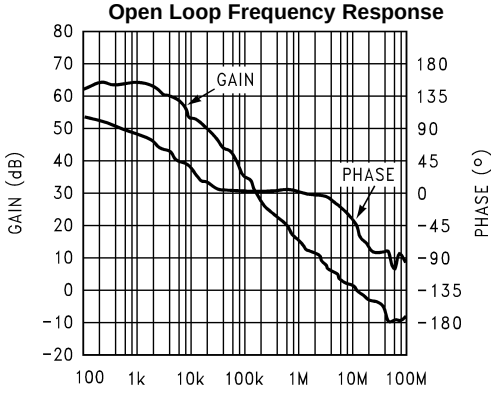


Figure 30.

Power Derating Curve

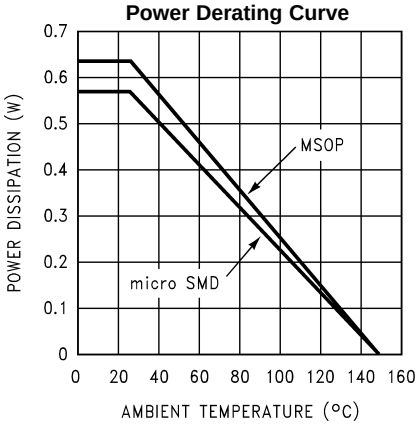


Figure 31.

Noise Floor

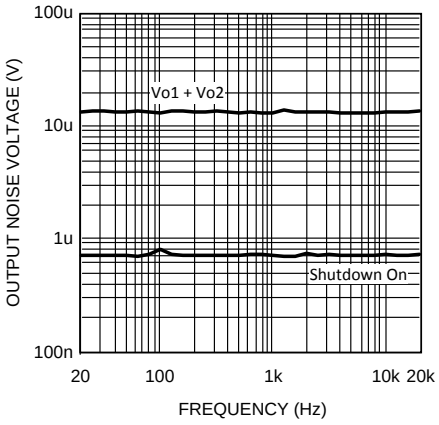


Figure 32.

Typical Performance Characteristics

Non-NGZ0010B Specific Characteristics (continued)

CMRR vs Frequency
V_{DD} = 5V, R_L = 8Ω, 200mV_{pp}

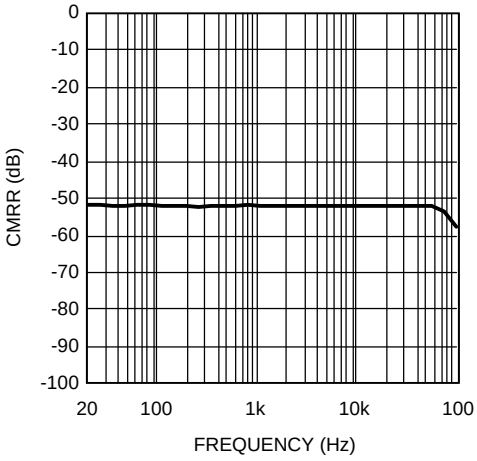


Figure 33.

CMRR vs Frequency
V_{DD} = 3V, R_L = 8Ω, 200mV_{pp}

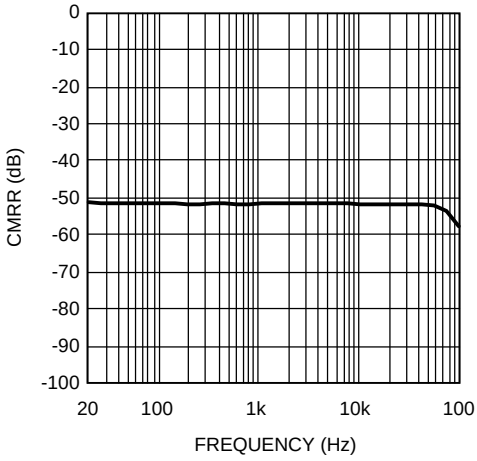


Figure 34.

PSRR vs Common Mode Voltage
V_{DD} = 5V

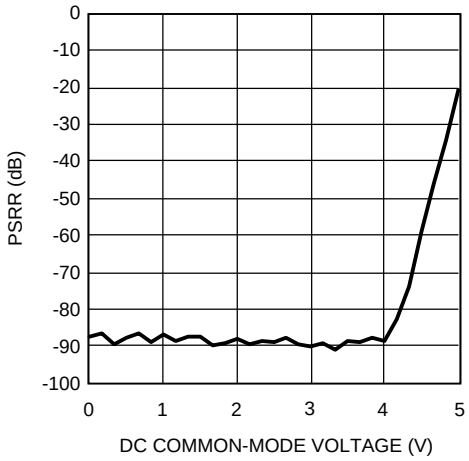


Figure 35.

PSRR vs Common Mode Voltage
V_{DD} = 3V, R_L = 8Ω, 217Hz, 200mV_{pp}

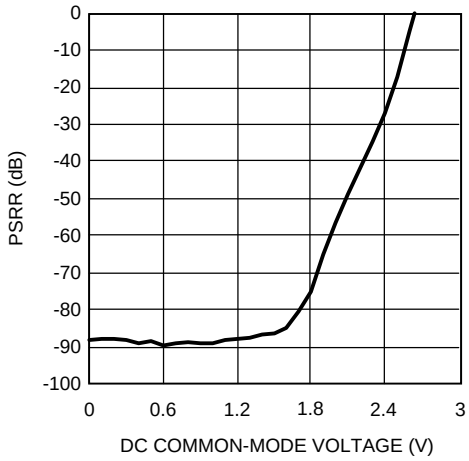


Figure 36.

APPLICATION INFORMATION

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM4898 is a fully differential audio amplifier that features differential input and output stages. Internally this is accomplished by two circuits: a differential amplifier and a common mode feedback amplifier that adjusts the output voltages so that the average value remains $V_{DD}/2$. When setting the differential gain, the amplifier can be considered to have two "halves". Each half uses an input and feedback resistor (R_i1 and R_f1) to set its respective closed-loop gain (see Figure 4). With $R_i1 = R_i2$ and $R_f1 = R_f2$, the gain is set at $-R_f/R_i$ for each half. This results in a differential gain of

$$A_{VD} = -R_f/R_i \quad (1)$$

It is extremely important to match the input resistors to each other, as well as the feedback resistors to each other for best amplifier performance. See the PROPER SELECTION OF EXTERNAL COMPONENTS section for more information. A differential amplifier works in a manner where the difference between the two input signals is amplified. In most applications, this would require input signals that are 180° out of phase with each other. The LM4898 can be used, however, as a single ended input amplifier while still retaining its fully differential benefits. In fact, completely unrelated signals may be placed on the input pins. The LM4898 simply amplifies the difference between them.

All of these applications, either single-ended or fully differential, provide what is known as a "bridged mode" output (bridge-tied-load, BTL). This results in output signals at Vo1 and Vo2 that are 180° out of phase with respect to each other. Bridged mode operation is different from the single-ended amplifier configuration that connects the load between the amplifier output and ground. A bridged amplifier design has distinct advantages over the single-ended configuration: it provides differential drive to the load, thus doubling maximum possible output swing for a specific supply voltage. Four times the output power is possible compared with a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excess clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN.

A bridged configuration, such as the one used in the LM4898, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2,are biased at half-supply, no net DC voltage exists across the load. This assumes that the input resistor pair and the feedback resistor pair are properly matched (see PROPER SELECTION OF EXTERNAL COMPONENTS). BTL configuration eliminates the output coupling capacitor required in single supply, single-ended amplifier configurations. If an output coupling capacitor is not used in a single-ended output configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage. Further advantages of bridged mode operation specific to fully differential amplifiers like the LM4898 include increased power supply rejection ratio, common-mode noise reduction, and click and pop reduction.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4898's exposed-DAP (die attach paddle) package (NGZ0010B) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.4W at ≤1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4898's high power performance and activate unwanted, though necessary, thermal shutdown protection. The NGZ0010B package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 4 (2x2) vias. The via diameter should be 0.012in - 0.013in with a 0.050in pitch. Ensure efficient thermal conductivity by plating through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4898 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4898's thermal shutdown protection. The LM4898's power derating curve in the TYPICAL PERFORMANCE CHARACTERISTICS shows the maximum power dissipation versus temperature. Further detailed and specific information concerning PCB layout, fabrication, and mounting an WSON package is available from Texas Instruments package Engineering Group under application note AN-1187 (SNOA401).

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 1.4W to1.37W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX}=(V_{DD})^2 /(2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation versus a single-ended amplifier operating at the same conditions.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \text{ Bridge Mode} \quad (3)$$

Since the LM4898 has bridged outputs, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4898 does not require additional heatsinking under most operating conditions and output loading. From Equation 3, assuming a 5V power supply and an 8. load,the maximum power dissipation point is 625mW. The maximum power dissipation point obtained from Equation 3 must not be greater than the power dissipation results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (4)$$

The LM4898's θ_{JA} in an DGS0010A package is 190°C/W. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased, the ambient temperature reduced, or theθ_{JA} reduced with heatsinking. In many cases, larger traces near the output, V_{DD}, and GND pins can be used to lower the θ_{JA}. The larger areas of copper provide a form of heatsinking allowing higher power dissipation. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 30°C provided that device operation is around the maximum power dissipation point. Recall that internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the LM4898 can operate at higher ambient temperatures. Refer to the TYPICAL PERFORMANCE CHARACTERISTICS curves for power dissipation information.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection ratio (PSRR). The capacitor location on both the bypass and power supply pins should be as close to the device as possible. A larger half-supply bypass capacitor improves PSRR because it increases half-supply stability. Typical applications employ a 5V regulator with 10µF and0.1µF bypass capacitors that increase supply stability. This, however, does not eliminate the need for bypassing the supply nodes of the LM4898. Although the LM4898 will operate without the bypass capacitor C_B, the PSRR may decrease. A 1µF capacitor is recommended for C_B. This value maximizes PSRR performance. Lesser values may be used, but PSRR decreases at frequencies below 1kHz. The issue of C_B selection is thus dependant upon desired PSRR and click and pop performance as explained in the PROPER SELECTION OF EXTERNAL COMPONENTS.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4898 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. In addition, the LM4898 contains a Shutdown Mode pin, allowing the designer to designate whether the part will be driven into shutdown with a high level logic signal or a low level logic signal. This allows the designer maximum flexibility in device use, as the Shutdown Mode pin may simply be tied permanently to either V_{DD} or GND to set the LM4898 as either a "shutdown-high" device or a "shutdown-low" device, respectively. The device may then be placed into shutdown mode by toggling the Shutdown Select pin to the same state as the Shutdown Mode pin. For simplicity's sake, this is called "shutdown same", as the LM4898 enters shutdown mode whenever the two pins are in the same logic state. The trigger point for either shutdown high or shutdown low is shown as a typical value in the Supply Current vs. Shutdown Voltage graphs in the TYPICAL PERFORMANCE CHARACTERISTICS section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current maybe greater than the typical value of 0.1µA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor (or pull-down, depending on shutdown high or low application). This scheme ensures that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical when optimizing device and system performance. Although the LM4898 is tolerant to a variety of external component combinations, consideration of component values must be made when maximizing overall system quality.

The LM4898 is unity-gain stable, giving the designer maximum system flexibility. The LM4898 should be used in low closed-loop gain configurations to minimize THD+N values and maximize signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the AUDIO POWER AMPLIFIER DESIGN section for a more complete explanation of proper gain selection. When used in its typical application as a fully differential power amplifier the LM4898 does not require input coupling capacitors for input sources with DC common-mode voltages of less than V_{DD}. Exact allowable input common-mode voltage levels are actually a function of V_{DD}, R_i, and R_f and may be determined by Equation 5:

$$V_{CMi}<(V_{DD}-1.2)*((R_f+(R_i)/(R_f)-V_{DD}*(R_i/2R_f) \quad (5)$$

$$R_f/R_i=A_{VD} \quad (6)$$

Special care must be taken to match the values of the feedback resistors (R_f1 and R_f2) to each other as well as matching the input resistors (R_i1 and R_i2) to each other (see Figure 4). Because of the balanced nature of differential amplifiers, resistor matching differences can result in net DC currents across the load. This DC current can increase power consumption, internal IC power dissipation, reduce PSRR, and possibly damaging the loudspeaker. The chart below demonstrates this problem by showing the effects of differing values between the feedback resistors while assuming that the input resistors are perfectly matched. The results below apply to the application circuit shown in Figure 4, and assumes that V_{DD} = 5V, R_L = 8Ω, and the system has DC coupled inputs tied to ground.

Tolerance	R_f1	R_f2	Vo2-Vo1	I_{LOAD}
20%	0.8R	1.2R	-0.5V	62.5mA
10%	0.9R	1.1R	-0.250V	31.25mA
5%	0.95R	1.05R	-0.125V	15.63mA
1%	0.99R	1.01R	-0.025V	3.125mA
0	R	R	R	0

Similar results would occur if the input resistors were not carefully matched. Adding input coupling capacitors in between the signal source and the input resistors will eliminate this problem, however, to achieve best performance with minimum component count it is highly recommended that both the feedback and input resistors matched to 1% tolerance or better.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W/8Ω Audio Amplifier

Given:

- Power Output 1W
- Load Impedance 8Ω
- Input Level 1Vrms
- Input Impedance 20kΩ
- Bandwidth 100Hz–20kHz ± 0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. The supply rail can easily be found by extrapolating from the Output Power vs. Supply Voltage graphs in the Typical Performance Characteristics section. A second way to determine the minimum supply rail is to calculate the required Vopeak using Equation 7 and add the dropout voltages. Using this method, the minimum supply voltage is (Vopeak +($V_{DO\ TOP}$+($V_{DO\ BOT}$)),where $V_{DO\ BOT}$ and $V_{DO\ TOP}$ are extrapolated from the Dropout Voltage vs. Supply Voltage curve in the Typical Performance Characteristics section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{7}$$

Using the Output Power vs. Supply Voltage graph for an 8Ω load, the minimum supply rail just about 5V. Extra supply voltage creates headroom that allows the LM4898 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section. Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 8.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{8}$$

$R_f / R_i = A_{VD}$

From Equation 8, the minimum A_{VD} is 2.83. Since the desired input impedance was 20kΩ, a ratio of 2.83:1 of R_f to R_i results in an allocation of R_i = 20kΩ for both input resistors and R_f= 60kΩ for both feedback resistors. The final design step is to address the bandwidth requirement which must be stated as a single -3dB frequency point. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

f_H = 20kHz * 5 =100kHz

The high frequency pole is determined by the product of the desired frequency pole, f_H , and the differential gain, A_{VD} .With a A_{VD} = 2.83 and f_H = 100kHz, the resulting GBWP = 150kHz which is much smaller than the LM4898 GBWP of 10MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4898 can still be used without running into bandwidth limitations.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4898MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	GB3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

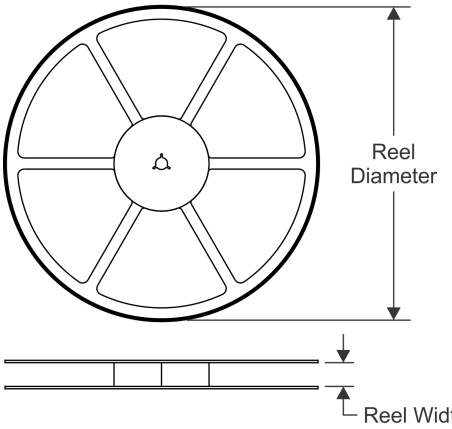
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

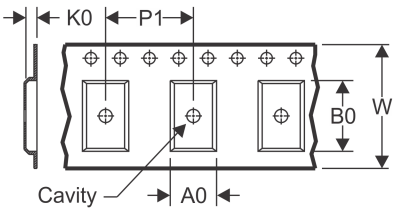
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

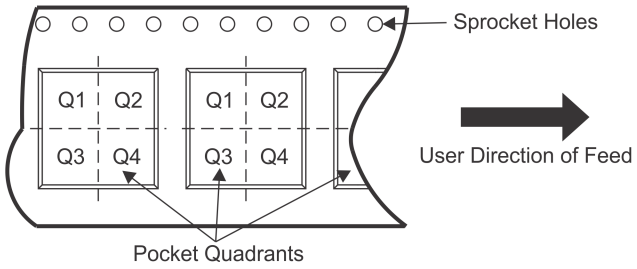


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

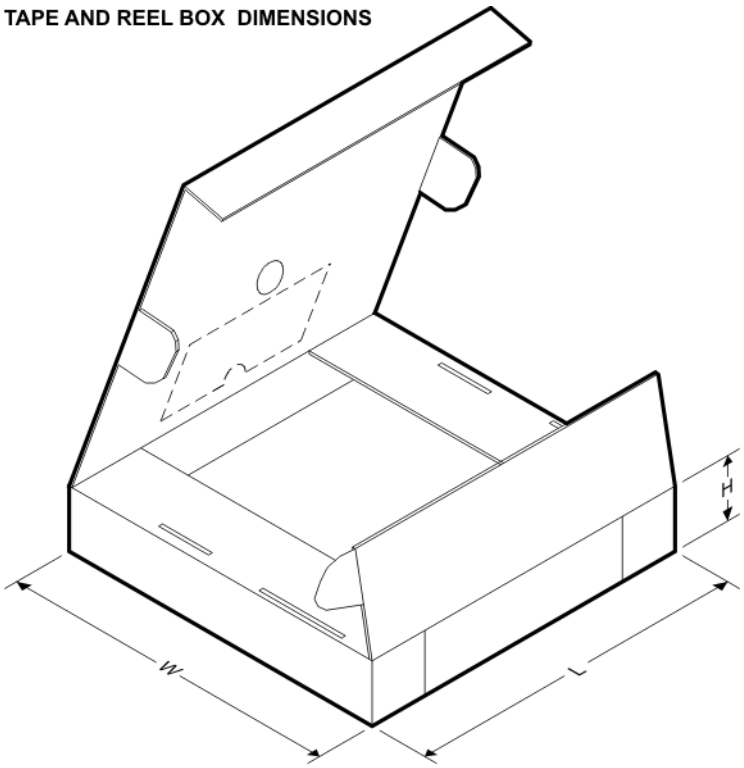
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4898MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

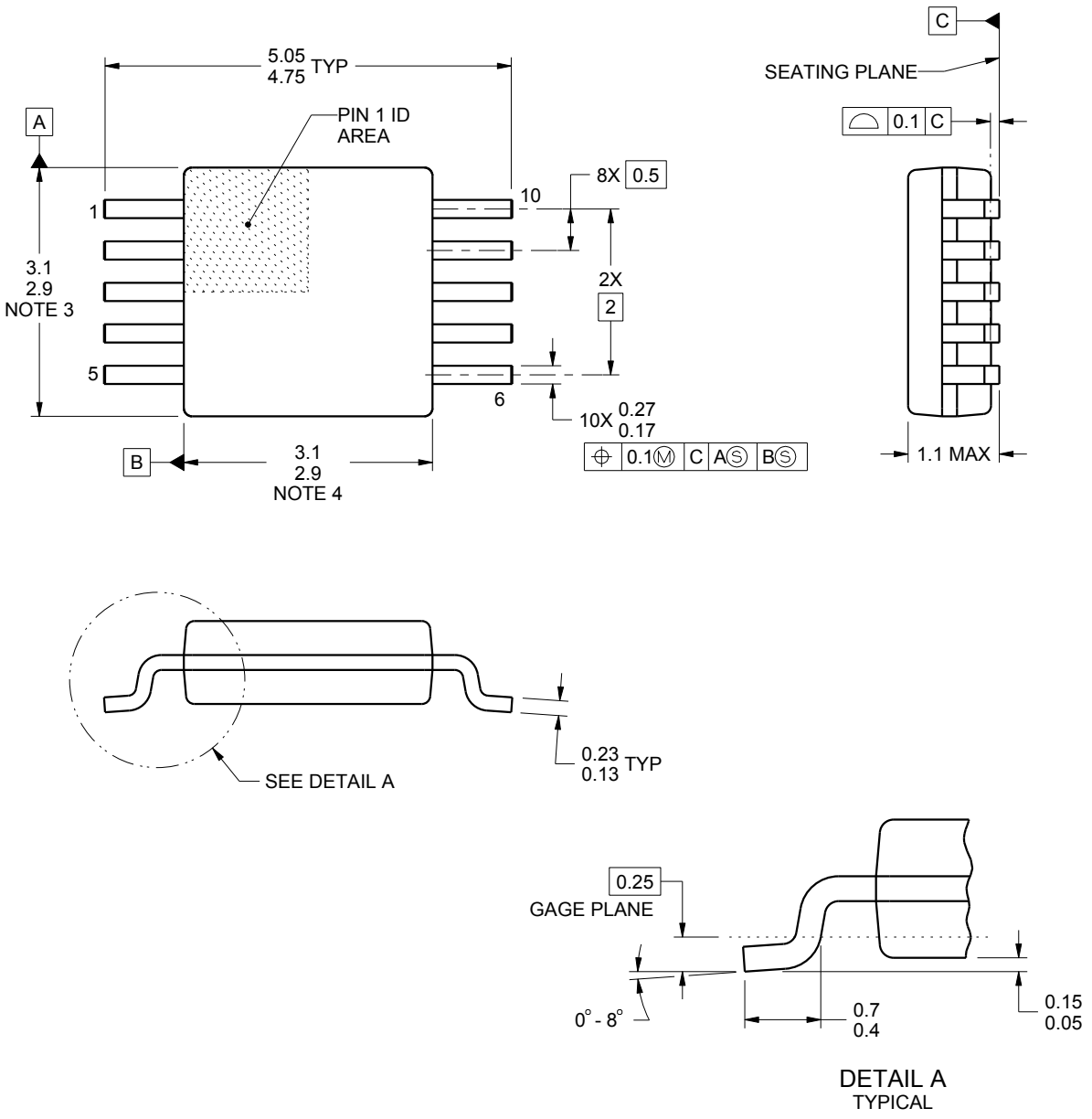
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4898MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0

PACKAGE OUTLINE

DGS0010A

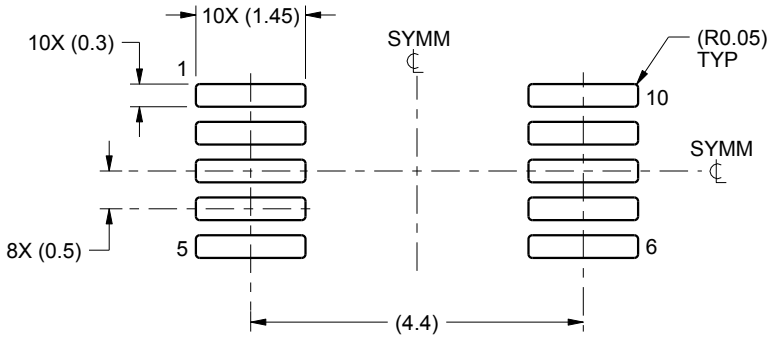
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

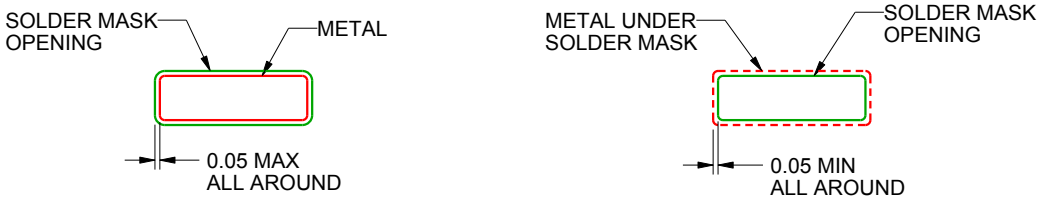


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

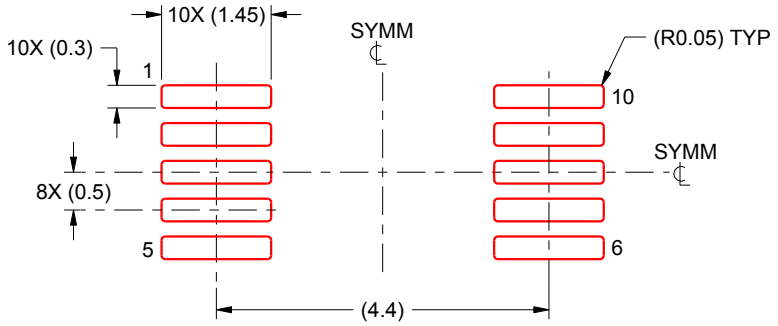


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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