

## TX4961XBG-240 64-bit RISC Processor with Integrated Graphics and Display Controller

### Highlights

- 64-bit TX49/H3 MIPS-compatible CPU runs large code base
- High integration reduces parts count and increases reliability
- Automotive/industrial temperature range
- 24-bit true color pixels with 8-bit alpha blending on all operations enables very high quality displays
- Graphics scheduler offloads CPU by reading display list commands directly from memory and dispatching operations to the hardware acceleration engines
- 5-layer graphics architecture eases task of managing overlays
- Transformation Engine can implement rotating display elements like indicator needles
- Blitting engine can perform font expansion and scaling
- Many basic graphics operations implemented in hardware
- ADC and PWM outputs can control LCD brightness and contrast

### Description

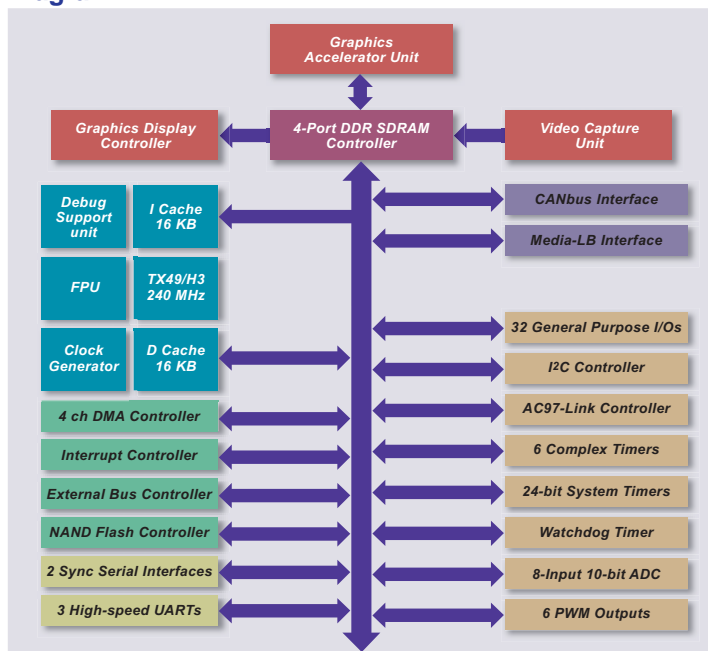
The TX4961 is designed for applications that combine general purpose computing with real-time graphic displays, such as driver information systems, car infotainment systems and car navigation systems. It integrates a TX49/H3 64-bit MIPS RISC CPU with a display controller and hardware graphics accelerators in a single system-on-a-chip IC. The integrated DDR SDRAM controller, unified memory architecture and multiple on-chip buses are designed to ensure that each on-chip subsystem has the memory bandwidth it needs.

The TX4961 also integrates a video frame grabber, AC-Link and I<sup>2</sup>C controllers, various timers and high-speed serial ports, 10-bit ADC, 16-bit PWM outputs, GPIO ports, and CANbus and Media-LB interfaces with DMA, interrupt, external bus, and NAND FLASH controllers.

### Features

- 240 MHz TX49/H3 CPU core
  - 16 KB Instruction cache
  - 16 KB Data cache
- Integrated IEEE754 single and double precision FPU
- MMU with 48-entry TLB
- Graphics display controller:
  - 24-bit true color pixels
  - 4 display planes
  - Hardware cursor to 64 x 64
- Hardware 8-bit alpha blending
- Hardware format conversion
- Hardware clipping windows
- Hardware antialiasing to 1/16 sub-pixel resolution
- Blitting Engine for moving, scaling, font expansion
- Transformation engine for 2D linear transforms
- Rotation Engine

### Diagram



# Product Brief

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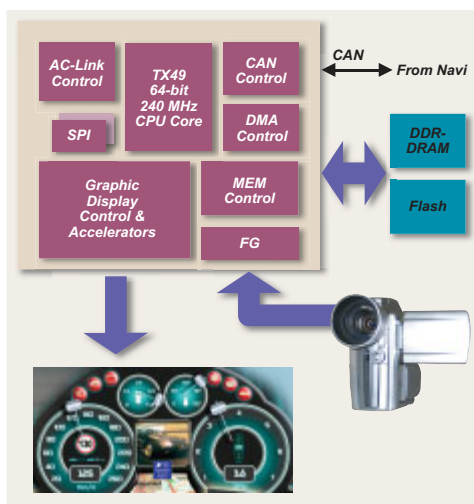
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[www.Toshiba.com/taec](http://www.Toshiba.com/taec)

- Line-Drawing Engine
- Frame Grabber
  - 16- or 8-bit RGB, or YCbCr
  - ITU-R 601/709 conversion
  - Frames up to 1024 x 512
  - Cropping and dotwise scaling
- External bus for 16-bit SRAM, ROM, NOR FLASH
- DDR SDRAM controller
  - 32/16-bit data, 2 channels
- DMA controller
- Interrupt controller
- NAND FLASH controller with HW ECC calculation
- Media-LB interface
- AC97-Link controller with 4-ch DMA
- I<sup>2</sup>C controller
- 3 high-speed UARTs
- 2 ESIE ports (SPI) with FIFOs
- 3 ch CAN-bus controller with 16 mailboxes each
- 30 general purpose IO pins
- 8 ch 10-bit ADC
- 6 x 16-bit PWM timers
- 6 x 16-bit complex timers
- 24-bit system timer
- Watchdog timer
- 4KB/4KB internal RAM/ROM
- On-chip clock and reset generators
- Halt, doze and standby power-down modes
- 130 nm process technology
- 456-pin PBGA, 1mm ball pitch
- -40°C to 85°C ambient operating temperature

## Diagram



## OS / Development Tools

- RBTX4961 Reference Board
- Greenhills Software
- Wind River Systems (under development)

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