REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R234-94	94-07-14	Monica L. Poelking
B	Add device types 03 and 04. Add case outlines N and Y. Editorial changes throughout.	96-09-03	Monica L. Poelking
C	Correct I_{OH} conditions for V_{OH} and the limits for V_{OH1} in table I. Correct symbols, definitions, and functional descriptions in section 6.5. Update boilerplate to MIL-PRF-38535 requirements. – CFS	02-05-10	Thomas M. Hess
D	Add case outline letter 4. – CFS	03-06-06	Thomas M. Hess
E	Update boilerplate to current MIL-PRF-38535 requirements. Correct descriptive designator for case outline letter 4 in paragraph 1.2.4. – CFS	08-07-15	Thomas M. Hess

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E	E	E							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
92-10-07

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CHMOS SINGLE-CHIP, 8-BIT MICROCONTROLLER WITH 32K BYTES OF EPROM PROGRAM MEMORY, MONOLITHIC SILICON

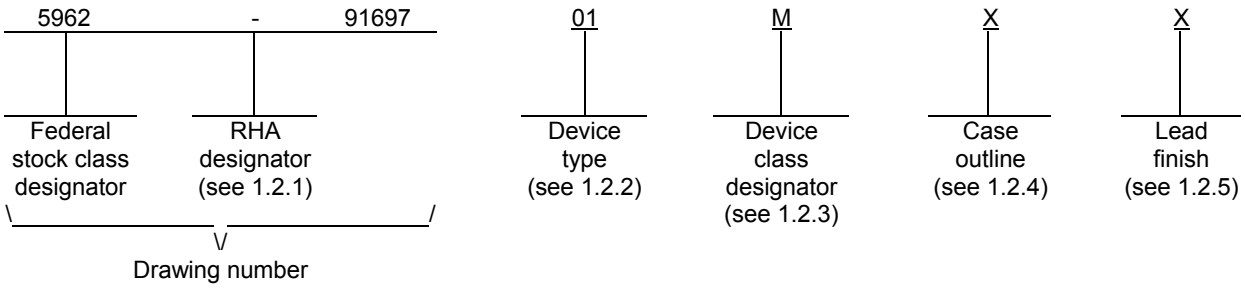
SIZE	CAGE CODE	
A	**67268**	**5962-91697**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C51FC or 87C51RC 1/	High performance CHMOS single chip 8-bit microcontroller with 32K bytes user programmable EPROM
02	87C51FC-16 or 87C51RC-16 1/	High performance CHMOS single chip 8-bit microcontroller with 32K bytes user programmable EPROM
03	87C51FC	High performance CHMOS single chip 8-bit microcontroller with 32K bytes user programmable EPROM
04	87C51FC-16	High performance CHMOS single chip 8-bit microcontroller with 32K bytes user programmable EPROM

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1/ Use of this die may require additional programming. Contact the device manufacturer for details.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
M	GQCC1-J44	44	Ceramic chip carrier, J-leaded package 1/	MIL-STD-1835
T	See figure 1	44	Ceramic chip carrier, J-leaded package 1/	
U	CQCC1-N44	44	Square chip carrier package 1/	MIL-STD-1835
X	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package 1/	MIL-STD-1835
Z	See figure 1	44	Ceramic chip carrier, gullwing-leaded package 1/	
Y	MS-018-AC	44	Plastic chip carrier, J-leaded	JEP 95
N	MS-011-AC	40	Plastic dual-in-line package	JEP 95
4	CQCC2-J44	44	Ceramic chip carrier, J-leaded package 2/	MIL-STD-1835

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 3/

Storage temperature range ..... -65ºC to +150ºC
Voltage on EA/V_{PP} pin to V_{SS} ..... 0.0 V dc to +13.0 V dc
Voltage on any other pin to V_{SS} ..... -0.5 V dc to +6.5 V dc
Maximum I_{OL} per I/O pin ..... 15 mA
Power dissipation (P_D) ..... 1.5 W 4/
Lead temperature (soldering 10 seconds) 265ºC
Thermal resistance, junction-to-case (θ_{JC}):
  Case U, X, and M ..... See MIL-STD-1835
  Case T, Z, and N 14ºC/W
  Case Y 15ºC/W
Endurance ..... 50 cycles/byte, minimum
Data retention ..... 10 years, minimum

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... +5.0 V dc ±20%
Oscillator frequency ..... 3.5 MHz to 16 MHz
Case operating temperature range (T_C):
  Device types 01 and 02 ..... -55ºC to +125ºC 5/
  Device types 03 and 04 ..... -40ºC to +85ºC 5/

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Non-windowed package.
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Power dissipation based on package heat transfer limitations, not device power consumption.
5/ Case temperatures are instant on.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of this document are available online at www.jedec.org/ or from the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2 herein.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3 herein.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4 herein.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5 herein.

3.11.2 Programmability of EPROMS. When specified, devices shall be programmed in accordance with the specified pattern using the procedures and characteristics specified in 4.6 herein and table III.

3.11.3 Verification and erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All	-0.5 2/	$0.2V_{CC}$ -0.1	V
Input high voltage (except XTAL1, RST)	V_{IH}		1, 2, 3	All	$0.2V_{CC}$ +0.9	V_{CC} +0.5 2/	V
Input high voltage (XTAL1, RST)	V_{IH1}		1, 2, 3	All	$0.7V_{CC}$	V_{CC} +0.5 2/	V
Output low voltage (ports 1, 2, 3) 3/	V_{OL}	I_{OL} = 100 µA 4/	1, 2, 3	All		0.3	V
		I_{OL} = 1.6 mA				0.45	
		I_{OL} = 3.5 mA				1.0	
Output low voltage (port 0, ALE, PSEN) 3/	V_{OL1}	I_{OL} = 200 µA 4/	1, 2, 3	All		0.3	V
		I_{OL} = 3.2 mA				0.45	
		I_{OL} = 7.0 mA				1.0	
Output high voltage (ports 1, 2, 3, ALE, PSEN)	V_{OH}	I_{OH} = -10 µA	1, 2, 3	All	V_{CC} -0.3		V
		I_{OH} = -30 µA			V_{CC} -0.7		
		I_{OH} = -60 µA			V_{CC} -1.5		
Output high voltage (port 0, in external bus mode)	V_{OH1}	I_{OH} = -200 µA 5/	1, 2, 3	All	V_{CC} -0.3		V
		I_{OH} = -3.2 mA			V_{CC} -0.7		
		I_{OH} = -7.0 mA			V_{CC} -1.5		
Logical 0 input current (ports 1, 2, and 3)	I_{IL}	V_{IL} = 0.45 V	1, 2, 3	All		-75	µA
Input leakage current (port 0)	I_{LI}	$0.45\ V \le V_{IN} \le V_{CC}$	1, 2, 3	All		±10	µA
Logical 1 to 0 transition current (ports 1, 2, 3)	I_{TL}	V_{IN} = 2.0 V	1, 2, 3	All		-750	µA
Power supply current	I_{CC}	6/ 7/ Running at 16 MHz	1, 2, 3	All		45	mA
		Idle mode at 16 MHz				15	mA
		Power down mode				130	µA
RST pull-down resistor	R_{RST}		1, 2, 3	All	40	225	kΩ
Pin capacitance 2/	C_{IO}	at 1.0 MHz, 25°C See 4.4.1c	4	All		10	pF
Functional testing		V_{CC} = 4.0 V See 4.4.1e	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ALE pulse width	t_{LHLL}	Load capacitance for port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF 8/	9, 10, 11	All	$2t_{CLCL}$-40		ns
Address valid to ALE low	t_{AVLL}		9, 10, 11	All	t_{CLCL}-40		ns
Address hold after ALE low	t_{LLAX}		9, 10, 11	All	t_{CLCL}-30		ns
ALE low to valid instruction in	t_{LLIV}		9, 10, 11	All		$4t_{CLCL}$-100	ns
ALE low to $\overline{PSEN}$ low	t_{LLPL}		9, 10, 11	All	t_{CLCL}-30		ns
$\overline{PSEN}$ pulse width	t_{PLPH}		9, 10, 11	All	$3t_{CLCL}$-45		ns
$\overline{PSEN}$ low to valid instruction in	t_{PLIV}		9, 10, 11	All		$3t_{CLCL}$-105	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}		9, 10, 11	All	0		ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}		9, 10, 11	All		t_{CLCL}-25	ns
Address to valid instruction in	t_{AVIV}		9, 10, 11	All		$5t_{CLCL}$-105	ns
$\overline{PSEN}$ low to address float	t_{PLAZ}		9, 10, 11	All		10	ns
$\overline{RD}$ pulse width	t_{RLRH}		9, 10, 11	All	$6t_{CLCL}$-100		ns
$\overline{WR}$ pulse width ALE low	t_{WLWH}		9, 10, 11	All	$6t_{CLCL}$-100		ns
$\overline{RD}$ low to valid data in	t_{RLDV}		9, 10, 11	All		$6t_{CLCL}$-165	ns
Data hold after $\overline{RD}$	t_{RHDX}		9, 10, 11	All	0		ns
Data float after $\overline{RD}$	t_{RHDZ}		9, 10, 11	All		$2t_{CLCL}$-60	ns
ALE low to valid data in	t_{LLDV}		9, 10, 11	All		$8t_{CLCL}$-150	ns
Address to valid data in	t_{AVDV}		9, 10, 11	All		$9t_{CLCL}$-165	ns
ALE low to $\overline{RD}$ or $\overline{WR}$ low	t_{LLWL}		9, 10, 11	All	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
Address valid to $\overline{WR}$ low	t_{AVWL}		9, 10, 11	All	$4t_{CLCL}$-130		ns
Data valid before $\overline{WR}$	t_{QVWX}		9, 10, 11	All	t_{CLCL}-50		ns
Data hold after $\overline{WR}$	t_{WHQX}		9, 10, 11	All	t_{CLCL}-50		ns
Data valid to $\overline{WR}$ high	t_{QVWH}		9, 10, 11	All	$7t_{CLCL}$-150		ns
$\overline{RD}$ low to address float	t_{RLAZ}		9, 10, 11	All		0	ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		9, 10, 11	All	t_{CLCL}-40	t_{CLCL}+40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial port clock cycle time	t_{XLXL}	Serial port timing-shift register mode load capacitance = 80 pF	9, 10, 11	All	$12t_{CLCL}$		ns
Output data setup to clock rising edge	t_{QVXH}		9, 10, 11	All	$10t_{CLCL}$-133		ns
Output data hold after clock rising edge	t_{XHQX}		9, 10, 11	All	$2t_{CLCL}$-117		ns
Input data hold after clock rising edge	t_{XHDX}		9, 10, 11	All	0		ns
Clock rising edge to input data valid	t_{XHDV}		9, 10, 11	All		$10t_{CLCL}$-133	ns
Oscillator frequency	$1/t_{CLCL}$ 8/	External clock drive	9, 10, 11	01, 03	3.5	12	MHz
				02, 04	3.5	16	
High time	t_{CHCX}		9, 10, 11	All	20		ns
Low time	t_{CLCX}		9, 10, 11	All	20		ns
Rise time 2/	t_{CLCH}		9, 10, 11	All		20	ns
Fall time 2/	t_{CHCL}		9, 10, 11	All		20	ns

1/ Case temperatures for devices 01, 02 are -55°C to +125°C, and for devices 03, 04 are -40°C to +85°C instant on. Unless otherwise specified, all test conditions shall be worst case condition. The supply voltage and operating temperature shall be as specified in section 1.4.

2/ Guaranteed to the limits specified in table I, if not tested.

3/ Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port - port 0: 26 mA

Maximum I_{OL} per ports 1, 2, and 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed conditions.

4/ Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pF, the noise pulse on the ALE signal may exceed 0.8 V. In these cases, it may be desirable to qualify ALE with Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.

5/ Capacitive loading on ports 0 and 2 cause the V_{OL} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

6/ Minimum V_{CC} for power down is 2.0 V.

7/ I_{CC} is measured with all output pins and XTAL2 disconnected; XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5\ V$, $V_{IH} = V_{CC} - 0.5\ V$ measured with $\overline{EA}$ and RST connected to V_{CC}. Idle and power down currents measured with $\overline{EA}$ and RST connected to V_{SS}. Power down currents measured with XTAL1 connected to V_{SS}.

8/ Timings tested at 16 MHz only but guaranteed across the specified operating frequency range.

Case T

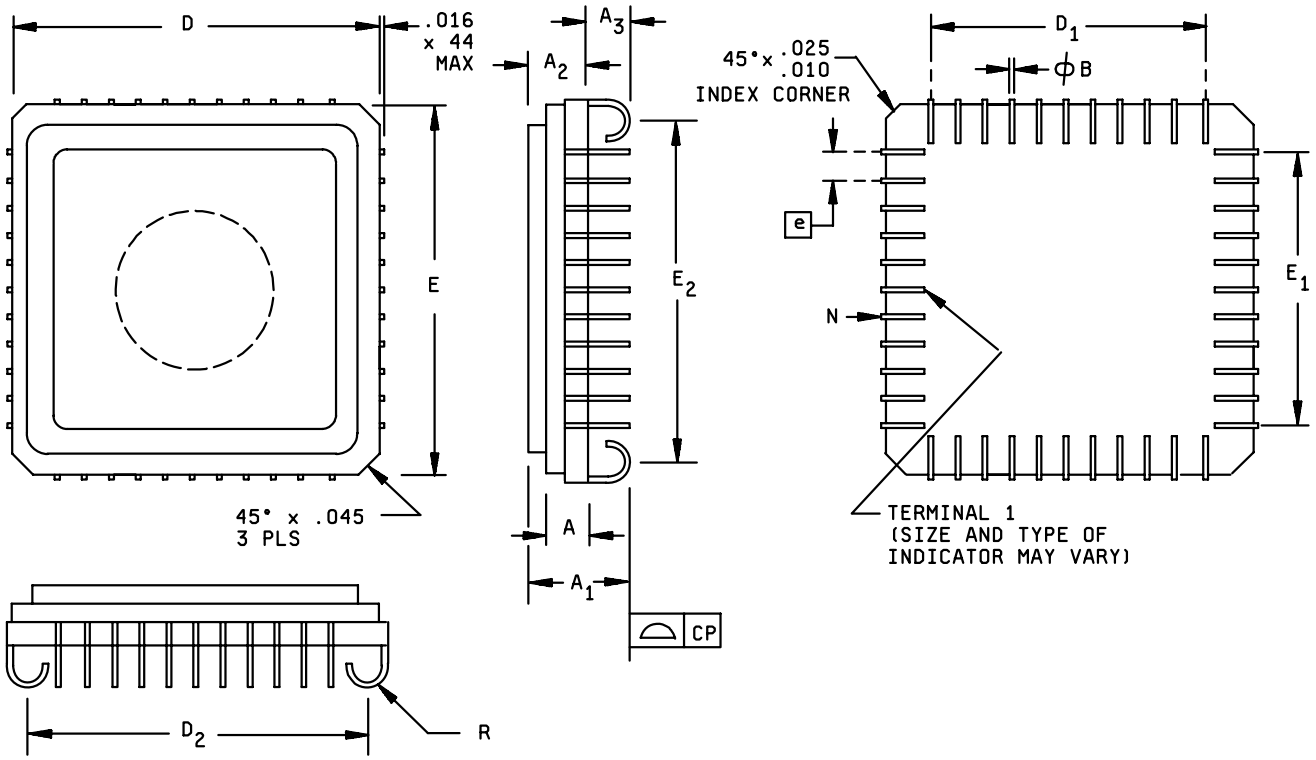


FIGURE 1. Case outlines.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-91697
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Case T

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.060	.088	1.52	2.23	
A_1	.157	.200	3.99	5.08	EPROM lid
A_2	.102	.134	2.59	3.40	EPROM lid
A_3	.055	.065	1.40	1.65	
B	.014	.018	0.35	0.46	
CP	.000	.004	0.00	0.10	
D	.640	.670	16.25	17.02	
D_1	.500		12.70		
D_2	.600		15.24		
E	.640	.670	16.25	17.02	
E_1	.500		12.70		
E_2	.600		15.24		
e	.044	.056	1.12	1.42	
N	44		44		
R	.027	.033	0.69	0.84	

FIGURE 1. Case outlines - Continued.

Case Z

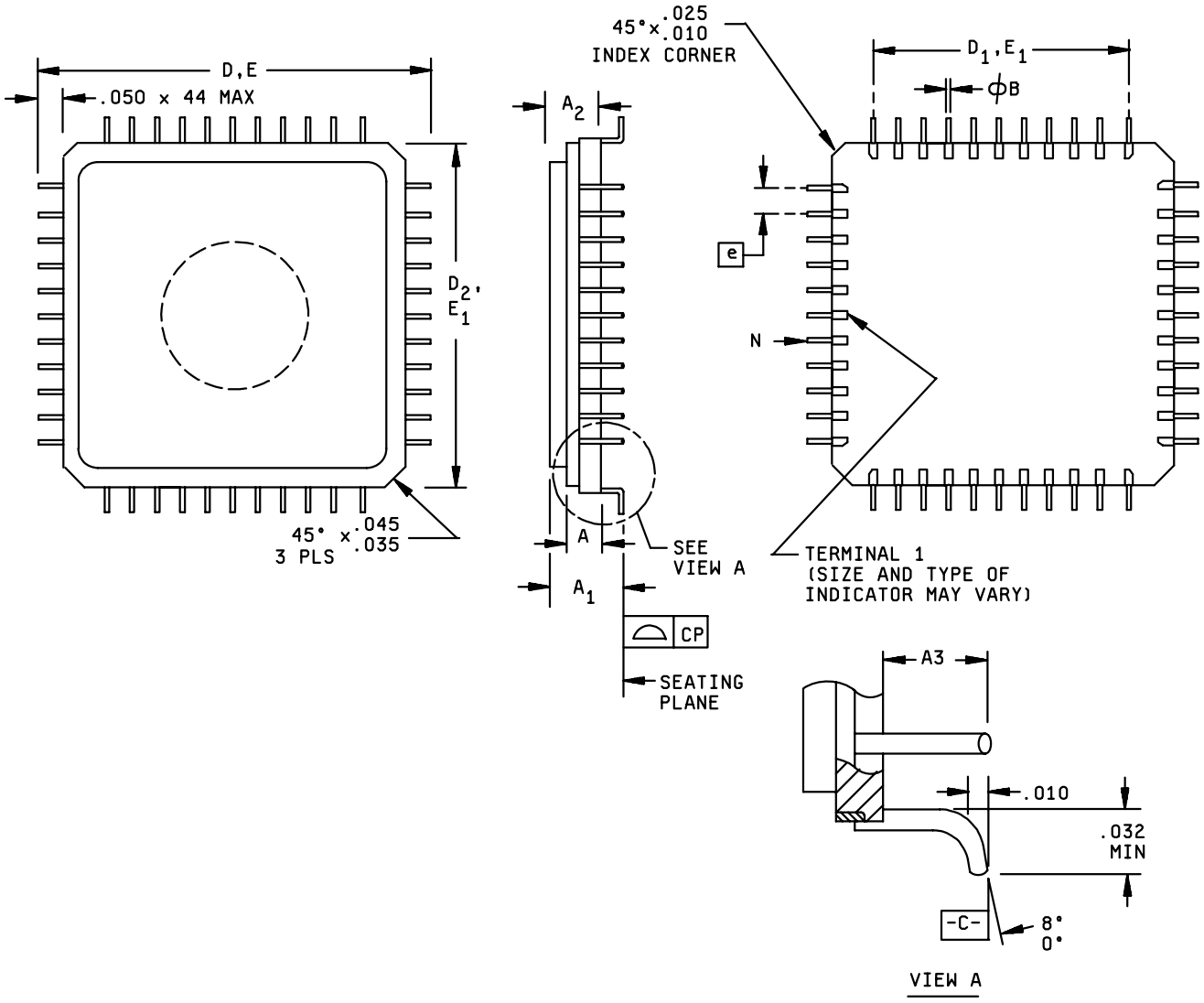


FIGURE 1. Case outlines - Continued.

Case Z

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.060	.090	1.52	2.29	
A_1	.157	.200	3.99	5.08	EPROM lid
A_2	.102	.134	2.59	3.40	EPROM lid
A_3	.055	.065	1.40	1.65	
B	.014	.018	0.35	0.46	
CP	.000	.004	0.00	0.10	
D	.716	.748	18.19	19.00	
D_1	.500		12.70		
D_2	.640	.660	16.25	16.76	
E	.716	.748	18.19	19.00	
E_1	.500		12.70		
E_2	.640	.660	16.25	16.76	
e	.044	.056	1.12	1.42	
N	44		44		

FIGURE 1. Case outlines - Continued.

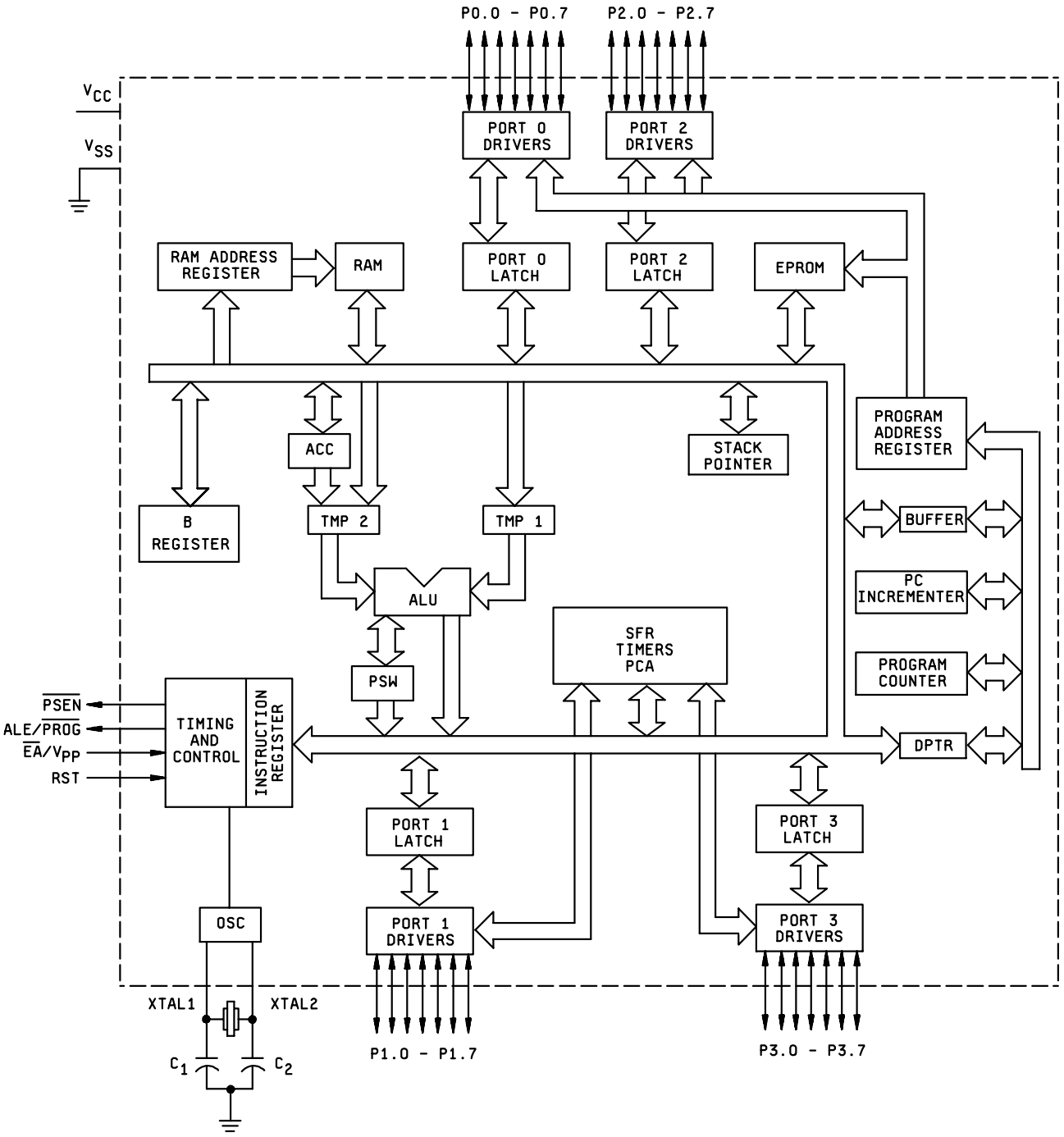
Device types	All		
Case outlines	X, N		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P1.0 (T2)	21	P2.0 (A8)
2	P1.1 (T2EX)	22	P2.1 (A9)
3	P1.2 (EC1)	23	P2.2 (A10)
4	P1.3 (CEX0)	24	P2.3 (A11)
5	P1.4 (CEX1)	25	P2.4 (A12)
6	P1.5 (CEX2)	26	P2.5 (A13)
7	P1.6 (CEX3)	27	P2.6 (A14)
8	P1.7 (CEX4)	28	P2.7 (A15)
9	RESET	29	$\overline{\text{PSEN}}$
10	P3.0 (RXD)	30	ALE/$\overline{\text{PROG}}$
11	P3.1 (TXD)	31	$\overline{\text{EA}}$ /V_{PP}
12	P3.2 ($\overline{\text{INT0}}$)	32	P0.7 (AD7)
13	P3.3 ($\overline{\text{INT1}}$)	33	P0.6 (AD6)
14	P3.4 (T0)	34	P0.5 (AD5)
15	P3.5 (T1)	35	P0.4 (AD4)
16	P3.6 ($\overline{\text{WR}}$)	36	P0.3 (AD3)
17	P3.7 ($\overline{\text{RD}}$)	37	P0.2 (AD2)
18	XTAL2	38	P0.1 (AD1)
19	XTAL1	39	P0.0 (AD0)
20	V_{SS}	40	V_{CC}

FIGURE 2. Terminal connections.

Device types	All		
Case outlines	M, T, U, Y, Z, 4		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC1}	23	NC
2	P1.0 (T2)	24	P2.0 (A8)
3	P1.1 (T2EX)	25	P2.1 (A9)
4	P1.2 (EC1)	26	P2.2 (A10)
5	P1.3 (CEX0)	27	P2.3 (A11)
6	P1.4 (CEX1)	28	P2.4 (A12)
7	P1.5 (CEX2)	29	P2.5 (A13)
8	P1.6 (CEX3)	30	P2.6 (A14)
9	P1.7 (CEX4)	31	P2.7 (A15)
10	RESET	32	$\overline{\text{PSEN}}$
11	P3.0 (RXD)	33	ALE/$\overline{\text{PROG}}$
12	NC	34	NC
13	P3.1 (TXD)	35	$\overline{\text{EA}}$ /V_{PP}
14	P3.2 ($\overline{\text{INT0}}$)	36	P0.7 (AD7)
15	P3.3 ($\overline{\text{INT1}}$)	37	P0.6 (AD6)
16	P3.4 (T0)	38	P0.5 (AD5)
17	P3.5 (T1)	39	P0.4 (AD4)
18	P3.6 ($\overline{\text{WR}}$)	40	P0.3 (AD3)
19	P3.7 ($\overline{\text{RD}}$)	41	P0.2 (AD2)
20	XTAL2	42	P0.1 (AD1)
21	XTAL1	43	P0.0 (AD0)
22	V_{SS}	44	V_{CC}

NC = No Connection.

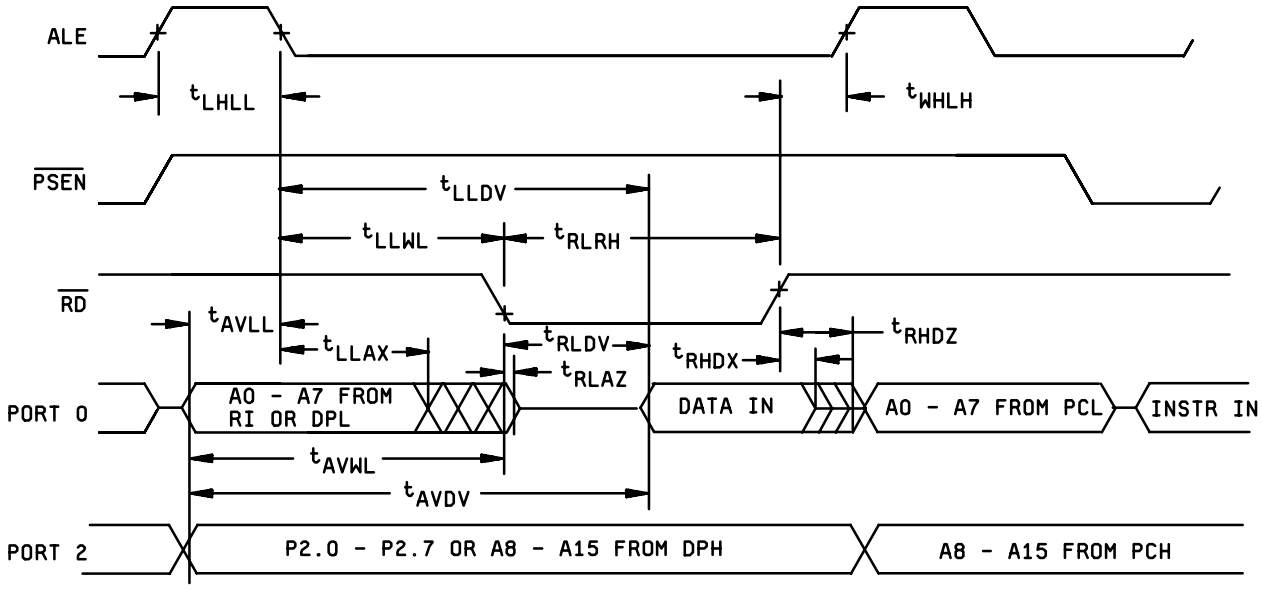
FIGURE 2. Terminal connections - Continued.



NOTE: C_1, C_2 = 30 pF ±10 pF for crystals.
C_1, C_2 = 10 pF for ceramic resonators.

FIGURE 3. Functional block diagram.

External data memory read cycle



External program memory read cycle

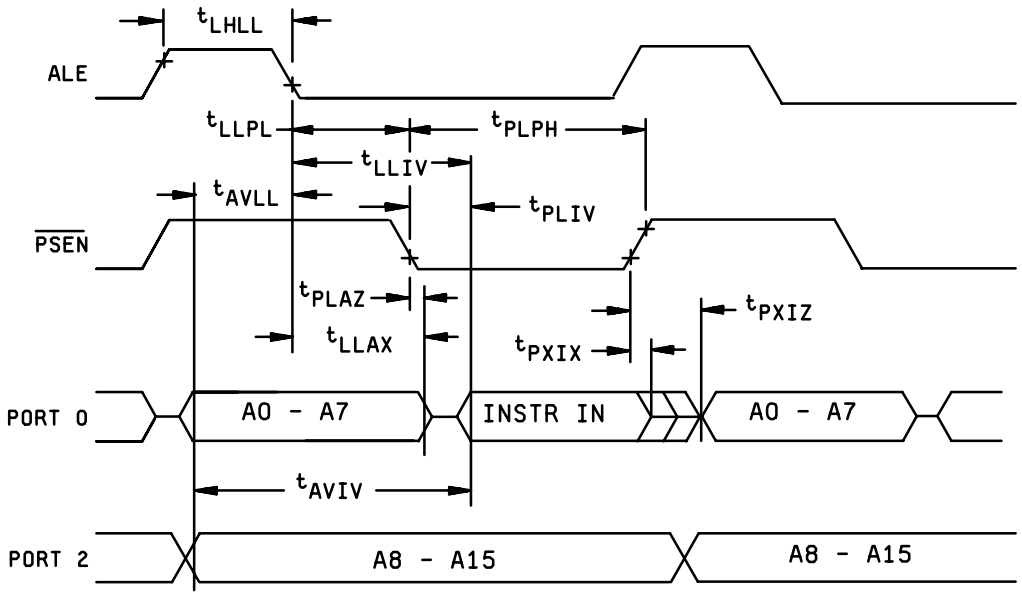
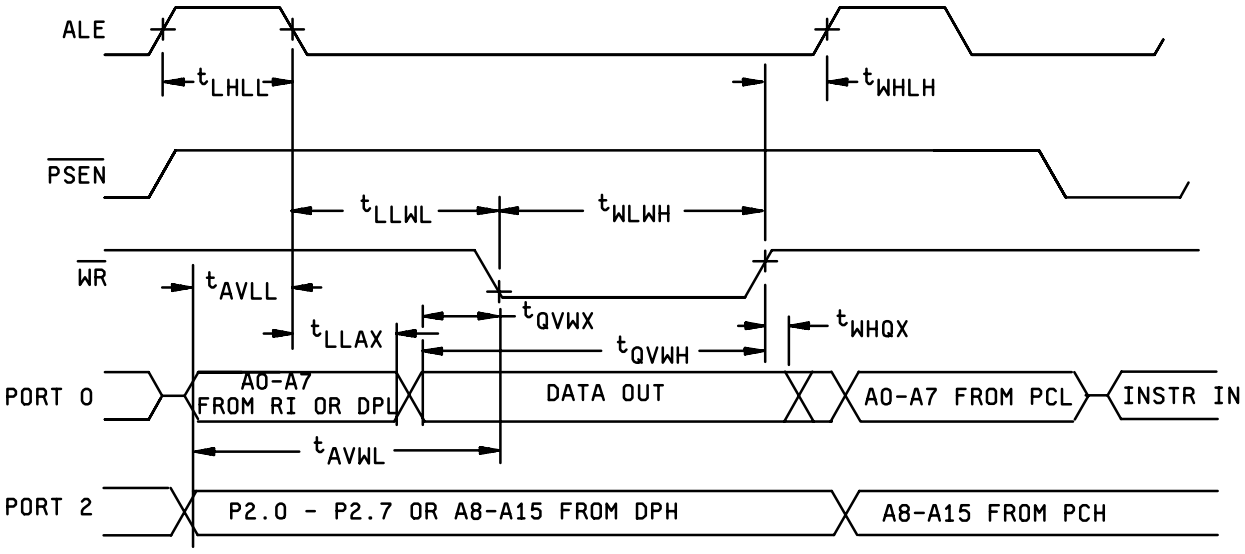


FIGURE 4. Switching waveforms and test circuit.

External data memory read cycle



External clock drive waveform

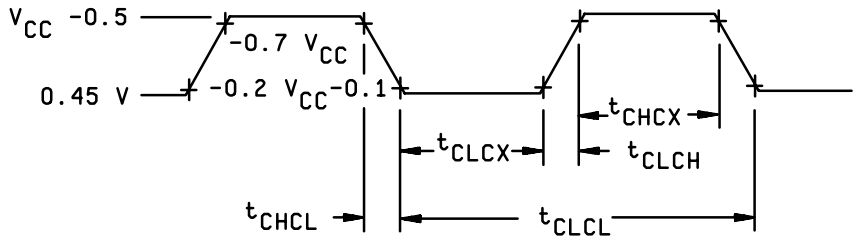
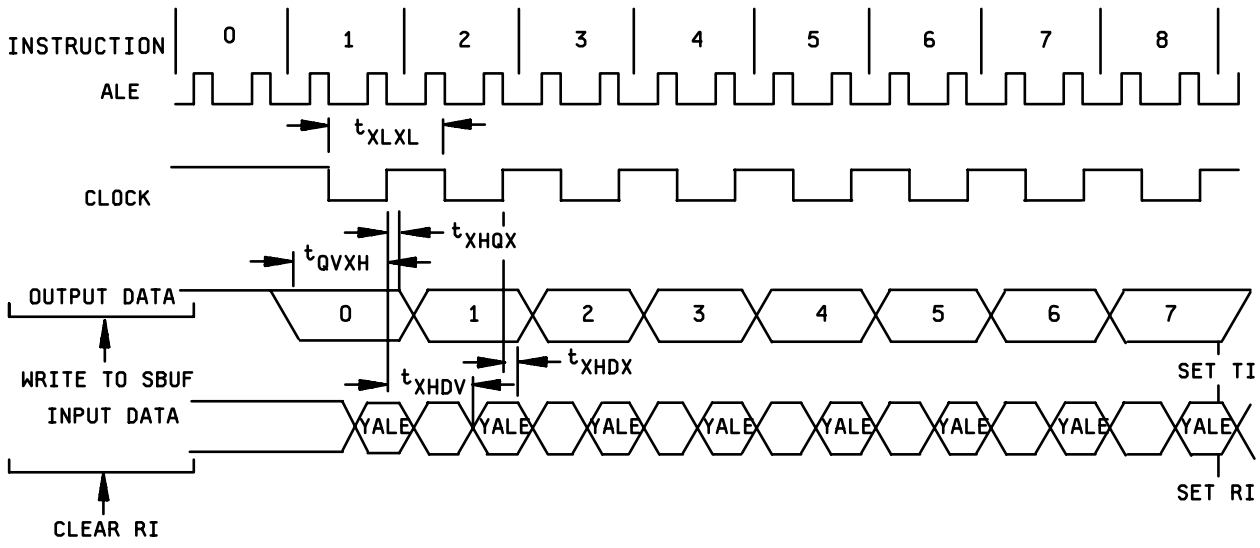
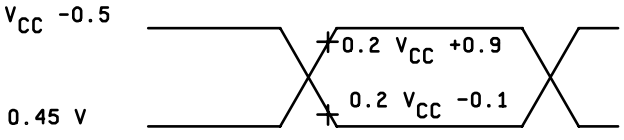


FIGURE 4. Switching waveforms and test circuit - Continued.

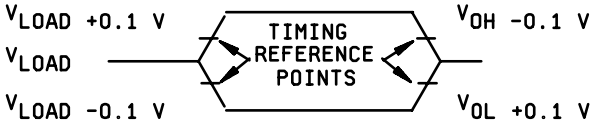
Shift register mode timing waveforms



AC testing input
Input, output waveforms



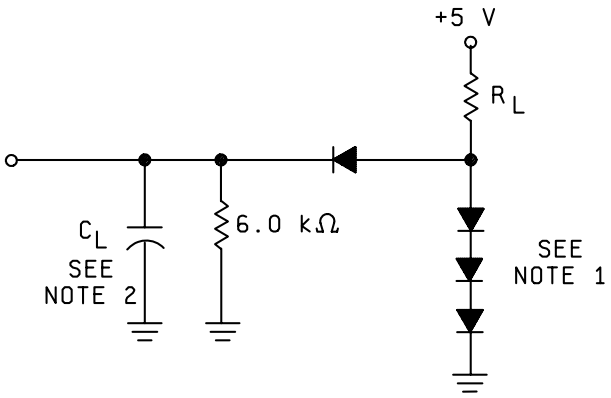
Float waveforms



AC inputs during testing are driven at V_{CC} – 0.5 V for a logic “1” and 0.45 V for a logic “0”. Timing measurements are made at V_{IH} minimum for a logic “1” and V_{IL} maximum for a logic “0”.

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA

FIGURE 4. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, $\overline{PSEN}$	1.2 KΩ	100 pF
All other outputs	2.4 KΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. 1/

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.
(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.
(3) Perform a margin test using V_M = +5.9 V at +25°C using loose timing (i.e., T_{ACC} >1 µs).
(4) Perform dynamic burn-in (see 4.2.1a).
(5) Margin at V_M = 5.9V.
(6) Perform electrical tests (see 4.2).
(7) Erase (see 3.11.1), except devices submitted for groups A, B, C and D testing.
(8) Verify erasure (see 3.11.3).

Margin test method B. 2/

(1) Program at +25°C, 100 percent of the bits.
(2) Bake, unbiased, for 24 hours at +250°C.
(3) Perform margin test at V_M = 5.9 V.
(4) Erase (see 3.11.1).
(5) Perform interim electrical tests in accordance with table II.
(6) Program 100 percent of the bits and verify (see 3.11.3).
(7) Perform burn-in (see 4.2a).
(8) One-hundred percent test at +25°C (group A, subgroups 1 and 7). V_M = 5.9 V with loose timing, apply PDA.
(9) Perform remaining final electrical subgroups and group A testing.
(10) Erase, devices may be submitted for groups B, C, and D at this time.
(11) Verify erasure (see 3.11.3). Steps 1 through 4 are performed at wafer level.

1/ Devices must have a transparent lid.
2/ For solid lid packages, steps 1-3 only.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. All devices, except devices using case outline letter 4, selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

f. The devices using case outline letter 4 shall be tested for programmability and AC performance compliance to the requirements of group A, subgroups 9, 10, 11. Either of the two techniques below is acceptable.

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and AC performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an un-programmed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted for programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total failures allowable. (Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample shall be increased to 20 total devices with no more than 4 total device failures allowable.)

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

a. For devices using case outline letter 4, the programmability shall be verified per 4.4.1f herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125ºC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

a. For devices using case outline letter 4, the programmability shall be verified per 4.4.1f herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms of figure 5 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.5).

TABLE III. EPROM programming and verification characteristics.

Parameter	Symbol	Conditions	Limits		Unit
			Min	Max	
Programming supply voltage	V_{PP}	EPROM programming and verification characteristics See figure 5 T_A = 21°C to 27°C V_{CC} = 5.0 V ±0.25 V V_{SS} = 0.0 V	12.5	13.0	V
Programming supply current	I_{PP}			75	mA
Oscillator frequency	$1/t_{CLCL}$		4	6	MHz
Address setup to $\overline{\text{PROG}}$ low 1/	t_{AVGL}		$48t_{CLCL}$		ns
Address hold after $\overline{\text{PROG}}$ 1/	t_{GHAX}		$48t_{CLCL}$		ns
Data setup to $\overline{\text{PROG}}$ low 1/	t_{DVGL}		$48t_{CLCL}$		ns
Data hold after $\overline{\text{PROG}}$ 1/	t_{GHDX}		$48t_{CLCL}$		ns
P2.7 (enable) high to V_{PP} 1/	t_{ENSH}		$48t_{CLCL}$		ns
V_{PP} setup to $\overline{\text{PROG}}$ low 1/	t_{SHGL}		10		μs
V_{PP} hold after $\overline{\text{PROG}}$ 1/	t_{GHSL}		10		μs
$\overline{\text{PROG}}$ width 1/	t_{GLGH}		90	110	μs
Address to data valid 1/	t_{AVQV}			$48t_{CLCL}$	μs
Enable low to data valid 1/	t_{ELQV}			$48t_{CLCL}$	μs
Data float after enable 1/	t_{EHQZ}		0	$48t_{CLCL}$	μs
$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	t_{GHGL}		10		μs

1/ Guaranteed to the limits specified in table III, if not tested.

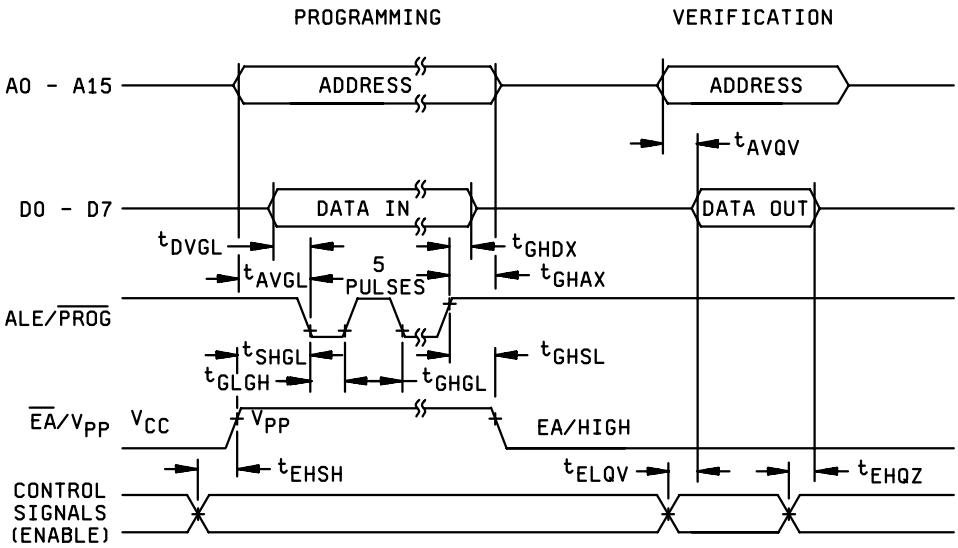


FIGURE 5. EPROM programming waveforms and configuration.

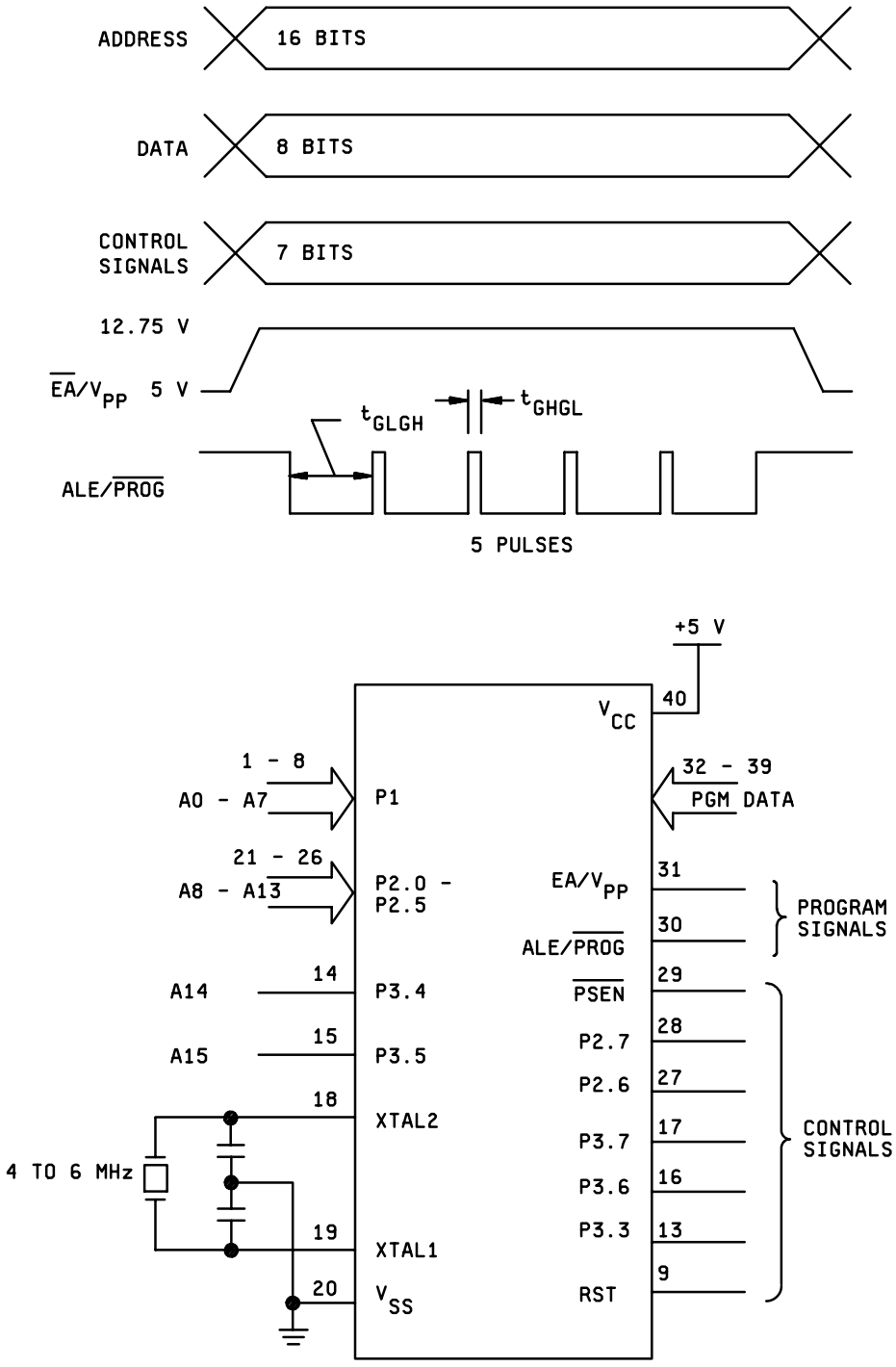


FIGURE 5. EPROM programming waveforms and configuration - Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

Symbol	Type	Functional description
V_{SS}	I	Ground: 0V reference.
V_{CC}	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0 - P0.7	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the device. External pull-ups are required during program verification.
P1.0 - P1.7	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification.
P2.0 - P2.7	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See Electrical Characteristics: I_{IL}). Port2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 special function register.

Symbol	Type	Functional description
P3.0 - P3.7	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull ups. Port 3 pins that have 1s written to them are pulled high by the internal pull ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the device family, as listed below:
	I	RxD (P3.0): Serial input port
	O	TxD (P3.1): Serial output port
	I	$\overline{INT0}$ (P3.2) External interrupt
	I	$\overline{INT1}$ (P3.3): External interrupt
	I	T0 (P3.4): Timer 0 external input
	I	T1 (P3.5): Timer 1 external input
	O	$\overline{WR}$ (P3.6): External data memory write strobe
	O	$\overline{RD}$ (P3.7): External data memory read strobe
RST	I	Reset: A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$ /V_{PP}	I	External Access Enable/Programming Supply Voltage: $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H through 0FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	Crystal 2: Output from the inverting oscillator amplifier.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-07-15

Approved sources of supply for SMD 5962-91697 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9169701MMA	0C7V7 3/	87C51RC/BMA 4/ 87C51FC/BMA
5962-9169701MTA	3/	MT87C51FC
5962-9169701MUA	3/	MR87C51FC
5962-9169701MXA	0C7V7 3/	87C51RC/BQA 4/ MD87C51FC
5962-9169701MZA	3/	MZ87C51FC
5962-9169701M4A	0C7V7	87C51RC/B4A 4/
5962-9169701NNA	3/	87C51FC/CN40A
5962-9169701NYA	3/	87C51FC/CA44A
5962-9169702MMA	0C7V7 3/	87C51RC-16/BMA 4/ 87C51FC-16/BMA
5962-9169702MTA	3/	MT87C51FC-16
5962-9169702MUA	3/	MR87C51FC-16
5962-9169702MXA	0C7V7 3/	87C51RC-16/BQA 4/ MD87C51FC-16
5962-9169702MZA	3/	MZ87C51FC-16
5962-9169702M4A	0C7V7	87C51RC-16/B4A 4/
5962-9169702NNA	3/	87C51FC-16/CN40A
5962-9169702NYA	3/	87C51FC-16/CA44A
5962-9169703NNA	3/	87C51FC/IN40A
5962-9169703NYA	3/	87C51FC/IA44A
5962-9169704NNA	3/	87C51FC-16/IN40A
5962-9169704NYA	3/	87C51FC-16/IA44A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.
4/ Use of this die may require additional programming. Contact manufacturer for details.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2954 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.