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NCP6914

Mini-PMIC - 1 x 0.8 A DC-DC LDOs, I2C

4 x 300 mA

The NCP6914 integrated circuits are part of the ON Semiconductor mini power management IC family (PMIC). They are optimized to supply battery powered portable application sub−systems such as camera function and microprocessors. These devices integrate 1 high efficiency 800 mA Step−down DC to DC converter with DVS (Dynamic Voltage Scaling) and four low−dropout (LDO) voltage regulators in a WLCSP20 1.77 x 2.06 mm package.

Features

- 1 DCDC Converter (3 MHz, 1 µH/10 µF, 800 mA)
  - Peak Efficiency 95%
  - Programmable Output Voltage from 0.6 V to 3.3 V by 12.5 mV Steps
- 4 Low Noise − Low Dropout Regulators (300 mA)
  - Programmable Output Voltage from 1.0 V to 3.3 V by 50 mV Steps
  - 50 μV_{rms} Typical Low Output Noise
- Control
  - 400 kHz / 3.4 MHz I^2C Compatible
  - Hardware Enable Pin
  - Power Good and Interrupt Output Pin
  - External Synchronization
  - Customizable Power Up Sequencer
- Extended Input Voltage Range 2.3 V to 5.5 V
- Optimized Power Efficiency
  - 72 µA Very Low Quiescent Current at No Load
  - Less than 1 µA Off Mode Current
- Small Footprint: Package 1.77 x 2.06 mm WLCSP
- These are Pb−Free Devices

Typical Applications

- Cellular Phones
- Digital Cameras
- Personal Digital Assistant and Portable Media Player
- GPS Systems

ON Semiconductor®

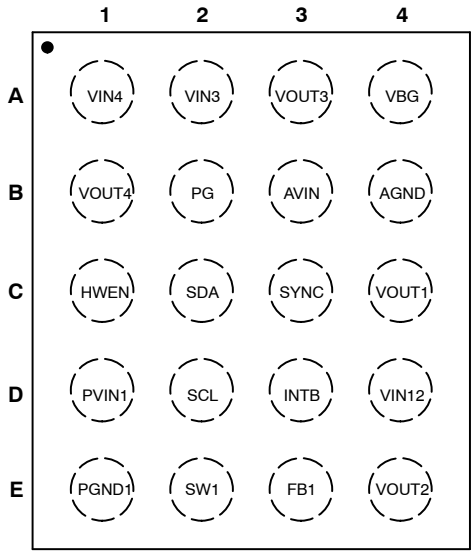
www.onsemi.com

WLCSP20
CASE 567CV

MARKING DIAGRAM*

x = A for NCP6914AA
= B for NCP6914AB
= D for NCP6914AD
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Pb−Free indicator, "G" or microdot " ▪", may or may not be present.)



(Top View)
20−Pin 1.77 x 2.06 mm WLCSP, 0.40 mm Pitch

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 36 of this data sheet.

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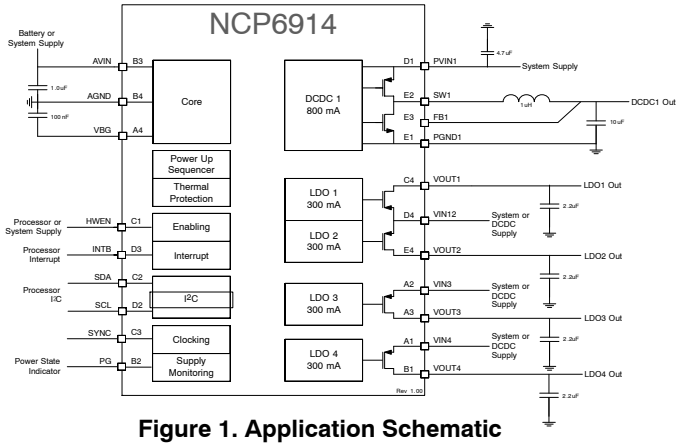

Figure 1. Application Schematic

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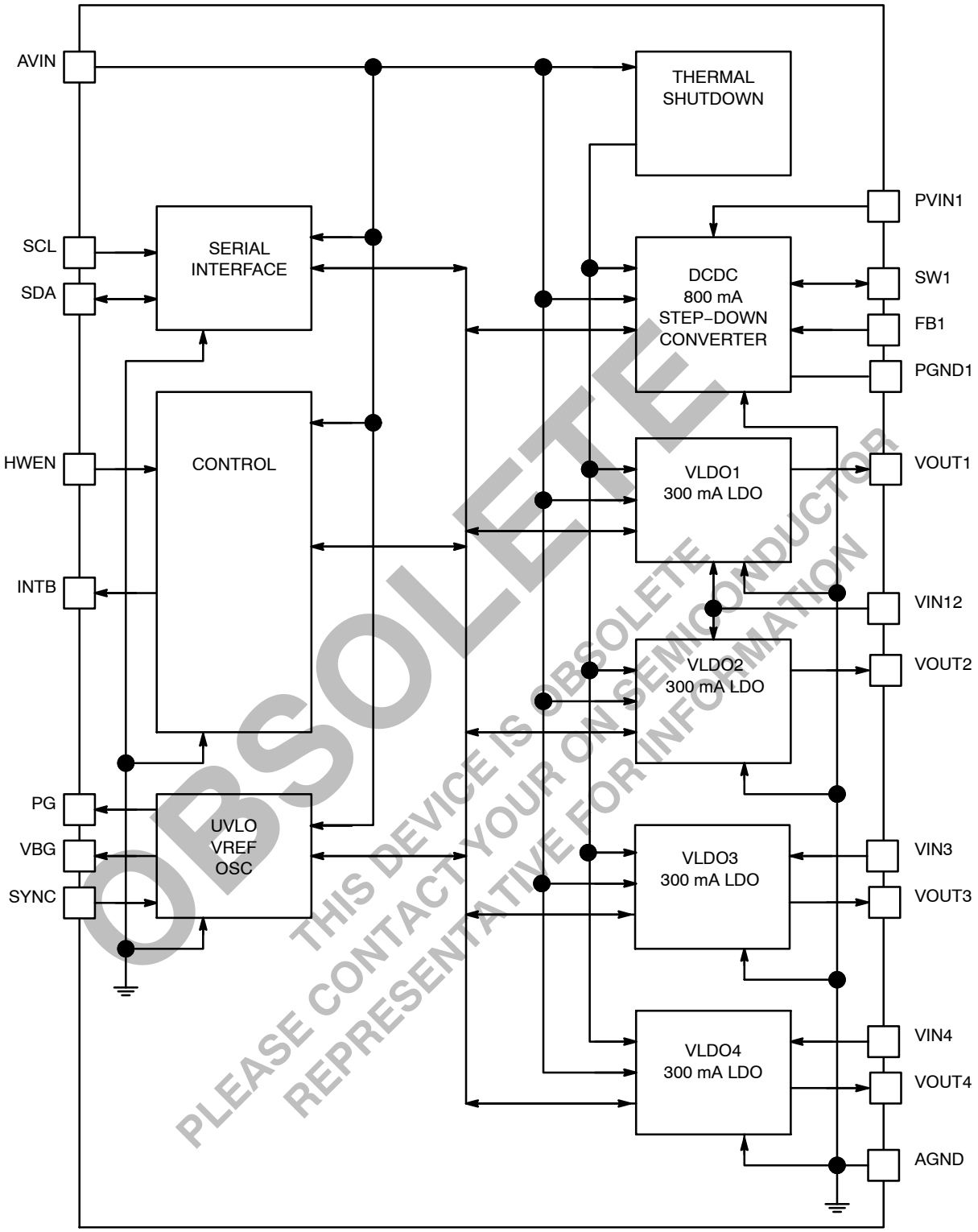

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Figure 2. Functional Block Diagram

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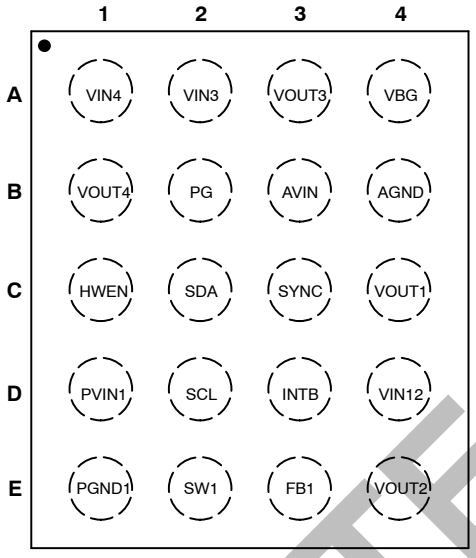

Figure 3. Pin Out (Top View)

Table 1. PINOUT DESCRIPTION

Pin	Name	Type	Description
POWER			
B3	AVIN	Analog Input	Analog Supply. This pin is the device analog and digital supply. A 1.0 μF ceramic capacitor or larger must bypass this input to ground. This capacitor should be placed as close as possible to this pin.
A4	VBG	Analog Output	Reference Voltage. A 0.1 μF ceramic capacitor must bypass this pin to the system ground.
B4	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
CONTROL AND SERIAL INTERFACE			
C1	HWEN	Digital Input	Hardware Enable. Active high will enable the part. There is an internal pull down resistor on this pin.
C3	SYNC	Digital Input	External Synchronization Input.
D2	SCL	Digital Input	I^2C interface Clock.
C2	SDA	Digital Input/Output	I^2C interface Data.
B2	PG	Digital Output	Power Good. Open drain output.
D3	INTB	Digital Output	Interrupt. Open drain output.
DCDC CONVERTER			
D1	PVIN1	Power Input	DCDC Power Supply. This pin must be decoupled to ground by a 4.7 μF ceramic capacitor. This capacitor should be placed as close as possible to this pin.
E2	SW1	Power Output	DCDC Switch Power. This pin connects the power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
E3	FB1	Analog Input	DCDC Feedback Voltage. This pin is the input to the error amplifier and must be connected to the output capacitor.
E1	PGND1	Power Ground	DCDC Power Ground. This pin is the power ground and carries the high switching current. A high quality ground must be provided to prevent noise spikes. A local ground plane is recommended to avoid high−density current flow in a limited PCB track.
LDO REGULATORS			
D4	VIN12	Power Input	LDO 1&2 Power Supply.
C4	VOUT1	Power Output	LDO 1 Output Power. This pin requires a 2.2 μF decoupling capacitor.
E4	VOUT2	Power Output	LDO 2 Output Power. This pin requires a 2.2 μF decoupling capacitor.
A2	VIN3	Power Input	LDO 3 Power Supply.
A3	VOUT3	Power Output	LDO 3 Output Power. This pin requires a 2.2 μF decoupling capacitor.
A1	VIN4	Power Input	LDO 4 Power Supply.
B1	VOUT4	Power Output	LDO 4 Output Power. This pin requires a 2.2 μF decoupling capacitor.

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Table 2. MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
V_A	Analog and power pins: AVIN, PVIN1, SW1, VIN12, VIN3, VIN4, VOUT1, VOUT2, VOUT3, VOUT4, PG, INTB, FB1, VBG	−0.3 to + 6.0	V
V_{DG} I_{DG}	Digital pins: SCL, SDA, HWEN, SYNC: Input voltage Input current	−0.3 to V_A +0.3 ≤ 6.0 10	V mA
ESD HBM	Human Body Model (HBM) ESD Rating (Note 2)	2000	V
ESD MM	Machine Model (MM) ESD Rating (Note 2)	200	V
I_{LU}	Latch up current: (Note 3) All digial pins All other pins	 ±10 ±100	mA
T_{STG}	Storage Temperature Range	−65 to + 150	°C
T_{JMAX}	Maximum Junction Temperature	−40 to +150	°C
MSL	Moisture Sensitivity (Note 4)	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltages are related to AGND.
2. ESD rated the following:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN}, PV_{IN}	Power Supply		2.3	–	5.5	V
LDO_{VIN}	LDO Input Voltage Range		1.7	–	5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range (Note 6)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction−to−Ambient (Note 7)	CSP−20 on Demo−board	–	60	–	°C/W
P_D	Power Dissipation Rating (Note 8)	T_A ≤ 85°C	–	660	–	mW
P_D	Power Dissipation Rating (Note 8)	T_A = 40°C	–	1400	–	mW
L	Inductor for DCDC Converter (Note 5)		0.47	1	2.2	μH
Co	Output Capacitor for DCDC Converter (Note 5)		–	10	–	μF
	Output Capacitors for LDO (Note 5)		1.20	2.2	–	μF
C_{in}	Input Capacitor for DCDC Converter (Note 5)		–	4.7	–	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Refer to the Application Information section of this data sheet for more details.
6. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
7. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a NCP6914EVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board.
8. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

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Table 4. ELECTRICAL CHARACTERISTICS

Min & Max Limits apply for T_J up to +125°C unless otherwise specified. $AV_{IN} = PV_{IN1} = V_{IN12} = V_{IN3} = V_{IN4} = 3.6$ V (unless otherwise noted). DCDC Output Voltage = 1.2 V, LDO1&2 = 1.8 V, LDO3&4 = 2.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PINS AVIN – PVIN1						
I_Q	Operating Quiescent Current	DCDC on – no load – no switching LDOs off T_A = up to +85°C	–	32	70	μA
		DCDC on – no load – no switching LDOs on – no load T_A = up to +85°C	–	72	190	
		DCDC Off All LDOs on – no load T_A = up to +85°C	–	55	100	μA
I_{SLEEP}	Product Sleep Mode Current	HWEN on DCDC and all LDOs off T_A = up to +85°C	–	7	15	μA
I_{OFF}	Product Off Current	HWEN off I^2C interface disabled V_{IN} = 2.3 V to 5.5 V T_A = up to +85°C	–	0.1	2.0	μA
DCDC Converter						
PV_{IN}	Input Voltage Range		2.3	–	5.5	V
I_{OUTMAX}	Maximum Output Current		0.8	–	–	A
Δ_{VOUT}	Output Voltage DC Error	Io = 300 mA, PWM mode T_A = up to +85°C	–1	0	1	%
F_{SW}	Switching Frequency		2.7	–	3.3	MHz
R_{ONHS}	P–Channel MOSFET On Resistance	From PVIN1 to SW1, T_A = up to +85°C Guarantee by design and characterization, production tested at Vin = 3.6 V	–	230	–	mΩ
R_{ONLS}	N–Channel MOSFET On Resistance	From SW1 to PGND1, T_A up to 85°C Guarantee by design and characterization, production tested at Vin=3.6 V	–	200	–	mΩ
I_{PK}	Peak Inductor Current	Open loop 2.3 V ≤ PV_{IN} ≤ 5.5 V	1.0	1.3	1.6	A
	Load Regulation	I_{OUT} from 300 mA to I_{OUTMAX}	–	5	–	mV/A
	Line Regulation	I_{OUT} = 300 mA 2.3 V ≤ V_{IN} ≤ 5.5 V	–	0	–	%/V
D	Maximum Duty Cycle		–	100	–	%
t_{START}	Soft–Start Time	Time from I^2C command ACK to 90% of Output Voltage	–	–	1	ms
$R_{DISDCDC}$	DCDC Active Output Discharge		–	7	–	Ω
LDO1 AND LDO2						
V_{IN12}	LDO1 and LDO2 input voltage Range 300 mA load	V_{OUT} ≤ 1.3 V, I_{OUT} = 300 mA	1.7	–	5.5	V
		V_{OUT} > 1.3 V, I_{OUT} = 300 mA	$V_{out} + V_{DROP}$	–	5.5	
$I_{OUTMAX1,2}$	Maximum Output Current		300	–	–	mA
$I_{SC1,2}$	Short Circuit Protection		360	–	700	mA

9. Devices that use non–standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull–up resistors R_P are connected.
10. Refer to the Application Information section of this data sheet for more details.
11. Guaranteed by design and characterized.

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Table 4. ELECTRICAL CHARACTERISTICS

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO1 AND LDO2						
$\Delta V_{OUT1,2}$	Output Voltage Accuracy DC	I_{OUT} = 300 mA	−2	V_{NOM}	+2	%
	Load Regulation	I_{OUT} = 0 mA to 300 mA	–	0.4	–	%
	Line Regulation	V_{IN} = max (1.7 V, $V_{OUT} + V_{DROP}$) to 5.5 V I_{OUT} = 300 mA	–	0.3	–	%
V_{DROP}	Dropout Voltage	I_{OUT} = 300 mA, $V_{OUT} = V_{NOM}$ − 2%	–	140	400	mV
PSRR	Ripple Rejection	F = 1 kHz, I_{OUT} = 150 mA	–	−75	–	dB
		F = 10 kHz, I_{OUT} = 150 mA	–	−60	–	
Noise		10 Hz → 100 kHz, I_{OUT} = 150 mA	–	50	–	μV
$R_{DISLDO1,2}$	LDO Active Output Discharge		–	25	–	Ω
LDO3 and LDO4						
V_{IN3}, V_{IN4}	LDO3 and LDO4 Input Voltage	$V_{OUT} \le 1.5$ V, I_{OUT} = 300 mA	1.7	–	5.5	V
		$V_{OUT} > 1.5$ V, I_{OUT} = 300 mA	$V_{out} + V_{DROP}$	–	5.5	
$I_{OUTMAX3,4}$	Maximum Output Current		300	–	–	mA
$I_{SC3,4}$	Short Circuit Protection		360	–	700	mA
ΔV_{OUT}	Output Voltage Accuracy	I_{OUT} = 300 mA	−2	V_{NOM}	+2	%
	Load Regulation	I_{OUT} = 0 mA to 300 mA	–	0.4	–	%
	Line Regulation	V_{DROP} to 5.5 V I_{OUT} = 300 mA	–	0.3	–	%
V_{DROP}	Dropout Voltage	I_{OUT} = 300 mA $V_{OUT} = V_{NOM}$ − 2%	–	90	200	mV
PSRR	Ripple Rejection	F = 1 kHz, I_{OUT} = 150 mA	–	−75	–	dB
		F = 10 kHz, I_{OUT} = 150 mA	–	−60	–	
Noise		10 Hz → 100 kHz, I_{OUT} = 150 mA	–	50	–	μV
$R_{DISLDO3,4}$	LDO Active Output Discharge		–	25	–	Ω
SYNC						
$CLKIN_{PK-PK}$	Input Clock Signal Amplitude	Square waveform, 3 MHz/, 50% DC	800	–	–	mV
		Sine Waveform, 3 MHz	800	–	–	
$CLKIN_{DC}$	Input Clock Signal Duty Cycle	Square waveform, 3 MHz	30	–	–	%
$CLKIN_V$	Input Clock Voltage Level	Sine waveform, 3 MHz, (Note 11)	−0.3	–	5.0	V
$f_{CLOCKINT}$	External Synchronization Clock Range	After Divider Ratio (Note 11)	2.55	–	3.45	MHz
f_{RANGE}	External Synchronization Operating Frequency Range	Square signal 50% Duty Cycle Input Signal on SYNC pin SYNCRATIO = 00001b to 01100b SYNCAUTO = 1 (Note 11)	2.55	–	100	MHz
$CLKIN_{PK-PK}$	Input clock signal amplitude	Square waveform, 3 MHz/, 50% DC	800	–	–	mV

9. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
10. Refer to the Application Information section of this data sheet for more details.
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HWEN						
V_{IH}	Positive Going Input High Voltage Threshold		1.1	–	–	V
V_{IL}	Negative Going Input Low Voltage Threshold		–	–	0.4	V
t_{HWEN}	Hardware Enable Filter	HWEN rising and falling (Note 11)	4	–	9	µs
I_{HWEN}	Hardware Enable Pull−Down (input bias current)		–	0.1	1	µA
PG						
V_{PGL}	Power Good Low Threshold	V_{OUT} falls down to cross the threshold (percentage of FB voltage)	86	90 of V_{NOM}	94	%
V_{PGHYS}	Power Good Hysteresis	V_{OUT} rises up to cross the threshold (percentage of Power Good Low Threshold (V_{PGL}) voltage)	0	3	5	%
t_{RT}	Power Good Reaction Time for DCDC	Falling (Note 11) Rising (Note 11)	– 4	5 –	– 9	µs
V_{PGL}	Power Good Low Output Voltage	I_{PG} = 5 mA	–	–	0.2	V
PG_{LK}	Power Good Leakage Current	3.6 V at PG pin when power good valid	–	–	100	nA
V_{PGH}	Power Good High Output Voltage	Open drain	–	–	5.5	V
INTB						
V_{INTBL}	INTB Low Output Voltage	I_{INT} = 5 mA	0	–	0.2	V
V_{INTBH}	INTB High Output Voltage	Open drain	–	–	5.5	V
$INTB_{LK}$	INTB Leakage Current	3.6 V at INTB pin when INTB valid	–	–	100	nA
I^2C						
V_{I2CINT}	High Level at SCL/SDA Line		–	–	5.0	V
V_{I2CIL}	SCL, SDA Low Input Voltage	SCL, SDA pin (Notes 9 and 11)	–	–	0.5	V
V_{I2CIH}	SCL, SDA High Input Voltage	SCL, SDA pin (Notes 9 and 11)	0.8 x V_{I2CINT}	–	–	V
V_{I2COL}	SCL, SDA Low Output Voltage	I_{SINK} = 3 mA (Note 11)	–	–	0.4	V
F_{SCL}	I^2C Clock Frequency		–	–	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	–	–	2.3	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	–	200	mV
T_{SD}	Thermal Shut Down Protection			150		°C
$T_{WARNING}$	Warning Rising Edge			135		°C
T_{SDH}	Thermal Shut Down Hysteresis			35		°C

9. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
10. Refer to the Application Information section of this data sheet for more details.
11. Guaranteed by design and characterized.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL OPERATING CHARACTERISTICS

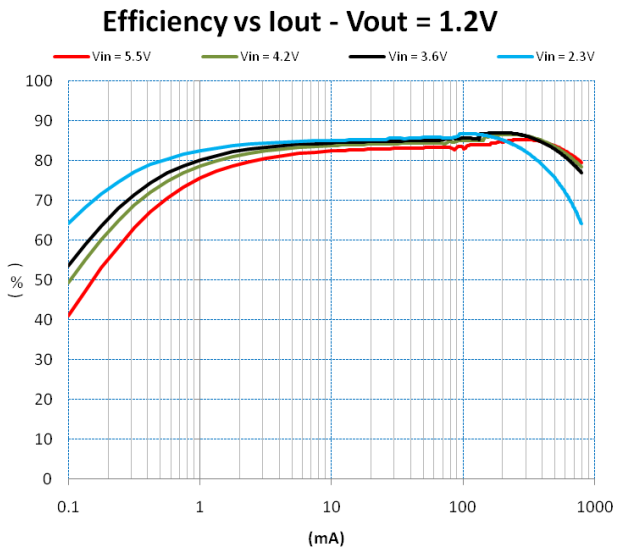

Figure 4. Efficiency vs. I_{OUT} (auto PFM / PWM mode)
L = 1.0 μH (LQH44PN1R0NJ0)
C_{OUT} = 10 μF (0603 size)
V_{OUT} = 1.2V

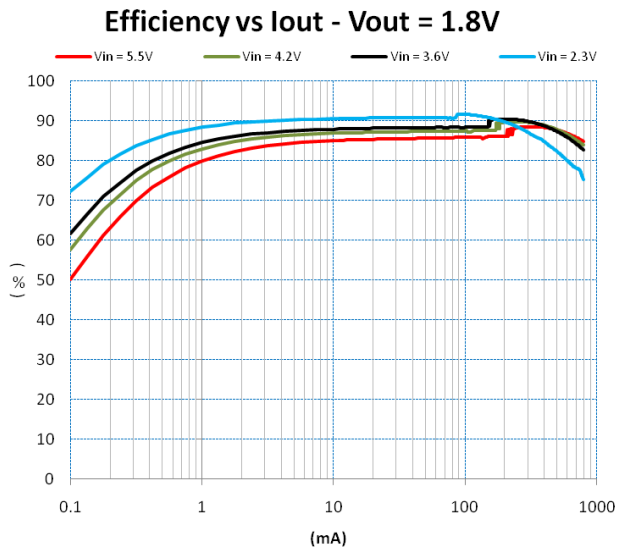

Figure 5. Efficiency vs. I_{OUT} (auto PFM / PWM mode)
L = 1.0 μH (LQH44PN1R0NJ0)
C_{OUT} = 10 μF (0603 size)
V_{OUT} = 1.8V

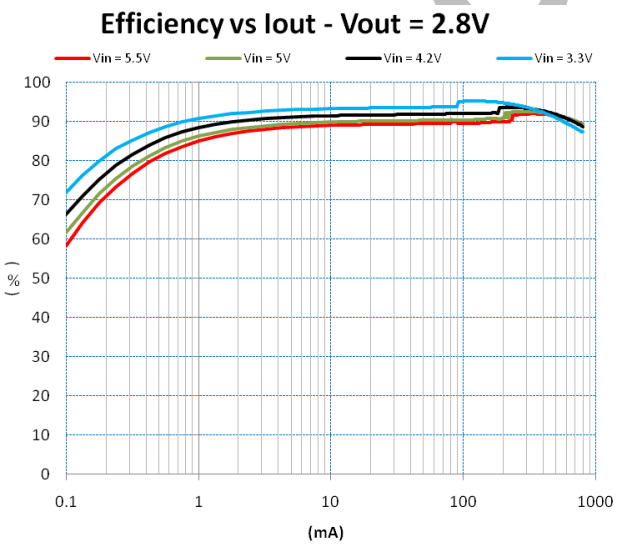

Figure 6. Efficiency vs. I_{OUT} (auto PFM / PWM mode)
L = 1.0 μH (LQH44PN1R0NJ0)
C_{OUT} = 10 μF (0603 size)
V_{OUT} = 2.8 V

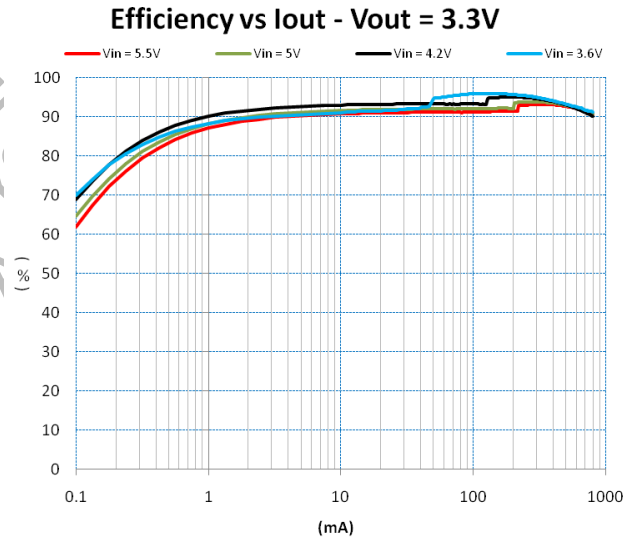

Figure 7. Efficiency vs. I_{OUT} (auto PFM / PWM mode)
L = 1.0 μH (LQH44PN1R0NJ0)
C_{OUT} = 10 μF (0603 size)
V_{OUT} = 3.3 V

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TYPICAL OPERATING CHARACTERISTICS

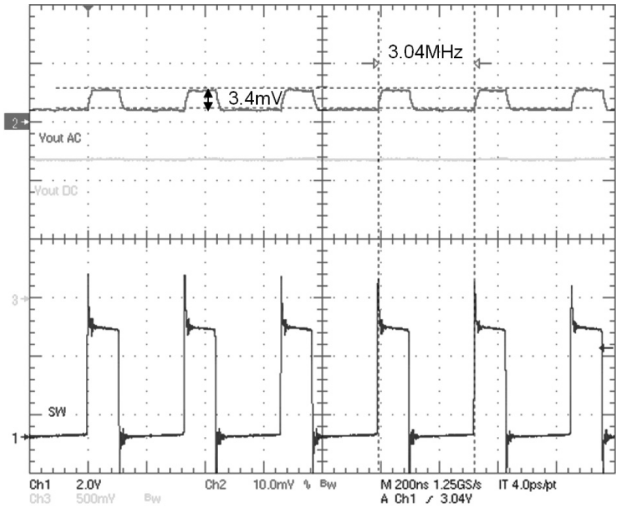

Figure 8. Ripple Voltage in PWM Mode (V_{in} = 3.6 V – V_{out} 1.2 V)

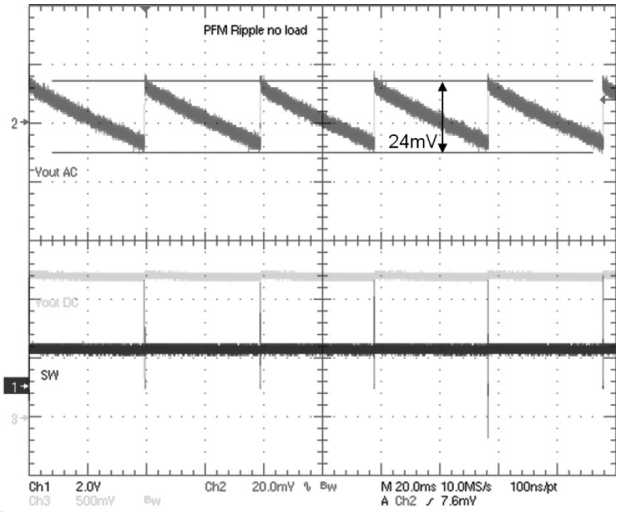

Figure 9. Ripple Voltage in PFM Mode (V_{in} = 3.6 V – V_{out} 1.2 V)

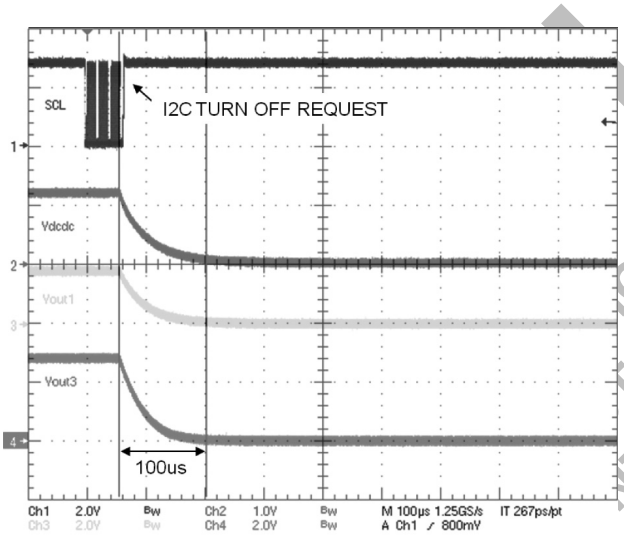

Figure 10. I²C Shutdown Sequence with Active Discharge Enabled

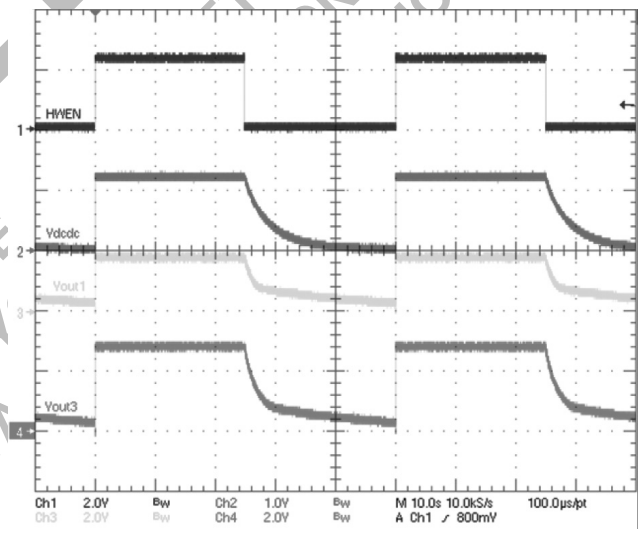

Figure 11. HWEN Shutdown Sequence with Active Discharge Disabled

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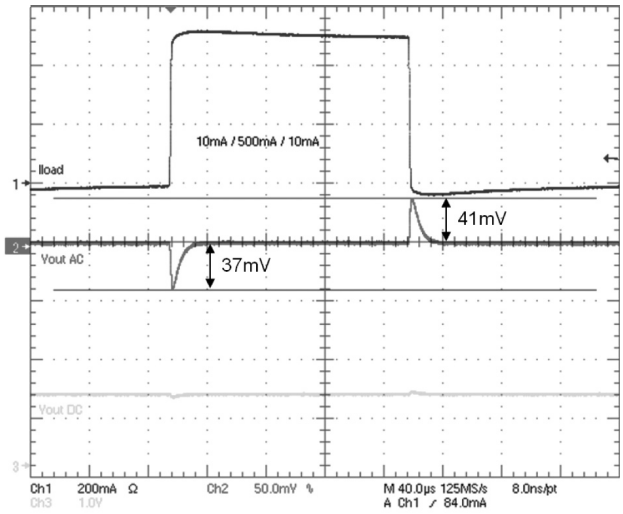

Figure 12. Load Transient Response of DCDC Converter (PWM Mode, V_{in} = 3.6 V – V_{out} = 1.2 V)

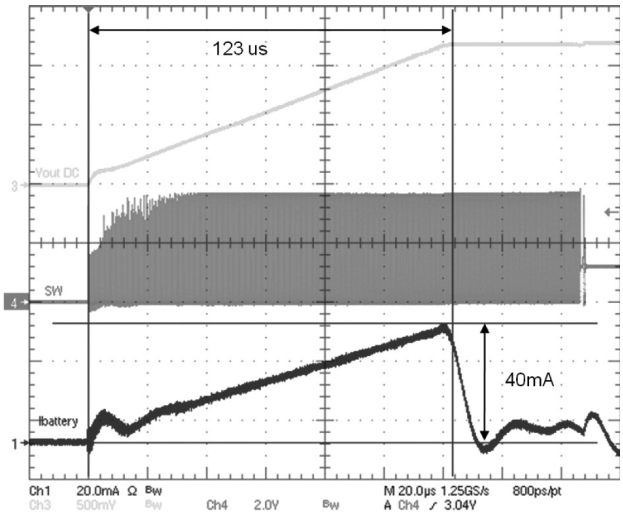

Figure 13. DCDC Soft−Start (Inrush Current, V_{in} = 3.6 V – V_{out} = 1.2 V)

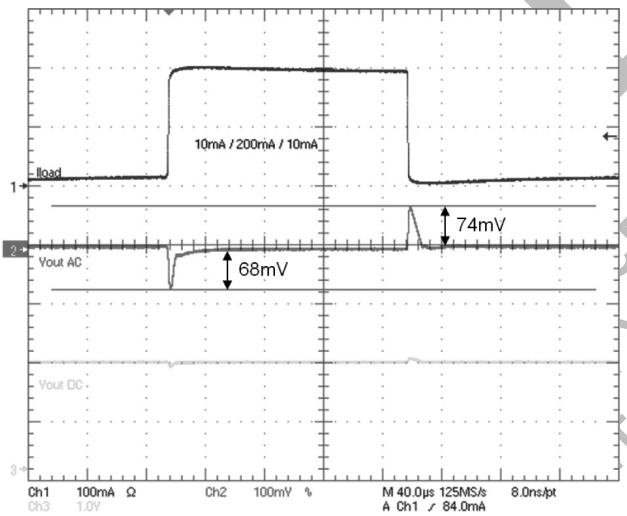

Figure 14. LDO1 Load Transient Response (V_{in} = 3.6 V – V_{out} = 1.8 V)

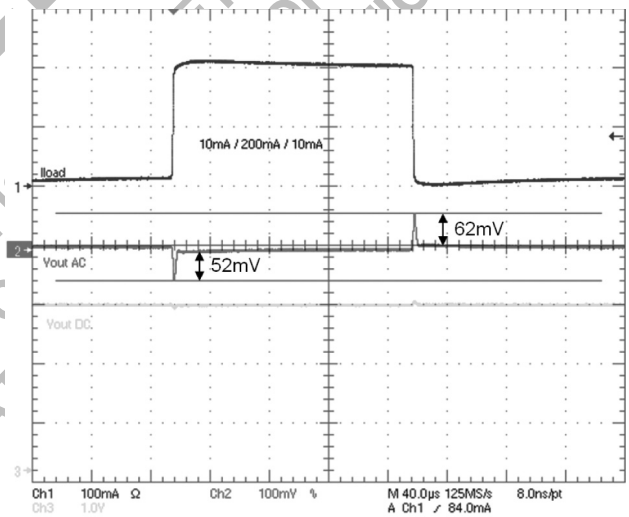

Figure 15. LDO3 Load Transient Response

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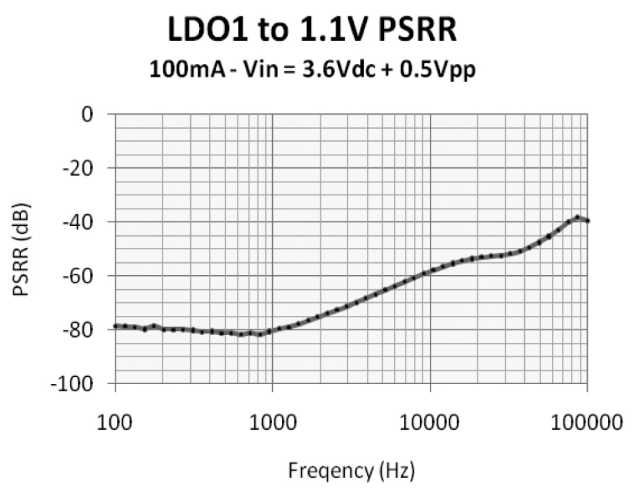

Figure 16. LDO1 PSRR

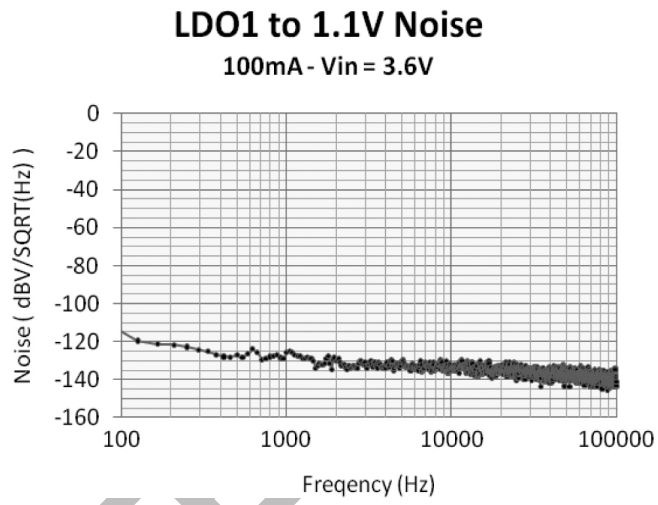

Figure 17. LDO1 Outputs Noise

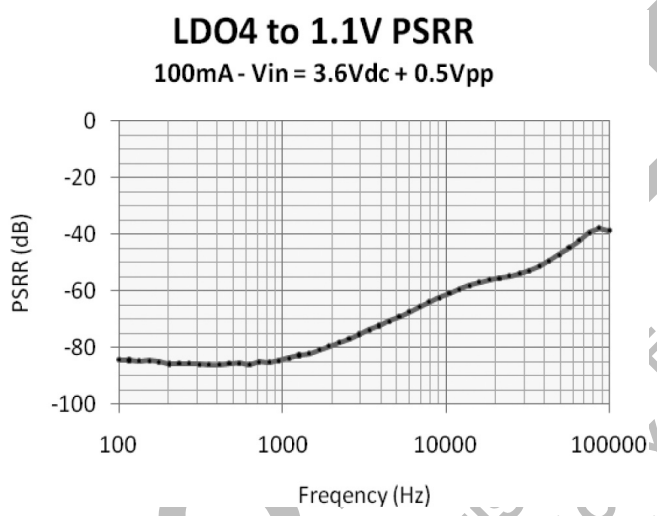

Figure 18. LDO4 PSRR

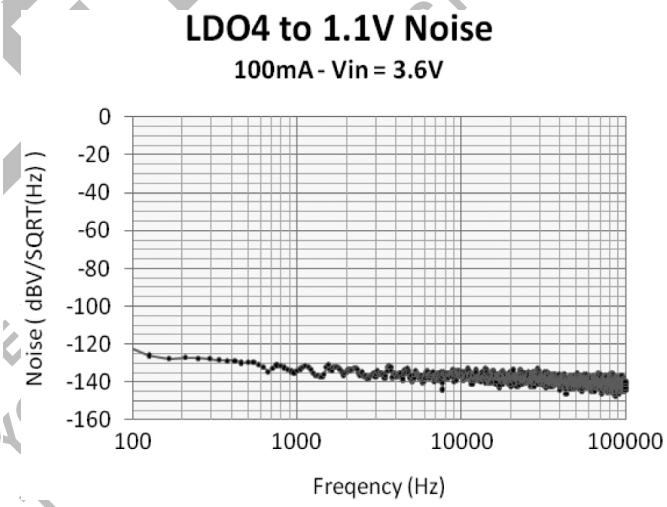

Figure 19. LDO4 Output Noise

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DETAILED DESCRIPTION

The NCP6914 is optimized to supply the different sub systems of battery powered portable applications. The IC can be supplied directly from the latest technology single cell batteries such as Lithium−Polymer as well as from triple alkaline cells. Alternatively, the IC can be supplied from a pre−regulated supply rail in case of multi−cell or main powered applications.

The output voltage range, current capabilities and performance of the switched mode DCDC converter are well suited to supply the different peripherals in the system as well as to supply processor cores. To reduce overall power consumption of the application, Dynamic Voltage Scaling (DVS) is supported on the DCDC converter. For PWM operation, the converter runs on a local 3 MHz clock. A low power PFM mode is provided that ensures that even at low loads high efficiency can be obtained. All the switching components are integrated including the compensation networks and synchronous rectifier. Only a small sized 1 μH inductor and 10 μF bypass capacitor are required for typical applications.

The general purpose low dropout regulators can be used to supply the lower power rails in the application. To improve the overall application standby current, the bias current of these regulators are made very low. The regulators each have their own input supply pin to be able to connect them independently to either the system supply voltage or to the output of the DCDC converter in the application. The regulators are bypassed with a small size 2.2 μF capacitor.

All IC features can be controlled through the I^2C interface. In addition to this bus, digital control pins including hardware enable (HWEN), power good (PG), external synchronization (SYNC) and interrupt (INTB) are provided.

UNDER VOLTAGE LOCKOUT

The core does not operate for voltages below the under voltage lockout (UVLO) threshold and all internal circuitry, both analog and digital, is held in reset.

NCP6914 functionality is guaranteed down to V_{UVLO} when the battery is falling. A hysteresis is implemented to avoid erratic on / off behavior of the IC. Due to its 200 mV hysteresis, re−start is guaranteed at 2.5 V when the battery is rising.

THERMAL SHUTDOWN

The thermal capabilities of the device can be exceeded due to the output power capabilities of the on chip step down converter and low drop out regulators. A thermal protection circuit is therefore implemented to prevent the part from being damaged. This protection circuit is only activated when the core is in active mode (at least one output channel is enabled). During thermal shutdown, all outputs of the NCP6914 are off.

When the NCP6914 returns from thermal shutdown mode, it can re−start in two different configurations depending on REARM[1:0] bits. If REARM[1:0] = 00 then NCP6914 re−starts with default register values, otherwise it re−starts with register values set prior to thermal shutdown.

In addition, a thermal warning is implemented which can inform the processor through an interrupt (if not masked) that NCP6914 is close to its thermal shutdown so that preventive measurement can be taken by software.

ACTIVE OUTPUT DISCHARGE

To prevent any disturbances on the power−up sequence, a quick active output discharge is done during the start−up sequence for all output channels.

Active output discharge can be independently enabled / disabled by the appropriate settings in the DIS register (refer to the register definition section)

When the IC is turned off through HWEN pin or AVIN drops down below UVLO threshold, no shut down sequence is expected, all supplies are disabled and outputs discharged simultaneously

ENABLING

The HWEN pin controls the device start up. If HWEN is raised, this starts the power up sequencer. If HWEN is made low, device enters in shutdown mode and all regulators are turned off.

A built−in pull−down resistor disables the device if this pin is left unconnected.

When HWEN is high, the different power rails can be independently enabled / disabled by writing the appropriate bit in the ENABLE register.

POWER UP/DOWN SEQUENCE AND HWEN

When enabling the part with the HWEN pin, the part will start up in the configuration factory programmed in the registers. Any order and output voltage setting can be factory programmed upon request.

By default (NCP6914AFCDT1G), the power up sequence is the following:

Table 5. DEFAULT POWER UP SEQUENCE FOR NCP6914AFCDT1G

Delay (in ms)	Default Assignment	Default V_{prog}	Default Mode and ON/OFF
2	DCDC	1.20 V	Auto mode ON
4	LDO1	1.80 V	ON
6	LDO2	1.80 V	ON
8	LDO3	2.80 V	ON
10	LDO4	2.80 V	ON

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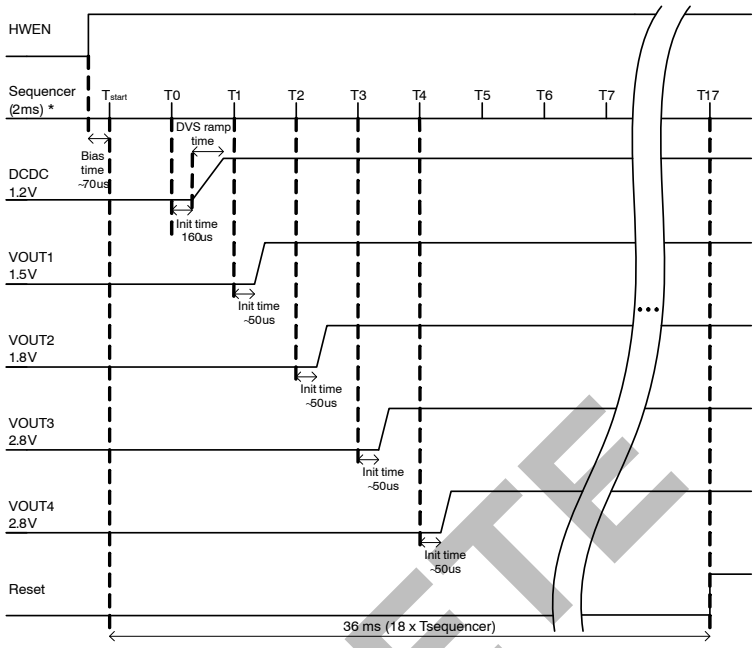

*64 μs, 128 μs and 1 ms available upon request.

Figure 20. Example of Power Up Sequence

I^{2}C registers can be read and written while HWEN pin is still low. By programming the appropriate registers (see registers description section), the power up sequence can be modified.

Reset to the factory default configuration can be achieved either by hardware reset (all power supplies removed) or by writing through the I^{2}C in the RESET register.

Table 6. POWER UP SEQUENCER

Delay (in ms)	Default Assignment	Default V_{prog}	Default Mode and ON/OFF
NCP6914AFCAT1G			
2	LDO1	1.20 V	ON
4	LDO2	1.80 V	ON
6	LDO3	2.80 V	ON
8	LDO4	2.80 V	OFF
10	DCDC	2.80 V	Auto mode ON
NCP6914AFCBT1G			
2	LDO1	1.80 V	ON
2	LDO2	1.80 V	ON
4	LDO3	2.80 V	ON
4	LDO4	2.80 V	ON
6	DCDC	2.80 V	Auto mode ON

SHUTDOWN

When shutting down the device, no shut down sequence is applied. All supplies are disabled and outputs are discharged simultaneously, and PG open drain is low whereas INTB open drain is released. However, the power down sequence can be achieved by disabling DCDC/LDOs via I2c before setting HWEN pin to low.

DYNAMIC VOLTAGE SCALING (DVS)

The step down converter support dynamic voltage scaling (DVS). This means that the output voltage can be reprogrammed based upon the I^{2}C commands to provide the different voltages required by the processor. The change between set points is managed in a smooth manner without disturbing the operation of the processor.

When programming a higher voltage, the reference of the switcher and therefore the output is raised in equidistant steps per defined time period such that the dV/dt is controlled (by default 12.5 mV/1.33 μs). When programming a lower voltage the output voltage will decrease accordingly. The DVS step is fixed and the speed is programmable.

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Figure 21. Dynamic Voltage Scaling Effect Timing Diagram

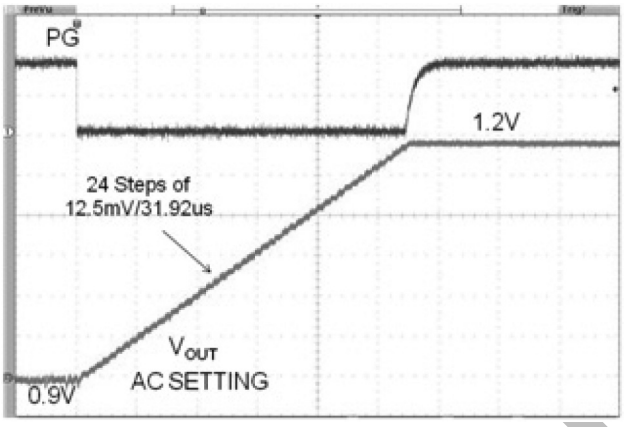

Figure 22. Dynamic Voltage Scaling Example (CH1 = PG – CH2 = V_{OUT})

Programmability

DCDC converter output voltage can be controlled by GOx bit (TIME register) with VPROGDCDC[7:0] / VDVSDCDC[7:0] registers, available output levels are listed in table VPROGDCDC[7:0] and VDVSDCDC[7:0] register description.

GOx bit determines whether DCDC output voltage value is set in VPROGDCDC[7:0] register or in VDVSDCDC[7:0] register.

Table 7. GO BIT DESCRIPTION

GO	Bit Description
0	Output voltage is set to VPROGDCDC
1	Output voltage is set to VDVSDCDC

The two DVS bits in the TIME register determine the ramp up time per each voltage step.

Table 8. DVS BITS DESCRIPTION

DVS [1:0]	Bit Description
00	1.33 μs per step (default)
01	2.67 μs per step
10	5.33us per step
11	10.67us per step

There are two ways of I^2C registers programming to switch the DCDC converters output voltages between different levels:

1. Preset VPROGDCDCx[7:0]/VDVSDCDCx[7:0] registers, and start DVS sequence by changing GOx bit state.
2. GOx bit remains unchanged, change output voltage value in either VPROGDCDCx[7:0] or VDVSDCDCx[7:0] register.

For example, the device needs to supply either 1.2 V or 0.9 V depending on working conditions. If using method 1, VPROGDCDCx[7:0] and VDVSDCDCx[7:0] should be set as shown in Table 5. GOx bit should be programmed to 1 to change DCDCx Output Voltage from 1.2 V to 0.9 V, and be programmed to 0 to move back from 0.9 V to 1.2 V.

Table 9. VPROGDCDC / VDVSDCDC SETTINGS FOR VDCDC SWITCHING BETWEEN 1.2 V AND 0.9 V

Register Name	Values	Target VDCDC (V)
VPROGDCDC	0$30	1.2
VDVSDCDC	0$18	0.9

EXTERNAL SYNCHRONIZATION

The NCP6914 allows synchronizing the DCDC converter to an external clock applied to the SYNC pin.

During the power−up sequence (or power−up of the DCDC), the IC ignores any signal applied on the SYNC pin and the DCDC converter starts switching in normal operation on the internal 3 MHz clock.

Once the power−up sequence is terminated (or DCDC output is established), external synchronization is operational depending on the internal registers settings.

If present, the signal frequency (f_{CLOCK}) applied to the SYNC pin is divided by the SYNCRATIO[4:0] bits of the SYNC register to derive the internal $f_{CLOCKINT}$.

If $f_{CLOCKINT}$ = f_{CLOCK} / SYNCRATIO[4:0] = 3 MHz ±15%, then the f_{CLOCK} is within operating frequency range.

Then, depending on the SYNCAUTO bit of SYNC register value, two cases can be considered:

- SYNCAUTO = 1: As soon as $f_{CLOCKINT}$ frequency is within the operating range, the DCDC converter clock will be $f_{CLOCKINT}$. As soon as the $f_{CLOCKINT}$ frequency is out of the operating range, the DCDC converter clock will switch back to the internal 3 MHz clock
- SYNCAUTO = 0: As soon as $f_{CLOCKINT}$ frequency is within the operating range and SYNCEN bit of SYNC register = 1, the DCDC converter clock will be $f_{CLOCKINT}$. As soon as the $f_{CLOCKINT}$ frequency is out of the operating range or SYNCEN bit of SYNC register = 0, the DCDC converter clock will switch back to the internal 3 MHz clock. If $f_{CLOCKINT}$ shifts

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out of the operating frequency range, the SYNCEN bit is automatically reset to 0.

SYNC INTERRUPTS

CLKOK (external clock ok) and CLKSEL (working clock selection) interrupt bits indicate about external clock validity and whether the DCDC converter works with the internal or external clock. Refer to the interrupt description section for more detailed information about these two bits.

PROGRAMMABILITY EXAMPLE

For a particular application where the user wants the NCP6914 DCDC converter to be synchronized with a 19.2 MHz clock:

- SYNC[4..0] = 00110: The clock frequency applied to the SYNC pin will be divided by 6 by the controller. The result will be a typical 3.2 MHz. This frequency is within the 3.0 MHz ±15% which is also within the SYNC operating range.
- SYNCAUTO = 1: The controller will continuously check the SYNC pin clock.
  SYNCEN = 1: The function is enabled.

Eventually, the user should program 66h in the SYNC register so that the IC can operate with a 19.2 MHz clock on the SYNC pin.

DCDC STEP DOWN CONVERTER AND LDO'S POWER GOOD

To indicate that the output of an output channel is established, a power good signal is available for each output channel.

The power good signal is high when the channel is off and goes low when enabling the channel. Once the output voltage reaches the expected output level, the power good signal becomes high again.

When during operation the output gets below 90% of the expected level, the power good signal goes low which indicates a power failure. When the voltage rises again above 95% the power good signal is made high again.

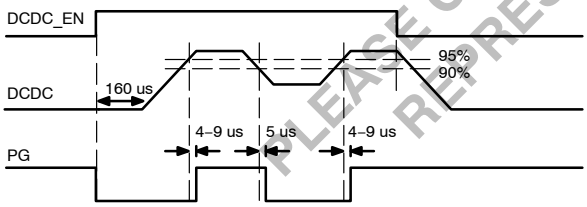

Figure 23. DCDC Channel Internal Power Good Signal

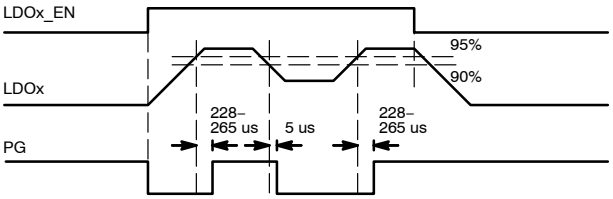

Figure 24. LDOx Channel Internal Power Good Signal

POWER GOOD ASSIGNMENT

Each channel generates an internal Power Good signal (either the DCDC or LDO's). These internal power good signals can be individually assigned to the PG pin through the PGOOD1 register. The PG pin state is an AND combination of assigned internal power good signals.

By default only the power good signal of the DCDC converter is assigned. The PG pin is an open drain output.

In addition, two other signals can be assigned to the PG pin: the internal reset signal register and the DVS signal through the PGOOD register. By assigning the internal reset signal, the PG pin is held low throughout the power up sequence and the reset period. By assigning the DVS signal of the DCDC converter, the PG pin is made low during the period the output voltage is being raised to the new setting as shown in Figure 21.

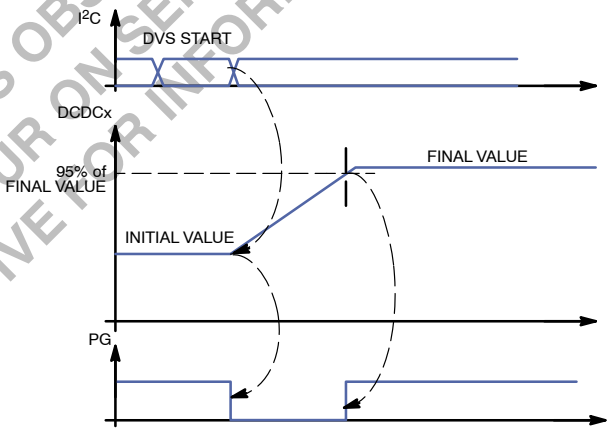

Figure 25. PG Operation in DVS Sequence

POWER GOOD DELAY

A delay can be programmed between the moment the AND result of the assigned internal power good signals becomes high and the moment the PG pin is released. The delay is set from 0 ms to 512 ms through the TOR[2:0] bits in the TIME register. The default delay is 32 ms.

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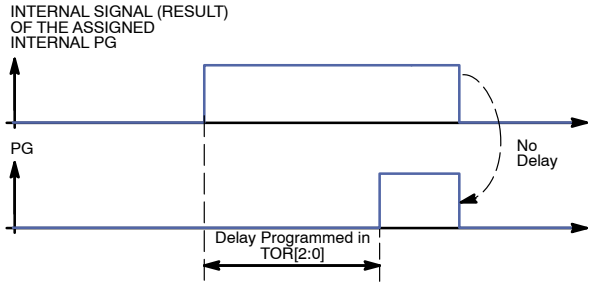

Figure 26. PG Delay

INTERRUPT

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring). The interrupt sources include:

Table 10. INTERRUPT SOURCES

PG_DCDC	Power good of DCDC converter
PG_LDO1	Power good of LDO1
PG_LDO2	Power good of LDO2
PG_LDO3	Power good of LDO3
PG_LDO4	Power good of LDO4
CLKOK	External clock valid
CLKSEL	Working clock selection
IDCDC	DCDC converter output over current
ILDO1	LDO1 output over current
ILDO2	LDO2 output over current
ILDO3	LDO3 output over current
ILDO4	LDO4 output over current
UVLO	UVLO state
WNRG	Thermal warning
TSD	Thermal shutdown

Individual bits generating interrupts will be set to 1 in the INT_ACK1/INT_ACK2 registers (I^2C read only registers), indicating the interrupt source. INT_ACK1/INT_ACK2 registers are reset by an I^2C read. INT_SEN1/INT_SEN2 registers (read only registers) are real time indicators of interrupt sources.

All interrupt sources can be masked by registers INT_MSK1/INT_MSK2. Masked sources will never generate an interrupt request on the INTB pin.

The INTB pin is an open drain output. A non masked interrupt request will result in the INTB pin driven low.

When the host reads the INT_ACK1/INT_ACK2 registers, the INTB pin is released to a high impedance state and the interrupt registers INT_ACK1/INT_ACK2 are cleared.

The figure below shows how the DCDC converter power good produces an interrupt on the INTB pin with INT_SEN1/INT_MSK1/INT_ACK1 and I^2C read access (assuming no other interrupt happens during this read period).

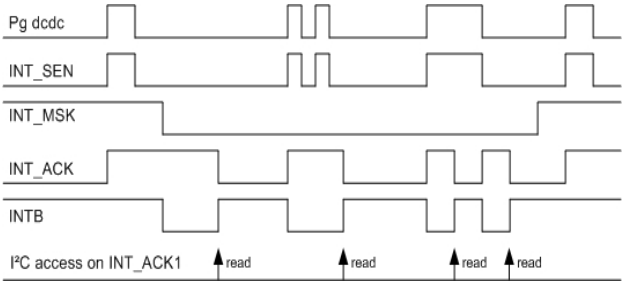

Figure 27. Interrupt Timing Chart Example of PG_DCDC

INT_MSK1 and INT_MSK2 registers are set to disable the INTB feature by default during power−up.

FORCE RESET AND I2C INTERFACE DISABLE

The I^2C interface can be disabled by the I2C_DISABLE bit in the SYNC register. This saves current consumption which is especially important when all supply channels of the NCP6914 are disabled. To re−activate the I^2C, the IC needs to be enabled through the HWEN pin.

The I^2C registers can be reset by setting the FORCERST bit in the RESET register. It forces a restart of the device with its default settings. After start−up the RSTSTATUS bit defaults to 1 and can be cleared through the I^2C.

DCDC CONVERTER

The converter can operate in two modes: PWM mode and PFM mode. In PWM mode the converter operates at a fixed frequency and adapts its duty cycle to regulate to the desired output voltage. The advantage of this mode is that the EMI noise is predictable. However, at lower loadings the efficiency is degraded. In PFM mode some switching pulses are skipped to control the output voltage. This allows maintaining high efficiency even at low loadings. In addition, no high frequency clock is required which provides additional current savings. The switchover point between both modes is chosen depending on the supply conditions such that highest efficiency is obtained over the entire load range.

The switch over between the PWM/PFM modes can occur automatically but the switcher can be set in forced PWM mode by I^2C programming.

A soft start is provided to limit inrush currents when enabling the converter. The soft start consists of ramping gradually the reference to the switcher.

Additional current limitation is provided by a peak current limiter that monitors and limits the current through the inductor.

DCDC converter output voltage can be set by the I^2C: MODEDCDC bit is used to program switcher mode control

Table 11. MODEDCDC BIT DESCRIPTION

MODEDCDC	DCDC Mode Control
0	Mode is auto switching PFM / PWM
1	Mode is PWM only

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I²C COMPATIBLE INTERFACE

NCP6914 can support a subset of I²C protocol, below are detailed introduction for I²C programming.

I²C Communication Description

ON Semiconductor communication protocol is a subset of the I²C protocol.

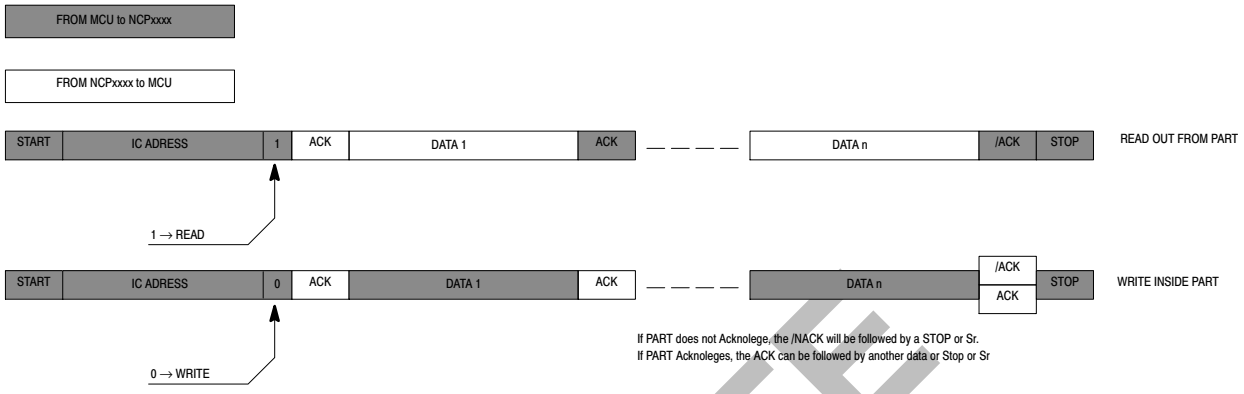

Figure 28. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a Read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) is followed by the data to be written in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1 .... The data is optional.
- In case of read operation, the NCP6914 will output the data out from the last register that has been accessed by the last write operation. Like the writing process, the reading process is an incremental process.

Read Out From Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address and the initial write transaction has set:

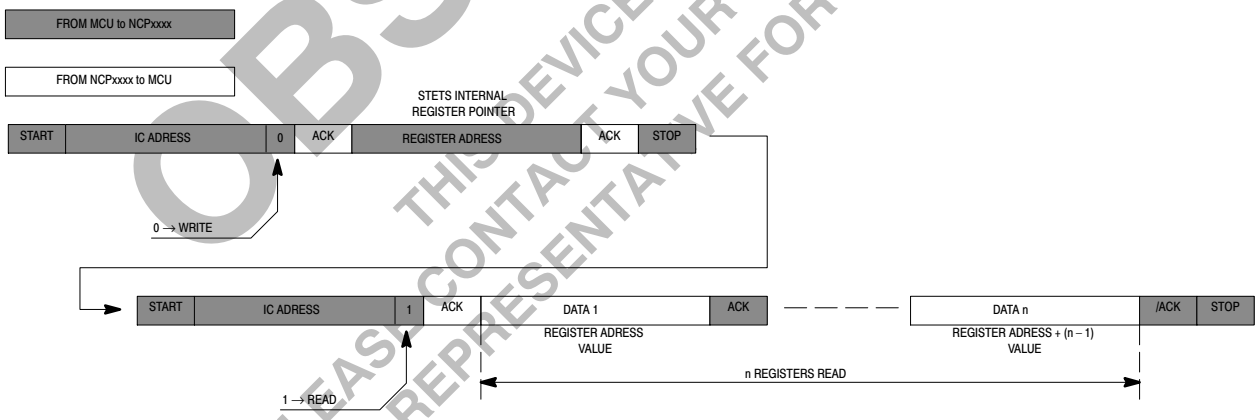

Figure 29. Read Out from Part

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The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

1. With Stop Then Start

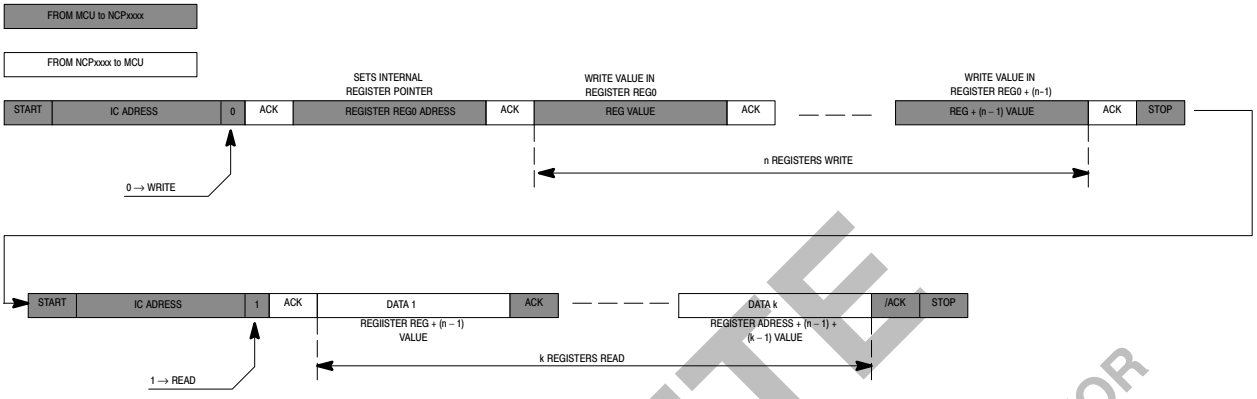

Figure 30. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2, ..., Reg +n.

Write n Registers:

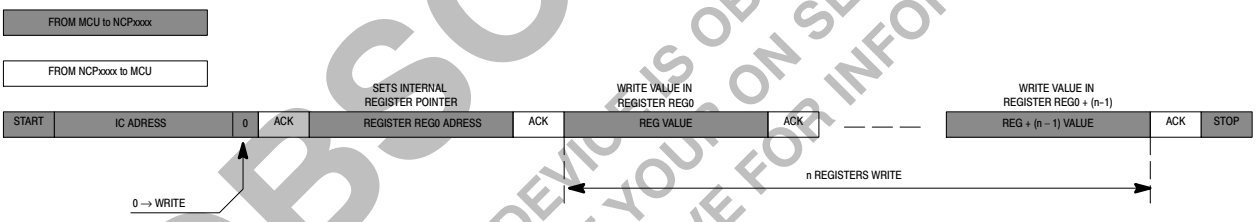

Figure 31. Write in n Registers

I²C Address

NCP6914 has fixed I²C but different I²C address (0$10, 7 bit address, see below table A7~A1), NCP6914 supports 7−bit address only.

Table 12. NCP6914 I²C Address

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
Default	$20 / $21	0	0	1	0	0	0	0	X

Other addresses are available upon request.

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REGISTER MAP

Following register map describes I^2C registers.

Registers can be:

R	Read only register
RC	Read then Clear
RW	Read and Write register
RWM	Read, Write and can be Modified by the IC
Reserved	Address is reserved and register is not physically designed
Spare	Address is reserved and register is physically designed

Address	Register Name	Type	Default	Function
$00 to 0$04	–	–	–	Reserved. Do not access to those registers
$05	–	–	–	Reserved for future use
$06 to 0$0C	–	–	–	Reserved. Do not access to those registers
$0D to $1F	–	–	–	Reserved for future use
$20	INT_ACK1	RC	$00	Interrupt 1 register (dual edge)
$21	INT_ACK2	RC	$00	Interrupt 2 register (dual edge)
$22	INT_SEN1	R	$00	Sense 1 register (real time status)
$23	INT_SEN2	R	$00	Sense 2 register (real time status)
$24	INT_MSK1	RW	$FF	Mask 1 register to enable or disable interrupt sources
$25	INT_MSK2	RW	$FF	Mask 2 register to enable or disable interrupt sources
$26 to $2F	–	–	–	Reserved for future use
$30	RESET	RW	$10	Reset internal registers to default
$31	PID	R	metal	Product Identification (metal)
$32	RID	R	metal	Revision Identification (metal)
$33	FID	R	fuse	Features Identification (fuse)
$34	ENABLE	RWM	$3E	Enable and mode register
$35	DIS	RW	$1F	Active output discharge register
$36	SYNC	RWM	$00	External synchronization setting register
$37	PGOOD	RW	$41	Power good pin assignment
$38	TIME	RW	$00	Timing definition
$39	SEQUENCER1	RW	$08	Sequencer register (DCDC and LDO1)
$3A	SEQUENCER2	RW	$1A	Sequencer register (LDO2 and LDO3)
$3B	SEQUENCER3	RW	$04	Sequencer register (LDO4)
$3C	SPARE	RW	$00	Spare register
$3D to $3F	–	–	–	Reserved for future use
$40	VPROGDCDC	RW	$30	DCDC Output Voltage Setting
$41	VDVSDCDC	RW	$30	DCDC DVS Output Voltage Setting
$42	VPROGLDO1	RW	$10	LDO1 Output Voltage Setting
$43	VPROGLDO2	RW	$10	LDO2 Output Voltage Setting
$44	VPROGLDO3	RW	$24	LDO3 Output Voltage Setting
$45	VPROGLDO4	RW	$24	LDO4 Output Voltage Setting
$46 to $FF	–	–	–	Reserved. Do not access to those registers

Details of the registers are in the following section.

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REGISTERS DESCRIPTION

Table 13. INT_ACK1 REGISTER

Name: INT_ACK1				Address: $20			
Type: RC				Default: $00			
D7	D6	D5	D4	D3	D2	D1	D0
ACK_CLKSEL	ACK_CLKOK	Spare = 0	ACK_PG_LDO4	ACK_PG_LDO3	ACK_PG_LDO2	ACK_PG_LDO1	ACK_PG_DCDC

Table 14. BIT DESCRIPTION OF INT_ACK1 REGISTER

Bit	Bit Description
ACK_PG_DCDC	DCDC1 Power Good Sense Acknowledgement 0: Cleared 1: DCDC Power Good Event detected
ACK_PG_LDO1	LDO1 Power Good Sense Acknowledgement 0: Cleared 1: LDO1 Power Good Event detected
ACK_PG_LDO2	LDO2 Power Good Sense Acknowledgement 0: Cleared 1: LDO2 Power Good Event detected
ACK_PG_LDO3	LDO3 Power Good Sense Acknowledgement 0: Cleared 1: LDO3 Power Good Event detected
ACK_PG_LDO4	LDO4 Power Good Sense Acknowledgement 0: Cleared 1: LDO4 Power Good Event detected
ACK_CLKOK	CLKOK Sense Acknowledgement 0: Cleared 1: CLKOK event detected
ACK_CLKSEL	CLKSEL Sense Acknowledgement 0: Cleared 1: CKLSEL event detected

Table 15. INT_ACK2 REGISTER

Name: INT_ACK2					Address: $21		
Type: RC					Default: $00		
D7	D6	D5	D4	D3	D2	D1	D0
ACK_TSD	ACK_WNRG	ACK_UVLO	ACK_ILDO4	ACK_ILDO3	ACK_ILDO2	ACK_ILDO1	ACK_IDCDC

Table 16. BIT DESCRIPTION OF INT_ACK2 REGISTER

Bit	Bit Description
ACK_IDCDC	DCDC Over Current Sense Acknowledgement 0: Cleared 1: DCDC1 Over Current Event detected
ACK_ILDO1	LDO1 Over Current Sense Acknowledgement 0: Cleared 1: LDO1 Over Current Event detected
ACK_ILDO2	LDO2 Over Current Sense Acknowledgement 0: Cleared 1: LDO2 Over Current Event detected
ACK_ILDO3	LDO3 Over Current Sense Acknowledgement 0: Cleared 1: LDO3 Over Current Event detected

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Table 16. BIT DESCRIPTION OF INT_ACK2 REGISTER

Bit	Bit Description
ACK_ILDO4	LDO4 Over Current Sense Acknowledgement 0: Cleared 1: LDO4 Over Current Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected
ACK_WNRG	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 17. INT_SEN1 REGISTER

Name: INT_SEN1				**Address: $22**			
Type: R				**Default: $00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_CLKSEL	SEN_CLKOK	Spare = 0	SEN_PG_LDO4	SEN_PG_LDO3	SEN_PG_LDO2	SEN_PG_LDO1	SEN_PG_DCDC

Table 18. BIT DESCRIPTION OF INT_SEN1 REGISTER

Bit	Bit Description
SEN_PG_DCDC	DCDC Power Good Sense 0: DCDC Output Voltage below target 1: DCDC Output Voltage within nominal range
SEN_PG_LDO1	LDO1 Power Good Sense 0: LDO1 Output Voltage below target 1: LDO1 Output Voltage within nominal range
SEN_PG_LDO2	LDO2 Power Good Sense 0: LDO2 Output Voltage below target 1: LDO2 Output Voltage within nominal range
SEN _PG_LDO3	LDO3 Power Good Sense 0: LDO3 Output Voltage below target 1: LDO3 Output Voltage within nominal range
SEN_PG_LDO4	LDO4 Power Good Sense 0: LDO4 Output Voltage below target 1: LDO4 Output Voltage within nominal range
SEN_CLKOK	External Clock Sense 0: Divided clock is out of the 3.0 MHz range or off 1: Divided clock is within the 3.0 MHz range
SEN_CLKSEL	Operating clock sense 0: NCP6914 is operating on internal clock 1: NCP6914 operating on external clock

Table 19. INT_SEN2 REGISTER

Name: INT_SEN2				**Address: $23**			
Type: R				**Default: $00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SEN_TSD	SEN_WNRG	SEN_UVLO	SEN_ILDO4	SEN_ILDO3	SEN_ILDO2	SEN_ILDO1	SEN_IDCDC

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Table 20. BIT DESCRIPTION OF INT_SEN2 REGISTER

Bit	Bit Description
SEN_IDCDC	DCDC over current sense 0: DCDC output current is below limit 1: DCDC output current is over limit
SEN_ILDO1	LDO1 Over Current Sense 0: LDO1 Output Current below limit 1: LDO1 Output Current over limit
SEN_ILDO2	LDO2 Over Current Sense 0: LDO2 Output Current below limit 1: LDO2 Output Current over limit
SEN_ILDO3	LDO3 Over Current Sense 0: LDO3 Output Current below limit 1: LDO3 Output Current over limit
SEN_ILDO4	LDO4 Over Current Sense 0: LDO4 Output Current below limit 1: LDO4 Output Current over limit
SEN_UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold
SEN_WNRG	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN_TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 21. INT_MSK1 REGISTER

Name: INT_MSK1				**Address: $24**			
Type: RW				**Default: $FF**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MSK_CLKSEL	MSK_CLKOK	Spare =1	MSK_PG_LDO4	MSK_PG_LDO3	MSK_PG_LDO2	MSK_PG_LDO1	MSK_PG_DCDC

Table 22. BIT DESCRIPTION OF INT_MSK1 REGISTER

Bit	Bit Description
MSK_PG_DCDC	DCDC Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_PG_LDO1	LDO1 Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_PG_LDO2	LDO2 Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_PG_LDO3	LDO3 Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_PG_LDO4	LDO4 Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked

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Table 22. BIT DESCRIPTION OF INT_MSK1 REGISTER

Bit	Bit Description
MSK_CLKOK	External Clock Detection interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_CLKSEL	Operating clock selection interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 23. INT_MSK2 REGISTER

Name: INT_MSK2					Address: $25		
Type: RW					Default: $FF		
D7	D6	D5	D4	D3	D2	D1	D0
MSK_TSD	MSK_WNRG	MSK_UVLO	MSK_ILDO4	MSK_ILDO3	MSK_ILDO2	MSK_ILDO1	MSK_IDCDC

Table 24. BIT DESCRIPTION OF INT_MSK2 REGISTER

Bit	Bit Description
MSK_IDCDC	DCDC over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO1	LDO1 over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO2	LDO2 over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO3	LDO3 over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ILDO4	LDO4 over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVLO	UVLO interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_WNRG	Thermal Warning interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TSD	Thermal Shutdown interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked

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Table 25. RESET REGISTER

Name: RESET					Address: $30		
Type: RW					Default: $10		
D7	D6	D5	D4	D3	D2	D1	D0
FORCERST	Spare = 0	Spare = 0	RSTSTATUS	Spare = 0	Spare = 0	REARM[1:0]	

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Table 26. BIT DESCRIPTION OF RESET REGISTER

Bit	Bit Description
REARM[1:0]	Rearming of device after TSD 00: Re-arming active after TSD with reset of I^2C registers: new power-up sequence is initiated with default I^2C registers values (default) 01: Re−arming active after TSD with no reset of I^2C registers: new power−up sequence is initiated with I^2C registers values 10: No re−arming after TSD 11: N / A
RSTSTATUS	Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)
FORCERST	Force Reset Bit 0: Default 1: Force reset of internal registers to default

Table 27. PID (PRODUCT IDENTIFICATION) REGISTER

Name: PID					**Address: $31**		
Type: R					**Default: Metal to $03**		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
pid7	pid6	pid5	pid4	pid3	pid2	pid1	pid0

Table 28. RID (REVISION IDENTIFICATION) REGISTER

Name: RID				**Address: $32**			
Type: R				**Default: Metal to $00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
rid7	rid6	rid5	rid4	rid3	rid2	rid1	rid0

Table 29. FID (FEATURES IDENTIFICATION) REGISTER

Name: FID					**Address: $33**		
Type: R					**Default: Fuse to $00**		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
fid7	fid6	fid5	fid4	fid3	fid2	fid1	fid0

Table 30. ENABLE REGISTER

Name: ENABLE				**Address: $34**			
Type: RWM				**Default: fuse $3E**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	ENLDO4	ENLDO3	ENLDO2	ENLDO1	ENDCDC	MODEDCDC

Table 31. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
MODEDCDC	DCDC Operating Mode 0: Auto switching PFM / PWM 1: Forced PWM
ENDCDC	DCDC Enabling 0: Disabled 1: Enabled

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Table 31. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
ENLDO1	LDO1 Enabling 0: Disabled 1: Enabled
ENLDO2	LDO2 Enabling 0: Disabled 1: Enabled
ENLDO3	LDO3 Enabling 0: Disabled 1: Enabled
ENLDO4	LDO4 Enabling 0: Disabled 1: Enabled

Table 32. DIS REGISTER

Name: DIS				Address: $35			
Type: RW				Default: $1F			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	Spare = 0	Spare = 0	DISLDO4	DISLDO3	DISLDO2	DISLDO1	DISDCDC

Table 33. BIT DESCRIPTION OF ACTIVE OUTPUT DISCHARGE REGISTER

Bit	Bit Description
DISDCDC	DCDC Active Output Discharge 0: Disabled 1: Enabled
DISLDO1	LDO1 Active Output Discharge 0: Disabled 1: Enabled
DISLDO2	LDO2 Active Output Discharge 0: Disabled 1: Enabled
DISLDO3	LDO3 Active Output Discharge 0: Disabled 1: Enabled
DISLDO4	LDO4 Active Output Discharge 0: Disabled 1: Enabled

Table 34. SYNC REGISTER

Name: SYNC				Address: $36			
Type: RWM				Default: 0$00			
D7	D6	D5	D4	D3	D2	D1	D0
I2C_DISABLE	SYNCEN	SYNCAUTO	SYNCRATIO [4:0]				

Table 35. BIT DESCRIPTION OF SYNC REGISTER

Bit	Bit Description
SYNCRATIO[4:0]	External clock divided ratio. Refer to Table 32
SYNCAUTO	Automatic External Synchronization 0: Automatic synchronization is disabled (Controlled by SYNCEN) 1: Automatic synchronization enabled and external clock is continually verified

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Table 35. BIT DESCRIPTION OF SYNC REGISTER

Bit	Bit Description
SYNCEN	External Synchronization Enabling 0: Disabled 1: Enabled
I2C_DISABLE	I^2C Interface Enabling 0: Enabled 1: Disabled

Table 36. SYNC DIVIDER RATIO VECTOR BITS DESCRIPTION

SYNCRATIO [4:0]	SYNC Ratio Divider	SYNC Typical Input Frequency	SYNCRATIO [4:0]	SYNC Ratio Divider	SYNC Typical Input Frequency
00000	0	off	10000	16	
00001	1	f_{CLOCK} = 3.0 MHz	10001	17	
00010	2		10010	18	
00011	3		10011	19	
00100	4	f_{CLOCK} = 13 MHz	10100	20	
00101	5	f_{CLOCK} = 15.36 MHz	10101	21	
00110	6	f_{CLOCK} = 16.8 MHz f_{CLOCK} = 19.2 MHz	10110	22	
00111	7		10111	23	
01000	8	f_{CLOCK} = 24 MHz f_{CLOCK} = 26 MHz	11000	24	
01001	9		11001	25	
01010	10		11010	26	
01011	11	f_{CLOCK} = 33.6 MHz	11011	27	
01100	12		11100	28	
01101	13	f_{CLOCK} = 38.4 MHz	11101	29	
01110	14		11110	30	
01111	15		11111	31	

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Table 37. PGOOD REGISTER

Name: PGOOD				Address: $37			
Type: RW				Default: $41			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	PGASSIGN_RST	PGASSIGN_DVS	PGASSIGN_LDO4	PGASSIGN_LDO3	PGASSIGN_LDO2	PGASSIGN_LDO1	PGASSIGN_DCDC

Table 38. BIT DESCRIPTION OF POWER GOOD REGISTER

Bit	Bit Description
PGASSIGN_DCDC	DCDC Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO1	LDO1 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO2	LDO2 Power Good Assignment 0: Not assigned 1: Assigned to PG

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Table 38. BIT DESCRIPTION OF POWER GOOD REGISTER

Bit	Bit Description
PGASSIGN_LDO3	LDO3 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_LDO4	LDO4 Power Good Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_DVS	DCDC DVS Assignment 0: Not assigned 1: Assigned to PG pin
PGASSIGN_RST	Internal Reset Signal Assignment 0: Not assigned 1: Assigned to PG pin

Table 39. TIME REGISTER

Name: TIME				**Address: $38**			
Type: RW				**Default: 0$00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	GO	Spare = 0	DVS [1:0]		TOR[2:0]		

Table 40. BIT DESCRIPTION OF TIMING PROGRAMMABILITY REGISTER

Bit	Bit Description
TOR[2:0]	Power Good Out of Reset Delay Time (ms) 000: 0(default) 001: 8 010: 16 011: 32 100: 64 101: 128 110: 256 111: 512
DVS[1:0]	DVS Timing (μs) 00: 1.33 μs (default) 01: 2.67 μs 10: 5.33 μs 11: 10.67 μs
GO	0: DCDC Output Voltage set to VPROGDCDC[7:0] 1: DCDC Output Voltage set to VDVSDCDC[7:0]

Table 41. SEQUENCER1 REGISTER

Name: SEQUENCER1				**Address: $39**			
Type: RW				**Default: $00**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	Spare = 0	Spare = 0	Spare = 0	DCDC_T[2:0]		

Table 42. SEQUENCER2 REGISTER

Name: SEQUENCER2				**Address: $3A**			
Type: RW				**Default: $11**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	LDO2_T[2:0]			LDO1_T[2:0]		

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Table 43. SEQUENCER3 REGISTER

Name: SEQUENCER3				Address: $3B			
Type: RW				Default: $23			
D7	D6	D5	D4	D3	D2	D1	D0
Spare = 0	Spare = 0	LDO4_T[2:0]			LDO3_T[2:0]		

Table 44. START−UP DELAY

LDOx_T[2:0] / DCDC_T[2:0]	Start−up Delay*
000	2 ms
001	4 ms
010	6 ms
011	8 ms
100	10 ms
101	12 ms
110	14 ms
111	16 ms

*64 μs, 128 μs and 1 ms available upon request.

Table 45. VPROGDCDC REGISTER

Name: VPROGDCDC				Address: $40			
Type: RW				Default: $30			
D7	D6	D5	D4	D3	D2	D1	D0
VPROGDCDC[7:0]							

Table 46. VDVSDCDC REGISTER

Name: VDVSDCDC				Address: $41			
Type: RW				Default: $30			
D7	D6	D5	D4	D3	D2	D1	D0
VDVSDCDC[7:0]							

Table 47. VPROGDCDC[7:0] AND VDVSDCDC[7:0] BITS DESCRIPTION

Bit[7:0]	VOUT(V)	Bit [7:0]	VOUT(V)	Bit [7:0]	VOUT(V)	Bit [7:0]	VOUT(V)
$00	0.6000	$40	1.4000	$80	2.2000	$C0	3.0000
$01	0.6125	$41	1.4125	$81	2.2125	$C1	3.0125
$02	0.6250	$42	1.4250	$82	2.2250	$C2	3.0250
$03	0.6375	$43	1.4375	$83	2.2375	$C3	3.0375
$04	0.6500	$44	1.4500	$84	2.2500	$C4	3.0500
$05	0.6625	$45	1.4625	$85	2.2625	$C5	3.0625
$06	0.6750	$46	1.4750	$86	2.2750	$C6	3.0750
$07	0.6875	$47	1.4875	$87	2.2875	$C7	3.0875
$08	0.7000	$48	1.5000	$88	2.3000	$C8	3.1000
$09	0.7125	$49	1.5125	$89	2.3125	$C9	3.1125
$0A	0.7250	$4A	1.5250	$8A	2.3250	$CA	3.1250
$0B	0.7375	$4B	1.5375	$8B	2.3375	$CB	3.1375

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Table 47. VPROGDCDC[7:0] AND VDVSDCDC[7:0] BITS DESCRIPTION

Bit[7:0]	VOUT(V)	Bit [7:0]	VOUT(V)	Bit [7:0]	VOUT(V)	Bit [7:0]	VOUT(V)
$0C	0.7500	$4C	1.5500	$8C	2.3500	$CC	3.1500
$0D	0.7625	$4D	1.5625	$8D	2.3625	$CD	3.1625
$0E	0.7750	$4E	1.5750	$8E	2.3750	$CE	3.1750
$0F	0.7875	$4F	1.5875	$8F	2.3875	$CF	3.1875
$10	0.8000	$50	1.6000	$90	2.4000	$D0	3.2000
$11	0.8125	$51	1.6125	$91	2.4125	$D1	3.2125
$12	0.8250	$52	1.6250	$92	2.4250	$D2	3.2250
$13	0.8375	$53	1.6375	$93	2.4375	$D3	3.2375
$14	0.8500	$54	1.6500	$94	2.4500	$D4	3.2500
$15	0.8625	$55	1.6625	$95	2.4625	$D5	3.2625
$16	0.8750	$56	1.6750	$96	2.4750	$D6	3.2750
$17	0.8875	$57	1.6875	$97	2.4875	$D7	3.2875
$18	0.9000	$58	1.7000	$98	2.5000	$D8	3.3000
$19	0.9125	$59	1.7125	$99	2.5125	$D9	3.3000
$1A	0.9250	$5A	1.7250	$9A	2.5250	$DA	3.3000
$1B	0.9375	$5B	1.7375	$9B	2.5375	$DB	3.3000
$1C	0.9500	$5C	1.7500	$9C	2.5500	$DC	3.3000
$1D	0.9625	$5D	1.7625	$9D	2.5625	$DD	3.3000
$1E	0.9750	$5E	1.7750	$9E	2.5750	$DE	3.3000
$1F	0.9875	$5F	1.7875	$9F	2.5875	$DF	3.3000
$20	1.0000	$60	1.8000	$A0	2.6000	$E0	3.3000
$21	1.0125	$61	1.8125	$A1	2.6125	$E1	3.3000
$22	1.0250	$62	1.8250	$A2	2.6250	$E2	3.3000
$23	1.0375	$63	1.8375	$A3	2.6375	$E3	3.3000
$24	1.0500	$64	1.8500	$A4	2.6500	$E4	3.3000
$25	1.0625	$65	1.8625	$A5	2.6625	$E5	3.3000
$26	1.0750	$66	1.8750	$A6	2.6750	$E6	3.3000
$27	1.0875	$67	1.8875	$A7	2.6875	$E7	3.3000
$28	1.1000	$68	1.9000	$A8	2.7000	$E8	3.3000
$29	1.1125	$69	1.9125	$A9	2.7125	$E9	3.3000
$2A	1.1250	$6A	1.9250	$AA	2.7250	$EA	3.3000
$2B	1.1375	$6B	1.9375	$AB	2.7375	$EB	3.3000
$2C	1.1500	$6C	1.9500	$AC	2.7500	$EC	3.3000
$2D	1.1625	$6D	1.9625	$AD	2.7625	$ED	3.3000
$2E	1.1750	$6E	1.9750	$AE	2.7750	$EE	3.3000
$2F	1.1875	$6F	1.9875	$AF	2.7875	$EF	3.3000
$30	1.2000	$70	2.0000	$B0	2.8000	$F0	3.3000
$31	1.2125	$71	2.0125	$B1	2.8125	$F1	3.3000
$32	1.2250	$72	2.0250	$B2	2.8250	$F2	3.3000
$33	1.2375	$73	2.0375	$B3	2.8375	$F3	3.3000

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Table 47. VPROGDCDC[7:0] AND VDVSDCDC[7:0] BITS DESCRIPTION

Bit[7:0]	VOUT(V)	Bit [7:0]	VOUT(V)	Bit [7:0]	VOUT(V)	Bit [7:0]	VOUT(V)
$34	1.2500	$74	2.0500	$B4	2.8500	$F4	3.3000
$35	1.2625	$75	2.0625	$B5	2.8625	$F5	3.3000
$36	1.2750	$76	2.0750	$B6	2.8750	$F6	3.3000
$37	1.2875	$77	2.0875	$B7	2.8875	$F7	3.3000
$38	1.3000	$78	2.1000	$B8	2.9000	$F8	3.3000
$39	1.3125	$79	2.1125	$B9	2.9125	$F9	3.3000
$3A	1.3250	$7A	2.1250	$BA	2.9250	$FA	3.3000
$3B	1.3375	$7B	2.1375	$BB	2.9375	$FB	3.3000
$3C	1.3500	$7C	2.1500	$BC	2.9500	$FC	3.3000
$3D	1.3625	$7D	2.1625	$BD	2.9625	$FD	3.3000
$3E	1.3750	$7E	2.1750	$BE	2.9750	$FE	3.3000
$3F	1.3875	$7F	2.1875	$BF	2.9875	$FF	3.3000

Table 48. VPROGLDO1 REGISTERS

Name: VPROGLDO1				**Address: $42**			
Type: RW				**Default: $10**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	VPROGLDO1[5:0]					

Table 49. VPROGLDO2 REGISTERS

Name: VPROGLDO2				**Address: $43**			
Type: RW				**Default: $10**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	VPROGLDO2[5:0]					

Table 50. VPROGLDO3 REGISTERS

Name: VPROGLDO3				**Address: $44**			
Type: RW				**Default: $24**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	VPROGLDO3[5:0]					

Table 51. VPROGLDO4 REGISTERS

Name: VPROGLDO4				**Address: $45**			
Type: RW				**Default: $24**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	VPROGLDO4[5:0]					

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Table 52. VPROGLDOX[5:0] BITS DESCRIPTION

VPROGLDOx [5:0]	VOUT (V)	VPROGLDOx [5:0]	VOUT (V)	VPROGLDOx [5:0]	VOUT (V)	VPROGLDOx [5:0]	VOUT (V)
$00	1.00	$10	1.80	$20	2.60	$30	3.30
$01	1.05	$11	1.85	$21	2.65	$31	3.30
$02	1.10	$12	1.90	$22	2.70	$32	3.30
$03	1.15	$13	1.95	$23	2.75	$33	3.30
$04	1.20	$14	2.00	$24	2.80	$34	3.30
$05	1.25	$15	2.05	$25	2.85	$35	3.30
$06	1.30	$16	2.10	$26	2.90	$36	3.30
$07	1.35	$17	2.15	$27	2.95	$37	3.30
$08	1.40	$18	2.20	$28	3.00	$38	3.30
$09	1.45	$19	2.25	$29	3.05	$39	3.30
$0A	1.50	$1A	2.30	$2A	3.10	$3A	3.30
$0B	1.55	$1B	2.35	$2B	3.15	$3B	3.30
$0C	1.60	$1C	2.40	$2C	3.20	$3C	3.30
$0D	1.65	$1D	2.45	$2D	3.25	$3D	3.30
$0E	1.70	$1E	2.50	$2E	3.30	$3E	3.30
$0F	1.75	$1F	2.55	$2F	3.30	$3F	3.30

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APPLICATION INFORMATION

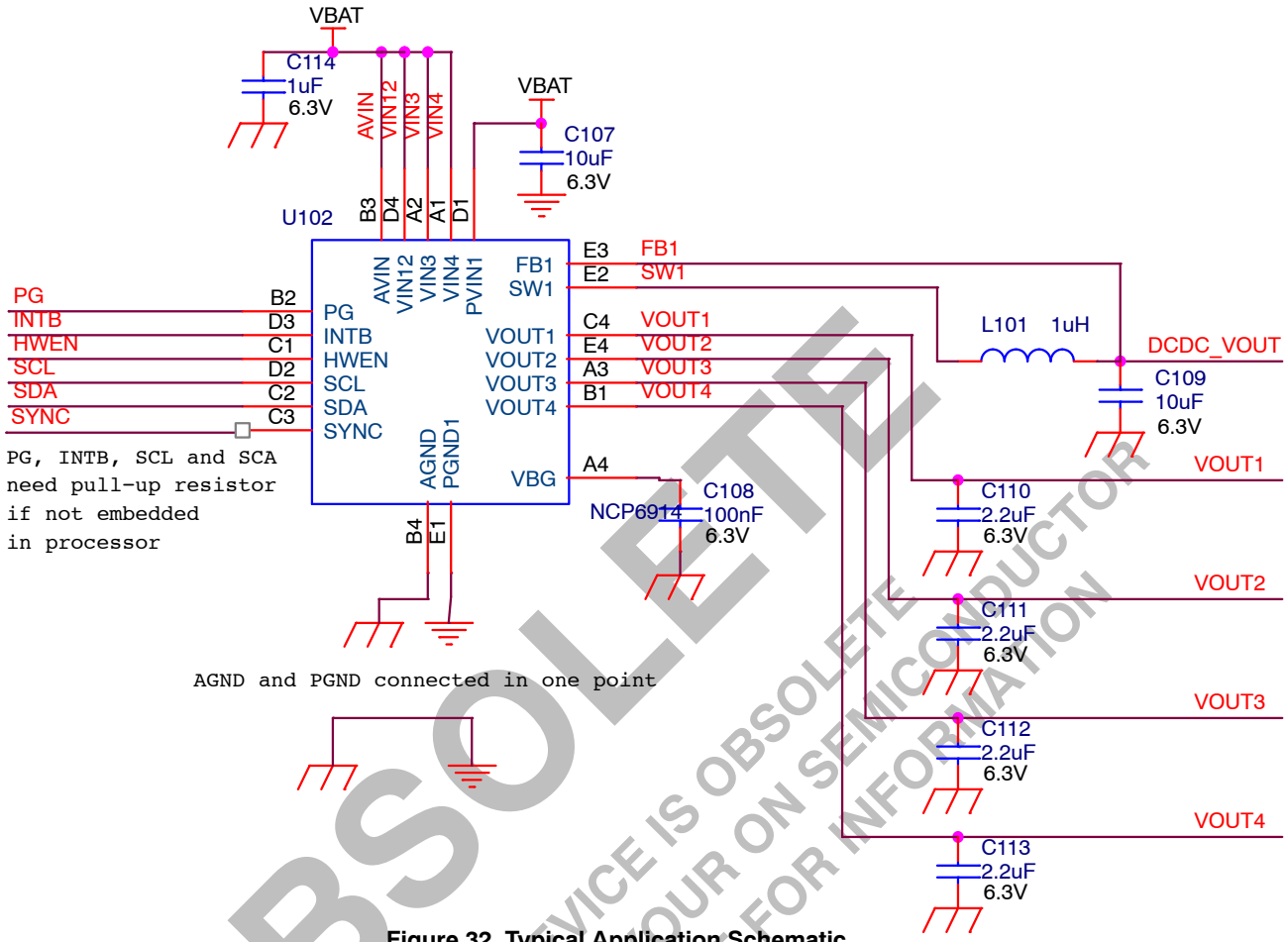

Figure 32. Typical Application Schematic

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Inductor Selection

NCP6914 DCDC converter typically uses 1 µH inductor. Use of different values can be considered to optimize operation in specific conditions. The inductor parameters directly related to device performances are saturation current, DC resistance and inductance value. The inductor ripple current (ΔI_L) decreases with higher inductance.

$$\Delta V_L = V_{szie}7O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \qquad \text{(eq. 1)}$$

$$I_{LMAX} = I_{OMAX} + \frac{\Delta I_L}{2} \qquad \text{(eq. 2)}$$

With:

- F_{SW} = Switching Frequency (Typical 3 MHz)
- L = Inductor value
- ΔI_L = Peak−To−Peak inductor ripple current
- I_{LMAX} = Maximum Inductor Current

To achieve better efficiency, ultra low DC resistance inductor should be selected.

The saturation current of the inductor should be higher than the I_{LMAX} calculated with the above equations.

Table 53. INDUCTOR L = 1.0 µH

Manufacturer	Part Number	Case Size	Height Typ. (mm)	L (µH)
MURATA	LQM2HPN1R0MG0	2.5 x 2.0	1.0	1.0
MURATA	LQH33PN1R0NJ0	3.0 x 3.0	1.2	1.0
MURATA	LQH44PN1R0NJ0	4.0 x 4.0	1.8	1.0
TDK	VLS201612ET−1R0	2.0 x 1.6	1.2	1.0

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Table 54. INDUCTOR L = 2.2 μH

Manufacturer	Part Number	Case Size	Height Typ. (mm)	L (μH)
MURATA	LQM2HPN2R2MG0	2.5 x 2.0	1.0	2.2
MURATA	LQH44PN2R2MP0	4.0 x 4.0	1.8	2.2
TDK	VLS201612ET−2R2	2.0 x 1.6	1.2	2.2

Output Capacitor Selection for DCDC Converter

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \times \left(\frac{1}{2 \times \pi \times C_O \times f} + ESR\right) \quad \text{(eq. 3)}$$

Table 55. RECOMMENDED OUTPUT CAPACITOR FOR DCDC CONVERTER

Manufac-turer	Part Number	Case Size	Height Typ. (mm)	C (μF)
MURATA	GRM188R60J106ME47	0603	0.8	10
MURATA	GRM219R60J106KE19	0805	1.25	10
MURATA	GRM21BR60J226ME39	0805	1.25	22
TDK	C1608X5R0C106K/M	0603	0.8	10
TDK	C2012X5R0C106K/M	0805	1.25	10
TDK	C2012X5R0C226K/M	0805	1.25	22

Input Capacitor Selection for DCDC Converter

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is 1/2 of maximum output current. A low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the VIN Pin.

Table 56. RECOMMENDED INPUT CAPACITOR FOR DCDC CONVERTER

Manufac-turer	Part Number	Case Size	Height Typ. (mm)	C (μF)
MURATA	GRM188R60J475KE	0603	0.8	4.7
MURATA	GRM188R60J106ME	0603	0.8	10
TDK	C1608X5R0C475K/M	0603	0.8	4.7
TDK	C1608X5R0C106K/M	0603	0.8	10

Output Capacitor Selection for LDOs

For stability reason, a typical 2.2 μF output capacitor is suitable for LDOs. The output capacitor should be placed as close as possible to the NCP6914 output pin.

Input Capacitor Selection for LDOs

NCP6914 LDOs do not require specific input capacitor. However, an input typical 1uF ceramic capacitor placed close to NCP6914 is helpful for load transient.

Input of LDO can be connected to main power supply. However, for optimum efficiency and lower NCP6914 thermal dissipation, lowest voltage available in the system is preferred. Input voltage of LDO, should always be higher than $V_{OUT} + V_{DROP}$ (V_{DROP}, being the dropout voltage at maximum current).

Capacitor DC bias Characteristics

Real capacitance of ceramic capacitor changes versus DC voltage. Special care should be taken to DC bias effect in order to make sure that the real capacitor value is always higher than the minimum allowable capacitor value specified.

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PCB LAYOUT RECOMMENDATION

The high speed operation of the NCP6914 demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device any high current copper trace which see high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground tracks.

Both the inductor and input/output capacitor of DCDC converter are in the high frequency switching path where current flow may be discontinuous. These components should be placed as close as possible to reduce parasitic inductance connection. Also it is important to minimize the area of the switching nodes and used the ground plane under them to minimize cross−talk to sensitive signals and IC. It's suggested to keep as complete ground plane under NCP6914 as possible.

PGND and AGND pin connection must be connected to the ground plane. Care should be taken to avoid noise interference between PGND and AGND.

Finally it is always good practice to keep the sensitive tracks such as feedback connection (FB1) away from switching signal connections (SW1) by laying the tracks on the other side or inner layer of PCB.

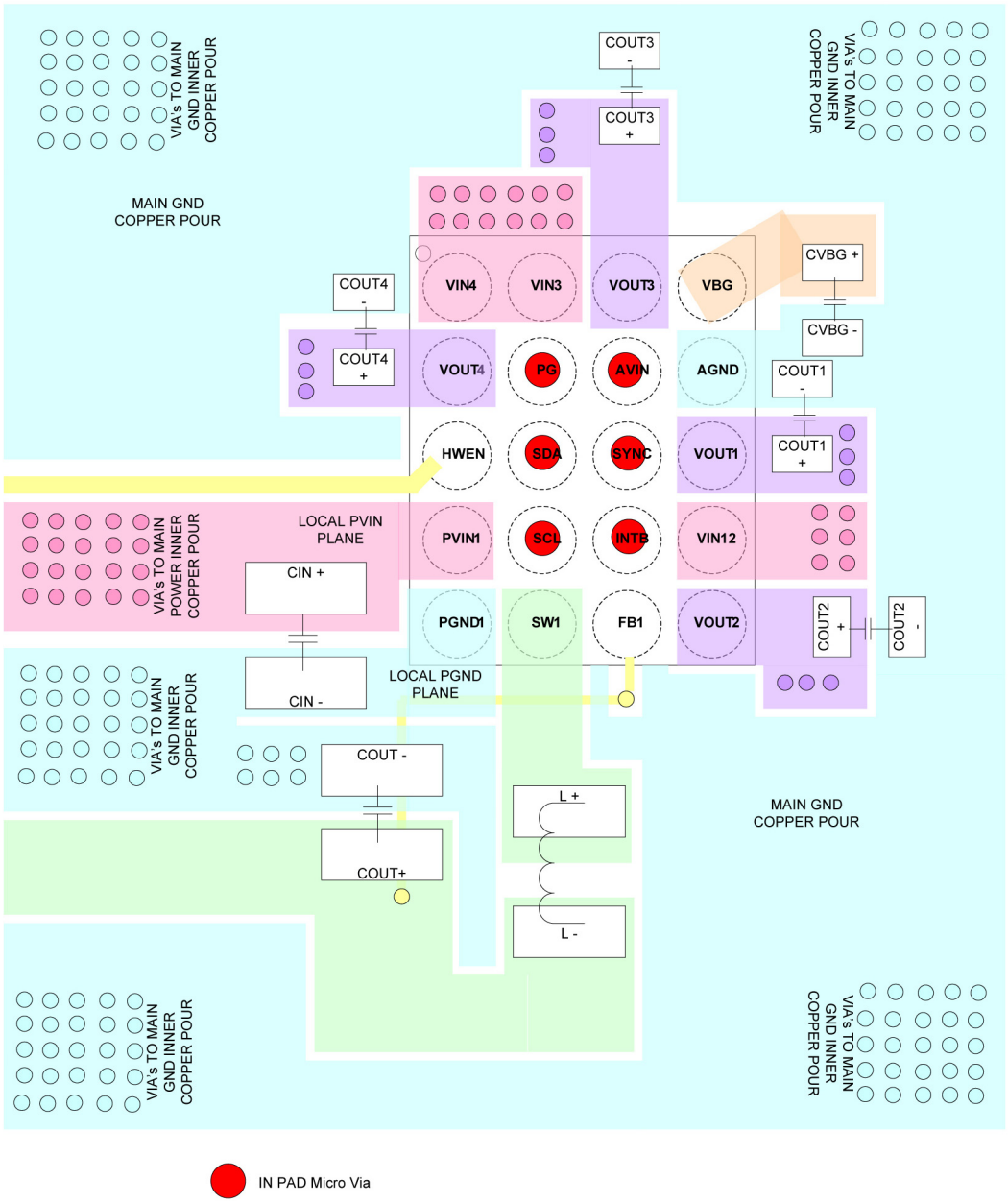

Figure 33. Recommended PCB Layout

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THERMAL CONSIDERATIONS

Careful attention must be paid to the internal power dissipation of the NCP6914. The power dissipation is a function of efficiency and output power. Hence, increasing the output power requires better components selection. Care should be taken of dropout voltage of LDOs, the larger it is, the higher dissipation it will bring to NCP6914. Keep large copper plane under and close to NCP6914 is helpful for thermal dissipation too.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP6914AFCDT1G (Default)*	6914AD	WLCSP20 – 1.77 x 2.06 mm (Pb–Free)	3000 / Tape & Reel
NCP6914AFCAT1G*	6914AA	WLCSP20 – 1.77 x 2.06 mm (Pb–Free)	3000 / Tape & Reel
NCP6914AFCBT1G*	6914AB	WLCSP20 – 1.77 x 2.06 mm (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This is flip chip package without die coating

Demo Board Available:
The NCP6914GEVB/D evaluation board configures the device in typical application to supply constant voltage.

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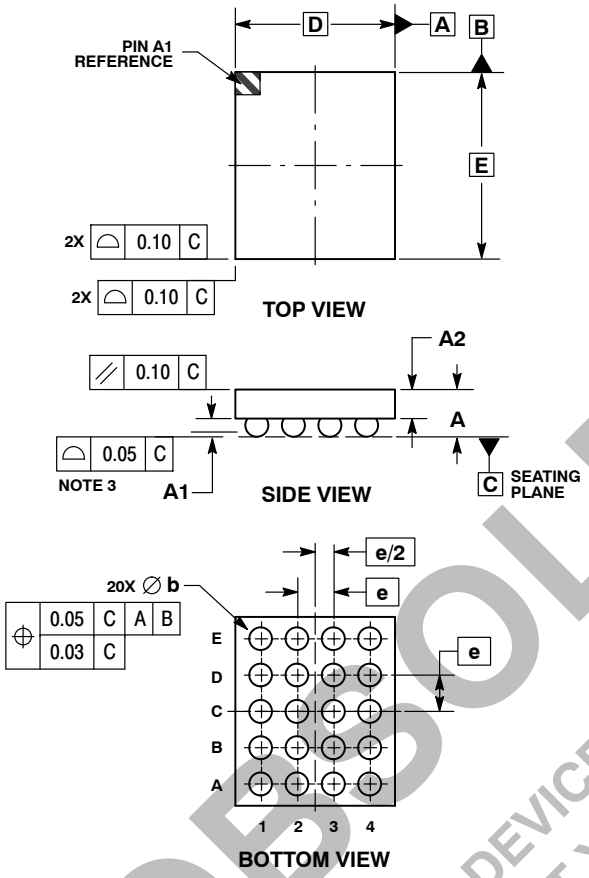
PACKAGE DIMENSIONS

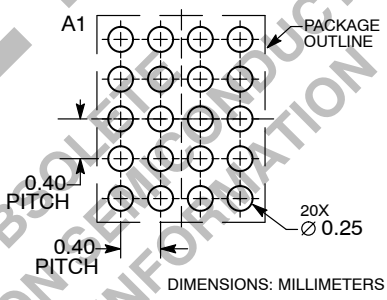
WLCSP20, 1.77x2.06
CASE 567CV
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.60
A1	0.17	0.23
A2	0.33	0.39
b	0.24	0.29
D	1.77 BSC	
E	2.06 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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