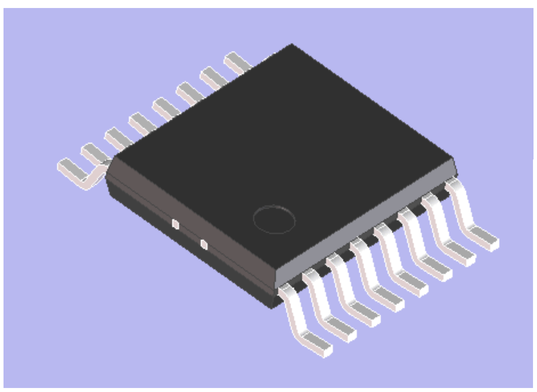
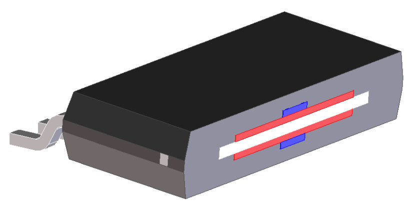
TAD4140 360° Angle Sensor

Product Datasheet





TDK

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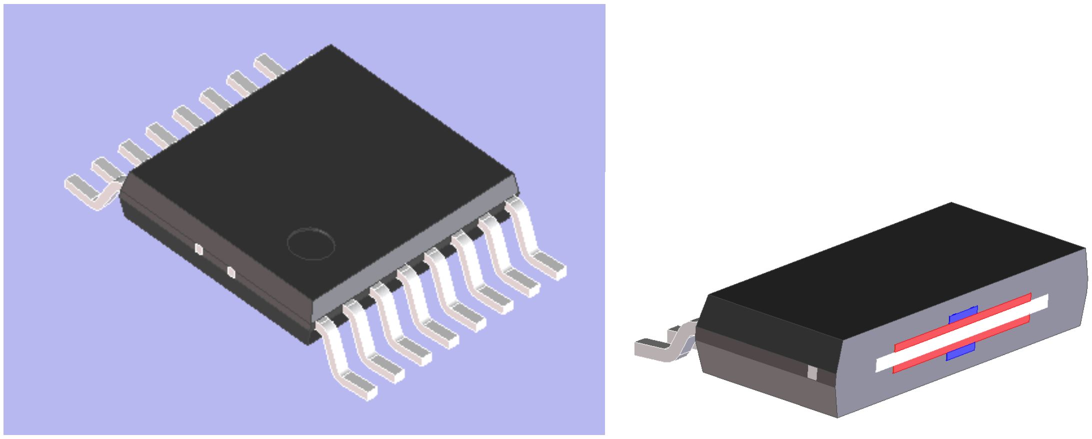
2 Product description



*In right figure, blue chips are TMR sensor chips, and red chips are ASIC chips.

Figure 1: TAD4140 Angle Sensor (TSSOP-16)

TAD4140 is an intelligent angle sensor with TMR (Tunnel Magnet Resistance) technology. It detects 360 degrees in one rotation. 2 chips of 2 full bridges of TMR angle sensor and 2 chips of digital signal processing ASIC are contained in one package.
TAD4140 is a pre-calibrated sensor. The calibration parameters are stored in NVM (Non Volatile Memory), which is OTP (One Time Programmable) memory. When customer uses it in his application, this sensor has "calibration mode". This calibration consists of "Static compensation" and "Dynamic compensation". The "Static compensation" targets the elimination of angle errors caused by the mechanical misalignment between magnet and sensor. In operation, TAD4140 improves the angle accuracy to excellent levels by using the "Dynamic compensation" mechanism, which eliminates magnetic, temperature, and lifetime effects.
TAD4140 supports various output interface functionality such as Encoder, HSM (Hall Switch Mode), PWM (Pulse Width Modulation), and SPI.

2.1 Product Features

- Intelligent angle sensor with TMR technology
- 360° contactless angle measurement
- 2 chips of TMR angle sensor and digital signal processing ASIC in one package.
- Static/Dynamic compensation achieves excellent angle accuracy
- Various & Configurable Digital output IF (Encoder, HSM, PWM, SPI).
- User programming interface of SPI for various IF configuration.
- Pb-free package, RoHS compliant

2.2 Safety Features

TAD4140 for Automotive use (TAD4140-BAXX) offers a number of safety functions to support ASIL D system requirements.
Safety feature are:

- The generic assumed safety goal is to avoid angular errors of bigger than 5° with a fault detection time tolerance of max 5ms.
- Two independent communication interfaces can be activated.

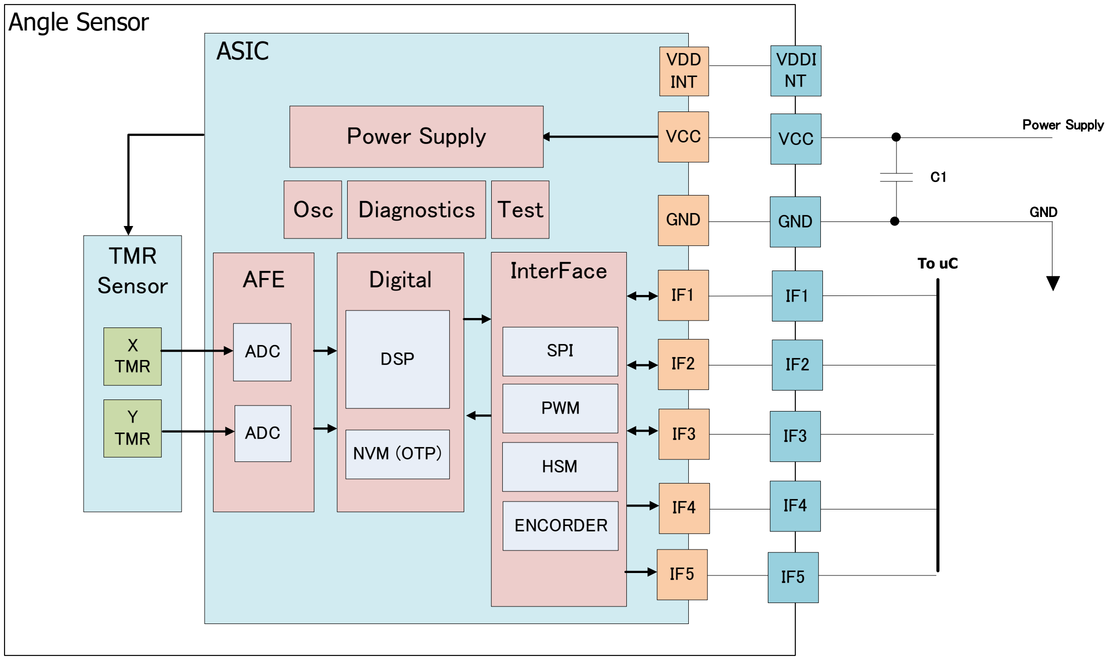
- Configuration and calibration data is stored into an OTP with redundant bit cells allowing Single Bit Detection. (Two physical bit cells)
- Diagnostic analysis is performed during and after start-up of sensor.
- The implemented diagnostics are "Magnet loss", "Speed limit", "OverVoltage Vcc", "UnderVoltage Vcc", "Sensor Abnormal", "Resistor CRC", "AFE check", "OTP CRC".

2.3 Product Application

TAD4140 can be applied into many applications where a magnetic field direction needs to be determined (within the magnetic specifications). This sensor can sense the angle of the subject by the magnetic field direction on x-y plane. TMR Angle Sensor chip has two Wheatstone bridges which output Sin, Cos waveforms when the subject with a magnet rotates. This product calculates the angle from the output of TMR Angle Sensor, compensates dynamically (i.e. under continuous rotation of the motor) for errors and generates the corresponding digital outputs, using Encoder or Hall Switch mode and SPI. A second and parallel communication channel is available using PWM interface protocol.
The target applications are those where a mechanical rotation of a magnet is to be measured.

3 Functional description

3.1 Function block diagram



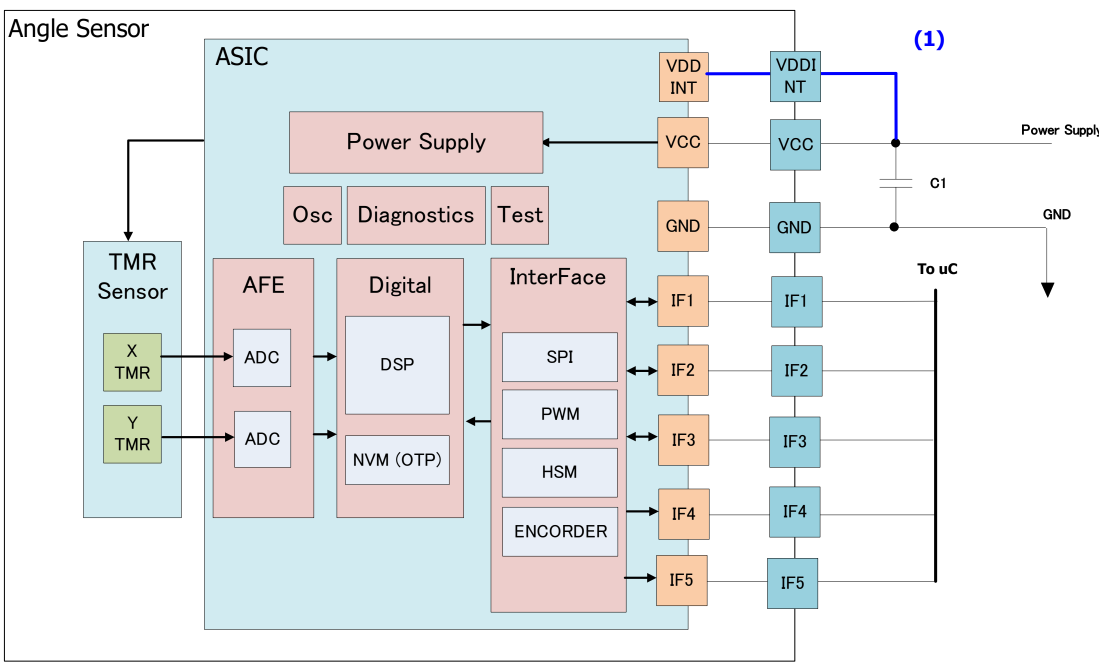


Figure 2: TAD4140 function block diagram (upper 5V operation, lower 3.3V operation)

Figure 2 is describing one of the 2 chips.

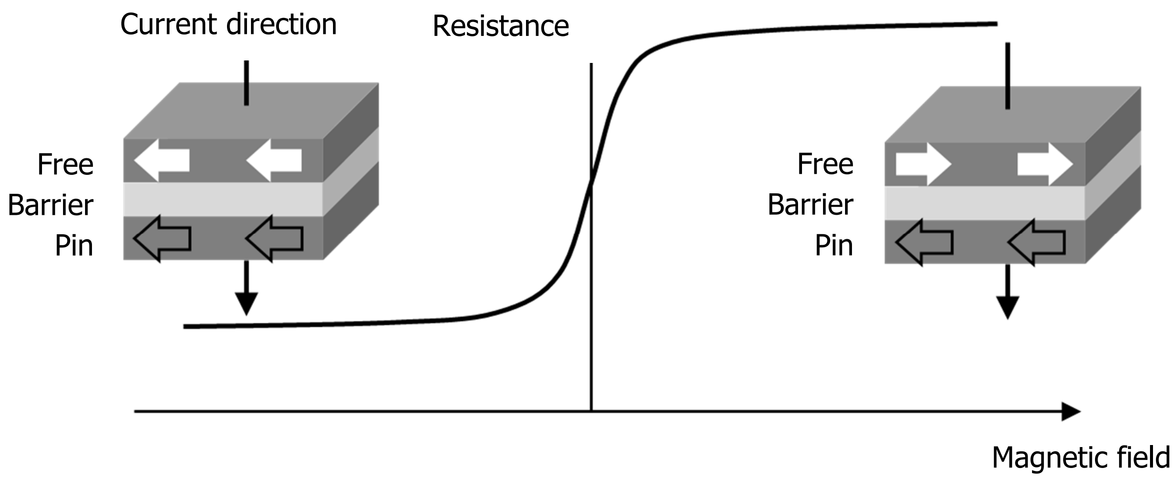
(1) User will connect VDDINT and VCC together at user's PCB side.

3.2 Function block description

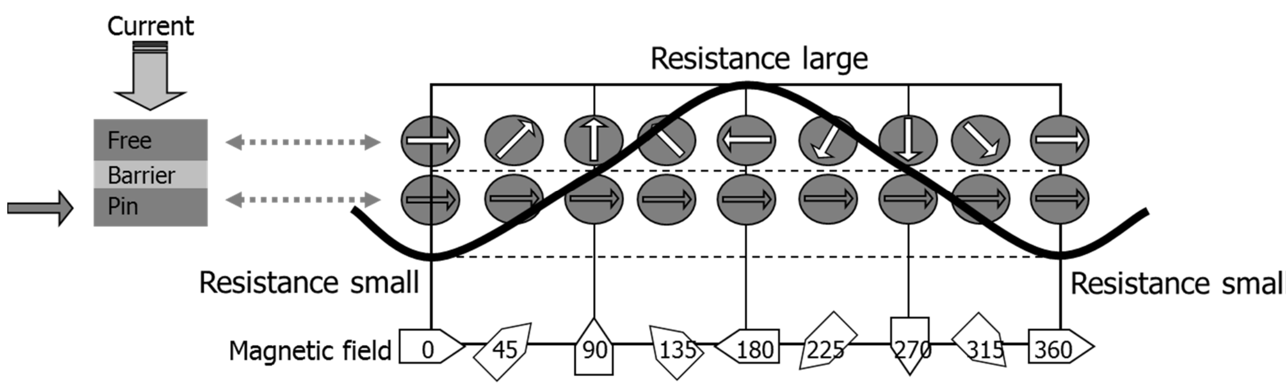
3.2.1 TMR Sensor

3.2.1.1 Sensor principle

TMR stands for Tunnel Magneto Resistance. It has a laminated thin film structure in which an insulating thin film layer (Barrier layer) is sandwiched between ferromagnetic thin film layers (Pin layer, Free layer). The magnetic direction of free layer moves toward external magnetic field, and the magnetic direction of Pin layer is fixed not to move by external magnetic field. When the magnetic direction of Free layer and Pin layer are parallel the resistance of TMR device is minimum. When both directions are anti-parallel the resistance of TMR device is maximum.



TMR sensor detects the magnetic direction on X-Y surface. The resistance of TMR device changes by relative magnetic direction of Pin layer and Fee layer. When pin layer and free layer close to parallel the resistance become small, and when both layer close to anti-parallel the resistance become large.



By combining TMR sensors that magnetic direction of Pin layer are different, Wheatstone bridge circuit which output Sin and Cos waveform in 1 system is composed.

The double TMR element in figure 3 represents the Angle Sensor. It can sense the angle of the subject by the magnetic field direction in x-y plane. The TMR elements change their bridge resistance depending on the direction of the magnetic field. Each TMR element is a Wheatstone bridges which output Sin or Cos waveforms when the subject rotates the magnetic field.

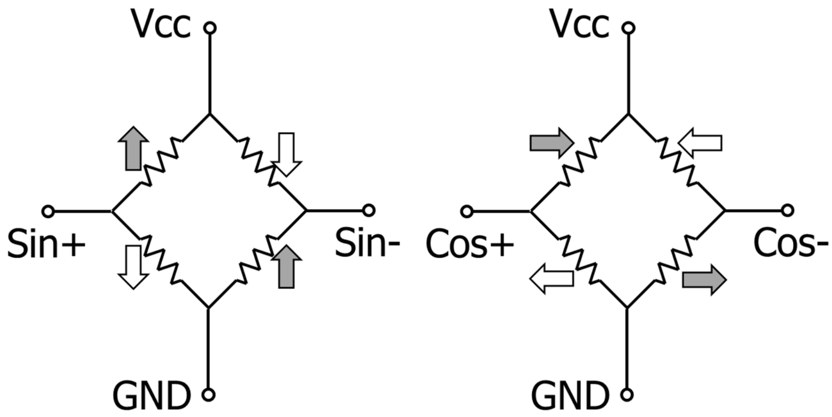


Figure 3: Wheatstone bridges structure of TMR sensor (not to scale)

Arrows in Figure 3 show the magnetic direction of Pin layer. When external magnetic field rotates 360deg, electrical output of Sin+, Sin-, Cos+ and Cos- are obtained from output terminal of each Wheatstone bridge circuit.
By taking voltage difference between Sin+ and Sin-, Cos+ and Cos-, TMR output is obtained such as Figure 4 when external magnetic field rotates 360 deg.

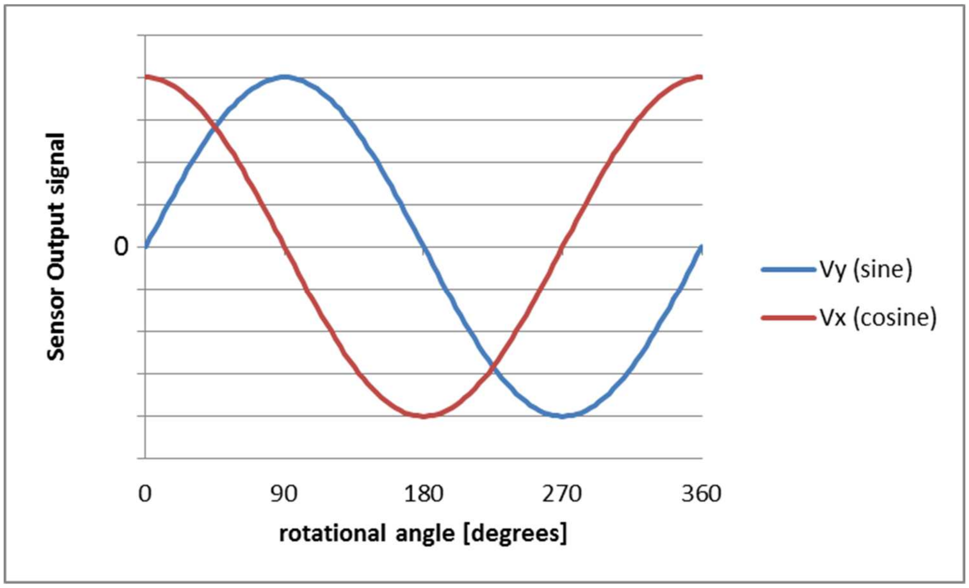


Figure 4: Ideal output signal of TMR sensor

3.3 Pin Description

Figure 5 shows the Pin layout of TAD4140 Angle Sensor (TSSOP-16).

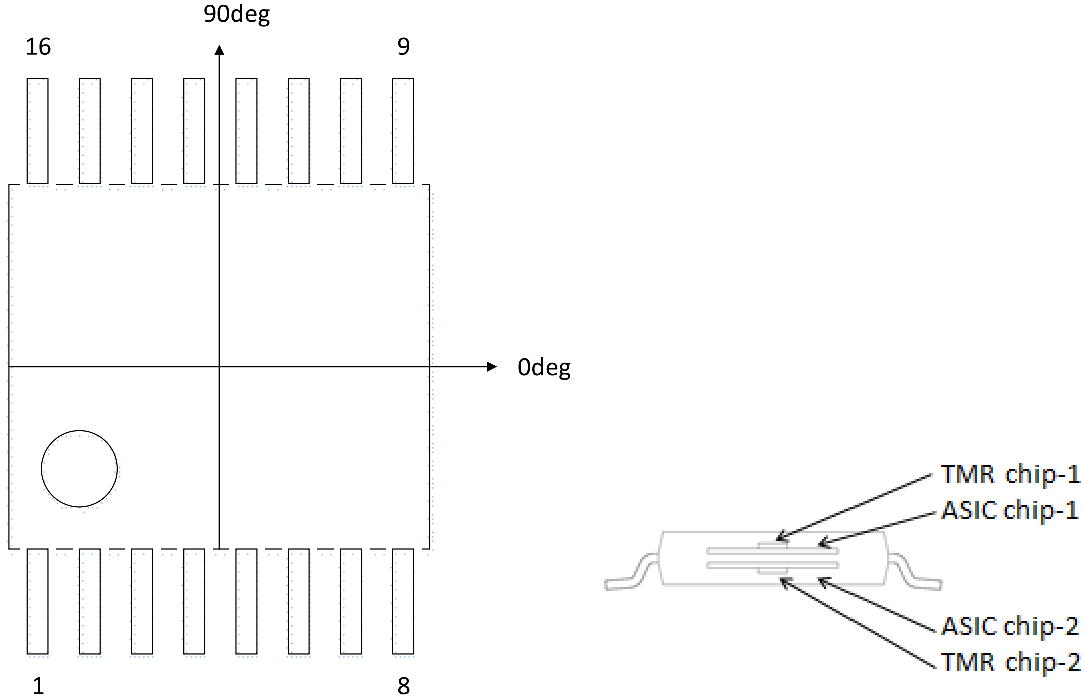


Figure 5: Pin layout and angle definition of TMR sensor (not to scale)

Table 1 shows Pin description for each mode 1~3.

Pin No.	chip	Symbol	Mode1 SPI/SPI	Mode2 UVW/UVW	Mode3 ENC/ENC	Mode3 ENC/UVW	Comment
1	1	IF1-1	MISO	U	A	A	VDDINT pin Needed only for 3.3V user
2		IF1-2	MOSI	V	B	B	
3		IF1-3	SCLK	W	Z	Z	
4		IF1-4	CS	N/A	N/A	N/A	
5		GND1	GND1	GND1	GND1	GND1	
6		IF1-5	PWM	PWM	PWM	PWM	
7		VCC1	VCC1	VCC1	VCC1	VCC1	
8		VDDINT1	VDDINT1	VDDINT1	VDDINT1	VDDINT1	
9	2	VDDINT2	VDDINT2	VDDINT2	VDDINT2	VDDINT2	
10		VCC2	VCC2	VCC2	VCC2	VCC2	
11		IF2-5	PWM	PWM	PWM	PWM	
12		GND2	GND2	GND2	GND2	GND2	
13		IF2-4	CS	N/A	N/A	N/A	
14		IF2-3	SCLK	W	Z	W	
15		IF2-2	MOSI	V	B	V	
16		IF2-1	MISO	U	A	U	

Table 1: Pin description for mode1~3 of TAD4140

(*) upper side chip is chip-1 and lower side chip is chip-2 as Figure 3 showed.

4 Operation modes

Figure 6 shows the different modes of operation of the sensor use case.

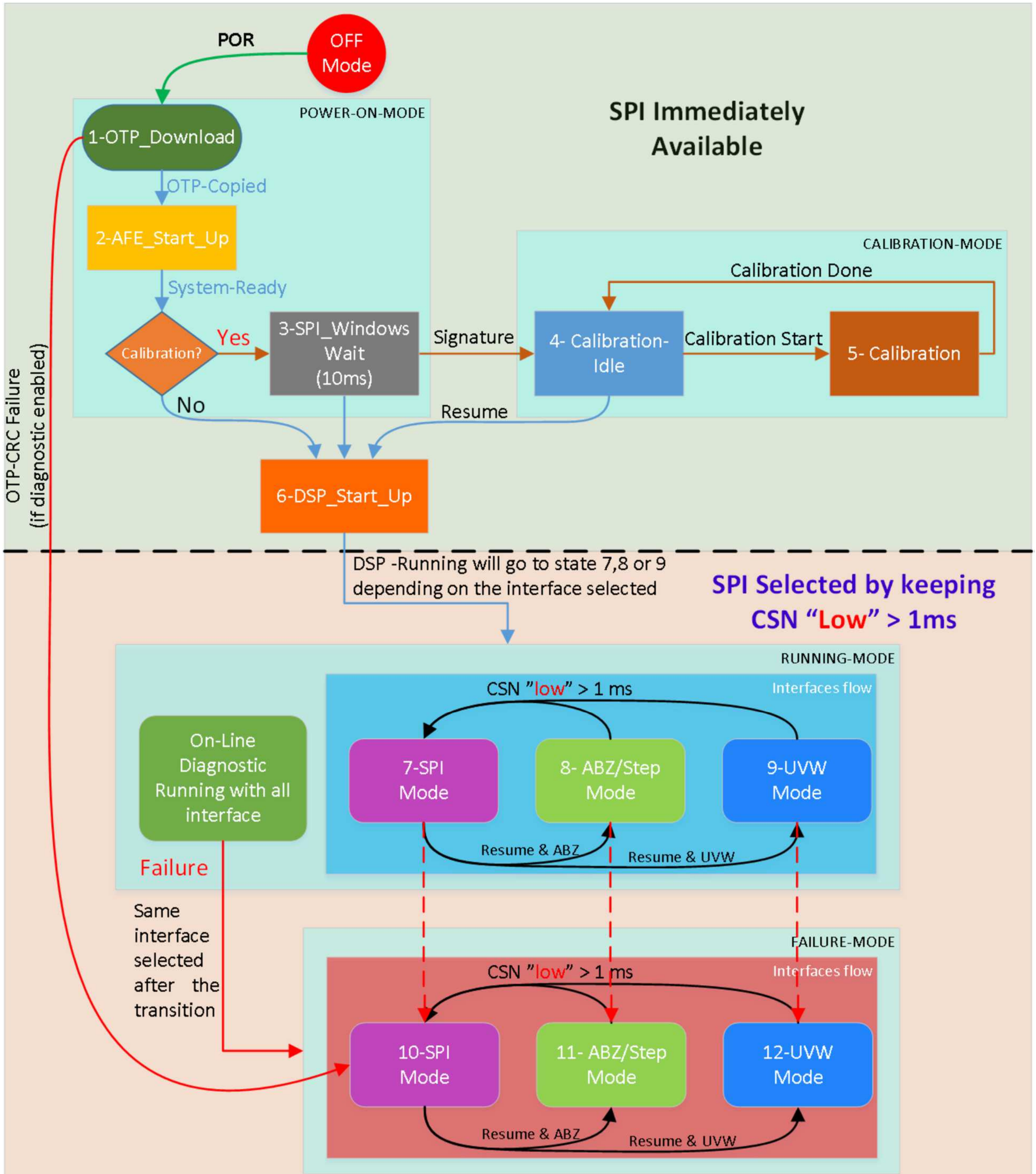


Figure 6: Operation modes and transitions

SPI is available in the green colored state and "7-SPI-Mode". In all other state, it is necessary to assert the CSN signal for more than 1ms to activate SPI.

4.1 Absolute maximum ratings

Stresses above those listed in this section may cause immediate and permanent device failure. It is not implied that more than one of these conditions can be applied simultaneously.
The pins are referenced towards the ground pin, which correspond to the 0V level.

Parameter	Description	Min	Typ	Max	Unit	Comments
VCC_abs	Absolute maximum ratings of VCC	-0.3		6.5	V	
VIF_abs	HV IO interface	-0.3		6.5	V	
VdGND	GND potential difference between System1 and System2	-16		16	V	Time limit < 24hours
Tj	Junction temperature	-40		175	degC	TAD41401-BAXX (for Automotive use)
		-20		150	degC	TAD4140-BIXX (for Industry use)
Ts	Storage temperature	-40		150	degC	TAD4140-BAXX (for Automotive use)
		-40		150	degC	TAD4140-BIXX (for Industry use)
B_max	Flux density (Absolute max.)	-	-	200	mT	Max. 5min @25C

Table 2: Absolute maximum ratings

4.2 Operating range

This product supports continuous operating under the following conditions:

Parameter	Description	Min	Typ	Max	Unit	Comments
VCC	5V mode Normal range	4.5	5	5.5	V	
	3.3V mode Normal range	3.1	3.3	3.6	V	
	Over voltage range	5.5		6.1	V	
	Under voltage range	2.7		3.1	V	3.3V mode
	POR	1.4		2.65	V	
	VCC ramp up time	0.01		1	ms	Ramp up time from VCC "POR_rise" to "Normal range"

Icc_dc	DC current consumption		7	11	mA	
Int_clk_freq	Internal clock frequency	14.7	16	17.3	MHz	
PO_time	Power-on time			3	ms	
Ta	Ambient temperature	-40		150	degC	TAD4140-BAXX (for Automotive use)
		-20		125	degC	TAD4140-BIXX (for Industry use)
Ang_range	Sensing range	0		360	Degrees	
B_Normal (1)	Magnetic field strength range	20		80	mT	
B_Ext(1)	Extended magnetic field strength range	80		120	mT	

(1) Assuming 0mT of vertical magnetic field.

Table 3: Operating range

4.3 Voltage range diagram

Figure 7 shows in more detail the different VCC supply ranges and corresponding ASIC behavior.

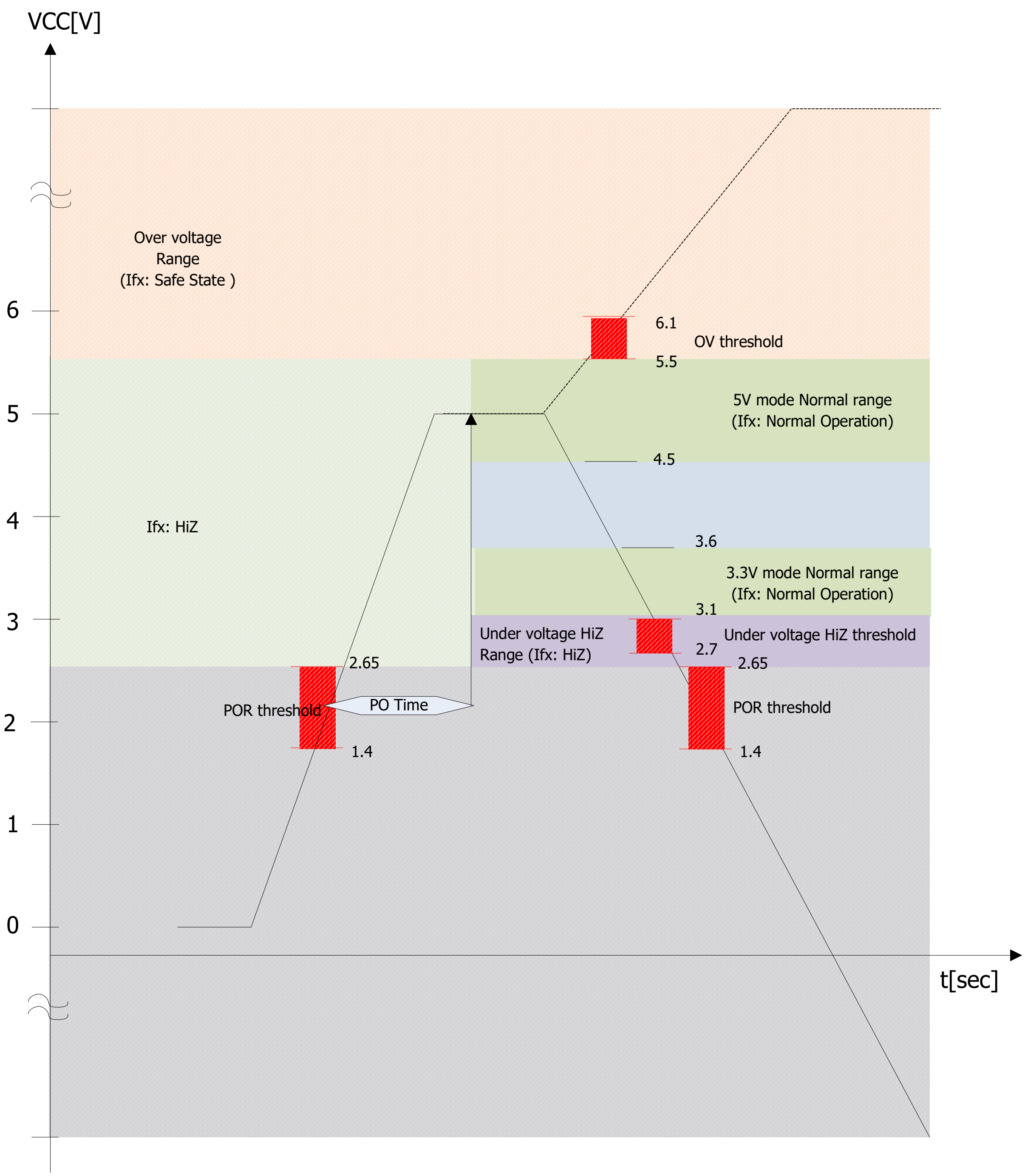


Figure 7: VCC supply range and behavior

4.4 Power on time sequence

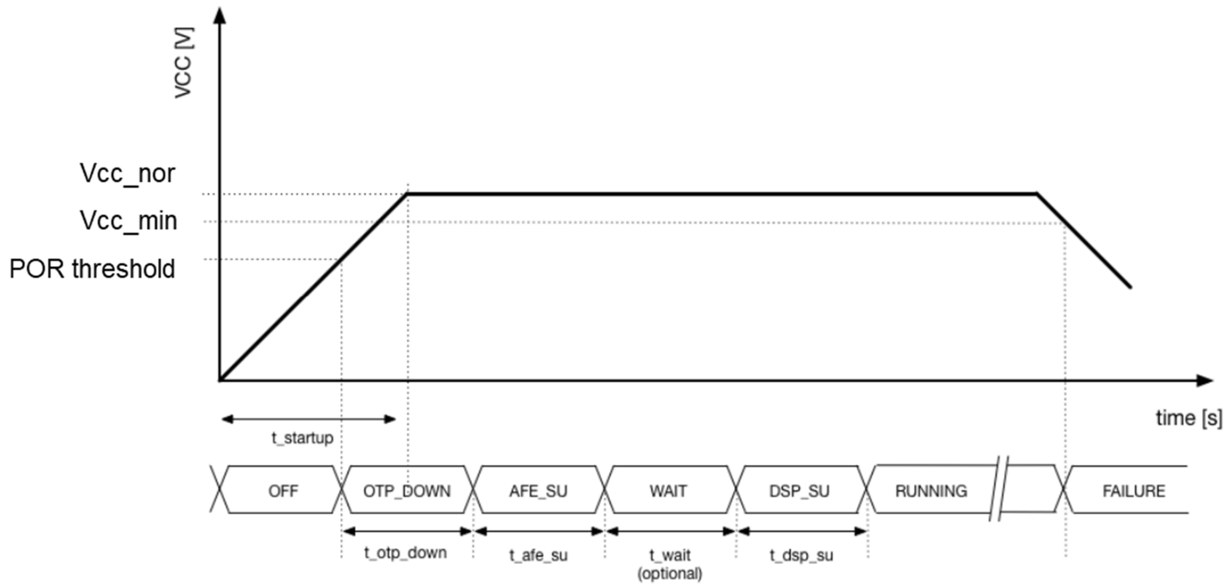


Figure 8: Normal operation with under voltage diagnostic

The timing in above figure is explained in the next table.

Timing	Min.	Typ.	Max.	Comment
t_startup	0.01ms	-	1ms	Startup slope of the supply
t_otp_down		-	300us	OTP download time.
t_afe_su		375us	0.05	Time for Analog blocks to power on.
t_wait	0ms	10ms		Wait state, can be disabled with an OTP setting.
t_dsp_su		625us		Time for DSP to settle.

Table 4: Angle accuracy specifications

4.5 Angle accuracy

Table 5 shows the angle detection performance of the sensor for each different condition. A calibration function of this sensor reduces the angular error due to misalignments, temperature drifts and life time drifts.

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..175] C.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
Ang_full*	with dynamic compensation (See 7.2.1)		-	±0.3	deg	Ta -20degC to 125degC (TAD4140-BIXX), 20mT-80mT
Ang_full*	with dynamic compensation (See 7.2.1)		-	±0.35	deg	Ta -40degC to 150degC (TAD4140-BAXX), 20mT-80mT
Ang_full_ext*	with dynamic compensation (extended range)		-	±0.7	deg	Ta -40degC to 150degC 80mT-120mT
Ang_noise	Angle noise		0.05		deg	Design value, no test
*Ang_full deterioration over lifetime is not included. Over lifetime deterioration is less than 0.1deg.						
** Can satisfy this specification after rotation of magnet, more than 13 rotations at > 60rpm.						
These angle errors assume that auto-calibration is being carried out. This product is optimized to work for rotation speeds up to 15k rpm. For higher rotational speeds, degradation of angular accuracy would occur. The maximum rotation speed is 50k rpm.						

Table 5: Angle accuracy specifications

Definition of Angle Error

Angle Error is a represented parameter to express non-linearity of sensor output. Therefore, only periodical components should be picked up from measurement data, and components which come from random noise should be eliminated. TDK performs following evaluation.
Measurement DataN: The prepared measurement data is the sensor's output error, which is evaluated by comparing to the reference absolute mechanical angle.

$$\mathrm{FFTData}_N = \mathrm{fft}(\mathrm{MeasurementData}_N)$$

$$\mathrm{AngleErrorCurve} = \mathrm{ifft}(\mathrm{FFTData}_{0to10})$$

$$\mathrm{AngleError} = \frac{\mathrm{PeakToPeak}(\mathrm{AngleErrorCurve})}{2}$$

unit: [±deg.]
fft means (fast) Fourier transfer. ifft means inversed (fast) Fourier transfer.

Definition of Angle Noise

Angle Noise is a represented parameter to express the width of sensor output. Except Angle Error components, all other components belong to Angle Noise.

$$\text{AngleNoiseCurve} = \text{ifft}(\text{FFTData}_{11\text{to}N})$$

$$\text{AngleNoise} = \frac{\text{PeakToPeak}(\text{AngleNoiseCurve})}{2}$$

unit: [±deg.]

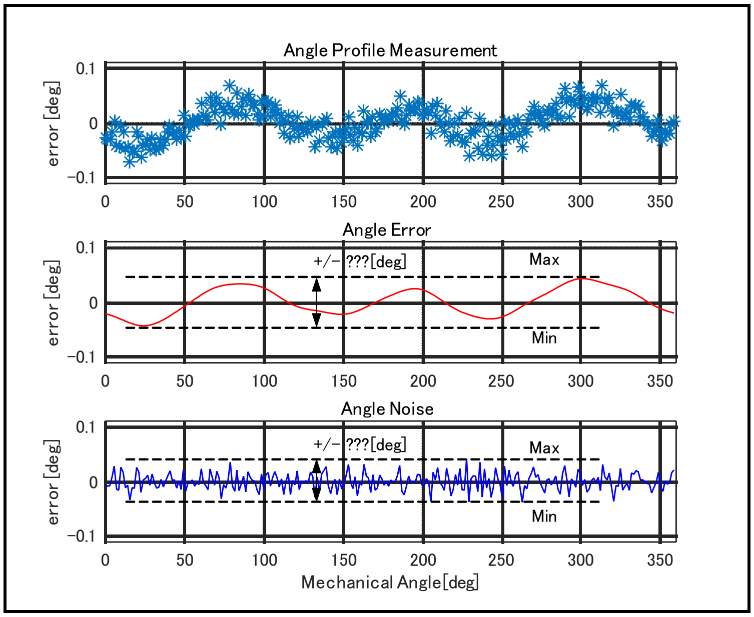


Figure 9: Evaluation of Angle Error and Angle Noise

4.6 Dynamic behavior

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..175] C.

Parameter	Description	Min	Typ	Max	Unit	Comments
Angle_acl	Maximum angle acceleration maintain angle accuracy			26.7	Δkrpm/s	@8000 rpm increase in 300 ms
Angle_usamp	Up-sampled angle data rate		16		MSample/sec	
Angle_delay	Angle delay time with prediction			5	us	
Angle_delay_wo	Angle delay time without prediction			225	us	

Table 6: Angle processing specifications

4.7 Delay compensation

TAD4140 has prediction feature that can reduce the speed dependent angle error. In applications under high-speed rotation, the time difference between Data sampling and sensor out update is not negligible. Prediction uses the latest angle data and past angle data to estimate the current angle position. Figure 10 shows the relationship of delay and prediction. In addition, the idea of interpolation that reduces the effect from update time is described in the figure. This feature fills up interspace of predicted angle data by linear approximation with system clock speed.
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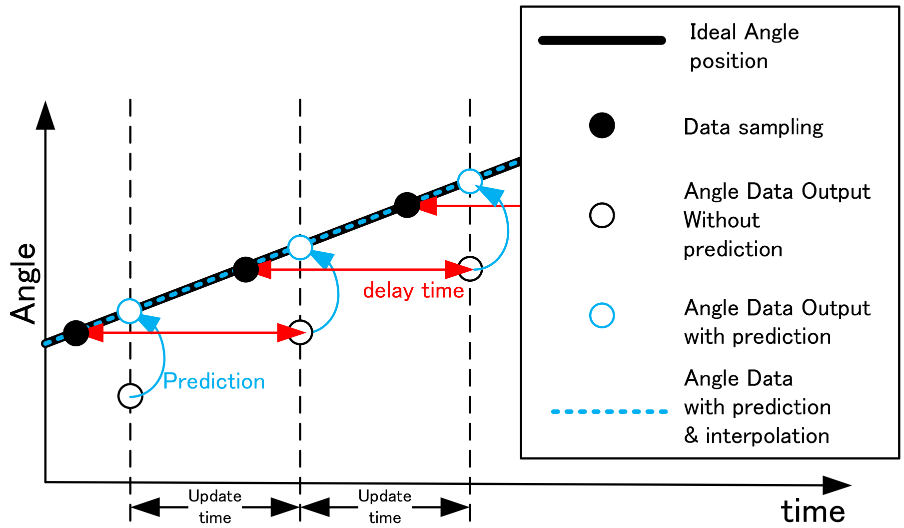


Figure 10: Delay compensation

4.8 Driver strength

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..175] C.

Parameter	Description	Min	Typ	Max	output impedance
Driver strength	Programmable driver strength setting for IFx (Drive capability at 0.5V)		2.6mA		200ohm
			3.9mA		130ohm
			6.5mA		77ohm
			7.8mA		65ohm

Table 7: Driver strength specifications

4.9 Interface Input/output voltage

Unless mentioned otherwise, the conditions are given as VCC = [3.1..3.6, 4.5..5.5] V, Tj = [-40..175] C.

Parameter	Description	Min	Typ	Max	Unit	Comments
voh	High output level, relative to VCC	-0.5			V	With load current in Table7
vol	Low output level, relative to ground			0.5	V	With load current in Table7
vih	High input level, relative to VCC	-0.9			V	
vil	Low input level, relative to ground			0.9	V	

Table 8: Angle processing specifications

4.10 External components

Table 9 shows the external components.

Parameter	Description	Min	Typ	Max	Unit	Comments
C_VCC	VCC/GND , 5V/3V mode	1			uF	
C_IFx	IFx/GND , 5V/3V mode			25	pF	Max load
Short	VDDINT/VCC, 3Vmode					

Table 9: External components

4.11 Application diagram

The minimal circuit diagram is shown in Figure 11. Different configurations are needed when the ASIC is supplied with 5V and 3.3V power supply.
The 3.3V operation requires a short between VCC and VDDINT pins. VDDINT should be left floating for the 5V operation.

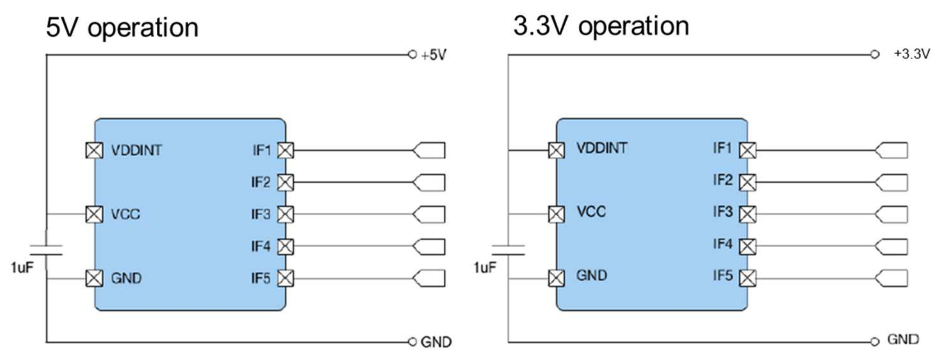


Figure 11. Minimal circuit diagram

*Figure 11~13 are describing one of the 2 chips.

Additional EM robustness can be achieved by placing external components on the interface lines. The total capacitor on each line (Cext) should be minimally 5pF for robustness, and maximally 20pF for speed requirements. This capacitance includes ECU input capacitor, external components and parasitic capacitance.

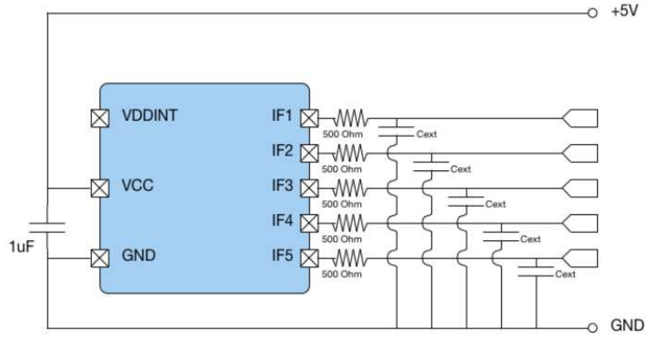


Figure 12. EM compliant diagram

A speed penalty must be taken into account with the components in Figure 13. The maximal frequency at each interface pin is now limited to 300 kHz. The maximal rotation speed is listed in the table below in function of the resolution of the rotary encoder interface:

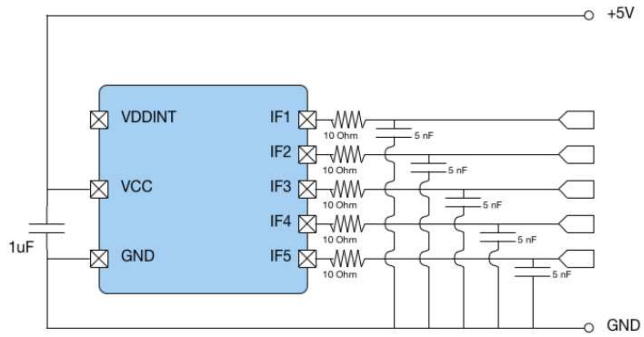


Figure 13. EM compliant diagram

Rotation speed	Max Rotary encoder resolution (X1-decoding)	Max Hall emulation pole pair	Max SPI frequency
< 4.4 krpm	12 bit	16	300 kHz
< 17.6 krpm	10 bit	16	300 kHz

Table 10. Maximal rotation speed

5 Interfaces

5.1 Hall Switch Mode (UVW)

5.1.1 Specifications

Unless mentioned otherwise, the conditions are given as VCC = [4.5 .. 5.5] V, Tj = [-40 .. 175] C.

Parameter		Description	Min	Typ	Max	Unit	Comments
UVW	**Hall_PPN**	Hall Pole Pair number	1		16	#	
	Hall_ang_acc	Electrical accuracy		0.2* PPN	0.7* PPN	deg	1-16PPNs NOTE
	Hall_hys	Hall emulation hysteresis	0		0.7	deg	See 5.1.3

Table 11: Hall Switch Emulation specifications

5.1.2 Interface description

The overview of the Hall Switch Emulation is shown in Figure 14. The signals HS_U, HS_V and HS_W are connected to pins IF1, IF2 and IF3 respectively.
During Hall Switch Interface usage, the signal states of '000' and '111' do not exist. Therefore these states are used for diagnostic purposes. The number of Pole Pairs (PPN) is a programmable number between 1 and 16.

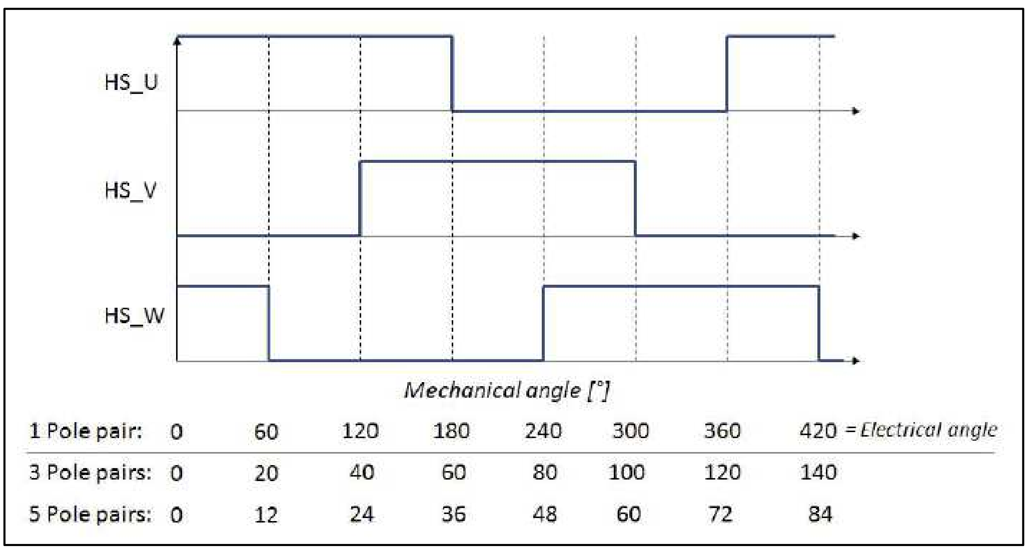


Figure 14: Hall Switch Emulation

5.1.3 Hysteresis

The Hall Switch Emulation interface implements a programmable mechanical hysteresis, shown in Table 1212 and depicted in Figure 15. Figure 16 shows the location where the mechanical hysteresis is added in the signal processing.

Mechanical hysteresis (°)
0 (no hysteresis)
0.087
0.175
0.35
0.7

Table 12: Hall Emulation hysteresis

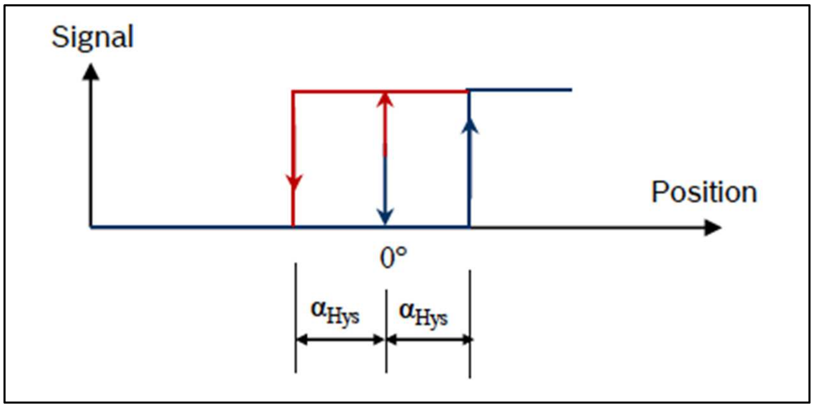


Figure 15: Definition of angle switching hysteresis

Figure 16 shows the implementation of the hysteresis. The Electrical hysteresis equals the programmed mechanical hysteresis multiplied by the programmed PPN.

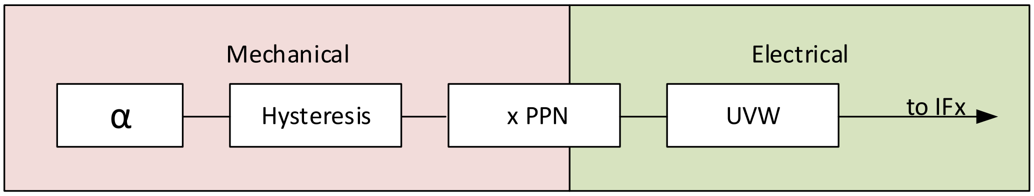


Figure 16: Mechanical hysteresis added prior to Pole Pair Number (PPN) emulation module

5.2 Encoder Mode (ABZ)

5.2.1 Specifications

Unless mentioned otherwise, the conditions are given as VCC = [4.5 .. 5.5] V, Tj = [-40 .. 175] C.

Parameter		Description	Min	Typ	Max	Unit	Comments
ENC	**ENC_resolution**	Encoder resolution	6		12	bit	ENC_resolution for each product name is listed in Table 22.
	ENC_frequency	Encoder frequency	2.79	3.41	3.7	MHz	
	ENC_phase_AB	Phase shift between A and B		90		deg	In AB mode
	ENC_z_duration	Z-pulse duration Programmable			4	us	Independent of motor rotation speed
	ENC_hys	Encoder Hysteresis Programmable	0		0.7	deg	

Table 13: Encoder mode specifications

5.2.2 AB-mode

When operating in AB-mode, pulse A and B are always 90° shifted, allowing to have 4 unique AB combinations ('00','01','10','11') in a single Encoder period. If B leads A (e.g. B is high at rising edge of A), this corresponds to CW. If A leads B, (e.g. B is low at rising edge of A) this corresponds to CCW.

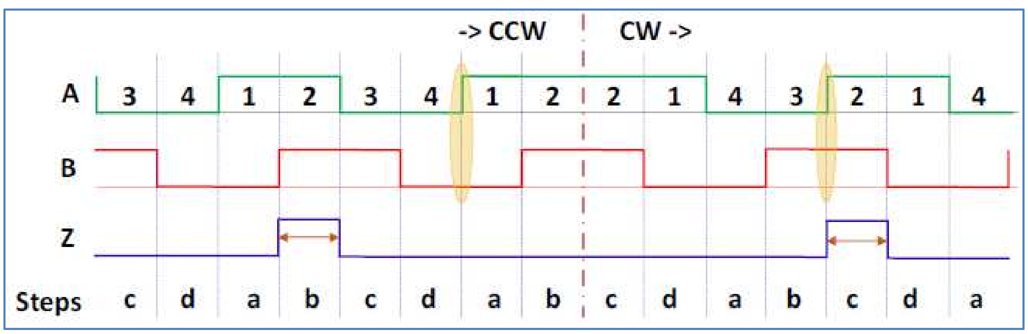


Figure 17: Encoder interface definition

5.2.3 Encoder AB mode configuration

The ENC interface can be decoded with three different decoding schemes. The definition of the accuracy depends on this decoding scheme:

- X1-decoding: TheCCW-counter increments @ rising-edge of 'A' signal; CW-counter decrement @ falling-edge of 'A'.
- X2-decoding: The CCW-counter increments @ every edge of the 'A' signal.
- X4-decoding: The CCW-counter increments @ every edge of 'A' and 'B' signal.

The definition used in this document always refers to X1-decoding, unless stated otherwise These three decoding schemes are displayed in figure 18.

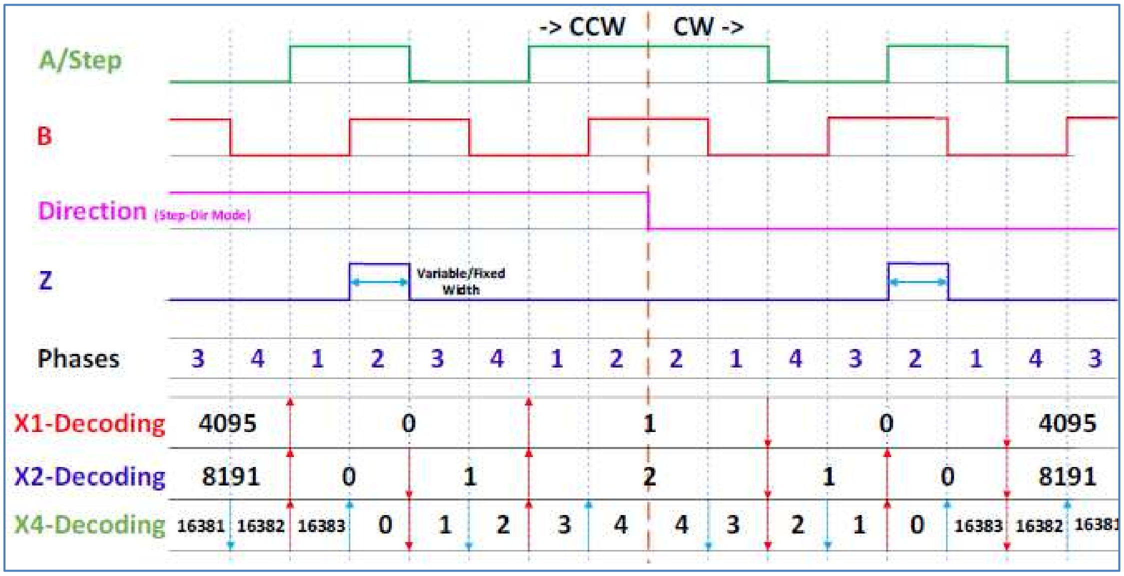


Figure 18: Encoder interface accuracy definition

5.2.4 Step direction mode

The B channel represents the rotation direction if the 'step direction mode' is selected in NVM. The B channel will output a '1' when turning CCW and '0' when turning CW instead of the 90 degree phase shifted A signal.

5.2.5 Z-pulse behavior

The Z-pulse will have a fixed. The edges of the Z pulse will be aligned according to the rotation direction:

- CCW: Rising edge of Z is aligned with rising edge of B signal
- CW: Rising edge of Z is aligned with rising edge of A signal
-

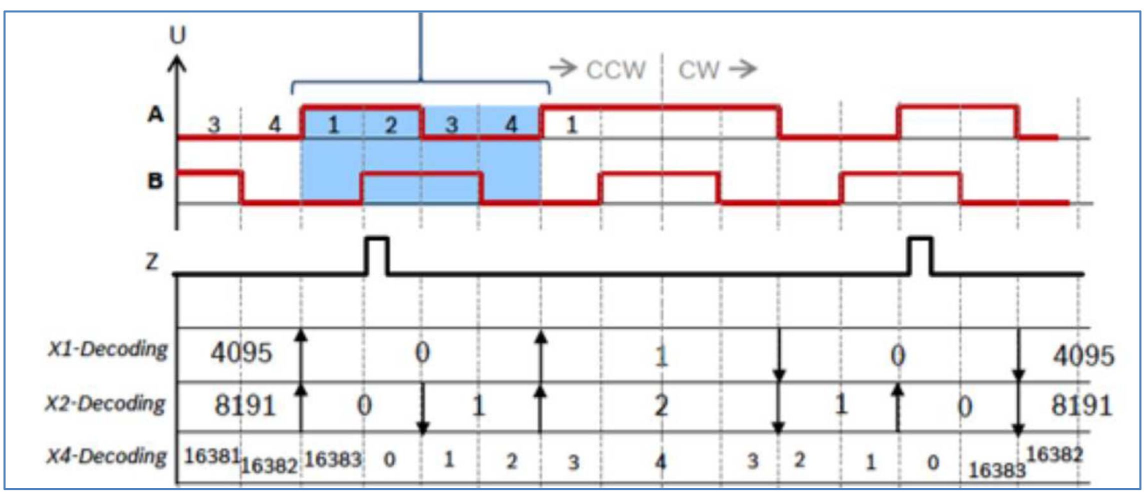


Figure 19: Behavior of Z-pulse

5.2.6 Z-pulse duration

The duration of the Z pulse can be selected through a setting in NVM in multiple steps of the system clock. A 4-bit word represents the duration, typically ranging from 250 nsec up to 4 usec. The clock spread should be taken into account

5.2.7 Hysteresis

The Encoder interface implements a programmable hysteresis, shown in Table 14. The hysteresis will act as an 'asymmetrical' hysteresis, meaning that it will blank pulses when the angle vibrates (e.g. due to noise) in the opposite direction as the general observed rotation direction.

Hysteresis (°)
0 (no hysteresis)
0.087
0.175
0.35
0.7

Table 14: Encoder hysteresis

5.2.7.1 **Fixed offset hysteresis**

Upon direction change, the hysteresis module shifts the input angle with the programmed hysteresis value. This means there is a fixed angle offset in one direction (CW or CCW) when using this type of hysteresis. The user can select through OTP option in which direction CW/CCW this fixed offset is added. Fig.20 shows the input/output angle behavior of the hysteresis module for 4 LSB setting (e.g. 0.087°).

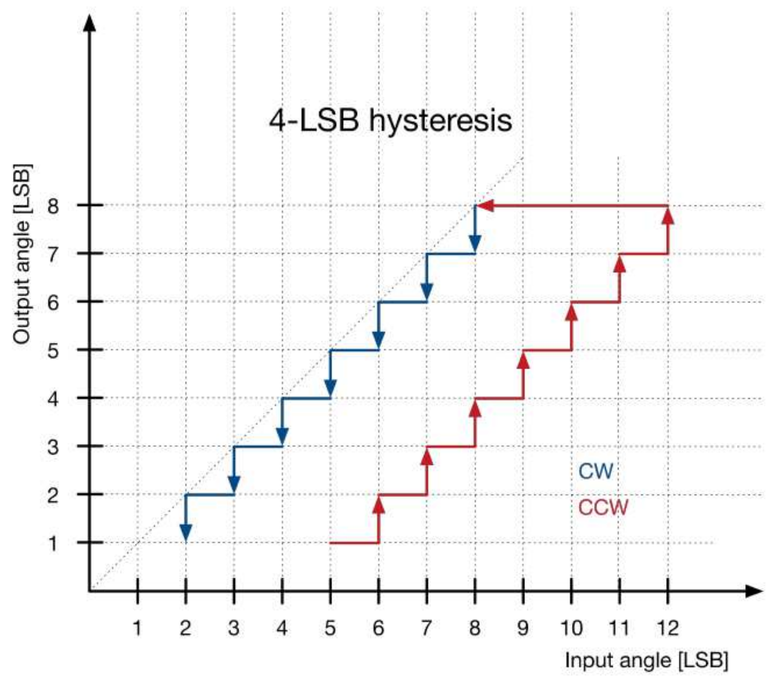


Figure 20: Encoder hysteresis

5.2.7.2 Fixed offset hysteresis

The gated hysteresis operation behaves as a pass or hold gate for the input angle. The input angle will pass right through the hysteresis module when the angle keeps progressing in the same direction. The hysteresis module will latch it's output value whenever the direction of the angle is changed. The output remains latched until the input angle crosses the hysteresis level in opposite direction. The hysteresis output angle will immediately track the input angle again after this level is crossed. This pass/hold mechanism is valid for CW to CCW transitions or CCW to CW transitions.

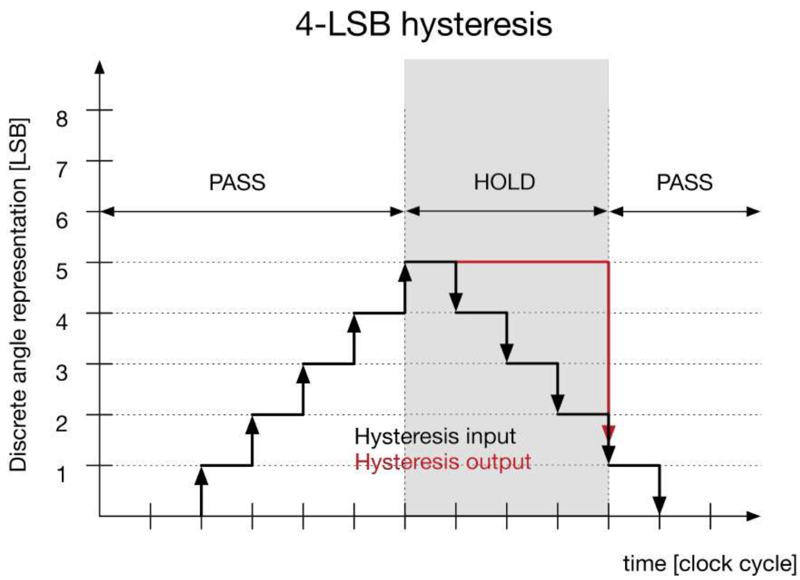


Figure 21: Encoder hysteresis

5.2.8 Missed pulses

The ENC module behavior depends on the selected type of hysteresis.
– In case the gated hysteresis has been selected, the ENC module will give output missed pulses after crossing the hysteresis level when changing direction.
– In case the fixed offset hysteresis is selected, the ENC module will not give output missed pulses.
As such, by selecting the desired hysteresis behavior, sending missed pulses can disabled in the ENC module.
Figure 22 and Figure 23 show the ENC behavior for the two different types of hysteresis

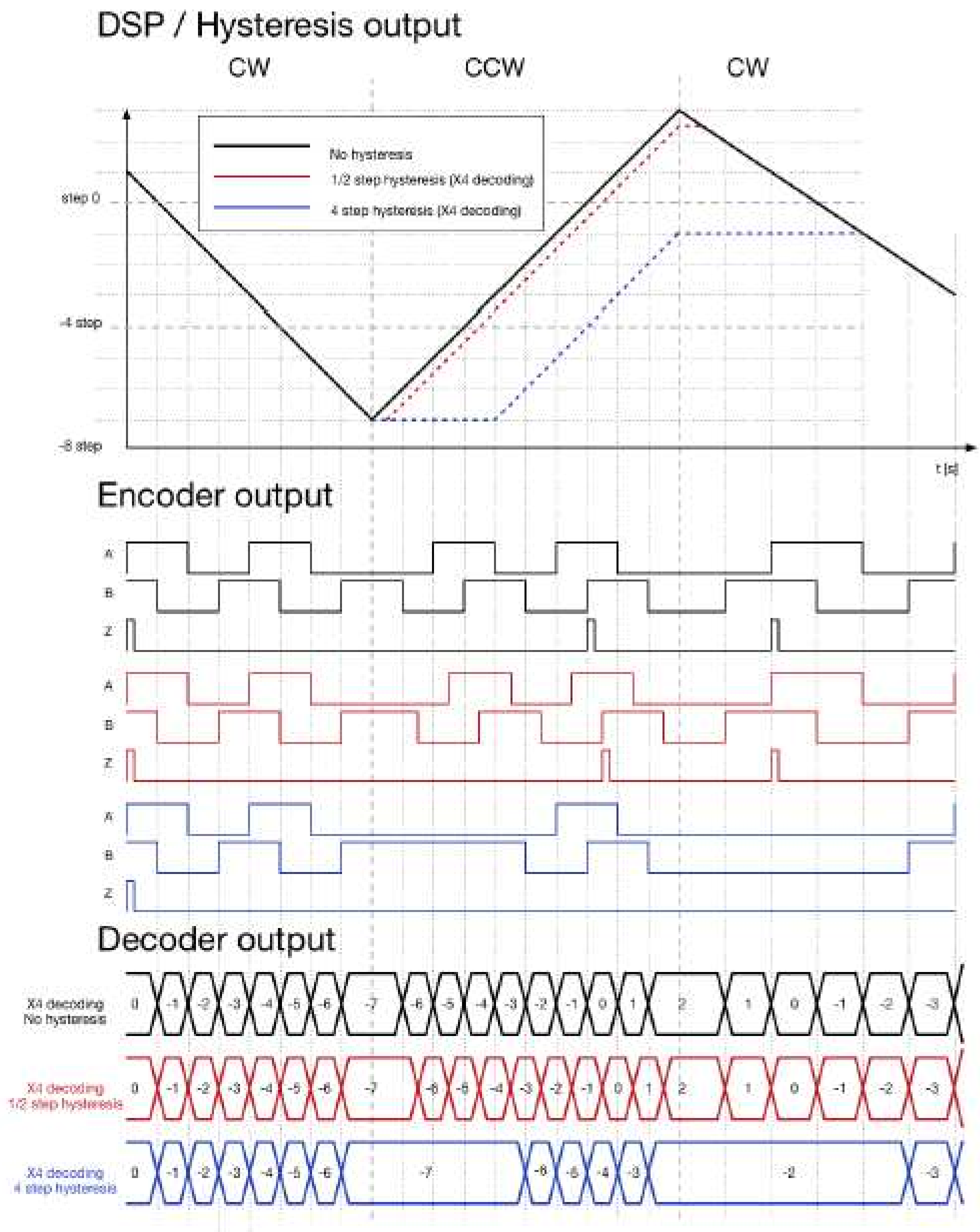


Figure 22: Encoder behavior with "fixed offset hysteresis"

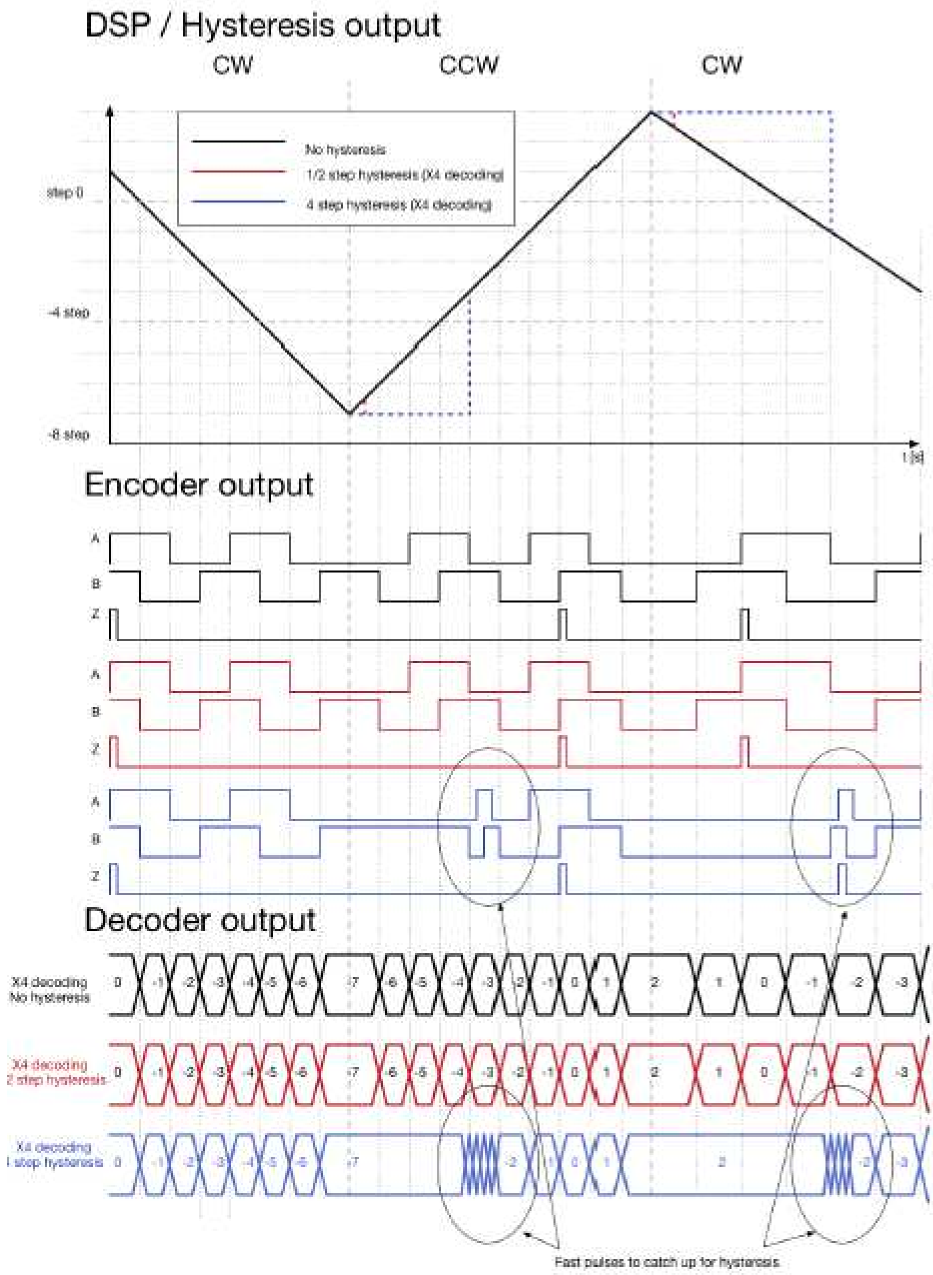


Figure 23: Encoder hysteresis with "gated hysteresis"

5.2.9 Start-up pulses

The output of the ENC module has two different operation modes when going to Running Mode:
1. The ENC interface starts giving pulses from 0° up to the initial angle. The frequency of these pulses is at maximal frequency, defined by the driver configuration.
– It is assumed that there is no motor rotation at startup when this mode is selected.
– Since the ENC interface will start from 0° in this mode, a Z-pulse is given directly at the beginning of the A, B pulse train.
– The start up pulses are given in CCW or CW direction, depending on the initial angle position. For an

initial angle between 0° and 270°, the start-up pulses will be given in CCW direction; for an initial angle between 270° and 360°, the start up pulses are given in CW direction
2. The ENC interface gives relative information starting from the initial angle. Absolute angular information can only be retrieved after a first zero angle crossing (Z-pulse) occurs. The behavior of the ENC module at start-up can be selected through OTP settings.

5.3 Pulse Width Modulation (PWM)

5.3.1 Specification

Unless mentioned otherwise, the conditions are given as VCC = [4.5 .. 5.5] V, Tj = [-40 .. 175] C.

Parameter		Description	Min	Typ	Max	Unit	Comments
PWM	**PWM_frequency**		1.84	2	2.16	kHz	+/- 8%
	PWM_resolution		12			bit	Contained in duty cycle from 5% to 95%
	PWM_pulse_acc	Tolerance of duty cycle for PWM	-110		110	ns	• Accuracy is defined at 50% crossing (VCC/2) • 2kHz, 12 bit

Table 15: PWM specifications

5.3.2 Interface description

Figure 24 shows the PWM definition. The PWM interface operates at 2kHz (+/-8%) with 12 bit resolution (from 5% to 95% duty cycle). Granularity of the duty cycle is 110 nsec.
Duty cycles below 4% and above 96% are treated as diagnostic modes (with 1% guard band). The angle value from the DSP will be sampled at the start of the PWMframe, therefore – by design- the evaluted angle by PWM has a delay equal to 1 PWM period.

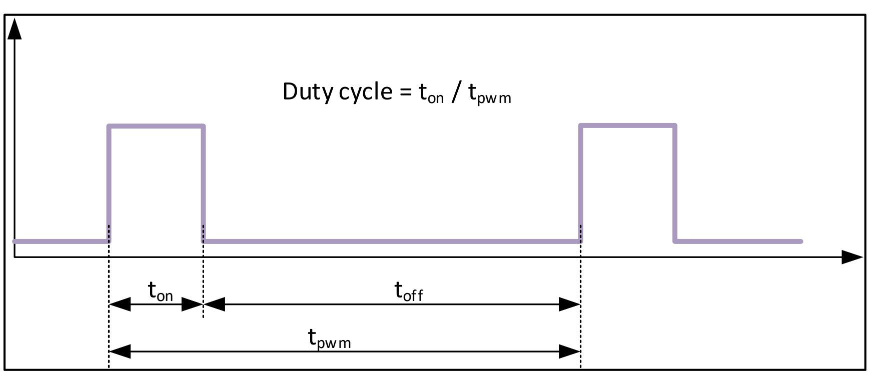


Figure 24: PWM Definition

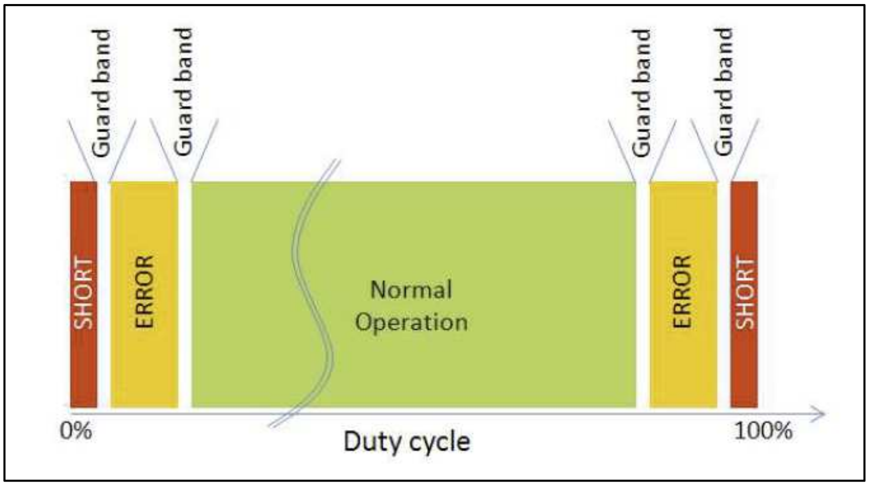


Figure 25: Duty Cycle Bands

5.4 Programming interface (SPI)

5.4.1 Specification

Following figure is showing timing definition of SPI interface.

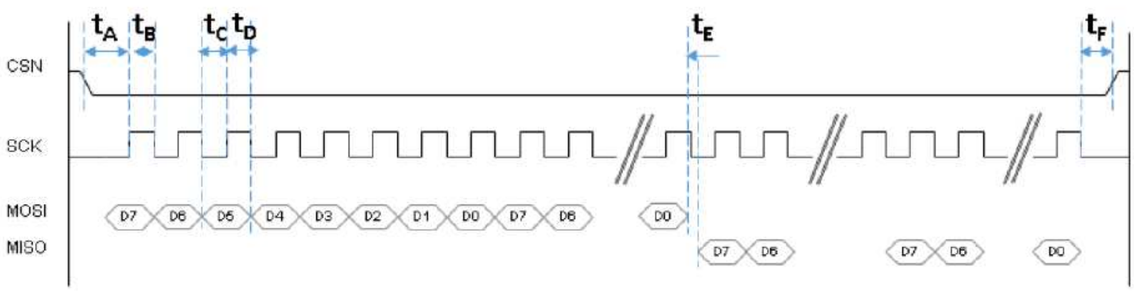


Figure 26 : SPI timing definition

Unless mentioned otherwise, the conditions are given as VCC = [4.5 .. 5.5] V, Tj = [-40 .. 175] C.

Parameter	Description	Min	Typ	Max	Unit	Comments
SPI_speed	SCLK speed			10	Mbit /sec	
ang_rate	Angular data output rate			312.5	kS/s	In streaming mode SPI, 10MHz SCLK
rw_delay	Idle time between two SPI commands	1			us	Due to clock domain transition
sck_dc	SCLK duty cycle	40		60	%	
t_b	SCLK pulse width	40			ns	
t_a	CSN low to SCLK	20			ns	
t_c	MOSI setup time	25			ns	
t_d	MOSI hold time	5			ns	
t_e	SCLK fall to MISO			25	ns	
t_f	SCLK to CSN high	25			ns	

Table 16: SPI specification

5.4.2 SPI communication

The chip will use a 4-wire SPI protocol using:

- pins IF1, IF2, IF3, IF4 for SPI

5.4.3 MISO idle state

The MISO output will be high impedance when not driven.

5.4.4 Normal SPI mode

5.4.4.1 Register access

All registers in the main register space can be written and read out in ‘normal SPI mode’.

5.4.4.2 SPI definition

The chip implements an SPI MODE0 interface with CPOL=0 and CPHA=0.
When the SPI interface is idle, SCLK is low (CPOL=0). Data is propagated on the clock's falling.

5.4.4.3 Write frame

The format of a SPI write frame is displayed in the figure below. This frame consists of the following elements:

- 8-bit command
- 8-bit address
- 16-bit data

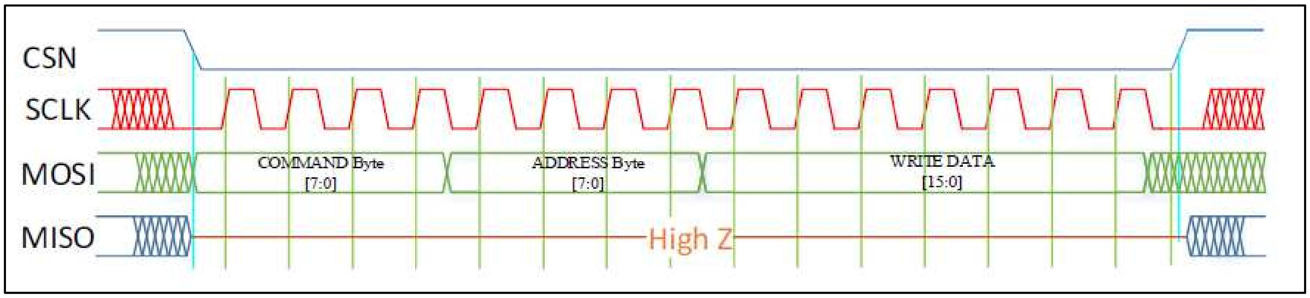


Figure 27: SPI write transfer overview

5.4.4.4 Read frame

If a ‘READ” command was received. After the address byte, before that a valid read data is send on the MISO line, a number of “sentinel bytes” will be transmitted. The sentinel bytes sequence is formatted as follows:

- n*(0x7E hex) + (0x81 hex)

The total frame consists of the following elements

- 8-bit command
- 8-bit address
- n times 8-bit sentinel
- 16-bit data

The format of a read frame is displayed in the figure below

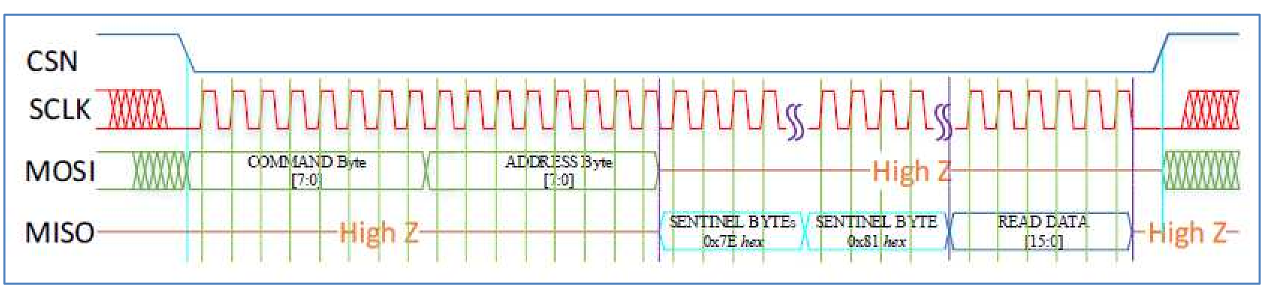


Figure 28: SPI read transfer overview

5.4.5 Streaming SPI mode

5.4.5.1 Register access

Angular data (output of DSP) can be read out in streaming SPI mode.

5.4.5.2 Streaming mode format

Streaming out angular data can be achieved through a dedicated SPI command. The streaming command enables the streaming out of angular data on the MISO pin as long as SCLK keeps giving pulses and CSN is asserted low. One read frame consists of the following elements:

- 16-bit Angular data
- 8-bit Status information (diagnostic information)
- CRC-8-SAE J1850 (Covers both angular data and status information)

This format is displayed in the figure below:

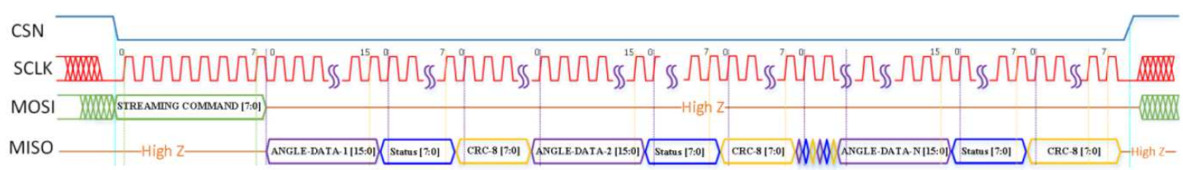


Figure 29: SPI streaming mode read transfer

5.4.5.3 Angular data timing

The time when the angular data is fetched from the system clock domain towards the SPI clock domain can be configured with a setting in the NVM. 1 to 7 clock periods are possible. The default setting is 3 clock cycles.

This is graphically displayed in the next figure. The programmable value is LOAD_DATA_PAR

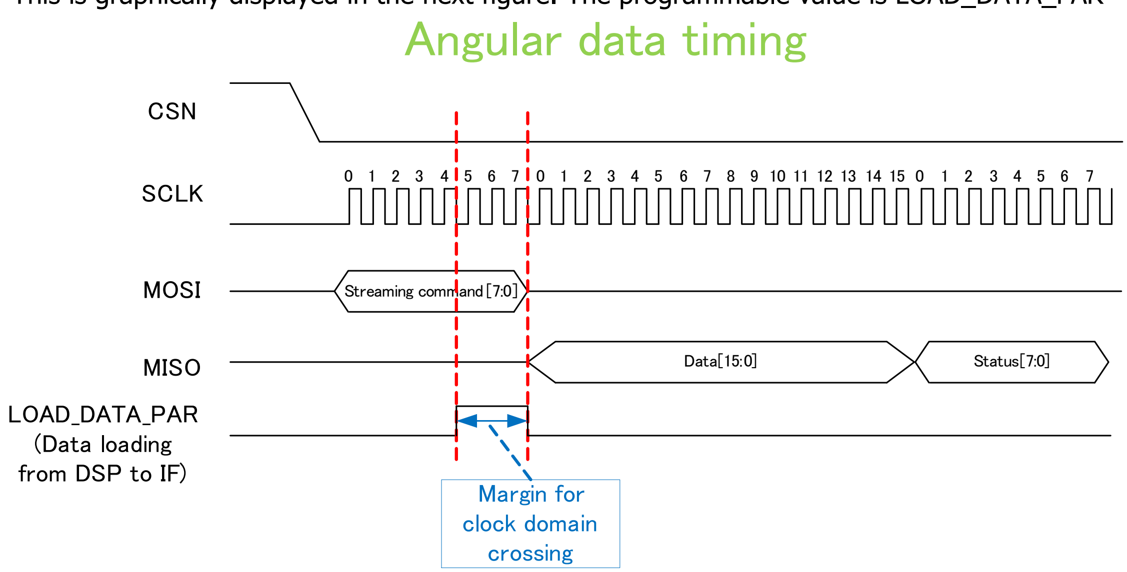


Figure 30: Angular data timing

5.4.5.4 Status byte content

The following diagnostic information is contained in the status byte

Status[7] : Magnet loss
Status[6] : Speed limit
Status[5] : VCC overvoltage
Status[4] : VCC under voltage
Status[3] : Sensor abnormality
Status[2] : CRC failure (OTP + Main regs)
Status[1] : ADC overflow
Status[0] : Parity bit

5.5 Register settings

See "User manual".

6 Functional Safety

6.1 Safety level

The TAD4140 for Automotive (TAD4140-BAXX) is being developed according to ISO26262 standard guidelines with ASIL D level target.

6.2 Safety goal

The generic assumed safety goal is to avoid angular errors of bigger than 5° with a fault detection time tolerance of max 5ms.

6.3 Diagnostic analysis & Safe states definition

Diagnostic analysis is performed during Power-On time and during Running Mode. The implemented diagnostic signatures are show in Table 18. The safe states are described in Table 17 as below

IF	Safe 1: Fault root cause external	Safe 2: Fault root cause internal
PWM	2 to 4%	96 to 98%
UVW	"000"	"111"
ABZ	"001" (Steady '1' on ENC Z line)	"111" (Steady '1' on ENC Z line)
Normal SPI	Diagnostic information can be fetched from the main register space through a read command	
Streaming SPI	Diagnostic information is given in the status byte with every angle update. **	

Table 17: Safe state

6.4 Diagnostics

Followings are implemented diagnostic signatures of this product.

Diagnostic	Function	Safe State
Magnet loss	Magnetic field strength error	Safe 1
Speed limit	Over rotational speed of motor	Safe 1
OV VCC	VCC is too high	Safe 1
UV VCC	VCC is too low	Drivers in HiZ
Sensor abnormal	Internal wire break of sensor	Safe 2
Register CRC	Perform CRC of register file	Safe 2
AFE check	SIN/COS channel overflow of AFE	Safe 2
OTP CRC	CRC of OTP using polynomial 0x83	Safe 2

Table 18: Implemented diagnostic functions

6.4.1 Details of Diagnostic function

See the "User manual" for the details of the calibration mode.

7 EOL Programming and Calibration

7.1 Calibration mode

For EOL and user calibration purposes, SPI interface is implemented through IFx pins.
The programming voltage of VCC during calibration mode is that of operating range.

With the following procedure, enter Calibration Mode.

- Transition to SPI mode during Power-On Mode. (See Operation modes 4)
- Start "Calibration Mode"
- Perform Calibration procedure.
  (see "User manual" for detail procedure and register access for Calibration process done)

7.2 Compensation overview

7.2.1 Dynamic compensation

Dynamic compensation reduces angle error caused by Gain error, Offset error, Orthogonal error, Harmonic distortion error, and their temperature drift (only at the full-rotation use case). At the full-rotation use case (>60rpm), the optimization of Dynamic compensation works all the time, even after shipment.

7.2.2 Static compensation

Static compensation reduces angle error caused by assembly error.
The parameter optimization should be done before the shipment. The parameter update does not happen after shipment. See the "User manual" for details.

7.2.3 Auto-Calibration

User can optimize both Dynamic compensation parameter and Static compensation parameter by executing Auto-Calibration before the shipment. See the "User manual" for details.

7.3 SPI Interface for programming

See the "User manual"

7.4 OTP register map

See the "User manual"

7.5 Package level ESD/Latch-up

Table 1919 shows the package level ESD/Latch-up specifications.

Parameter	Description	Min	Typ	Max	Unit	Comments
ESD_HBM	Electrostatic Discharge Human Body Model			2k	V	AEC Q100-002
Latch-Up	Latch-up			100	mA	AEC Q100-004

Table 19: package level ESD/Latch-up specifications

All pins are designed to withstand

- 2kV pulses according to the MIL-STD-833 method 3015.7 (HBM) standard
- Latch-up: 100mA according to the EIA/JESD 78 standard

8 Application note

8.1 Recommendation of power supply control circuit

For calibration of TAD4140, SPI signature needs to be issued within 10ms time window from Power on. In case that uC and TAD4140 have common power supply on PCB, TAD4140 power on time should be observable from uC. The easiest way is to haveTAD4140 power supply controllable by uC. Figure 31 shows a recommendation of power supply control circuit to consist power switching by signal from uC. Table 20 shows On/off relation between uC port and FET device.

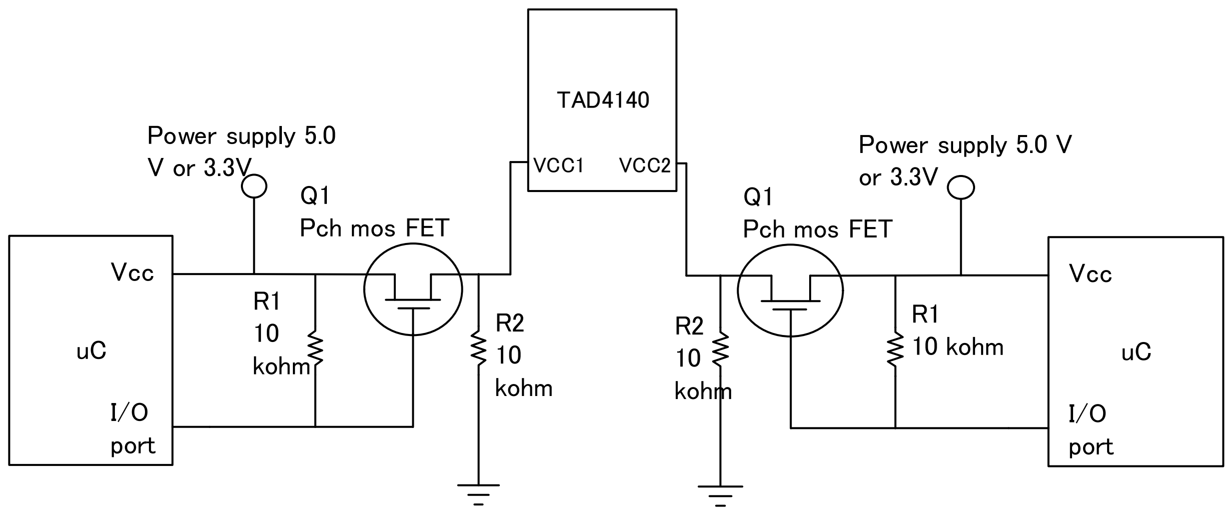


Figure 31: Example of power supply control circuit

uC i/O port	Pch mos FET
'Low'	'on'
'High'	'off'

Table 20: On/off relation between uC port and FET device

If Vcc is Open with high state of CS and MOSI, Vcc voltage at ASIC PIN does not down (Stopped at around POR voltage). If VCC is connected again, ASIC ends up in state as with slow VCC ramp-up. Then, sensor will detect under voltage diagnostic alarm and go to safe mode till re-Power on. CSN/MOSI I/O must low state before Vcc Enable/Disable.

8.2 State of CSN/MOSI

If Vcc is Open with high state of CS and MOSI, Vcc voltage at ASIC PIN does not down (Stopped at around POR voltage). If VCC is connected again, ASIC ends up in state as with slow VCC ramp-up. Then, sensor will detect under voltage diagnostic alarm and go to safe mode till re-Power on. CSN/MOSI I/O must low state before Vcc Enable/Disable.

8.3 Power cycle

In case that operation under -30degC is assumed, long power on/off cycle time is needed. VCC Power-ON requires more than 500ms of wait time from the VCC Power-OFF.

9 Package Information

9.1 Package Mechanical Drawing

Figure 32 shows the package drawing of TSSOP-16

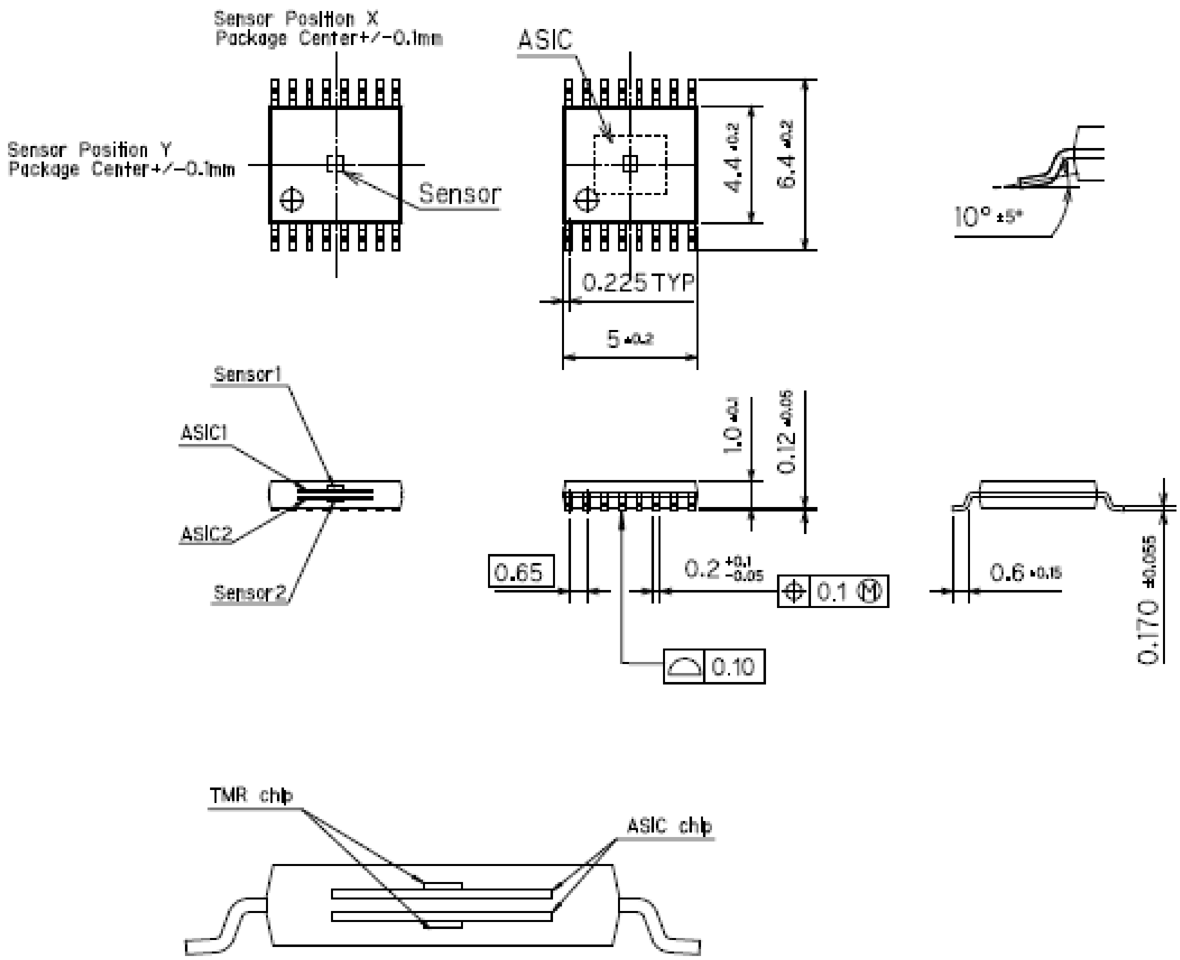
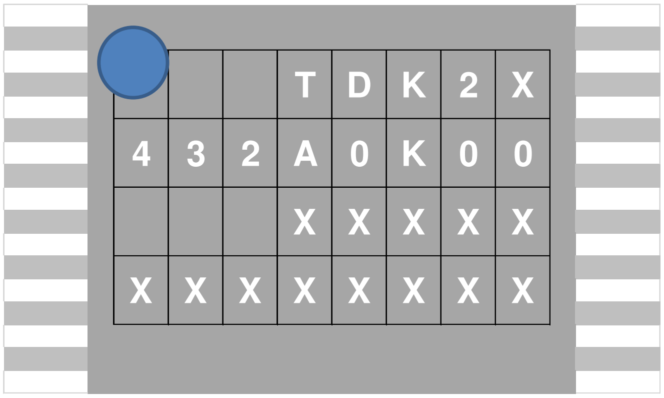


Figure 32 : Package drawing

9.2 Laser Marking

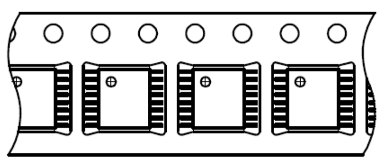


1st row (5digit) : TDK2* → 1pin mark + name of company + base of processing (2 means SAE) + lot
2nd row (8digit) : ********* → product number (above is one example.)
3rd row(5digit) : ***** → Wafer number of sensor
4th row(8digit) : ******** → sensor chip address (6 digit) + OCR (2 digit)
Note : In sample stage, 5th row has the information of ASIC lot.

10 Packing Information

10.1 Taping

E2 Type



10.2 Product storage method

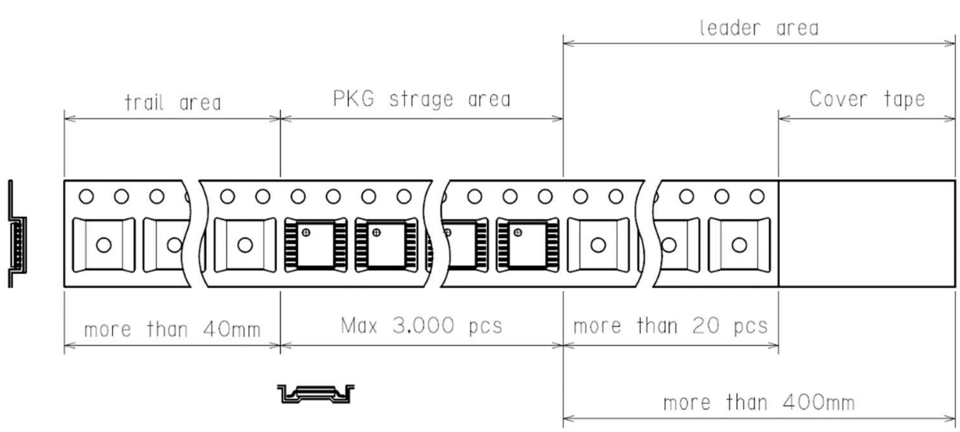


Figure 33: Product storage method

10.3 Carrier tape

Material : Polystyrene + carbon, Surface resistance : 1×10⁷Ω/10cm, Color: black

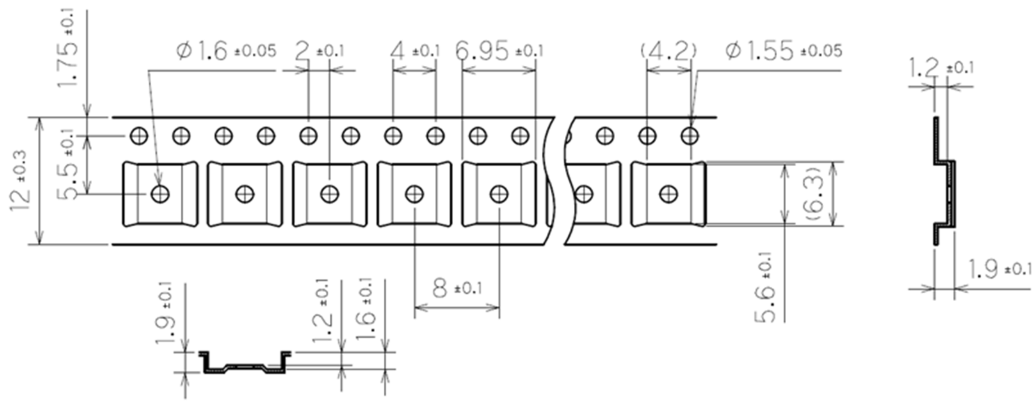


Figure 34: Carrier tape

10.4 Peel strength of cover tape

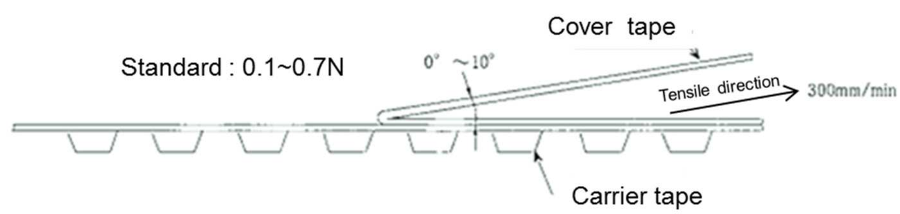


Figure 35: Peel strength

10.5 Reel specifications

Material : Polystyrene, Surface resistance : 1×10⁷Ω/10cm, Color: black

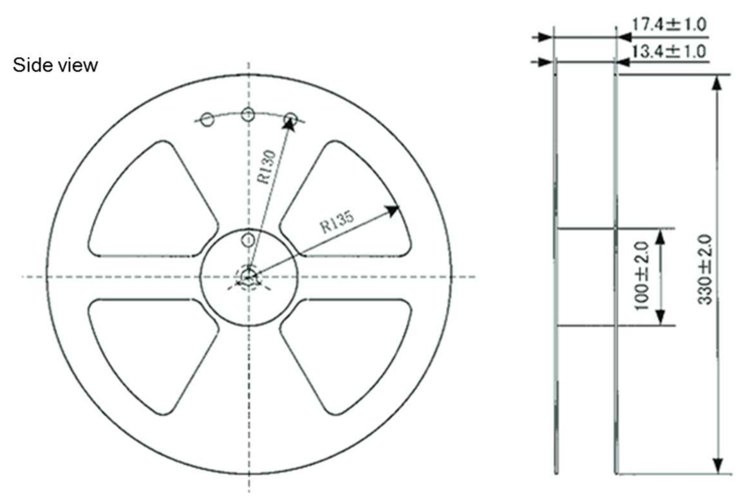


Figure 36: specification of reel

11 Reflow profile (Reference)

Peak temperature should not exceed 260degC.

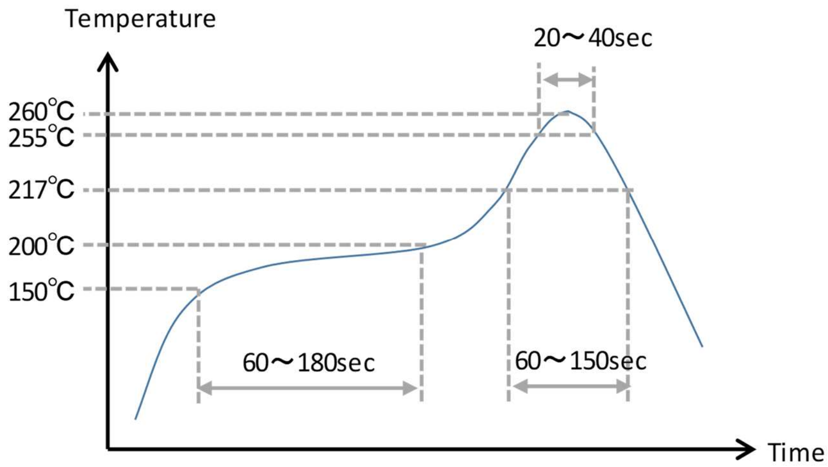


Figure 37: Reflow profile

Item	Contents
Peak temperature	260℃
Peak temperature time	20～40sec, 255～260℃
Reflow time	60～150sec, 217℃ or more
Residual heat condition	60～180sec, 150～200℃
Heating rate	3℃/sec Max, 217～255℃
Cooling rate	6℃/sec Max
Total heating time	8min or less
Number of reflows	3times Max

Table 21: Reflow item and contents

12 Product Order information

TAD4140 family has the following product name by IF.

	IF mode				product name
	Chip1		Chip2		
Automotive use	SPI/PWM		SPI/PWM		TAD4140-BAAA
	UVW/PWM		UVW/PWM		TAD4140-BAFA
	ENC/PWM	ENC resolution 10bit	ENC/PWM	ENC resolution 10bit	TAD4140-BADA
		ENC resolution 12bit		ENC resolution 12bit	TAD4140-BAKA
Industial use	SPI/PWM		SPI/PWM		TAD4140-BIAA
	UVW/PWM		UVW/PWM		TAD4140-BIFA
	ENC/PWM	ENC resolution 10bit	ENC/PWM	ENC resolution 10bit	TAD4140-BIDA
		ENC resolution 12bit		ENC resolution 12bit	TAD4140-BIKA
	ENC/PWM	ENC resolution 12bit	UVW/PWM		TAD4140-BIHA

Table 22: Product name list

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Appendix C : Lexicons

Following list defines a number of terms used throughout the document:

Abbreviation	Explanation
AAF	Anti-Alias Filter
ADC	Analog to Digital Conversion
AFE	Analog Front-End
ASIC	Application Specific Integrated Circuit
BCI	Bulk Current Injection
CORDIC	Coordinate Rotation Digital Computer

CRC	Cyclic redundancy code
DAC	Digital to Analog Conversion
DPI	Direct power injection
EOL	End Of Line
ESD	Electrostatic Discharge
FMEDA	Failure Modes Effects and Diagnostic Analysis
FSM	Finite State Machine
HBM	Human body model
HiZ	High Impedant
NVM	Non Volatile Memory
OTP	One Time Programmable
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
Ta	Ambient temperature
TBD	To be defined
TMR	Tunnel Magneto Resistance Effect
Tj	Junction temperature

Table 23: Lexicon

Appendix D : document Revision History

Revision	Date	Description
1.0	2017.4.28	Initial release of the document as draft
2.0	2017.10.6	6.2 : OTP programming temperature comment
3.0	2018.3.12	Add 6.5 minimum circuit design, etc
3.1	2018.7.13	Revised to ASIL D
3.2	2018.7.27	Corrected Table 3, 10, 14
3.3	2018.11.26	Corrected 3.2 : diagnostics items
3.4	2018.12.18	Added 13. Reflow profile (reference)
3.5	2019.1.9	Added 6.3 Power on time sequence and 6.6 Interface Input/output voltage
3.6	2019.11.07	Added the TMR principle. Operating range is modified. Added Voltage range diagram. Angle accuracy table is modified. Explanation of delay compensation is added. Circuit diagram is modified.

		Hysteresis part is modified. Laser marking is added. Packing information is added. Reflow profile is added. Update the product name list
3.7	2019.12.05	Induce angle (Figure32) is modified. Product name list (table22) is updated.
3.8	2020.1.10	Table 1. Pin description is modified. From VDD to VCC.
3.9	2020.2.26	Table 2. Parameter of VdGND is added.
3.10	2020.4.15	Table 10 is revised (11bit and 9 bit of ENC resolution is removed.)
3.11	2020.6.04	Figure 32 is revised. Correct lead floating.

Appendix E : Document Reference

Document name	Abbrev.
TAD4140_user_manual	User manual