

## FEATURES

**Locks to 1.25 Gbps NRZ serial data input**  
**Patented clock recovery architecture**  
**No reference clock required**  
**Loss-of-lock indicator**  
**I<sup>2</sup>C interface to access optional features**  
**Single-supply operation: 3.3 V**  
**Low power: 390 mW typical**  
**5 mm × 5 mm 32-lead LFCSP, Pb free**

## APPLICATIONS

GbE line card

## GENERAL DESCRIPTION

The ADN2805 provides the receiver functions of quantization and clock and data recovery for 1.25 Gbps. The ADN2805 automatically locks to all data rates without the need for an external reference clock or programming. All SONET jitter requirements are met, including jitter transfer, jitter generation, and jitter tolerance.

All specifications are specified for  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ambient temperature, unless otherwise noted. The ADN2805 is available in a compact 5 mm × 5 mm 32-lead LFCSP.

## FUNCTIONAL BLOCK DIAGRAM

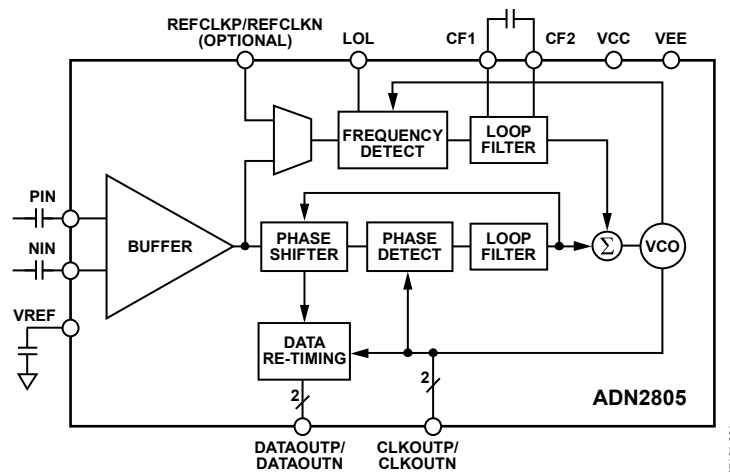


Figure 1.

## Rev. B

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## REVISION HISTORY

### 3/12—Rev. A to Rev. B

|                                  |    |
|----------------------------------|----|
| Updated Outline Dimensions ..... | 16 |
| Changes to Ordering Guide .....  | 16 |

### 5/10—Rev. 0 to Rev. A

|                                                        |    |
|--------------------------------------------------------|----|
| Changes to Figure 5 and Table 6 .....                  | 7  |
| Changes to Figure 14 .....                             | 14 |
| Added Exposed Pad Notation to Outline Dimensions ..... | 16 |

### 1/08—Revision 0: Initial Version

## SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = V_{MIN}$  to  $V_{MAX}$ ,  $V_{EE} = 0$  V,  $C_F = 0.47$   $\mu$ F, SLICEP = SLICEN = VEE, input data pattern: PRBS  $2^{23} - 1$ , unless otherwise noted.

Table 1.

| Parameter                            | Conditions                     | Min | Typ  | Max  | Unit         |
|--------------------------------------|--------------------------------|-----|------|------|--------------|
| QUANTIZER—DC CHARACTERISTICS         |                                |     |      |      |              |
| Input Voltage Range                  | @ PIN or NIN, dc-coupled       | 1.8 |      | 2.8  | V            |
| Peak-to-Peak Differential Input      | PIN – NIN                      | 0.2 |      | 2.0  | V            |
| Input Common-Mode Level              | DC-coupled                     | 2.3 | 2.5  | 2.8  | V            |
| QUANTIZER—AC CHARACTERISTICS         |                                |     |      |      |              |
| Data Rate                            |                                |     |      | 1250 | Mbps         |
| S11                                  | @ 2.5 GHz                      |     | –15  |      | dB           |
| Input Resistance                     | Differential                   |     | 100  |      | $\Omega$     |
| Input Capacitance                    |                                |     | 0.65 |      | pF           |
| LOSS-OF-LOCK (LOL) DETECT            |                                |     |      |      |              |
| VCO Frequency Error for LOL Assert   | With respect to nominal        |     | 1000 |      | ppm          |
| VCO Frequency Error for LOL Deassert | With respect to nominal        |     | 250  |      | ppm          |
| LOL Response Time                    |                                |     | 200  |      | $\mu$ s      |
| ACQUISITION TIME                     |                                |     |      |      |              |
| Lock-to-Data Mode                    | GbE                            |     | 1.5  |      | ms           |
| Optional Lock to REFCLK Mode         |                                |     | 20.0 |      | ms           |
| DATA RATE READBACK ACCURACY          |                                |     |      |      |              |
| Fine Readback                        | In addition to REFCLK accuracy |     |      | 100  | ppm          |
| POWER SUPPLY                         |                                |     |      |      |              |
| Power Supply Voltage                 |                                | 3.0 | 3.3  | 3.6  | V            |
| Power Supply Current                 | Locked to 1.25 Gbps            |     | 118  | 131  | mA           |
| OPERATING TEMPERATURE RANGE          |                                |     |      |      |              |
|                                      |                                | –40 |      | +85  | $^{\circ}$ C |

## JITTER SPECIFICATIONS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = V_{MIN}$  to  $V_{MAX}$ ,  $V_{EE} = 0$  V,  $C_F = 0.47$   $\mu$ F, SLICEP = SLICEN = VEE, input data pattern: PRBS  $2^{23} - 1$ , unless otherwise noted.

Table 2.

| Parameter                         | Conditions               | Min   | Typ   | Max   | Unit   |
|-----------------------------------|--------------------------|-------|-------|-------|--------|
| PHASE-LOCKED LOOP CHARACTERISTICS |                          |       |       |       |        |
| Jitter Peaking                    |                          |       | 0     | 0.03  | dB     |
| Jitter Generation                 |                          |       | 0.001 | 0.003 | UI rms |
|                                   |                          |       | 0.02  | 0.04  | UI p-p |
| Jitter Tolerance                  | GbE, IEEE 802.3, 637 kHz | 0.749 |       |       | UI p-p |

## OUTPUT AND TIMING SPECIFICATIONS

Table 3.

| Parameter                                      | Conditions                                               | Min                     | Typ  | Max     | Unit          |
|------------------------------------------------|----------------------------------------------------------|-------------------------|------|---------|---------------|
| LVDS OUTPUT CHARACTERISTICS                    |                                                          |                         |      |         |               |
| CLKOUTP/CLKOUTN, DATAOUTP/DATAOUTN             |                                                          |                         |      |         |               |
| Differential Output Swing                      | $V_{OD}$ (see Figure 3)                                  | 240                     | 300  | 400     | mV            |
| Output Offset Voltage                          | $V_{OS}$ (see Figure 3)                                  | 1125                    | 1200 | 1275    | mV            |
| Output Impedance                               | Differential                                             |                         | 100  |         | $\Omega$      |
| LVDS Outputs Timing                            |                                                          |                         |      |         |               |
| Rise Time                                      | 20% to 80%                                               |                         | 115  | 220     | ps            |
| Fall Time                                      | 80% to 20%                                               |                         | 115  | 220     | ps            |
| Setup Time                                     | $T_S$ (see Figure 2), GbE                                | 360                     | 400  | 440     | ps            |
| Hold Time                                      | $T_H$ (see Figure 2), GbE                                | 360                     | 400  | 440     | ps            |
| I <sup>2</sup> C® INTERFACE DC CHARACTERISTICS |                                                          |                         |      |         |               |
| Input High Voltage                             | $V_{IH}$                                                 | 0.7 VCC                 |      |         | V             |
| Input Low Voltage                              | $V_{IL}$                                                 |                         |      | 0.3 VCC | V             |
| Input Current                                  | $V_{IN} = 0.1 \text{ VCC}$ or $V_{IN} = 0.9 \text{ VCC}$ | −10.0                   |      | +10.0   | $\mu\text{A}$ |
| Output Low Voltage                             | $V_{OL}, I_{OL} = 3.0 \text{ mA}$                        |                         |      | 0.4     | V             |
| I <sup>2</sup> C INTERFACE TIMING              |                                                          |                         |      |         |               |
| SCK Clock Frequency                            | See Figure 10                                            |                         |      | 400     | kHz           |
| SCK Pulse Width High                           | $t_{HIGH}$                                               | 600                     |      |         | ns            |
| SCK Pulse Width Low                            | $t_{LOW}$                                                | 1300                    |      |         | ns            |
| Start Condition Hold Time                      | $t_{HD,STA}$                                             | 600                     |      |         | ns            |
| Start Condition Setup Time                     | $t_{SU,STA}$                                             | 600                     |      |         | ns            |
| Data Setup Time                                | $t_{SU,DAT}$                                             | 100                     |      |         | ns            |
| Data Hold Time                                 | $t_{HD,DAT}$                                             | 300                     |      |         | ns            |
| SCK/SDA Rise/Fall Time                         | $t_R/t_F$                                                | $20 + 0.1 \text{ Cb}^1$ |      | 300     | ns            |
| Stop Condition Setup Time                      | $t_{SU,STO}$                                             | 600                     |      |         | ns            |
| Bus Free Time Between a Stop and a Start       | $t_{BUF}$                                                | 1300                    |      |         | ns            |
| REFCLK CHARACTERISTICS                         |                                                          |                         |      |         |               |
| Input Voltage Range                            | Optional lock-to-REFCLK mode<br>@ REFCLKP or REFCLKN     |                         |      |         |               |
| Input Low Voltage                              | $V_{IL}$                                                 |                         | 0    |         | V             |
| Input High Voltage                             | $V_{IH}$                                                 |                         | VCC  |         | V             |
| Minimum Differential Input Drive               |                                                          |                         | 100  |         | mV p-p        |
| Reference Frequency                            |                                                          | 10                      |      | 160     | MHz           |
| Required Accuracy                              |                                                          |                         | 100  |         | ppm           |
| LVTTL DC INPUT CHARACTERISTICS                 |                                                          |                         |      |         |               |
| Input High Voltage                             | $V_{IH}$                                                 | 2.0                     |      |         | V             |
| Input Low Voltage                              | $V_{IL}$                                                 |                         |      | 0.8     | V             |
| Input High Current                             | $I_{IH}, V_{IN} = 2.4 \text{ V}$                         |                         |      | 5       | $\mu\text{A}$ |
| Input Low Current                              | $I_{IL}, V_{IN} = 0.4 \text{ V}$                         | −5                      |      |         | $\mu\text{A}$ |
| LVTTL DC OUTPUT CHARACTERISTICS                |                                                          |                         |      |         |               |
| Output High Voltage                            | $V_{OH}, I_{OH} = -2.0 \text{ mA}$                       | 2.4                     |      |         | V             |
| Output Low Voltage                             | $V_{OL}, I_{OL} = 2.0 \text{ mA}$                        |                         |      | 0.4     | V             |

<sup>1</sup> Cb = total capacitance of one bus line in pF. If mixed with high speed mode devices, faster fall times are allowed.

## Timing Characteristics

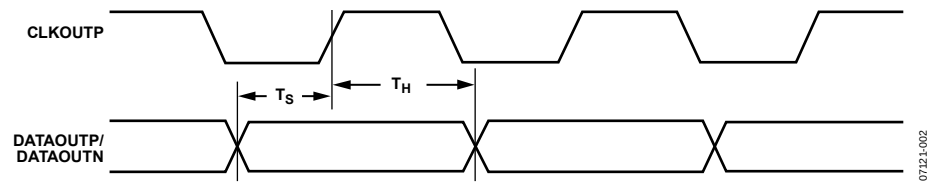


Figure 2. Output Timing

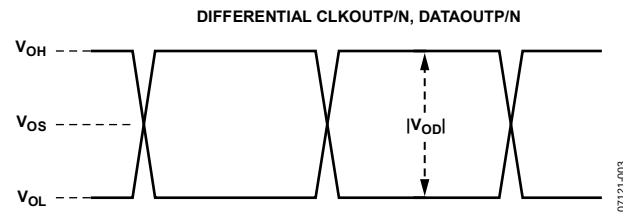


Figure 3. Differential Output Specifications

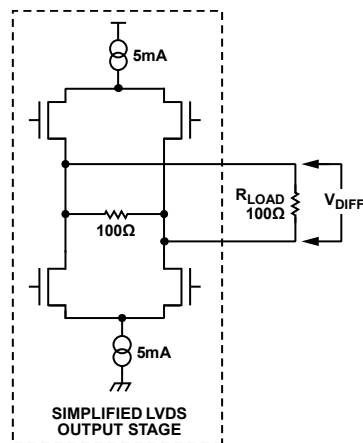


Figure 4. Differential Output Stage

## ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = V_{MIN}$  to  $V_{MAX}$ ,  $V_{EE} = 0\text{ V}$ ,  $C_F = 0.47\text{ }\mu\text{F}$ ,  $SLICEP = SLICEN = V_{EE}$ , unless otherwise noted.

Table 4.

| Parameter                          | Rating                  |
|------------------------------------|-------------------------|
| Supply Voltage (VCC)               | 4.2 V                   |
| Minimum Input Voltage (All Inputs) | $V_{EE} - 0.4\text{ V}$ |
| Maximum Input Voltage (All Inputs) | $V_{CC} + 0.4\text{ V}$ |
| Maximum Junction Temperature       | 125°C                   |
| Storage Temperature Range          | -65°C to +150°C         |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

### Thermal Resistance

4-layer board with exposed paddle soldered to VEE.

Table 5. Thermal Resistance

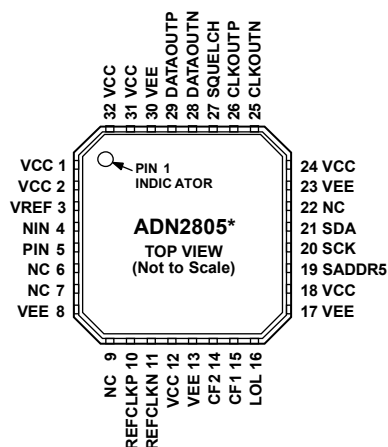
| Package Type  | $\theta_{JA}$ | Unit |
|---------------|---------------|------|
| 32-Lead LFCSP | 28            | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



\* THERE IS AN EXPOSED PAD ON THE BOTTOM OF THE PACKAGE THAT MUST BE CONNECTED TO GND.

07121-005

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No.     | Mnemonic | Type <sup>1</sup> | Description                                                          |
|-------------|----------|-------------------|----------------------------------------------------------------------|
| 1           | VCC      | AI                | Connect to VCC.                                                      |
| 2           | VCC      | P                 | Power for Limiting Amplifier, LOS.                                   |
| 3           | VREF     | AO                | Internal VREF Voltage. Decouple to GND with a 0.1 $\mu$ F capacitor. |
| 4           | NIN      | AI                | Differential Data Input. CML.                                        |
| 5           | PIN      | AI                | Differential Data Input. CML.                                        |
| 6, 7, 9, 22 | NC       |                   | No Connect.                                                          |
| 8           | VEE      | P                 | GND for Limiting Amplifier, LOS.                                     |
| 10          | REFCLKP  | DI                | Differential REFCLK Input. 10 MHz to 160 MHz.                        |
| 11          | REFCLKN  | DI                | Differential REFCLK Input. 10 MHz to 160 MHz.                        |
| 12          | VCC      | P                 | VCO Power.                                                           |
| 13          | VEE      | P                 | VCO GND.                                                             |
| 14          | CF2      | AO                | Frequency Loop Capacitor.                                            |
| 15          | CF1      | AO                | Frequency Loop Capacitor.                                            |
| 16          | LOL      | DO                | Loss-of-Lock Indicator. LVTTTL active high.                          |
| 17          | VEE      | P                 | FLL Detector GND.                                                    |
| 18          | VCC      | P                 | FLL Detector Power.                                                  |
| 19          | SADDR5   | DI                | Slave Address Bit 5.                                                 |
| 20          | SCK      | DI                | I <sup>2</sup> C Clock Input.                                        |
| 21          | SDA      | DI                | I <sup>2</sup> C Data Input.                                         |
| 23          | VEE      | P                 | Output Buffer, I <sup>2</sup> C GND.                                 |
| 24          | VCC      | P                 | Output Buffer, I <sup>2</sup> C Power.                               |
| 25          | CLKOUTN  | DO                | Differential Recovered Clock Output. LVDS.                           |
| 26          | CLKOUTP  | DO                | Differential Recovered Clock Output. LVDS.                           |
| 27          | SQUELCH  | DI                | Disable Clock and Data Outputs. Active high. LVTTTL.                 |
| 28          | DATAOUTN | DO                | Differential Recovered Data Output. LVDS.                            |
| 29          | DATAOUTP | DO                | Differential Recovered Data Output. LVDS.                            |
| 30          | VEE      | P                 | Phase Detector, Phase Shifter GND.                                   |
| 31          | VCC      | P                 | Phase Detector, Phase Shifter Power.                                 |
| 32          | VCC      | AI                | Connect to VCC.                                                      |
| Exposed Pad | Pad      | P                 | Connect to GND. Works as a heat sink.                                |

<sup>1</sup> Type: P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output.

| SLAVE ADDRESS [6...0] |    |   |   |   |   |   | R/W CTRL. |
|-----------------------|----|---|---|---|---|---|-----------|
| 1                     | A5 | 0 | 0 | 0 | 0 | 0 | X         |

MSB = 1 SET BY PIN 19

0 = WR  
1 = RD

W7121-006

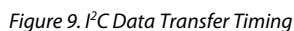




Table 7. Internal Register Map<sup>1, 2</sup>

| Reg. Name | R/W | Address | D7                     | D6            | D5           | D4                                   | D3            | D2                         | D1                | D0                 |
|-----------|-----|---------|------------------------|---------------|--------------|--------------------------------------|---------------|----------------------------|-------------------|--------------------|
| FREQ0     | R   | 0x0     | MSB                    |               |              |                                      |               |                            |                   | LSB                |
| FREQ1     | R   | 0x1     | MSB                    |               |              |                                      |               |                            |                   | LSB                |
| FREQ2     | R   | 0x2     | 0                      | MSB           |              |                                      |               |                            |                   | LSB                |
| RATE      | R   | 0x3     | COARSE_RD[8] MSB       |               |              | Coarse Data Rate Readback            |               |                            | COARSE_RD[1]      |                    |
| MISC      | R   | 0x4     | X                      | X             | X            | Static LOL                           | LOL Status    | Data Rate Measure Complete | X                 | COARSE_RD[0] (LSB) |
| CTRLA     | W   | 0x8     | f <sub>REF</sub> Range |               |              | Data Rate/DIV_f <sub>REF</sub> Ratio |               |                            | Measure Data Rate | Lock to Reference  |
| CTRLB     | W   | 0x9     | Config LOL             | Reset MISC[4] | System Reset | 0                                    | Reset MISC[2] | 0                          | 0                 | 0                  |
| CTRLC     | W   | 0x11    | 0                      | 0             | 0            | 0                                    | 0             | 0                          | Squelch Mode      | Output Boost       |

<sup>1</sup> All writeable registers default to 0x00.<sup>2</sup> X = don't care.Table 8. Miscellaneous Register, MISC<sup>1</sup>

| D7 | D6 | D5 | Static LOL                                             | LOL Status                  | Data Rate Measurement Complete                      | D1 | Coarse Rate Readback LSB |
|----|----|----|--------------------------------------------------------|-----------------------------|-----------------------------------------------------|----|--------------------------|
|    |    |    | D4                                                     | D3                          | D2                                                  |    | D0                       |
| X  | X  | X  | 0 = waiting for next LOL<br>1 = static LOL until reset | 0 = locked<br>1 = acquiring | 0 = measuring data rate<br>1 = measurement complete | X  | COARSE_RD[0]             |

<sup>1</sup> X = don't care.Table 9. Control Register, CTRLA<sup>1</sup>

| f <sub>REF</sub> Range |    |                   | Data Rate/DIV_f <sub>REF</sub> Ratio |    |    |                | Measure Data Rate             | Lock to Reference           |
|------------------------|----|-------------------|--------------------------------------|----|----|----------------|-------------------------------|-----------------------------|
| D7                     | D6 |                   | D5                                   | D4 | D3 | D2             | D1                            | D0                          |
| 0                      | 0  | 10 MHz to 20 MHz  | 0                                    | 0  | 0  | 1              | Set to 1 to measure data rate | 0 = lock to input data      |
| 0                      | 1  | 20 MHz to 40 MHz  | 0                                    | 0  | 0  | 1              |                               | 1 = lock to reference clock |
| 1                      | 0  | 40 MHz to 80 MHz  | 0                                    | 0  | 1  | 0              |                               |                             |
| 1                      | 1  | 80 MHz to 160 MHz |                                      |    | n  | 2 <sup>n</sup> |                               |                             |
|                        |    |                   | 1                                    | 0  | 0  | 0              | 256                           |                             |

<sup>1</sup> Where DIV\_f<sub>REF</sub> is the divided down reference referred to the 10 MHz to 20 MHz band.

Table 10. Control Register, CTRLB

| Configure LOL                                             | Reset MISC[4]                            | System Reset                             | D4       | Reset MISC[2]                            | D2       | D1       | D0       |
|-----------------------------------------------------------|------------------------------------------|------------------------------------------|----------|------------------------------------------|----------|----------|----------|
| D7                                                        | D6                                       | D5                                       |          | D3                                       |          |          |          |
| 0 = LOL pin normal operation<br>1 = LOL pin is static LOL | Write a 1 followed by 0 to reset MISC[4] | Write a 1 followed by 0 to reset ADN2805 | Set to 0 | Write a 1 followed by 0 to reset MISC[2] | Set to 0 | Set to 0 | Set to 0 |

Table 11. Control Register, CTRLC

| D7       | D6       | D5       | D4       | D3       | D2       | Squelch Mode                                                    | Output Boost                                       |
|----------|----------|----------|----------|----------|----------|-----------------------------------------------------------------|----------------------------------------------------|
|          |          |          |          |          |          | D1                                                              | D0                                                 |
| Set to 0 | Set to 0 | Set to 0 | Set to 0 | Set to 0 | Set to 0 | 0 = SQUELCH DATAOUT and CLKOUT<br>1 = SQUELCH DATAOUT or CLKOUT | 0 = default output swing<br>1 = boost output swing |

## THEORY OF OPERATION

The ADN2805 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops that share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, comprised of the VCO, tracks the low frequency components of input jitter. The initial frequency of the VCO is set by yet a third loop, which compares the VCO frequency with the input data frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop (PLL) controls the VCO by the fine-tuning control.

The delay and phase loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the VCO to a higher frequency and increases the delay through the phase shifter; both of these actions serve to reduce the phase error between the clock and data. The faster clock picks up phase, while simultaneously, the delayed data loses phase. Because the loop filter is an integrator, the static phase error is driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and, thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay and phase loops together simultaneously provide wideband jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 11 shows that the jitter transfer function,  $Z(s)/X(s)$ , is second-order low-pass, providing excellent filtering. Note that the jitter transfer has no zero, unlike an ordinary second-order phase-locked loop. This means that the main PLL has virtually zero jitter peaking (see Figure 12). This makes this circuit ideal for signal regenerator applications where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer,  $e(s)/X(s)$ , has the same high-pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wideband jitter accommodation because the jitter transfer function,  $Z(s)/X(s)$ , provides the narrow-band jitter filtering.

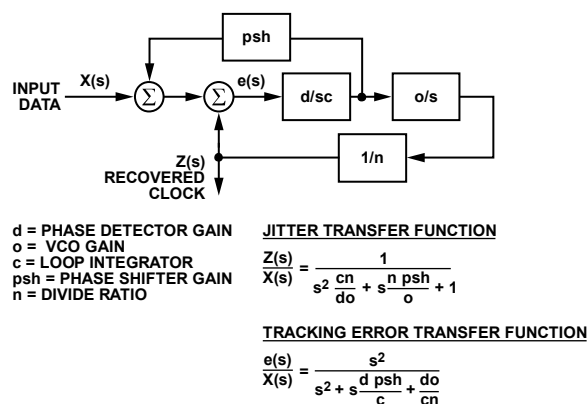


Figure 11. ADN2805 PLL/DLL Architecture

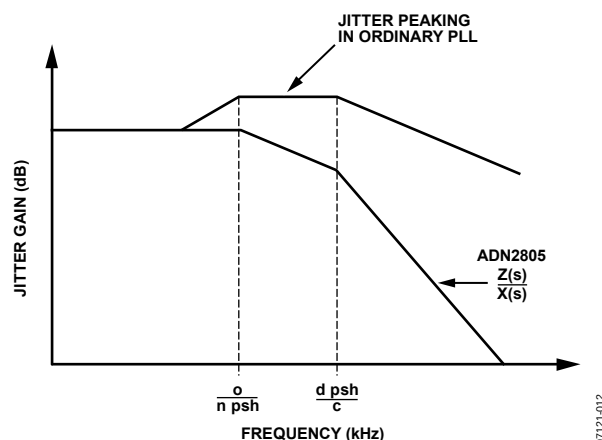


Figure 12. ADN2805 Jitter Response vs. Conventional PLL

The delay and phase loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the VCO is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCO tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors; therefore, the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCO are not large enough to track input jitter. In this case, the VCO control voltage becomes large and saturates, and the VCO frequency dwells at either one extreme of its tuning range or at the other. The size of the VCO tuning range, therefore, has only a small effect on the jitter accommodation. As such, the delay-locked loop control voltage is larger, and, consequently, the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2 UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies; therefore, larger phase differences are needed to make the loop control voltage large enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region, the gain of the integrator determines the jitter accommodation. Because the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the

phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly 1.5 MHz at 1.25 Gbps.

## FUNCTIONAL DESCRIPTION

### FREQUENCY ACQUISITION

The ADN2805 acquires frequency from the data at 1.25 Gbps. The lock detector circuit compares the frequency of the VCO and the frequency of the incoming data. When these frequencies differ by more than 1000 ppm, LOL asserts. This initiates a frequency acquisition cycle. An on-chip frequency-locked loop (FLL) forces the frequency of the VCO to be approximately equal to the frequency of the incoming data. LOL is deasserted once the VCO frequency is within 250 ppm of the data frequency.

When LOL deasserts, the FLL turns off. The PLL/DLL pulls in the VCO frequency until the VCO frequency equals the data frequency.

The frequency loop requires a single external capacitor between CF1 and CF2, Pin 15 and Pin 14. A  $0.47\ \mu\text{F} \pm 20\%$ , X7R ceramic chip capacitor with  $<10\ \text{nA}$  leakage current is recommended. Calculate the leakage current of the capacitor by dividing the maximum voltage across the  $0.47\ \mu\text{F}$  capacitor,  $\sim 3\ \text{V}$ , by the insulation resistance of the capacitor. The insulation resistance of the  $0.47\ \mu\text{F}$  capacitor should be greater than  $300\ \text{M}\Omega$ .

### INPUT BUFFER

The input buffer has differential inputs (PIN/NIN), which are internally terminated with  $50\ \Omega$  to an on-chip voltage reference ( $V_{\text{REF}} = 2.5\ \text{V}$  typically). The minimum differential input level required to achieve a BER of  $10^{-10}$  is  $200\ \text{mV p-p}$ .

### LOCK DETECTOR OPERATION

The lock detector on the ADN2805 has three modes of operation: normal mode, REFCLK mode, and static LOL mode.

#### Normal Mode

In normal mode, the ADN2805 locks onto 1.25 Gbps NRZ data without the use of a reference clock as an acquisition aid. In this mode, the lock detector monitors the frequency difference between the VCO and the input data frequency, and deasserts the loss-of-lock signal, which appears on Pin 16 (LOL) when the VCO is within 250 ppm of the data frequency. This enables the DLL/PLL, which pulls the VCO frequency in the remaining amount and acquires phase lock. When locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss-of-lock signal reasserts and control returns to the frequency loop, which begins a new frequency acquisition. The LOL pin remains asserted until the VCO locks onto a valid input data stream to within 250 ppm frequency error. This hysteresis is shown in Figure 13.

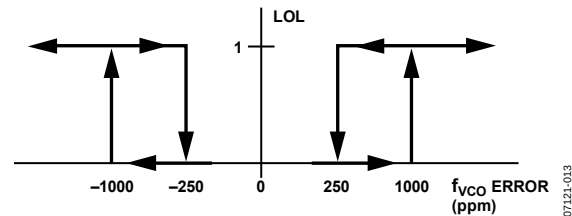


Figure 13. Transfer Function of LOL

#### LOL Detector Operation Using a Reference Clock

In REFCLK mode, a reference clock is used as an acquisition aid to lock the ADN2805 VCO. Lock-to-reference mode is enabled by setting CTRLA[0] to 1. The user also needs to write to the CTRLA[7:6] and CTRLA[5:2] bits to set the reference frequency range and the divide ratio of the data rate with respect to the reference frequency. In this mode, the lock detector monitors the difference in frequency between the divided down VCO and the divided down reference clock. The loss-of-lock signal, which appears on Pin 16 (LOL), deasserts when the VCO is within 250 ppm of the desired frequency. This enables the DLL/PLL, which pulls the VCO frequency in the remaining amount with respect to the input data and acquires phase lock. When locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss-of-lock signal reasserts and control returns to the frequency loop, which reacquires with respect to the reference clock. The LOL pin remains asserted until the VCO frequency is within 250 ppm of the desired frequency. This hysteresis is shown in Figure 13.

#### Static LOL Mode

The ADN2805 implements a static LOL feature to indicate whether a loss-of-lock condition has ever occurred and remains asserted, even if the ADN2805 regains lock, until the static LOL bit is manually reset. The I<sup>2</sup>C register bit, MISC[4], is the static LOL bit. If there is ever an occurrence of a loss-of-lock condition, this bit internally asserts to Logic high. The MISC[4] bit remains high even after the ADN2805 has reacquired lock to a new data rate. This bit can be reset by writing a 1 followed by 0 to I<sup>2</sup>C Register Bit CTRLB[6]. When reset, the MISC[4] bit remains deasserted until another loss-of-lock condition occurs.

Writing a 1 to I<sup>2</sup>C Register Bit CTRLB[7] causes the LOL pin, Pin 16, to become a static LOL indicator. In this mode, the LOL pin mirrors the contents of the MISC[4] bit and has the functionality described in the previous paragraph.

The CTRLB[7] bit defaults to 0. In this mode, the LOL pin operates in the normal operating mode, that is, it asserts only when the ADN2805 is in acquisition mode and deasserts when the ADN2805 reacquires lock.

## SQUELCH MODE

Two squelch modes are available with the ADN2805. The SQUELCH DATAOUT and CLKOUT mode is selected when CTRLC[1] = 0 (default mode). In this mode, when the SQUELCH input, Pin 27, is driven to a TTL high state, both the clock and data outputs are set to the zero state to suppress downstream processing. If the squelch function is not required, tie Pin 27 to VEE.

SQUELCH DATAOUT or CLKOUT mode is selected when CTRLC[1] is 1. In this mode, when the SQUELCH input is driven to a high state, the DATAOUTN/DATAOUTP pins are squelched. When the SQUELCH input is driven to a low state, the CLKOUT pins are squelched. This feature is especially useful in repeater applications, where the recovered clock may not be needed.

## SYSTEM RESET

A frequency acquisition can be initiated by writing a 1 followed by a 0 to the I<sup>2</sup>C Register Bit CTRLB[5]. This initiates a new frequency acquisition while keeping the ADN2805 in the operating mode that it was previously programmed to in Register CTRL[A], Register CTRL[B], and Register CTRL[C].

## I<sup>2</sup>C INTERFACE

The ADN2805 supports a 2-wire, I<sup>2</sup>C-compatible, serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any devices connected to the bus. Each slave device is recognized by a unique address. The ADN2805 has two possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address is factory programmed to 1. Bit 5 of the slave address is set by Pin 19, SADDR5. Slave Address Bits[4:0] are defaulted to all 0s. The slave address consists of the 7 MSBs of an 8-bit word. The LSB of the word either sets a read or write operation (see Figure 6). Logic 1 corresponds to a read operation whereas Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit).

The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCK lines waiting for the start condition and correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2805 acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses, plus the R/W bit. The ADN2805 has eight subaddresses to enable the user-accessible internal registers (see Table 7 through Table 11). It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Auto-increment mode is supported, allowing data to be read from or written to the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions assert out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCK high period, the user should issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADN2805 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while reading back in auto-increment mode, the highest subaddress register contents continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. In a no-acknowledge condition, the SDA line is not pulled low on the ninth pulse. See Figure 7 and Figure 8 for sample read and write data transfers and Figure 9 for a more detailed timing diagram.

## APPLICATIONS INFORMATION

### PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

#### Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. To reduce series inductance, solder the VEE pins directly to the ground plane. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance, especially on Pin 23, which is the ground return for the output buffers. Connect the exposed pad to the ground plane using plugged vias to prevent solder from leaking through the vias during reflow.

Use of a 22  $\mu\text{F}$  electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1  $\mu\text{F}$  and 1 nF ceramic chip capacitors, place them between the IC power supply VCC and VEE, as close as possible to the ADN2805 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pin 24, which supplies power to the high speed CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN output buffers. Refer to Figure 14 for the recommended connections.

By using adjacent power supply and ground planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{\text{PLANE}} = 0.88\epsilon_r A/d (\text{pF})$$

where:

$\epsilon_r$  is the dielectric constant of the PCB material.

$A$  is the area of the overlap of power and ground planes ( $\text{cm}^2$ ).  
 $d$  is the separation between planes (mm).

For FR-4,  $\epsilon_r = 4.4$  mm and 0.25 mm spacing,  $C \sim 15 \text{ pF/cm}^2$ .

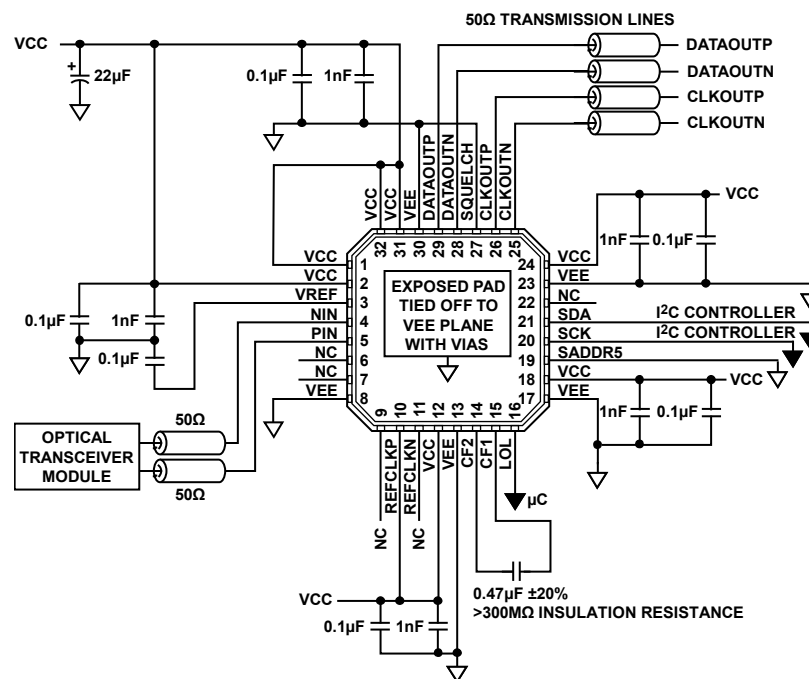


Figure 14. Typical Applications Circuit

### Transmission Lines

Use of 50  $\Omega$  transmission lines is required for all high frequency input and output signals to minimize reflections: PIN, NIN, CLKOUTP, CLKOUTN, DATAOUTP, and DATAOUTN (also REFCLKP and REFCLKN, if a high frequency reference clock is used, such as 155 MHz). It is also necessary for the PIN/NIN input traces to be matched in length, and the CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN output traces to be matched in length to avoid skew between the differential traces.

The high speed inputs, PIN and NIN, are internally terminated with 50  $\Omega$  to an internal reference voltage (see Figure 15).

A 0.1  $\mu\text{F}$  is recommended between VREF, Pin 3, and GND to provide an ac ground for the inputs.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

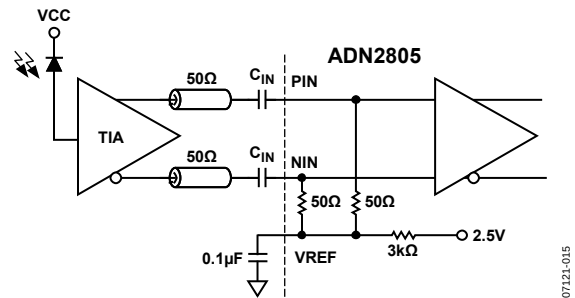


Figure 15. AC-Coupled Input Configuration

### Soldering Guidelines for Lead Frame Chip Scale Package

The lands on the 32-lead LFCSP are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the PCB should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

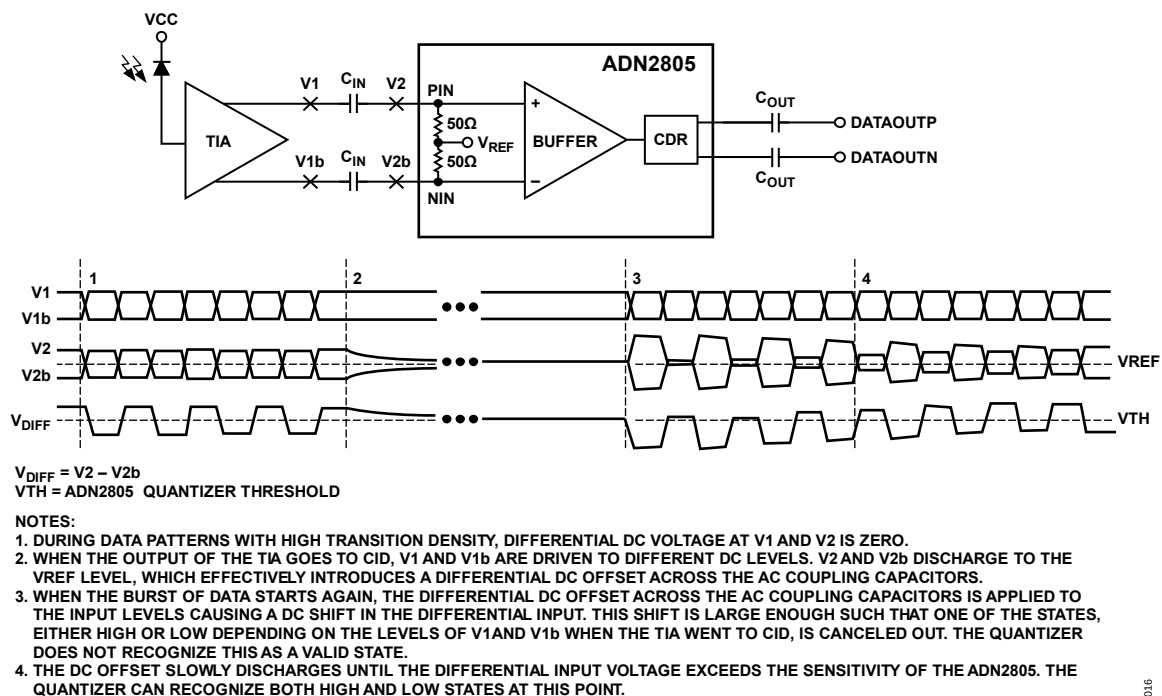
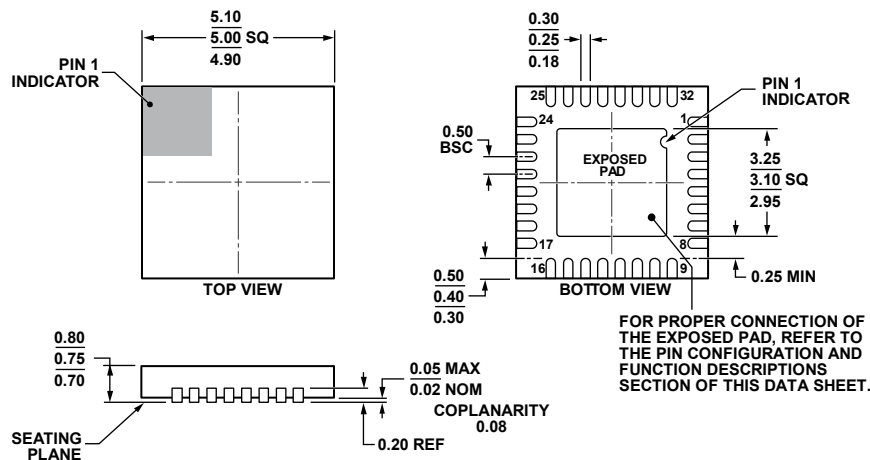


Figure 16. Example of Baseline Wander



OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.  
Figure 17. 32-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
5 mm x 5 mm Body, Very Thin Quad  
(CP-32-7)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                       | Package Option |
|--------------------|-------------------|-------------------------------------------|----------------|
| ADN2805ACPZ        | −40°C to +85°C    | 32-Lead LFCSP_WQ                          | CP-32-7        |
| ADN2805ACPZ-500RL7 | −40°C to +85°C    | 32-Lead LFCSP_WQ, Tape-Reel, 500 pieces   | CP-32-7        |
| ADN2805ACPZ-RL7    | −40°C to +85°C    | 32-Lead LFCSP_WQ, Tape-Reel, 1,500 pieces | CP-32-7        |
| EVAL-ADN2805EBZ    |                   | Evaluation Board                          |                |

<sup>1</sup> Z = RoHS Compliant Part.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).