TEXAS INSTRUMENTS

LMV358, LMV321, LMV324, LMV324S

SLOS263W −AUGUST 1999−REVISED OCTOBER 2014
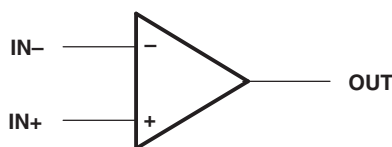
LMV3xx Low-Voltage Rail-to-Rail Output Operational Amplifiers

1 Features

- 2.7-V and 5-V Performance
- −40°C to 125°C Operation
- Low-Power Shutdown Mode (LMV324S)
- No Crossover Distortion
- Low Supply Current
  - LMV321: 130 µA Typ
  - LMV358: 210 µA Typ
  - LMV324: 410 µA Typ
  - LMV324S: 410 µA Typ
- Rail-to-Rail Output Swing
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Desktop PCs
- HVAC: Heating, Ventilating, and Air Conditioning
- Motor Control: AC Induction
- Netbooks
- Portable Media Players
- Power: Telecom DC/DC Module: Digital
- Pro Audio Mixers
- Refrigerators
- Washing Machines: High-End and Low-End

3 Description

The LMV321, LMV358, LMV324, and LMV324S devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. These devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. With package sizes down to one-half the size of the DBV (SOT-23) package, these devices can be used for a variety of applications.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE
LMV324	SOIC (14)	8.65 mm × 3.91 mm
LMV321	SOT-23 (5)	2.90 mm × 1.60 mm
	SC-70 (5)	2.00 mm × 1.25 mm
LMV358	VSSOP (8)	2.30 mm × 2.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

Table of Contents

5 Revision History

Changes from Revision V (December 2013) to Revision W   **Page**

Changes from Revision U (July 2012) to Revision V   **Page**
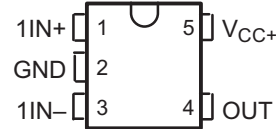
6 Pin Configuration and Functions

LMV358 . . . D (SOIC), DDU (VSSOP),
DGK (VSSOP), OR PW (TSSOP) PACKAGE
(TOP VIEW)

```
1OUT [ 1      8 ] V_CC+
1IN– [ 2      7 ] 2OUT
1IN+ [ 3      6 ] 2IN–
GND [ 4      5 ] 2IN+
```
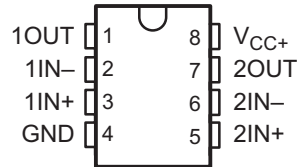
LMV321 . . . DBV (SOT-23)
OR DCK (SC-70) PACKAGE
(TOP VIEW)

```
1IN+ [ 1      5 ] V_CC+
GND [ 2
1IN– [ 3      4 ] OUT
```

LMV324 . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)

```
1OUT [ 1      14 ] 4OUT
1IN– [ 2      13 ] 4IN–
1IN+ [ 3      12 ] 4IN+
V_CC+ [ 4      11 ] GND
2IN+ [ 5      10 ] 3IN+
2IN– [ 6       9 ] 3IN–
2OUT [ 7       8 ] 3OUT
```
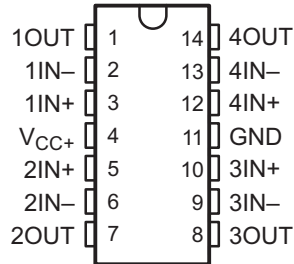
LMV324S . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)

```
1OUT [ 1      16 ] 4OUT
1IN– [ 2      15 ] 4IN–
1IN+ [ 3      14 ] 4IN+
V_CC [ 4      13 ] GND
2IN+ [ 5      12 ] 3IN+
2IN– [ 6      11 ] 3IN–
2OUT [ 7      10 ] 3OUT
1/2 SHDN [ 8    9 ] 3/4 SHDN
```
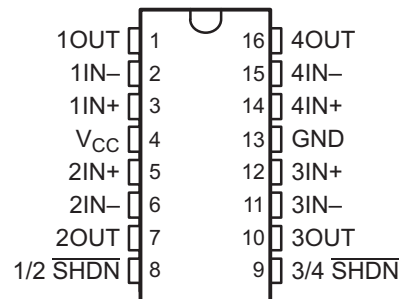
Pin Functions

	PIN				TYPE	DESCRIPTION
	LMV358	LMV321	LMV324	LMV324S		
NAME	D, DDU, DGK, PW	DBV or DCK	D or PW	D or PW		
3/4 SHDN	—	—	—	9	I	Shutdown (logic low)/enable (logic high)
1/2 SHDN	—	—	—	8	I	Shutdown (logic low)/enable (logic high)
1IN+	3	1	3	3	I	Noninverting input
1IN–	2	3	2	2	I	Inverting input
2IN+	5	—	5	5	I	Noninverting input
2IN–	6	—	6	6	I	Inverting input
2OUT	7	—	7	7	O	Output
3IN+	—	—	10	12	I	Noninverting input
3IN–	—	—	9	11	I	Inverting input
3OUT	—	—	8	10	O	Output
4IN+	—	—	12	14	I	Noninverting input
4IN–	—	—	13	15	I	Inverting input
4OUT	—	—	14	16	O	Output
GND	4	2	11	13	-	Negative supply
OUT	1	4	1	1	O	OUT
VCC+	8	5	4	4	-	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]			5.5	V
V_{ID}	Differential input voltage[3]			±5.5	V
V_I	Input voltage range (either input)		−0.2	5.7	V
	Duration of output short circuit (one amplifier) to ground[4]	At or below T_A = 25°C, V_{CC} ≤ 5.5 V	Unlimited		
T_J	Operating virtual junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)		2.7	5.5	V
V_{IH}	Amplifier turn-on voltage level (LMV324S)[2]	V_{CC} = 2.7 V	1.7		V
		V_{CC} = 5 V	3.5		
V_{IL}	Amplifier turn-off voltage level (LMV324S)	V_{CC} = 2.7 V		0.7	V
		V_{CC} = 5 V		1.5	
T_A	Operating free-air temperature	I temperature (LMV321, LMV358, LMV324, LMV321IDCK)	−40	125	°C
		I temperature (LMV324S)	-40	85	
		Q temperature	−40	125	

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) V_{IH} should not be allowed to exceed V_{CC}.

7.4 Thermal Information

THERMAL METRIC[1]	LMV3xx										UNIT
	D			DBV	DCK	DDU	DGK	PW			
	8 PIN	14 PIN	16 PIN	5 PIN	5 PIN	8 PIN	8 PIN	8 PIN	14 PIN	16 PIN	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	97	86	73	206	252	210	172	149	113	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

7.5 Electrical Characteristics: $V_{CC}+$ = 2.7 V

V_{CC+} = 2.7 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IO}	Input offset voltage				1.7	7	mV
α_{VIO}	Average temperature coefficient of input offset voltage				5		μV/°C
I_{IB}	Input bias current				11	250	nA
I_{IO}	Input offset current				5	50	nA
CMRR	Common-mode rejection ratio	V_{CM} = 0 to 1.7 V		50	63		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 2.7 V to 5 V, V_O = 1 V		50	60		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		0	–0.2		V
				1.9	1.7		
V_O	Output swing	R_L = 10 kΩ to 1.35 V	High level	V_{CC} – 100	V_{CC} – 10		mV
			Low level		60	180	
I_{CC}	Supply current	LMV321I			80	170	μA
		LMV358I (both amplifiers)			140	340	
		LMV324I and LMV324SI (all four amplifiers)			260	680	
B_1	Unity-gain bandwidth	C_L = 200 pF			1		MHz
Φ_m	Phase margin				60		deg
G_m	Gain margin				10		dB
V_n	Equivalent input noise voltage	f = 1 kHz			46		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.17		pA/√Hz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.6 Electrical Characteristics: V$_{CC}$+ = 5 V

V$_{CC+}$ = 5 V, at specified free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T$_A$ (1)	MIN	TYP(2)	MAX	UNIT
V$_{IO}$	Input offset voltage			25°C		1.7	7	mV
				Full range			9	
α$_{VIO}$	Average temperature coefficient of input offset voltage			25°C		5		µV/°C
I$_{IB}$	Input bias current			25°C		15	250	nA
				Full range			500	
I$_{IO}$	Input offset current			25°C		5	50	nA
				Full range			150	
CMRR	Common-mode rejection ratio	V$_{CM}$ = 0 to 4 V		25°C	50	65		dB
k$_{SVR}$	Supply-voltage rejection ratio	V$_{CC}$ = 2.7 V to 5 V, V$_O$ = 1 V, V$_{CM}$ = 1 V		25°C	50	60		dB
V$_{ICR}$	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	−0.2		V
					4.2	4		
V$_O$	Output swing	R$_L$ = 2 kΩ to 2.5 V	High level	25°C	V$_{CC}$ − 300	V$_{CC}$ − 40		mV
				Full range	V$_{CC}$ − 400			
			Low level	25°C		120	300	
				Full range			400	
		R$_L$ = 10 kΩ to 2.5 V	High level	25°C	V$_{CC}$ − 100	V$_{CC}$ − 10		
				Full range	V$_{CC}$ − 200			
			Low level	25°C		65	180	
				Full range			280	
A$_{VD}$	Large-signal differential voltage gain	R$_L$ = 2 kΩ		25°C	15	100		V/mV
				Full range	10			
I$_{OS}$	Output short-circuit current	Sourcing, V$_O$ = 0 V		25°C	5	60		mA
		Sinking, V$_O$ = 5 V			10	160		
I$_{CC}$	Supply current	LMV321I		25°C		130	250	µA
				Full range			350	
		LMV358I (both amplifiers)		25°C		210	440	
				Full range			615	
		LMV324I and LMV324SI (all four amplifiers)		25°C		410	830	
				Full range			1160	
B$_1$	Unity-gain bandwidth	C$_L$ = 200 pF		25°C		1		MHz
Φ$_m$	Phase margin			25°C		60		deg
G$_m$	Gain margin			25°C		10		dB
V$_n$	Equivalent input noise voltage	f = 1 kHz		25°C		39		nV/√Hz
I$_n$	Equivalent input noise current	f = 1 kHz		25°C		0.21		pA/√Hz
SR	Slew rate			25°C		1		V/µs

(1) Full range T$_A$ = −40°C to 125°C for I temperature(LMV321, LMV358, LMV324, LMV321IDCK), −40°C to 85°C for (LMV324S) and −40°C to 125°C for Q temperature.
(2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

7.7 Shutdown Characteristics, LMV324S: $V_{CC}+$ = 2.7 V

V_{CC+} = 2.7 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{SHDN}$ ≤ 0.6 V			5	µA
$t_{(on)}$	Amplifier turn-on time	A_V = 1, R_L = Open (measured at 50% point)		2		µs
$t_{(off)}$	Amplifier turn-off time	A_V = 1, R_L = Open (measured at 50% point)		40		ns

(1)   Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.8 Shutdown Characteristics, LMV324S: $V_{CC}+$ = 5 V

V_{CC+} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{SHDN}$ ≤ 0.6 V, T_A = Full Temperature Range			5	µA
$t_{(on)}$	Amplifier turn-on time	A_V = 1, R_L = Open (measured at 50% point)		2		µs
$t_{(off)}$	Amplifier turn-off time	A_V = 1, R_L = Open (measured at 50% point)		40		ns

(1)   Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
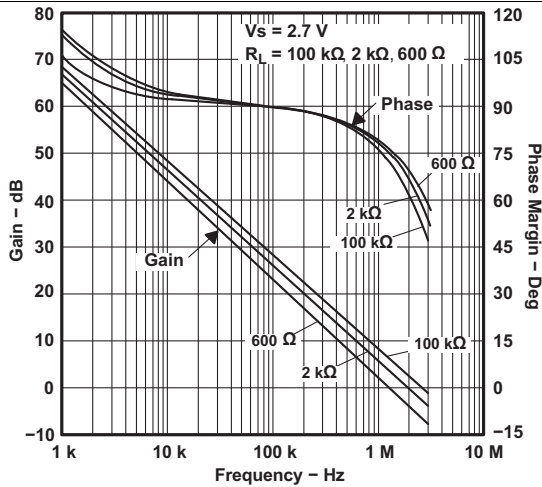
7.9 Typical Characteristics

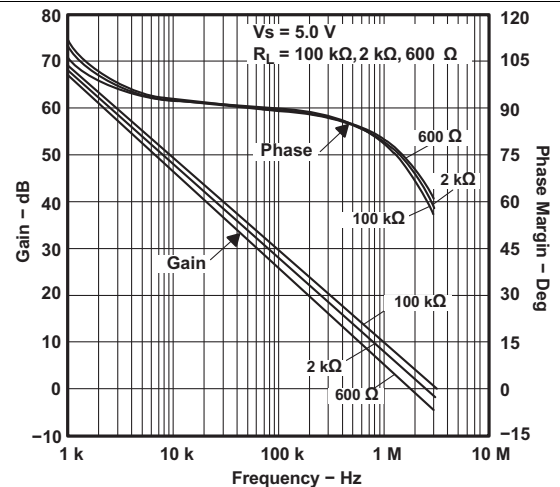**Figure 1. LMV321 Frequency Response vs Resistive Load**

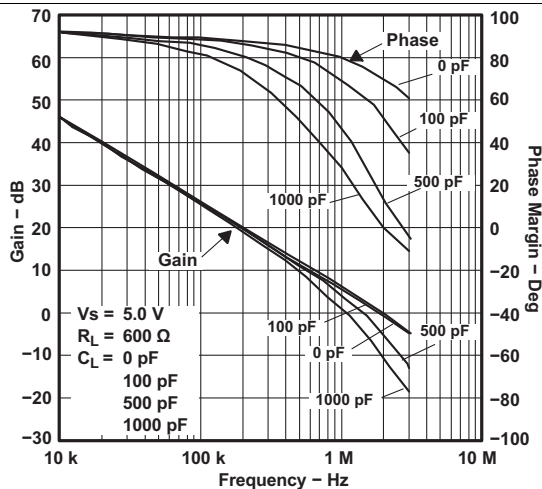**Figure 2. LMV321 Frequency Response vs Resistive Load**

Figure 3. LMV321 Frequency Response vs Capacitive Load
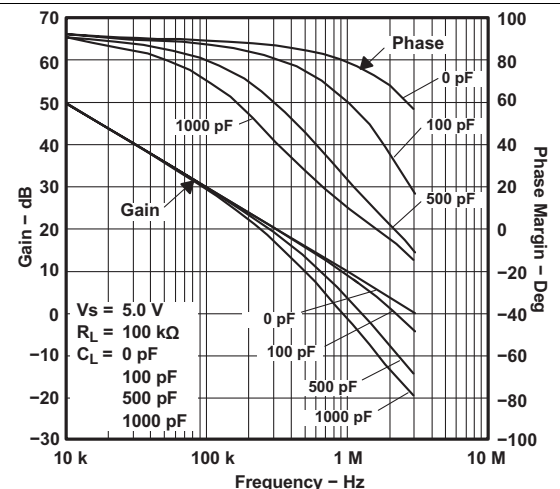

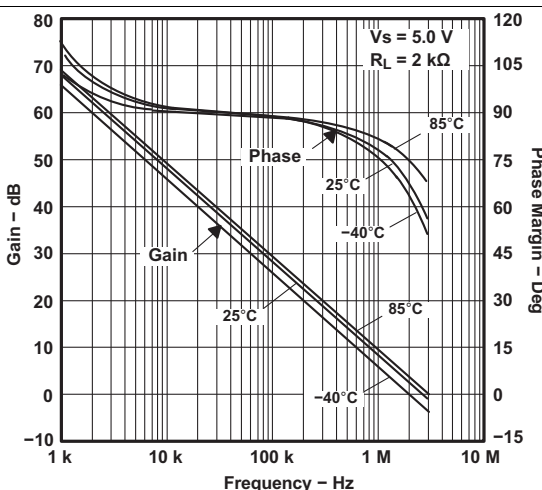**Figure 4. LMV321 Frequency Response vs Capacitive Load**

Figure 5. LMV321 Frequency Response vs Temperature
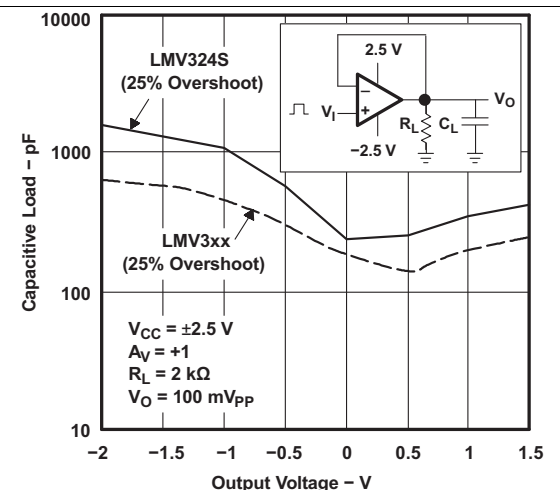
Figure 6. Stability vs Capacitive Load

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Characteristics (continued)

**Figure 7. Stability
vs Capacitive Load**

**Figure 8. Stability
vs Capacitive Load**

**Figure 9. Stability
vs Capacitive Load**

**Figure 10. Slew Rate
vs Supply Voltage**

**Figure 11. Supply Current
vs Supply Voltage - Quad Amplifier**

**Figure 12. Input Current
vs Temperature**

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*
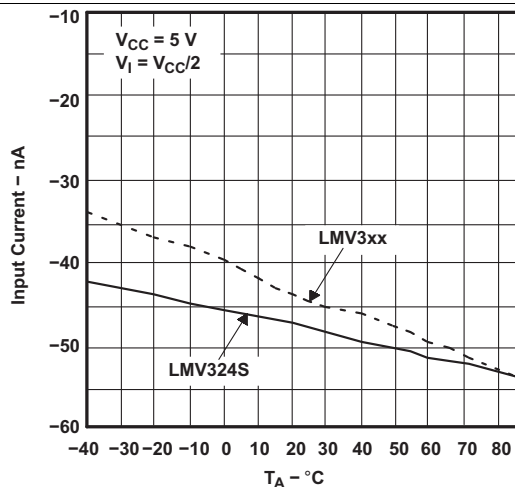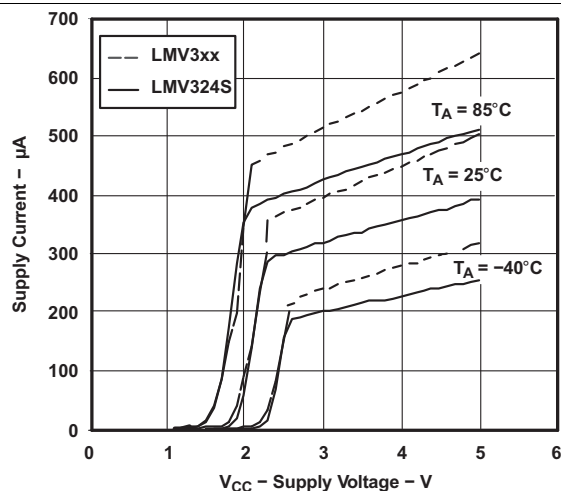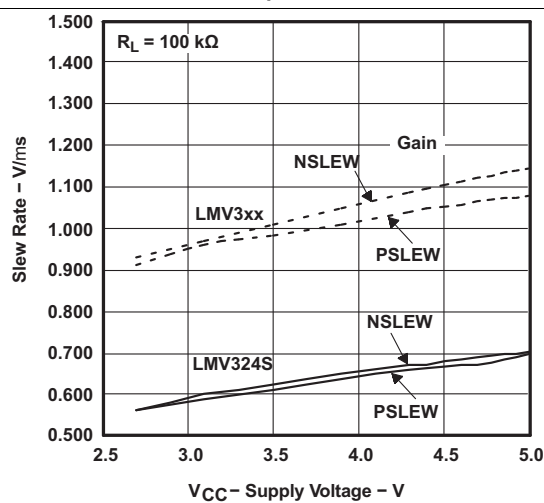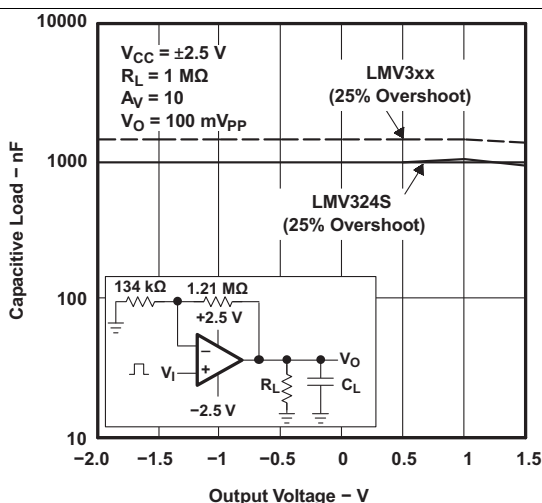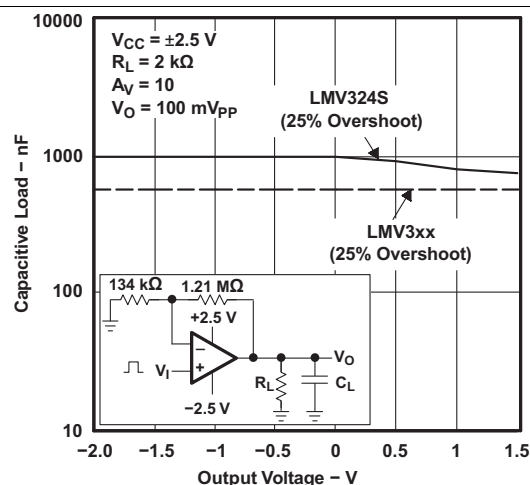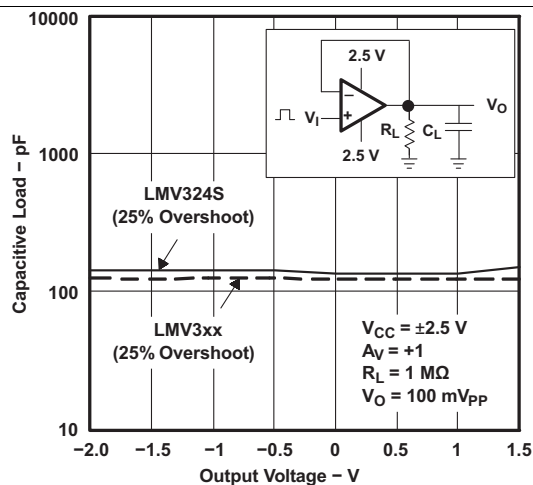
Typical Characteristics (continued)
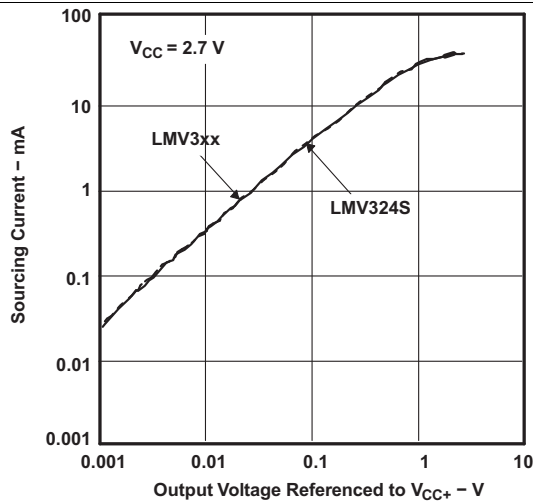
Figure 13. Source Current
vs Output Voltage
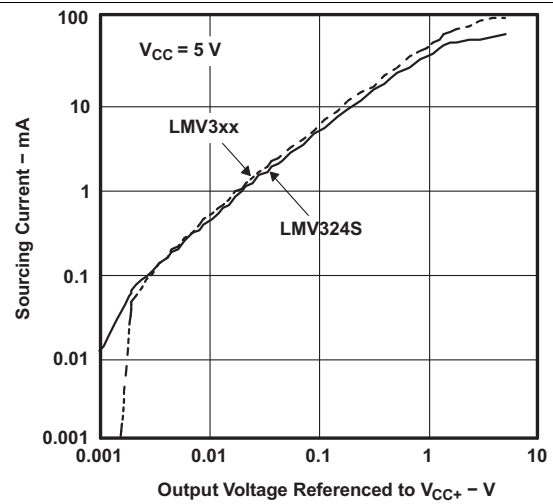
Figure 14. Source Current
vs Output Voltage
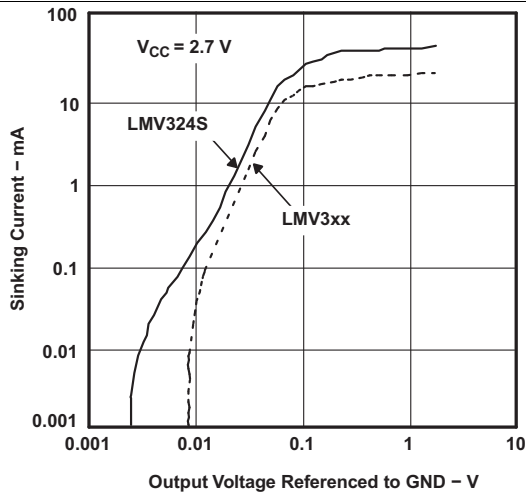
Figure 15. Sinking Current
vs Output Voltage
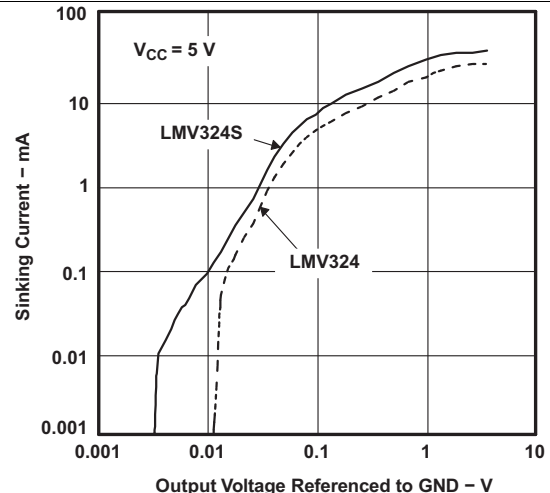
Figure 16. Sinking Current
vs Output Voltage
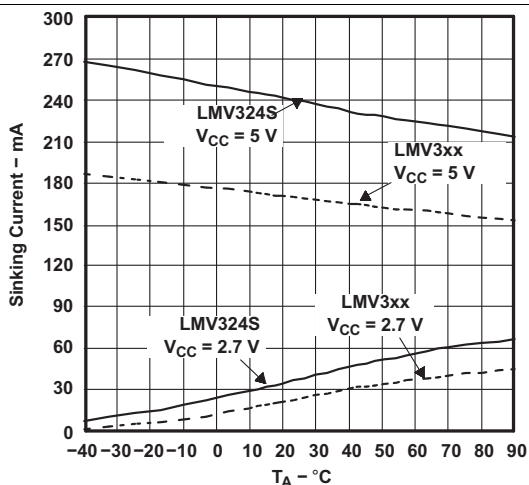
Figure 17. Short-Circuit Current
vs Temperature
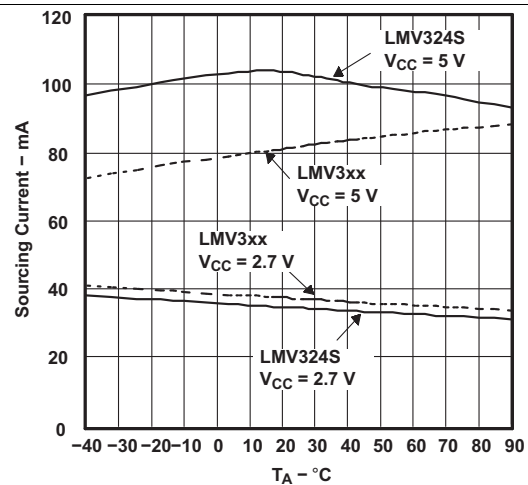
Figure 18. Short-Circuit Current
vs Temperature

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Characteristics (continued)
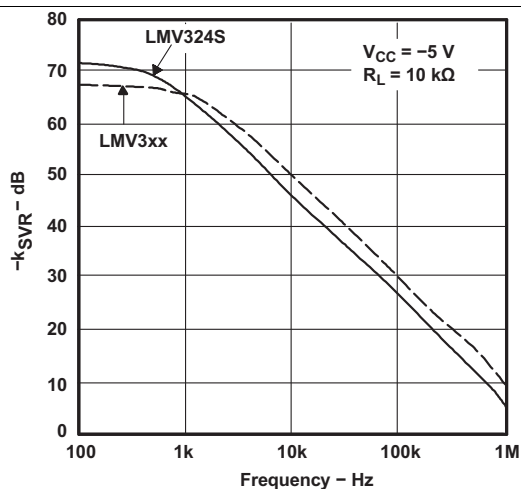
Figure 19. −k_SVR
vs Frequency
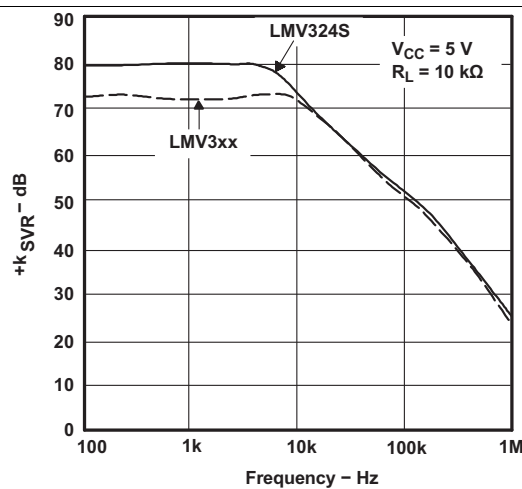
Figure 20. +k_SVR
vs Frequency
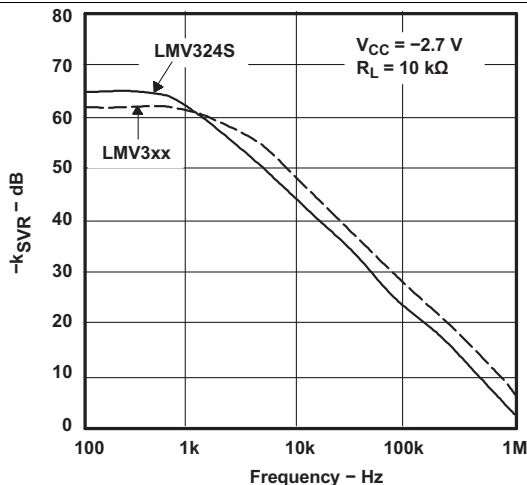
Figure 21. −k_SVR
vs Frequency
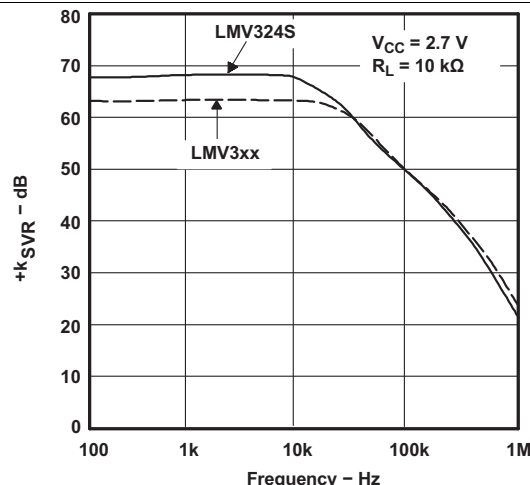
Figure 22. +k_SVR
vs Frequency
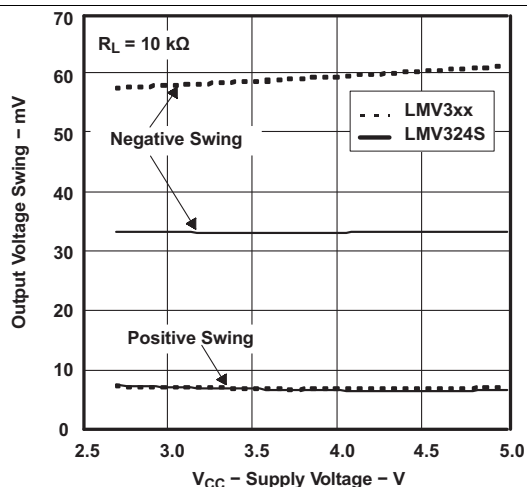
Figure 23. Output Voltage Swing From Rails
vs Supply Voltage
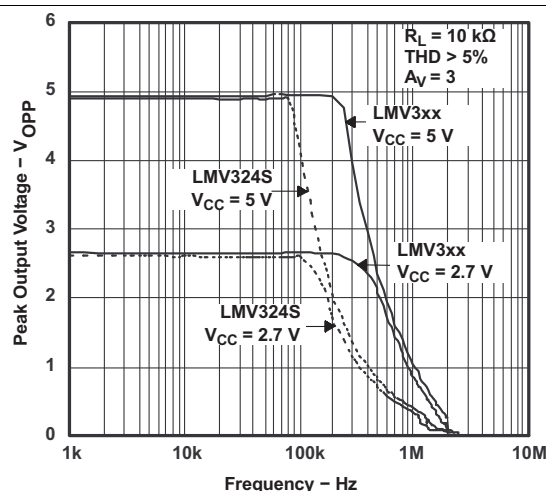
Figure 24. Output Voltage
vs Frequency

Submit Documentation Feedback   11

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Characteristics (continued)
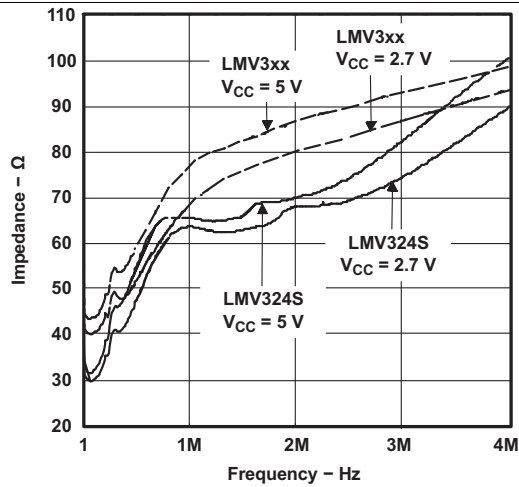
**Figure 25. Open-Loop Output Impedence
vs Frequency**
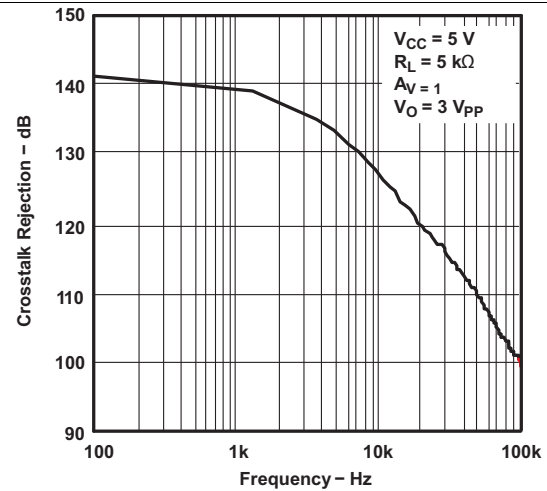
**Figure 26. Cross-Talk Rejection
vs Frequency**
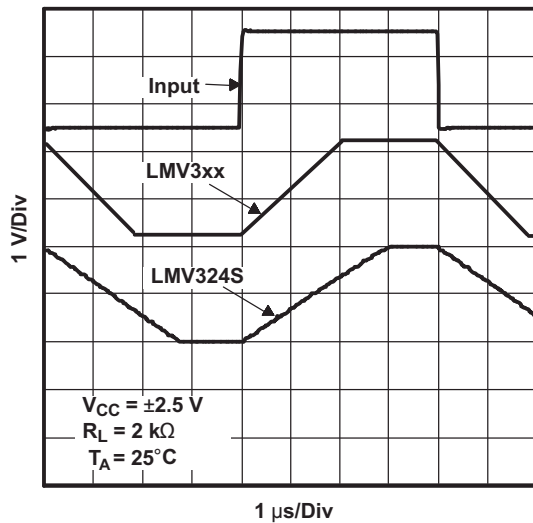
Figure 27. Noninverting Large-Signal Pulse Response
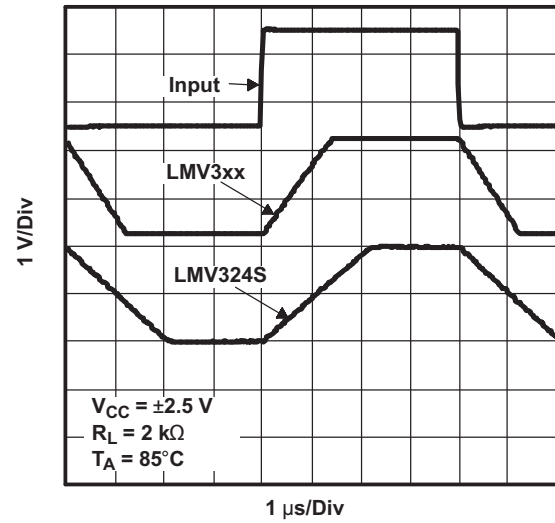
Figure 28. Noninverting Large-Signal Pulse Response
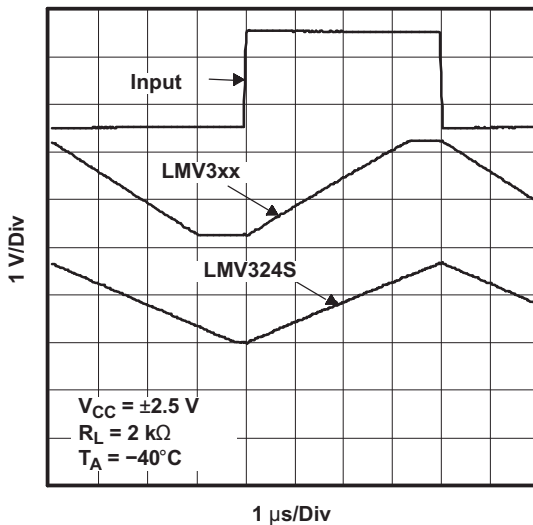
Figure 29. Noninverting Large-Signal Pulse Response
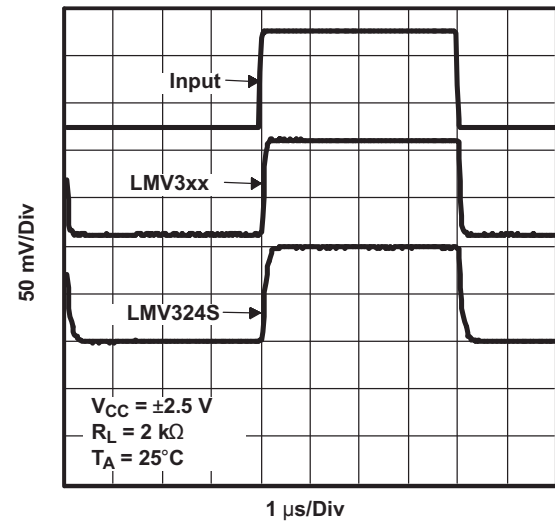
Figure 30. Noninverting Small-Signal Pulse Response

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Characteristics (continued)

$V_{CC} = \pm 2.5$ V
$R_L = 2$ kΩ
$T_A = 85°C$

1 µs/Div
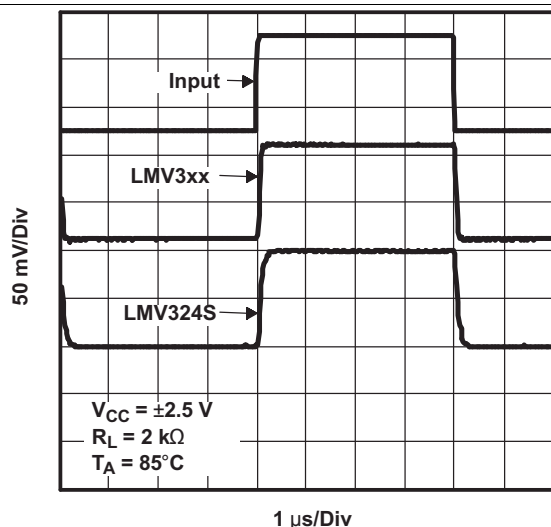
Figure 31. Noninverting Small-Signal Pulse Response

$V_{CC} = \pm 2.5$ V
$R_L = 2$ kΩ
$T_A = -40°C$

1 µs/Div
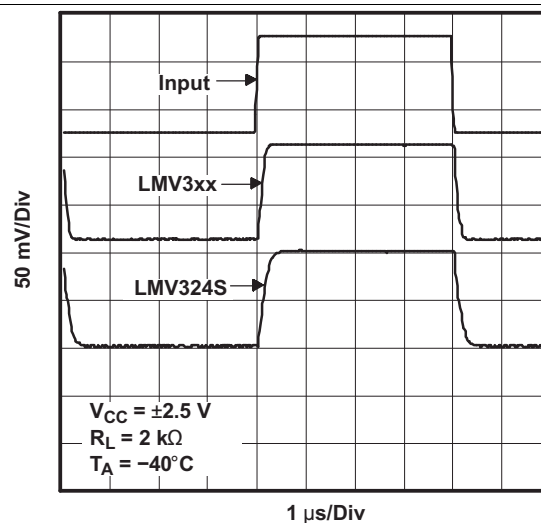
Figure 32. Noninverting Small-Signal Pulse Response

$V_{CC} = \pm 2.5$ V
$R_L = 2$ kΩ
$T_A = 25°C$

1 µs/Div
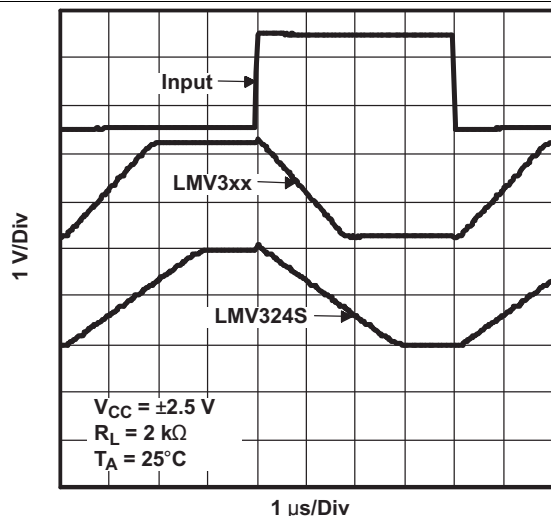
Figure 33. Inverting Large-Signal Pulse Response

$V_{CC} = \pm 2.5$ V
$R_L = 2$ kΩ
$T_A = 85°C$

1 µs/Div
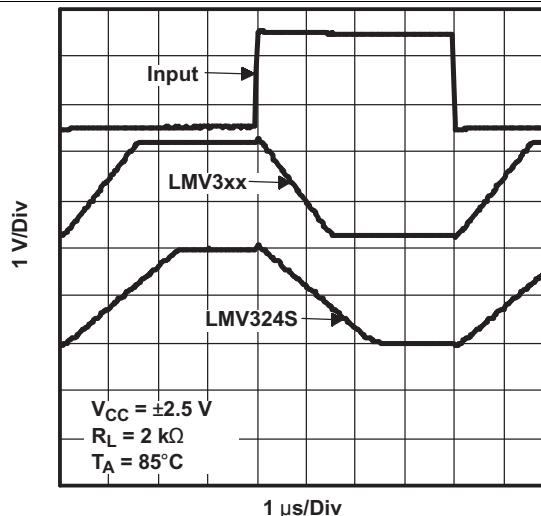
Figure 34. Inverting Large-Signal Pulse Response

$V_{CC} = \pm 2.5$ V
$R_L = 2$ kΩ
$T_A = -40°C$

1 µs/Div
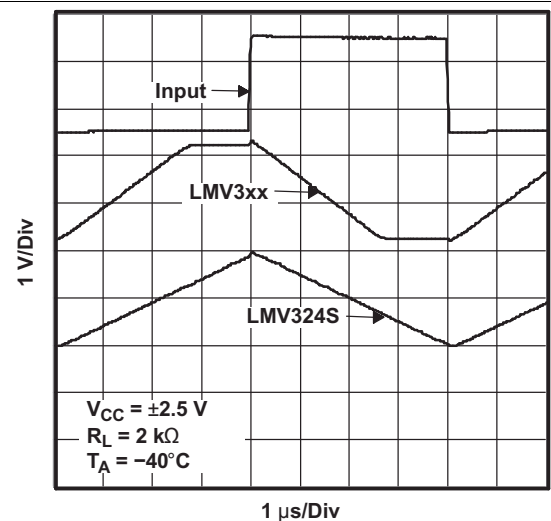
Figure 35. Inverting Large-Signal Pulse Response

$V_{CC} = \pm 2.5$ V
$R_L = 2$ kΩ
$T_A = 25°C$

1 µs/Div
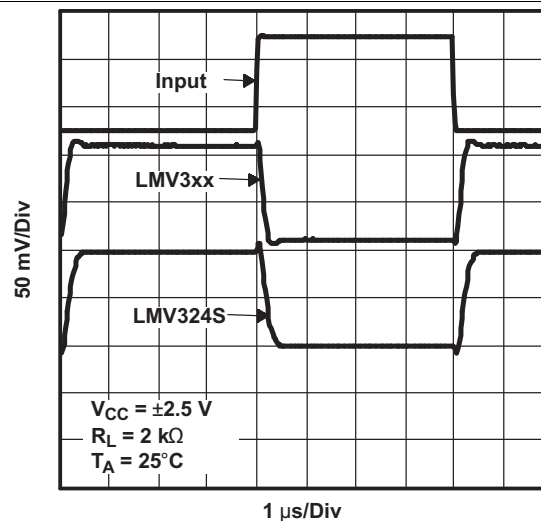
Figure 36. Inverting Small-Signal Pulse Response

Submit Documentation Feedback   13

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Characteristics (continued)
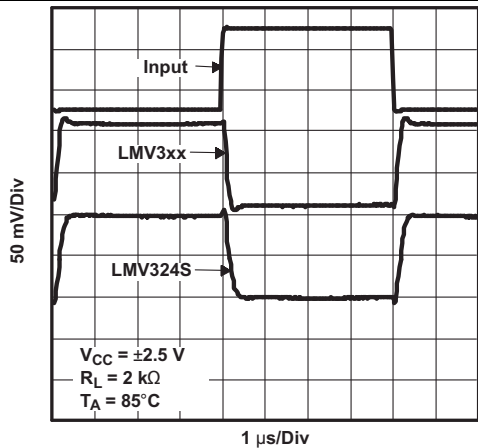
Figure 37. Inverting Small-Signal Pulse Response
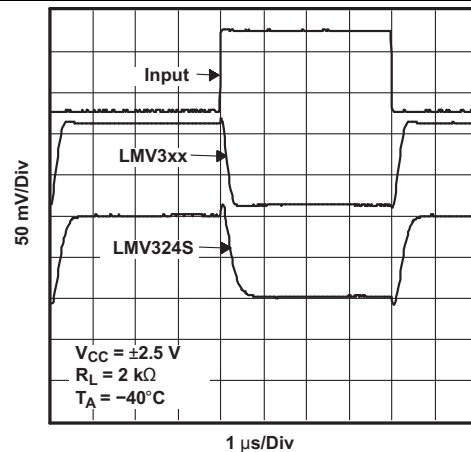
Figure 38. Inverting Small-Signal Pulse Response
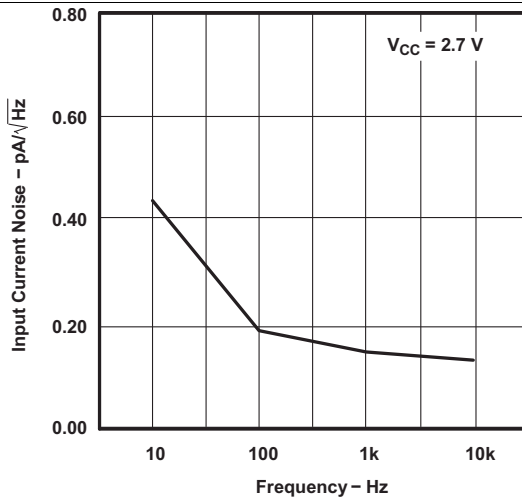
Figure 39. Input Current Noise
vs Frequency
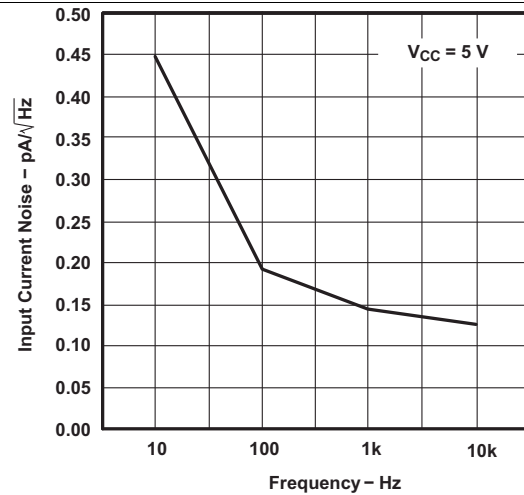
Figure 40. Input Current Noise
vs Frequency
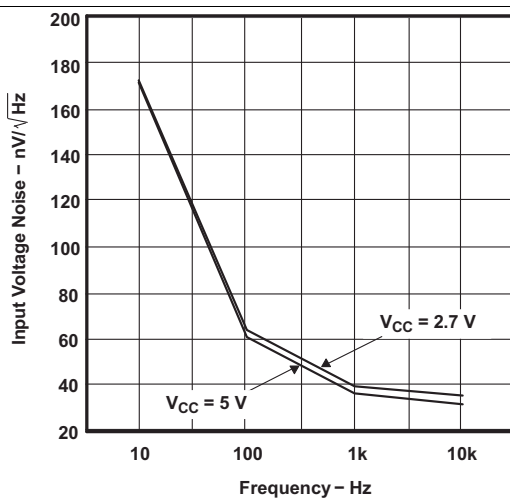
Figure 41. Input Voltage Noise
vs Frequency
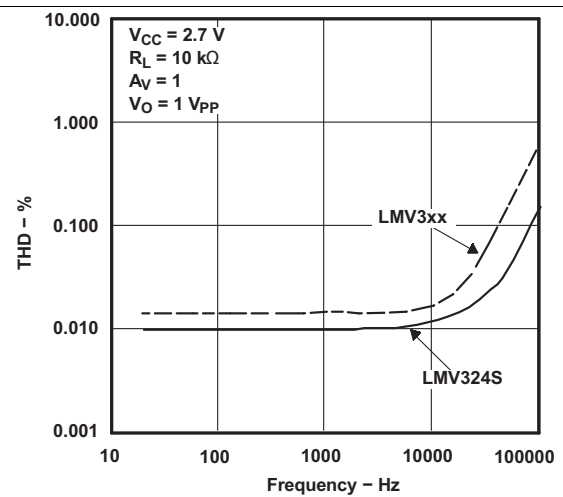
Figure 42. THD + N
vs Frequency

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Characteristics (continued)
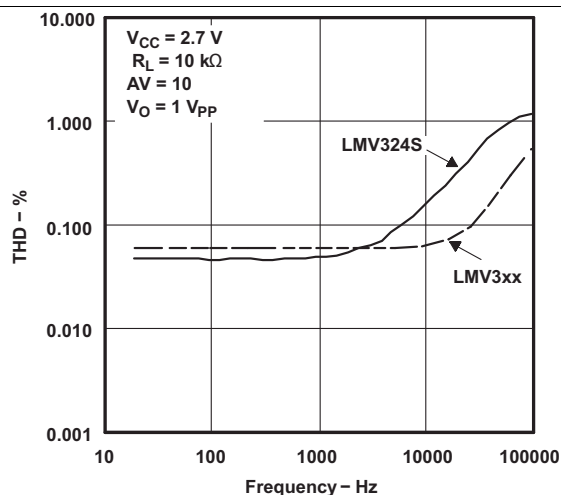
Figure 43. THD + N vs Frequency
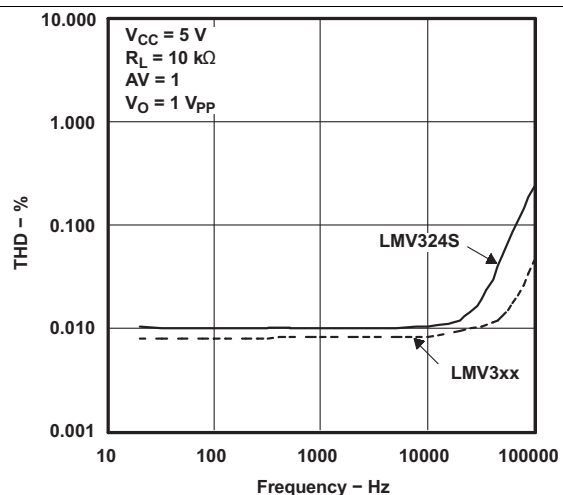
Figure 44. THD + N vs Frequency
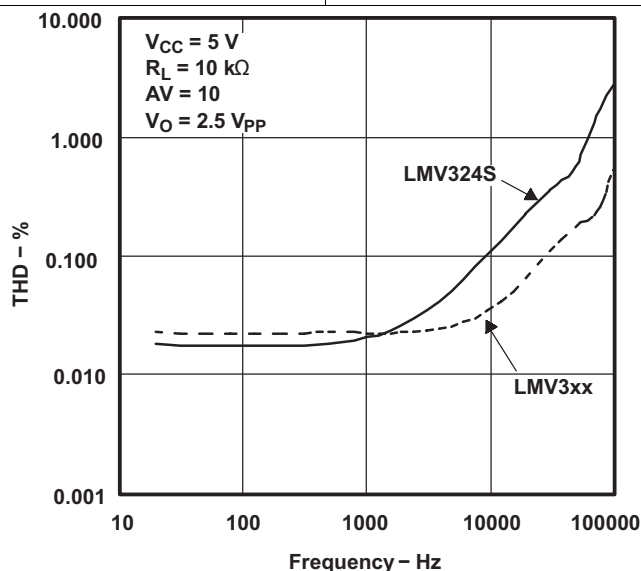
Figure 45. THD + N vs Frequency

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

8 Detailed Description

8.1 Overview

The LMV321, LMV358, LMV324, and LMV324S devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. The LMV324S device, which is a variation of the standard LMV324 device, includes a power-saving shutdown feature that reduces supply current when the amplifiers are not needed. Channels 1 and 2 together are put in shutdown, as are channels 3 and 4. While in shutdown, the outputs actively are pulled low.

The LMV321, LMV358, LMV324, and LMV324S devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/µs slew rate.

The LMV321 device is available in the ultra-small package, which is approximately one-half the size of the DBV (SOT-23) package. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

8.2 Functional Block Diagram

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*
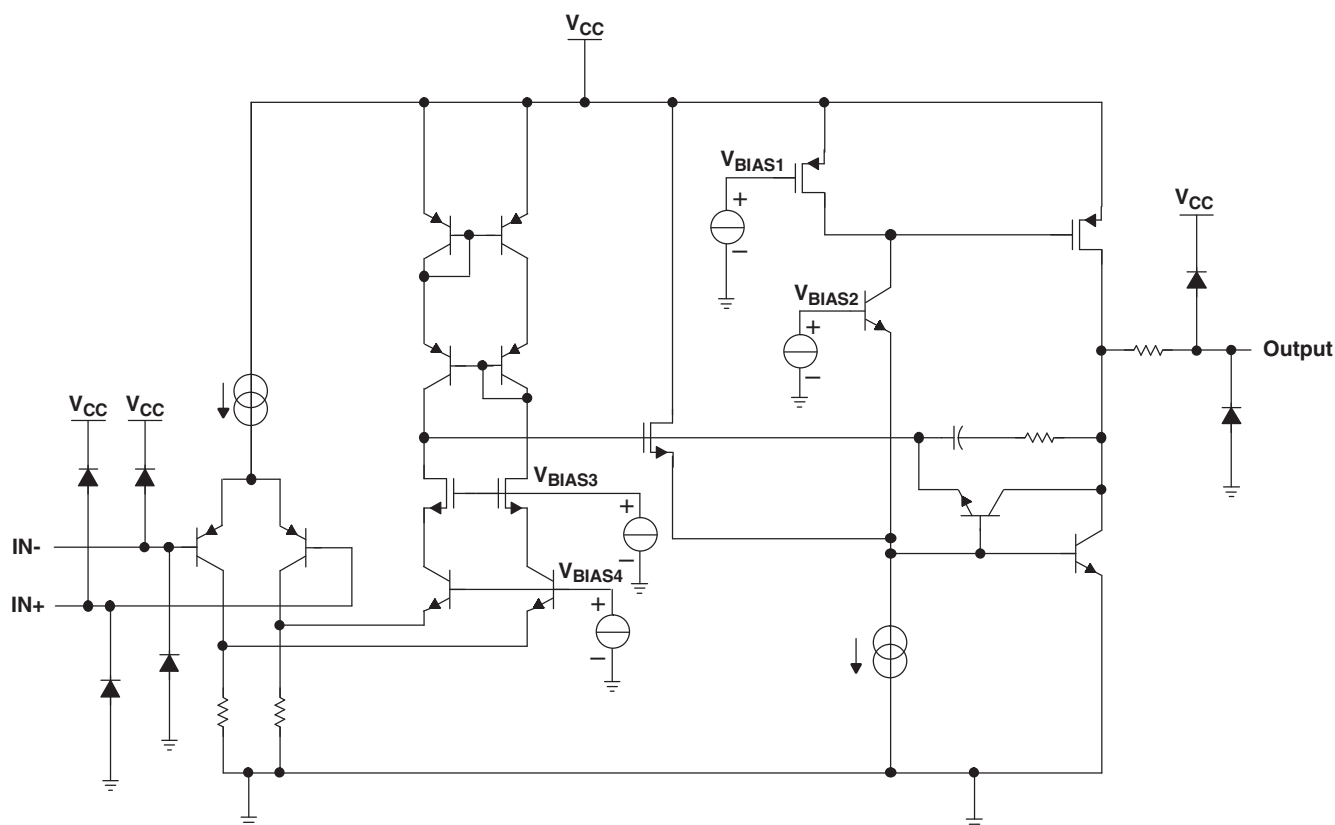
8.3   Feature Description

8.3.1   Operating Voltage

The LMV321, LMV358, LMV324, LMV324S devices are fully specified and ensured for operation from 2.7 V to 5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs.

8.3.2   Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The LMV321, LMV358, LMV324, LMV324S devices have a 1-MHz unity-gain bandwidth.

8.3.3   Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The LMV321, LMV358, LMV324, LMV324S devices have a 1-V/µs slew rate.

8.4   Device Functional Modes

The LMV321, LMV358, LMV324, LMV324S devices are powered on when the supply is connected. The LMV324S device, which is a variation of the standard LMV324 device, includes a power-saving shutdown feature that reduces supply current to a maximum of 5 µA per channel when the amplifiers are not needed. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

Some applications require differential signals. Figure 46 shows a simple circuit to convert a single-ended input of 0.5 to 2 V into differential output of ±1.5 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-}. Both V_{OUT+} and V_{OUT-} range from 0.5 to 2 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and V_{OUT-}. The LMV358 was used to build this circuit.
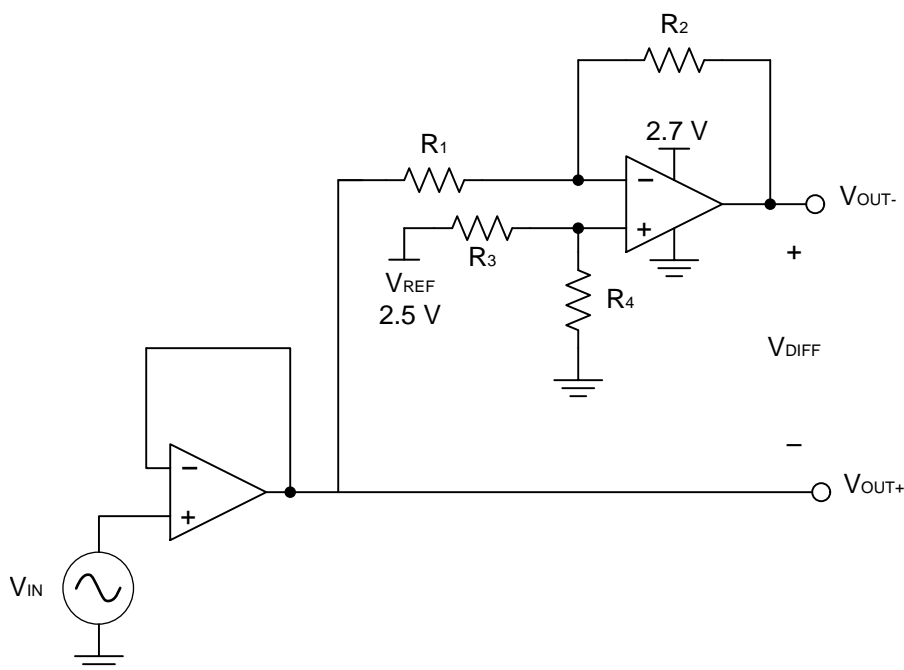
Figure 46. Schematic for Single-Ended Input to Differential Output Conversion

Typical Application (continued)

9.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.5 to 2 V
- Output differential: ±1.5 V

9.1.2 Detailed Design Procedure

The circuit in Figure 46 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see Equation 1). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

9.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because LMV358 has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

9.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

Typical Application (continued)

9.1.3 Application Curves

The measured transfer functions in Figure 47, Figure 48, and Figure 49 were generated by sweeping the input voltage from 0 V to 2.5 V. However, this design should only be used between 0.5 V and 2 V for optimum linearity.
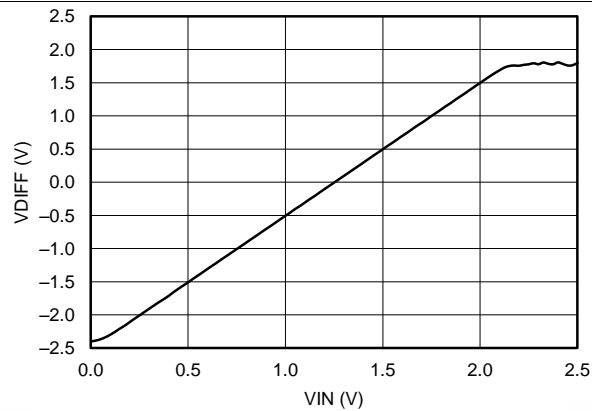
Figure 47. Differential Output Voltage vs Input Voltage
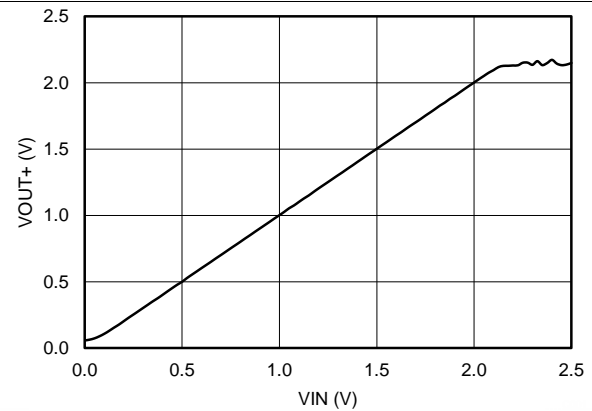
Figure 48. Positive Output Voltage Node vs Input Voltage
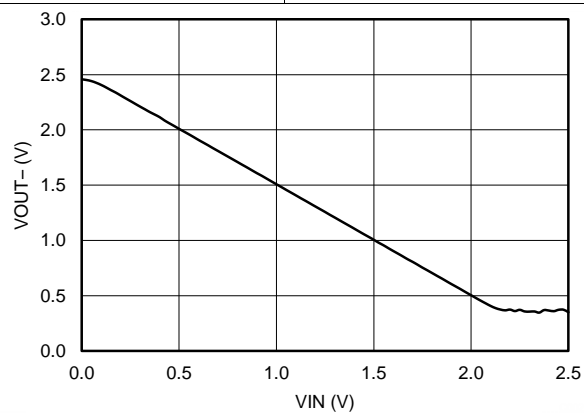
Figure 49. Positive Output Voltage Node vs Input Voltage

10   Power Supply Recommendations

The LMV321, LMV358, LMV324, LMV324S devices are specified for operation from 2.7 to 5 V; many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example
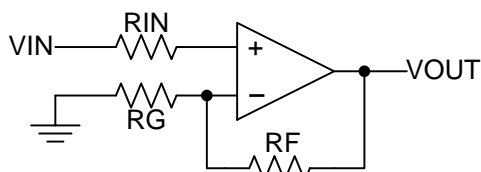
Figure 50. Operational Amplifier Schematic for Noninverting Configuration
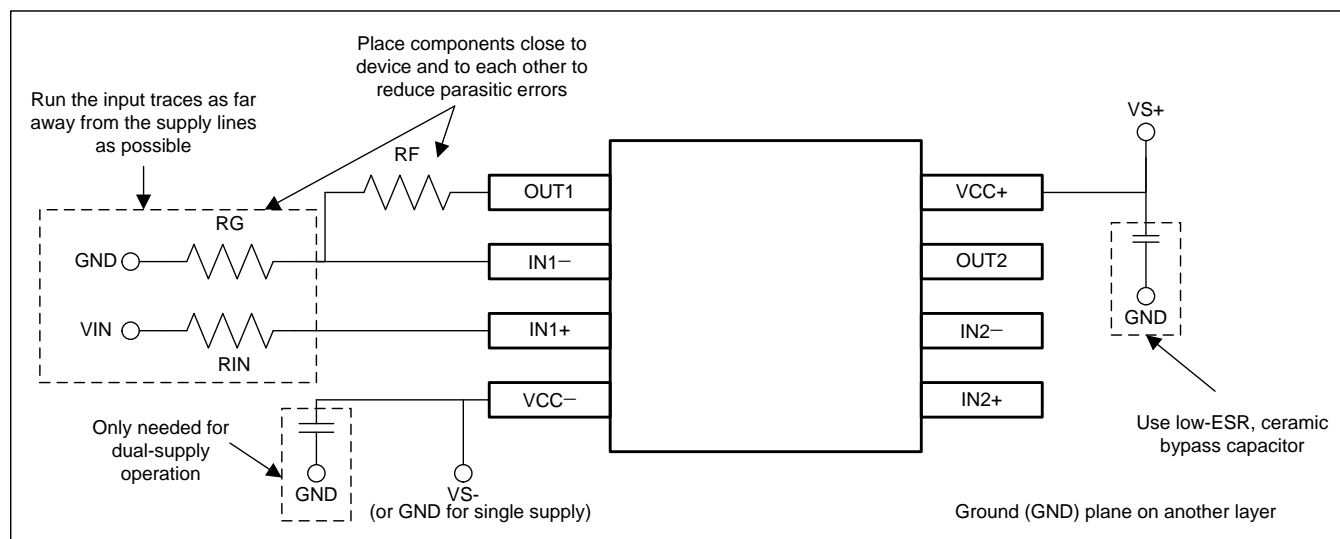
Figure 51. Operational Amplifier Board Layout for Noninverting Configuration

Product Folder Links: *LMV358 LMV321 LMV324 LMV324S*

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV321	Click here	Click here	Click here	Click here	Click here
LMV358	Click here	Click here	Click here	Click here	Click here
LMV324	Click here	Click here	Click here	Click here	Click here
LMV324S	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F ~ RC1K)	Samples
LMV321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F ~ RC1K)	Samples
LMV321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F ~ RC1K)	Samples
LMV321IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F ~ RC1K)	Samples
LMV321IDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F ~ RC1K)	Samples
LMV321IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F ~ RC1K)	Samples
LMV321IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R3C ~ R3F ~ R3O ~ R3R ~ R3Z)	Samples
LMV321IDCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(R3C ~ R3F ~ R3O ~ R3R ~ R3Z)	Samples
LMV321IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R3C ~ R3F ~ R3O ~ R3R ~ R3Z)	Samples
LMV321IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R3C ~ R3F ~ R3R)	Samples
LMV321IDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R3C ~ R3F ~ R3R)	Samples
LMV324ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	MV324I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV324IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324I	Samples
LMV324IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324I	Samples
LMV324QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV324QPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV324QPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV324QPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV358ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RA5R	Samples
LMV358IDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RA5R	Samples
LMV358IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R5B ~ R5Q ~ R5R)	Samples
LMV358IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R5B ~ R5Q ~ R5R)	Samples
LMV358IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	CU SN	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV358IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	CU SN	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples
LMV358QDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAHR	Samples
LMV358QDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAHR	Samples
LMV358QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples
LMV358QDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RHO ~ RHR)	Samples
LMV358QDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RHO ~ RHR)	Samples
LMV358QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples
LMV358QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
LMV324IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV358IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358QDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV358QDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
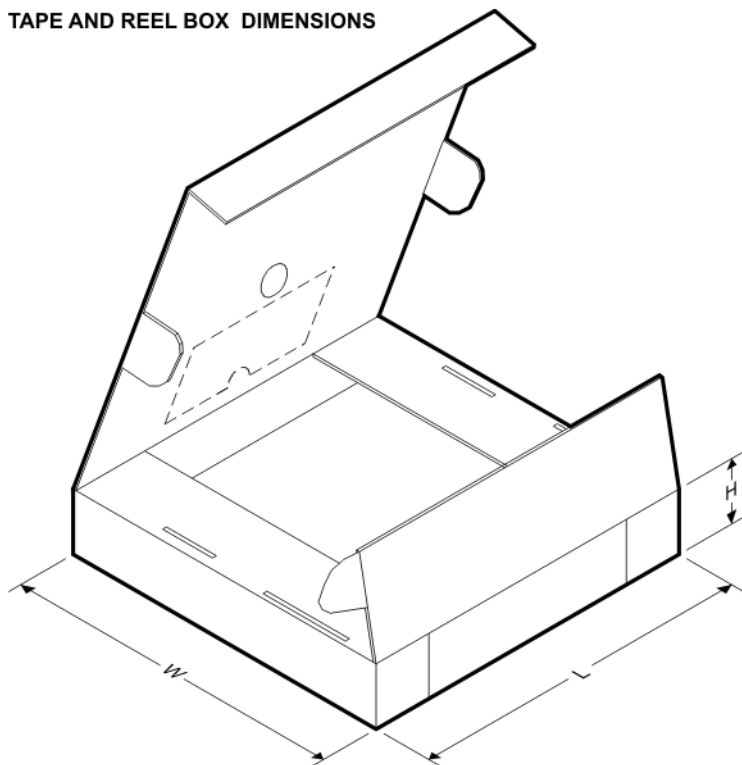
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV321IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV321IDCKR	SC70	DCK	5	3000	205.0	200.0	33.0
LMV321IDCKT	SC70	DCK	5	250	205.0	200.0	33.0
LMV321IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV324IDR	SOIC	D	14	2500	333.2	345.9	28.6

PACKAGE MATERIALS INFORMATION

TEXAS INSTRUMENTS

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV324IDR	SOIC	D	14	2500	367.0	367.0	38.0
LMV324IDR	SOIC	D	14	2500	364.0	364.0	27.0
LMV324IDRG4	SOIC	D	14	2500	333.2	345.9	28.6
LMV324IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV324IPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LMV324IPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV324QDR	SOIC	D	14	2500	367.0	367.0	38.0
LMV324QPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV358IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV358IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IDR	SOIC	D	8	2500	367.0	367.0	35.0
LMV358IDR	SOIC	D	8	2500	364.0	364.0	27.0
LMV358IDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IPWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LMV358IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LMV358IPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LMV358QDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV358QDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358QDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

5   4

2,40
1,80

1,40
1,10

Pin 1
Index Area

1   3

0,65   5X 0,30
0,15

1,30

⊕ 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

0,10 0,10

Seating Plane

0,10
0,00

4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

TEXAS
INSTRUMENTS
www.ti.com

DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x0,65

2x1,30

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

TEXAS
INSTRUMENTS
www.ti.com

DDU (R−PDSO−G8) PLASTIC SMALL−OUTLINE PACKAGE

0,50

0,25
0,17 ⊕ 0,08 Ⓜ

8   5

2,40
2,20   3,20
3,00

PIN 1
INDEX AREA

1   4

2,10
1,90

0,13 NOM

Gage Plane

0°−6°   0,12

0,35
0,20

0,90 MAX

0,10
0,00

Seating Plane

⌒ 0,10

4205140/A 05/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion.
         D.   Falls within JEDEC MO−187 variation CA.

TEXAS
INSTRUMENTS
www.ti.com

DDU (S−PDSO−G8)   PLASTIC SMALL OUTLINE PACKAGE (DIE UP)
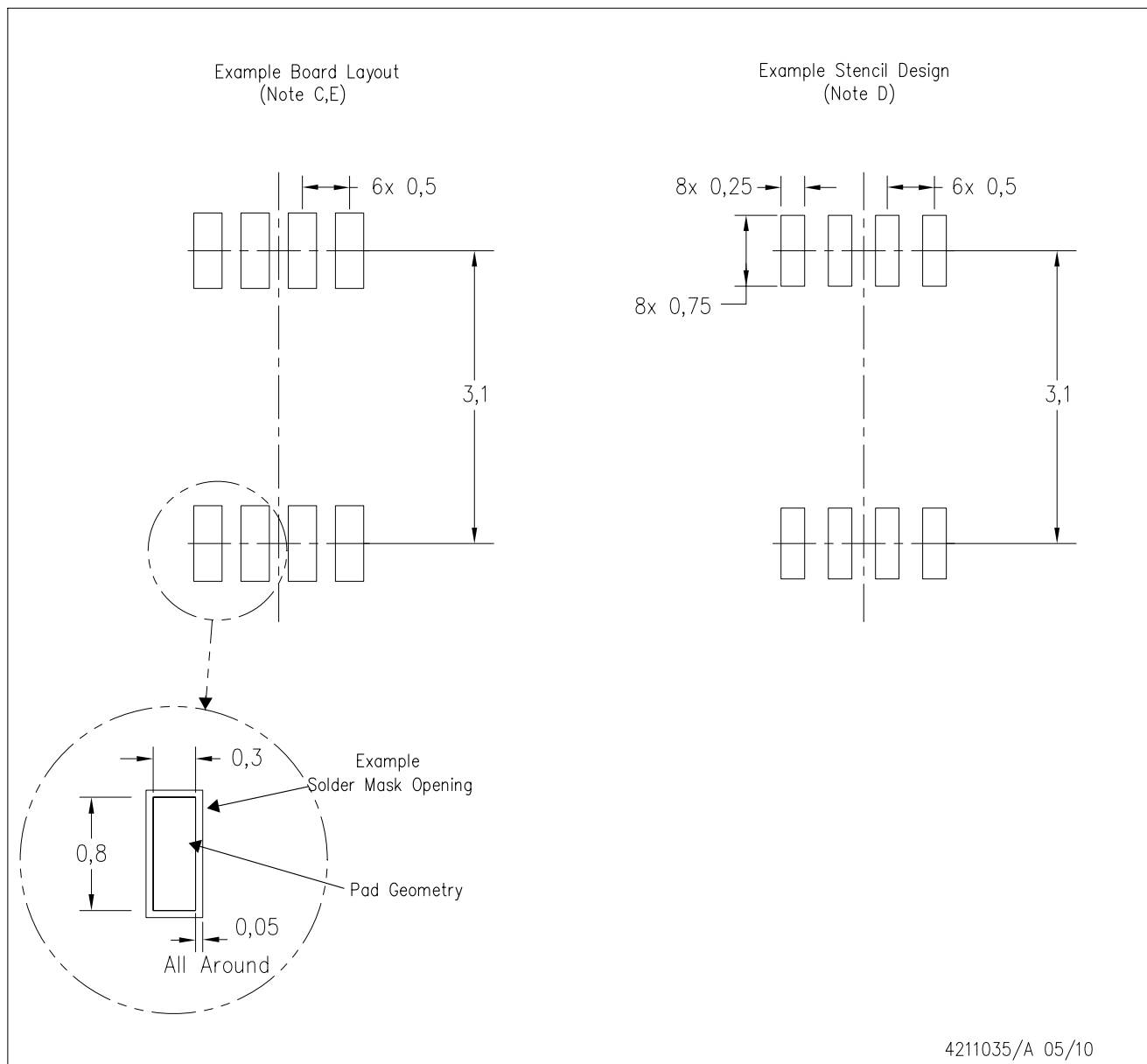
Example Board Layout
(Note C,E)

6x 0,5

3,1

Example Stencil Design
(Note D)

8x 0,25   6x 0,5

8x 0,75

3,1

0,3

Example
Solder Mask Opening

0,8

Pad Geometry

0,05
All Around

4211035/A 05/10

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**TEXAS
INSTRUMENTS**
www.ti.com

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
⬡C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⬡D

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      ⬡C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
      ⬡D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

14x1,50

12x1,27

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Publication IPC−7351 is recommended for alternate designs.
           D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
           E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS INSTRUMENTS
www.ti.com

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65 | 0,30 / 0,19   ⊕ | 0,10 Ⓜ

14   8

Ⓓ 4,50 / 4,30   6,60 / 6,20

1   7

5,10 / 4,90
Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane

◯ | 0,10

4040064−3/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
          Ⓒ   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
          Ⓓ   Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

![Texas Instruments logo] TEXAS INSTRUMENTS
www.ti.com

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

|←—12x0,65

5,60

Stencil Openings
(Note D)

|←—14x0,30
|←—12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
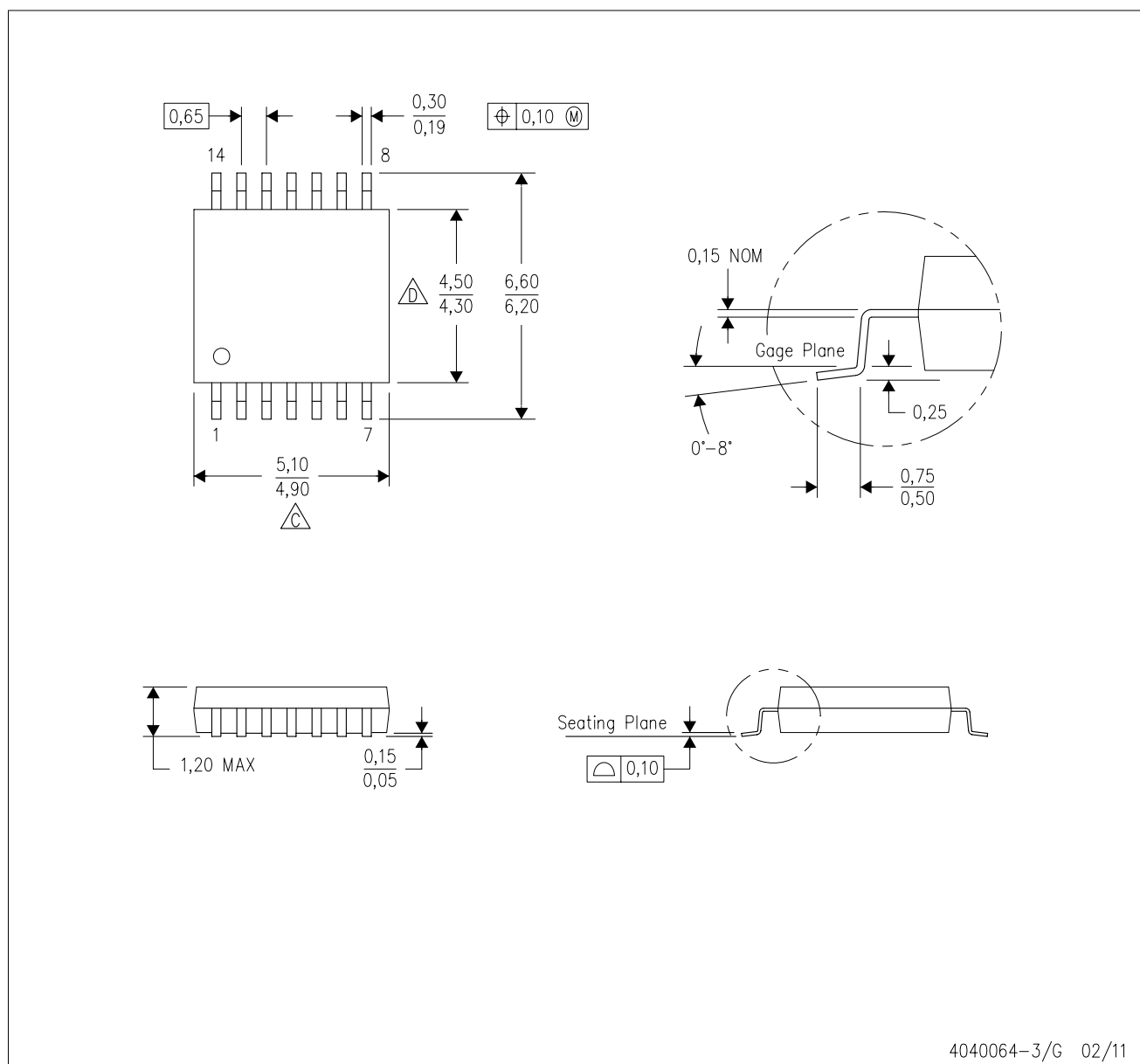(See Note E)

0,07
All Around

4211284−2/G 08/15

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE
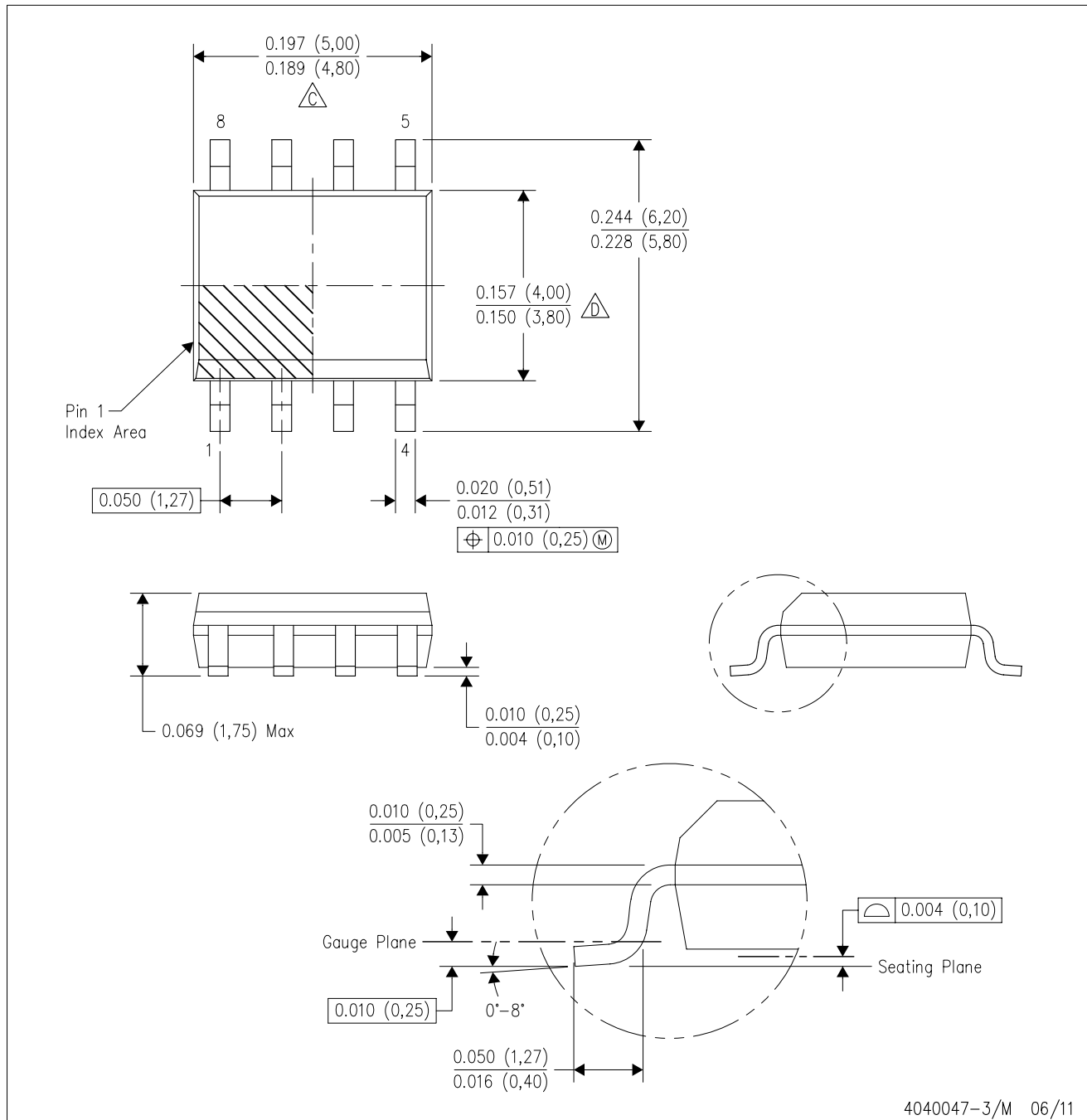
0.197 (5,00)
0.189 (4,80)
△C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   △D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.010 (0,25)
0.004 (0,10)

0.069 (1,75) Max

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      △C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
      △D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.

**TEXAS
INSTRUMENTS**
www.ti.com

D (R−PDSO−G8)   **PLASTIC SMALL OUTLINE**

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

8x1,50

6x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0,07

All Around

Example
Solder Mask Opening
(See Note E)

4211283−2/E   08/12

NOTES: A.   All linear dimensions are in millimeters.
             B.   This drawing is subject to change without notice.
             C.   Publication IPC−7351 is recommended for alternate designs.
             D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.   Customers should
                 contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
             E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**TEXAS
INSTRUMENTS**
www.ti.com

DBV (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

0,95   5X $\frac{0,50}{0,30}$ ⌖ 0,20 Ⓜ

5   4

$\frac{1,75}{1,45}$ $\frac{3,00}{2,60}$

Pin 1
Index Area
(Optional)

1   3

$\frac{3,05}{2,75}$

$\frac{0,22}{0,08}$

Gage Plane

0°−8°   0,25

$\frac{0,60}{0,30}$

1,45 MAX

$\frac{0,15}{0,00}$

Seating Plane

⌒ 0,10

4073253−4/N   12/14
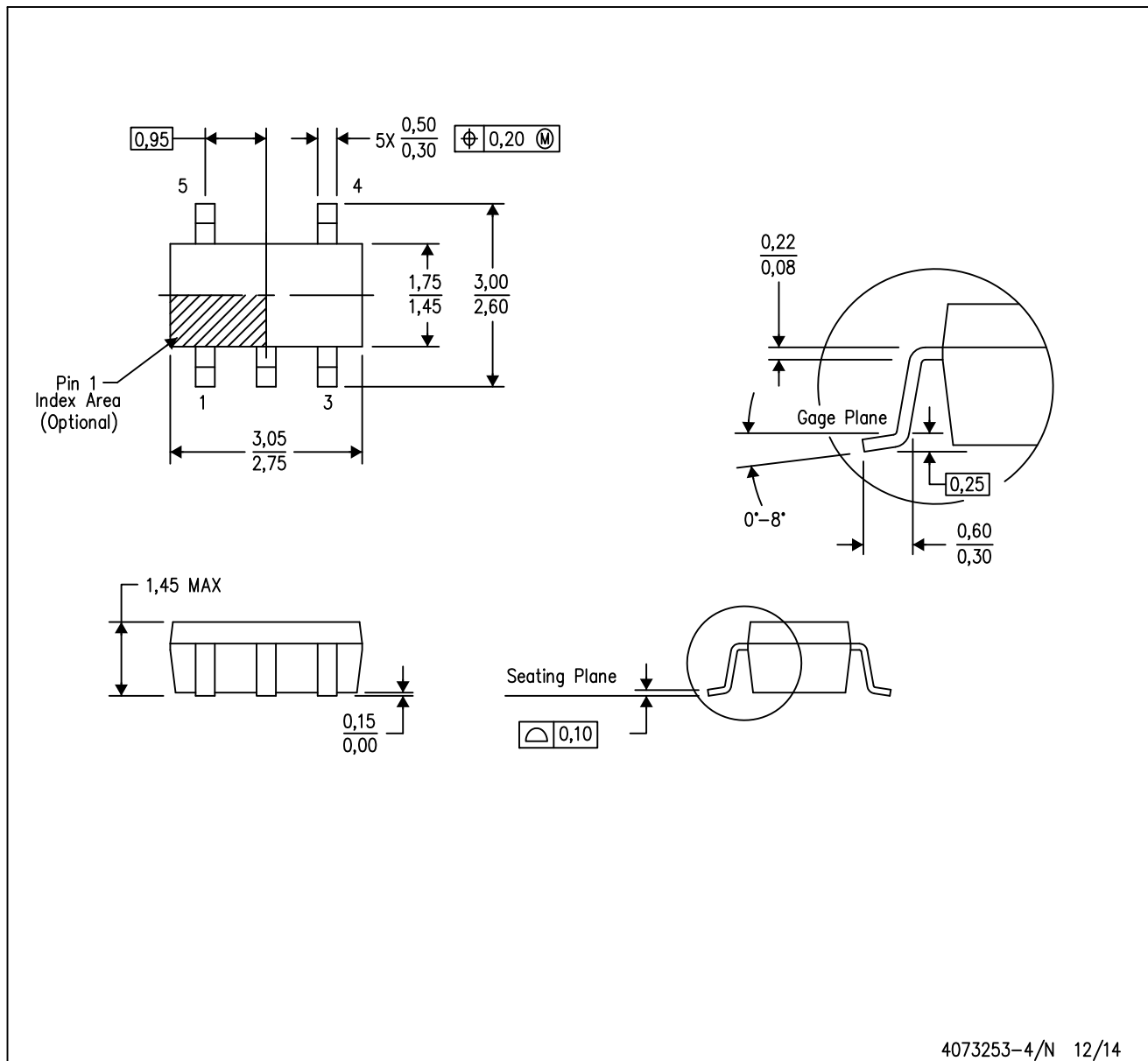
NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
          D.   Falls within JEDEC MO−178 Variation AA.

TEXAS
INSTRUMENTS
www.ti.com

DBV (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90

1,90

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−3/C 08/11

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D.   Publication IPC−7351 is recommended for alternate designs.
          E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
               metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

TEXAS INSTRUMENTS
www.ti.com

DGK (S−PDSO−G8) PLASTIC SMALL−OUTLINE PACKAGE

0,65

0,38
0,25

⊕ | 0,13 Ⓜ

8

5

D ▷ 3,10
2,90

5,05
4,75

1

4

C ▷
3,10
2,90

0,23
0,13

Gauge Plane

0°−8°

0,25

0,70
0,40

1,10 MAX

0,15
0,05

Seating Plane

◠ | 0,10

4073329/E 05/06

NOTES: A.   All linear dimensions are in millimeters.
  B.   This drawing is subject to change without notice.
  C ▷ Body length does not include mold flash, protrusions, or gate burrs.   Mold flash, protrusions, or gate burrs shall
        not exceed 0.15 per end.
  D ▷ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  E.   Falls within JEDEC MO−187 variation AA, except interlead flash.

TEXAS
INSTRUMENTS
www.ti.com

DGK (S–PDSO–G8)   PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

(0,65)TYP.

8   5

PKG
℄

(4,4)

1   4

PKG
℄

8X(0,45)   (0,65)TYP.

8X(1,45)

PKG
℄

(4,4)

PKG
℄

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

(0,45)

(1,45)

Pad Geometry
(See Note C)

(0,05)
All Around

4221236/A 11/13

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC–7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**TEXAS
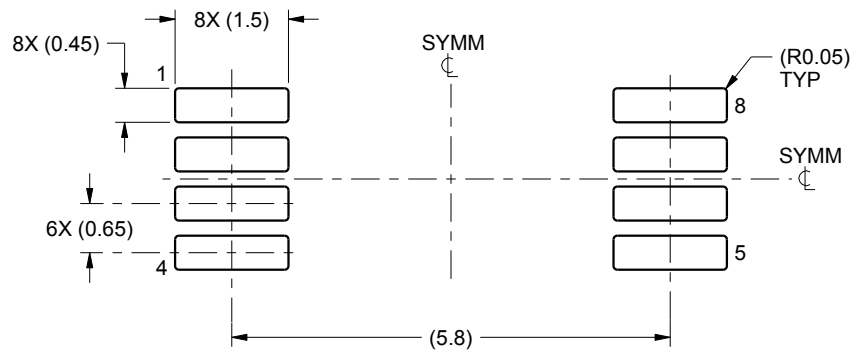INSTRUMENTS**
www.ti.com

4221848/A   02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
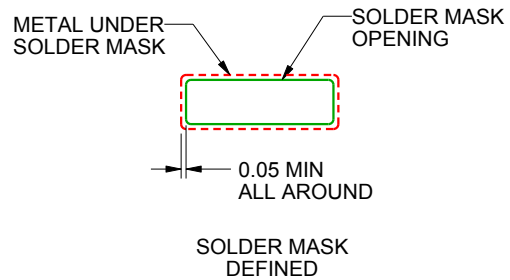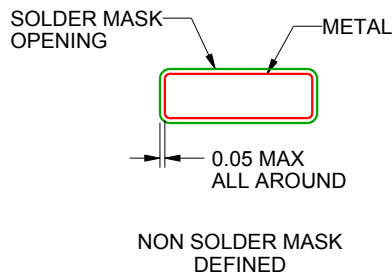5. Reference JEDEC registration MO-153, variation AA.

TEXAS INSTRUMENTS
www.ti.com

8X (0.45)

8X (1.5)

SYMM

(R0.05)
TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A   02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.5)

8X (0.45)

SYMM

(R0.05) TYP

1

8

SYMM

6X (0.65)

4

5

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A   02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

TEXAS INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.