



**IS25LP040E**

**IS25LP020E**

**IS25LP010E**

**IS25LP512E**

**IS25LP025E**

**IS25WP040E**

**IS25WP020E**

**IS25WP010E**

**IS25WP512E**

**IS25WP025E**

**4M/2M/1M/512K/256Kb**

**SERIAL FLASH MEMORY WITH 104MHZ MULTI I/O SPI &  
QPI INTERFACE**

**DATA SHEET**

## **4M/2M/1M/512K/256Kb**

**SERIAL FLASH MEMORY WITH 104MHZ MULTI I/O SPI & QPI INTERFACE**

### **FEATURES**

- **Industry Standard Serial Interface**

- IS25LP040E: 4Mbit/512Kbyte
- IS25WP040E: 4Mbit/512Kbyte
- IS25LP020E: 2Mbit/256Kbyte
- IS25WP020E: 2Mbit/256Kbyte
- IS25LP010E: 1Mbit/128Kbyte
- IS25WP010E: 1Mbit/128Kbyte
- IS25LP512E: 512Kbit/64Kbyte
- IS25WP512E: 512Kbit/64Kbyte
- IS25LP025E: 256Kbit/32Kbyte
- IS25WP025E: 256Kbit/32Kbyte
- 256 bytes per Programmable Page
- Supports standard SPI, Multi-I/O SPI, and QPI
- Supports Serial Flash Discoverable Parameters (SFDP)

- **High Performance Serial Flash (SPI)**

- 50MHz Normal and 104MHz Fast Read
- 416 MHz equivalent QPI
- Supports SPI Modes 0 and 3
- More than 100,000 Erase/Program Cycles
- More than 20-year Data Retention

- **Flexible & Efficient Memory Architecture**

- Chip Erase with Uniform Sector/Block Erase (4/32/64 Kbyte)
- Program 1 to 256 Bytes per Page
- Program/Erase Suspend & Resume
- Soft RESET & In-Band RESET

- **Efficient Read and Program modes**

- XIP Read Operation; Dual I/O & Quad IO Read with AX mode
- Continuous Read & Wrap Burst Read (8/16/32/64-Byte)
- Program Operation during Erase Suspend Mode

- **Low Power with Wide Temp. Ranges**

- Single Voltage Supply:  
IS25LP: 2.30V to 3.60V  
IS25WP: 1.70V to 1.95V
- 6 mA Active Read Current
- 17  $\mu$ A Standby Current
- 3  $\mu$ A Deep Power Down
- Temp Grades:  
Extended: -40°C to +105°C  
Auto Grade (A3): -40°C to +125°C

- **Advanced Security Protection**

- Software and Hardware Write Protection
- Power Supply Lock Protect
- 4x256-Byte Dedicated Security Area with OTP User-lockable Bits
- 128 bit Unique ID for Each Device (Call Factory)

- **Industry Standard Pin-out & Packages<sup>(1)</sup>**

- B = 8-pin SOIC 208mil (Call Factory)
- N = 8-pin SOIC 150mil
- D = 8-pin TSSOP (Call Factory)
- V = 8-pin VVSOP 150mil (Call Factory)
- K = 8-contact WSON 6x5mm (Call Factory)
- Y = 8-contact USON 2x3mm
- KGD (Call Factory)

Note:

1. Call Factory for other package



## **GENERAL DESCRIPTION**

The IS25LP/WP040E/020E/010E/512E/025E and Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 104MHz allow for equivalent clock rates of up to 416MHz (104MHz x 4) which equates to 52Mbytes/s of data throughput. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256-bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle instruction further reducing instruction times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

## **GLOSSARY**

### ***Standard SPI***

In this operation, a 4-wire SPI Interface is utilized, consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. Instructions are sent via the SI pin to encode instructions, addresses, or input data to the device on the rising edge of SCK. The SO pin is used to read data or to check the status of the device. This device supports SPI bus operation modes (0, 0) and (1, 1).

### ***Multi I/O SPI***

Multi-I/O operation utilizes an enhanced SPI protocol to allow the device to function with Dual Output, Dual Input and Output, Quad Output, and Quad Input and Output capability. Executing these instructions through SPI mode will achieve double or quadruple the transfer bandwidth for READ and PROGRAM operations.

### ***QPI***

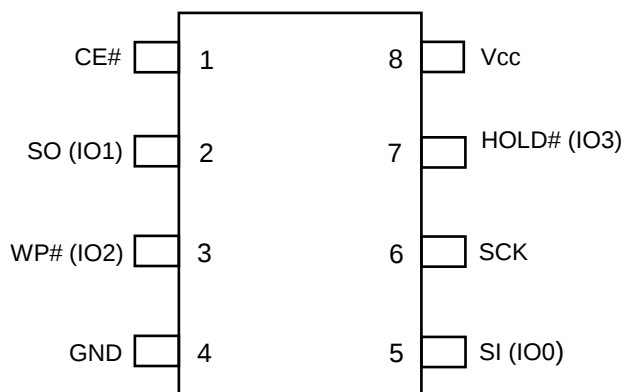
The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the enter QPI (35h) instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four I/O pins to input the instruction code thus requiring only two serial clocks. This can significantly reduce the SPI instruction overhead and improve system performance. Only QPI mode or SPI/Dual/Quad mode can be active at any given time. Enter QPI (35h) and Exit QPI (F5h) instructions are used to switch between these two modes, regardless of the non-volatile Quad Enable (QE) bit status in the Status Register. Power Reset or Software Reset will return the device into the standard SPI mode. SI and SO pins become bidirectional I/O0 and I/O1, and WP# and HOLD# pins become I/O2 and I/O3 respectively during QPI mode.

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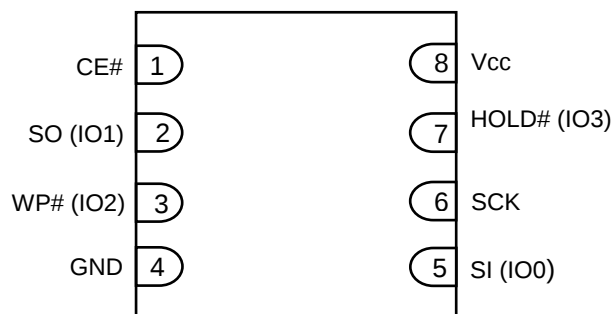
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## 1. PIN CONFIGURATION



8-pin SOIC 208mil (Package: B)  
 8-pin SOIC 150mil (Package: N)  
 8-pin TSSOP (Package: D)  
 8-pin VVSOP 150mil (Package: V)

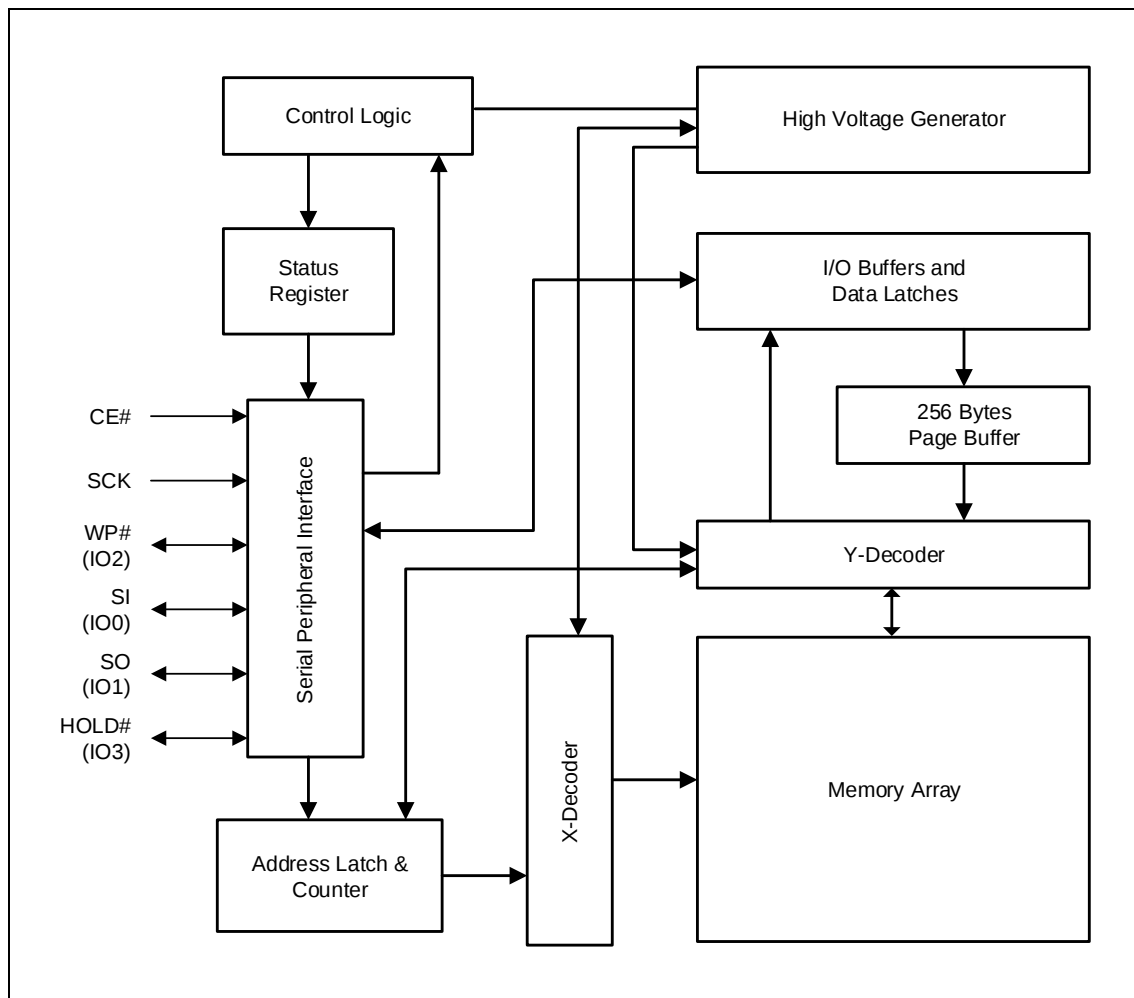


8-pin USON 2x3mm (Package: Y)  
 8-pin WSON 6x5mm (Package: K)

## 2. PIN DESCRIPTIONS

| SYMBOL                | TYPE         | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CE#                   | INPUT        | <p><b>Chip Enable:</b> The Chip Enable (CE#) pin enables and disables the devices operation. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the devices non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state.</p> <p>When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted.</p> <p>Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.</p>                                 |
| SI (IO0),<br>SO (IO1) | INPUT/OUTPUT | <p><b>Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):</b></p> <p>This device supports standard SPI, Dual SPI, and Quad SPI operation. Standard SPI instructions use the unidirectional SI (Serial Input) pin to write instructions, addresses, or data to the device on the rising edge of the Serial Clock (SCK). Standard SPI also uses the unidirectional SO (Serial Output) to read data or status from the device on the falling edge of the serial clock (SCK).</p> <p>In Dual and Quad SPI mode, SI and SO become bidirectional IO pins to write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) and read data or status from the device on the falling edge of SCK. Quad SPI instructions use the WP# and HOLD# pins as IO2 and IO3 respectively.</p> |
| WP# (IO2)             | INPUT/OUTPUT | <p><b>Write Protect/Serial Data IO (IO2):</b> The WP# pin protects the Status Register from being written in conjunction with the SRWD bit. When the SRWD is set to "1" and the WP# is pulled low, the Status Register bits (SRWD, QE, BP3, BP2, BP1, BP0) are write-protected and vice-versa for WP# high. When the SRWD is set to "0", the Status Register is not write-protected regardless of WP# state.</p> <p>When the QE bit is set to "1", the WP# pin (Write Protect) function is not available since this pin is used for IO2.</p>                                                                                                                                                                                                                                                                               |
| HOLD# (IO3)           | INPUT/OUTPUT | <p><b>Hold/Serial Data IO (IO3):</b> Pauses serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register is set to "1", HOLD# pin is not available since it becomes IO3.</p> <p>The HOLD# pin allows the device to be paused while it is selected. The HOLD# pin is active low. When HOLD# is in a low state, and CE# is low, the SO pin will be at high impedance.</p> <p>Device operation can resume when HOLD# pin is brought to a high state. When the QE bit of Status Register is set for Quad I/O, the HOLD# pin function is not available and becomes IO3 for Multi-I/O SPI mode.</p>                                                                                                                                                                       |
| SCK                   | INPUT        | <b>Serial Data Clock:</b> Synchronized Clock for input and output timing operations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Vcc                   | POWER        | <b>Power:</b> Device Core Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| GND                   | GROUND       | <b>Ground:</b> Connect to ground when referenced to Vcc                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| NC                    | Unused       | <b>NC:</b> Pins labeled "NC" stand for "No Connect". Not internally connected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3. BLOCK DIAGRAM



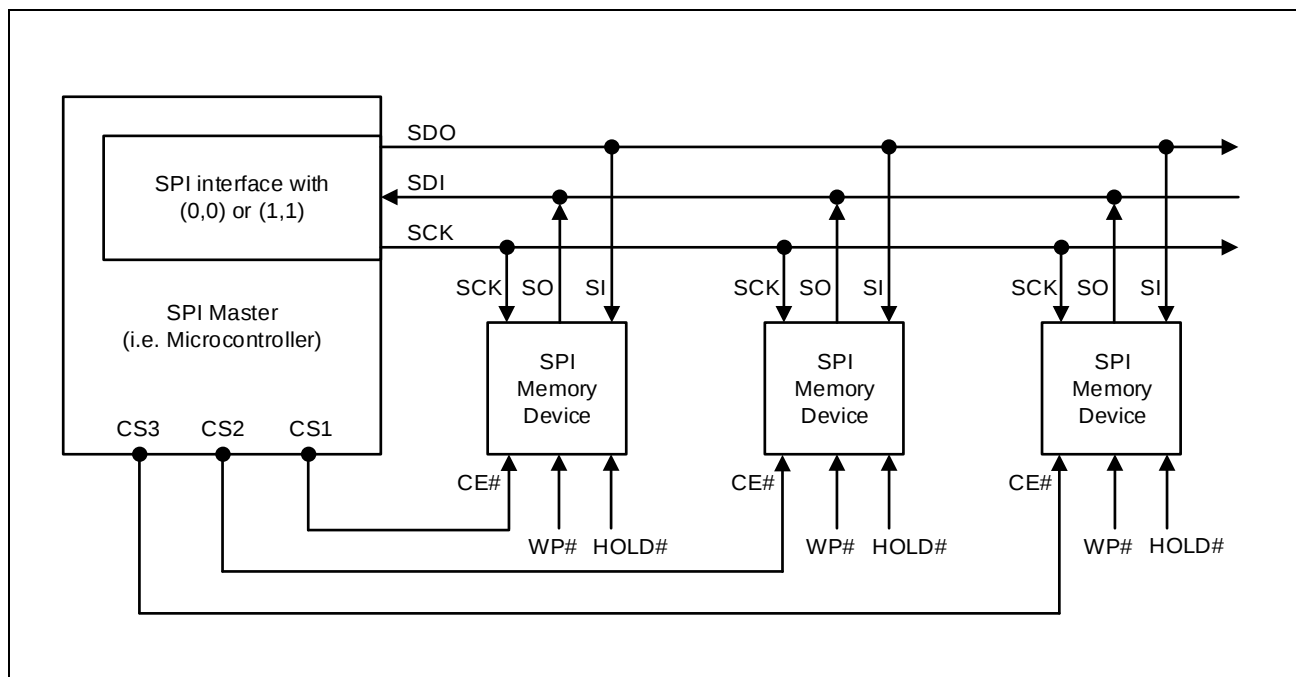
## 4. SPI MODES DESCRIPTION

Multiple IS25LP/WP040E/020E/010E/512E/025E devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)  
 Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at “0” (SCK = 0) for Mode 0 and the clock remains at “1” (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

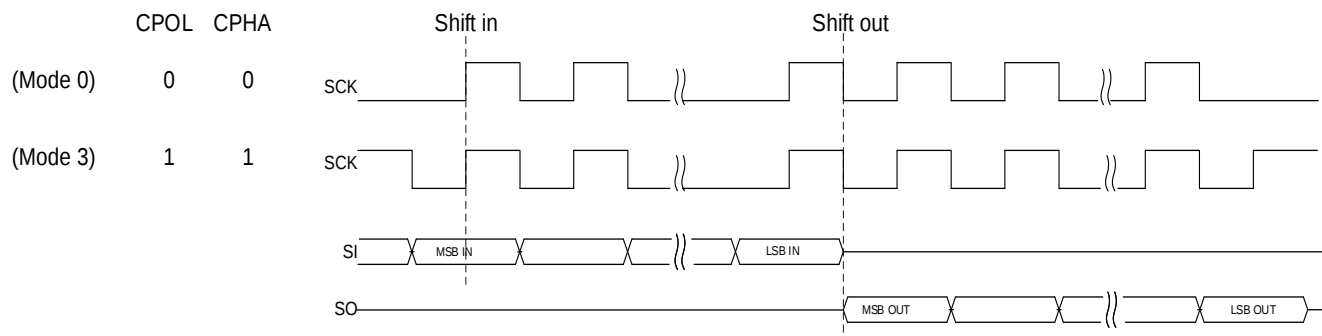
**Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)**



### Notes:

1. The Write Protect (WP#) and Hold (HOLD#) signals should be driven high or low as necessary.
2. SI and SO pins become bidirectional IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3 respectively during Multi-IO mode.

**Figure 4.2 SPI Mode Support**



## 5. SYSTEM CONFIGURATION

The memory array of IS25LP/WP512E/025E is divided into uniform 4Kbyte sectors or uniform 32Kbyte blocks (a block consists of eight adjacent sectors). The memory array of IS25LP/WP040E/020E/010E is divided into uniform 4Kbyte sectors or uniform 32/64Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

**Note: Optional 1Mb device (Option C) is also divided into uniform 4Kbyte sectors or uniform 32Kbyte blocks.**

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is protected.

### 5.1 BLOCK/SECTOR ADDRESSES

**Table 5.1 Block/Sector Addresses of IS25LP/WP0512E/025E**

| Memory Density |       | Block No. (32Kbyte) | Sector No. | Sector Size (Kbyte) | Address Range     |
|----------------|-------|---------------------|------------|---------------------|-------------------|
| 256Kb          | 512Kb | Block 0             | Sector 0   | 4                   | 000000h - 000FFFh |
|                |       |                     | Sector 1   | 4                   | 001000h - 001FFFh |
|                |       |                     | :          | :                   | :                 |
|                |       |                     | Sector 7   | 4                   | 007000h - 007FFFh |
| Block 1        |       | Sector 8            | 4          | 008000h - 008FFFh   |                   |
|                |       | Sector 9            | 4          | 009000h - 009FFFh   |                   |
|                |       | :                   | :          | :                   |                   |
|                |       | Sector 15           | 4          | 00F000h - 00FFFFh   |                   |

**Table 5.2 Block/Sector Addresses of IS25LP/WP040E/020E/010E**

| Memory Density     |     |     | Block No.<br>(64Kbyte) | Block No.<br>(32Kbyte) | Sector No. | Sector Size<br>(Kbyte) | Address Range     |
|--------------------|-----|-----|------------------------|------------------------|------------|------------------------|-------------------|
| 1Mb <sup>(1)</sup> | 2Mb | 4Mb | Block 0                | Block 0                | Sector 0   | 4                      | 000000h - 000FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 1                | Block 1                | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 15  | 4                      | 00F000h - 00FFFFh |
|                    |     |     | Block 2                | Block 2                | Sector 16  | 4                      | 010000h - 010FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 3                | Block 3                | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 31  | 4                      | 01F000h - 01FFFFh |
|                    |     |     | Block 4                | Block 4                | Sector 32  | 4                      | 020000h - 020FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 5                | Block 5                | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 47  | 4                      | 02F000h - 02FFFFh |
|                    |     |     | Block 6                | Block 6                | Sector 48  | 4                      | 030000h - 030FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 7                | Block 7                | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 63  | 4                      | 03F000h - 03FFFFh |
|                    |     |     | Block 8                | Block 8                | Sector 64  | 4                      | 040000h - 040FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 9                | Block 9                | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 79  | 4                      | 04F000h - 04FFFFh |
|                    |     |     | Block 10               | Block 10               | Sector 80  | 4                      | 050000h - 050FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 11               | Block 11               | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 95  | 4                      | 05F000h - 05FFFFh |
|                    |     |     | Block 12               | Block 12               | Sector 96  | 4                      | 060000h - 060FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 13               | Block 13               | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 111 | 4                      | 06F000h - 06FFFFh |
|                    |     |     | Block 14               | Block 14               | Sector 112 | 4                      | 070000h - 070FFFh |
|                    |     |     |                        |                        | :          | :                      | :                 |
|                    |     |     | Block 15               | Block 15               | :          | :                      | :                 |
|                    |     |     |                        |                        | Sector 127 | 4                      | 07F000h - 07FFFFh |

Note: Optional 1Mb device (Option C) is divided into uniform 4Kbyte sectors or uniform 32Kbyte blocks like 512Kb. Then both D8h and 52h commands are for 32KB Block Erase operation .

## 5.2 SERIAL FLASH DISCOVERABLE PARAMETERS

The Serial Flash Discoverable Parameters (SFDP) standard defines the structure of the SFDP database within the memory device. SFDP is the standard of JEDEC JESD216.

The JEDEC-defined header with Parameter ID FF00h and related Basic Parameter Table is mandatory. Additional parameter headers and tables are optional.

**Table 5.2 Signature and Parameter Identification Data Values**

| Description                               |       | Address<br>(Byte) | Address<br>(Bit) | Data |
|-------------------------------------------|-------|-------------------|------------------|------|
| SFDP Signature                            |       | 00h               | 7:0              | 53h  |
|                                           |       | 01h               | 15:8             | 46h  |
|                                           |       | 02h               | 23:16            | 44h  |
|                                           |       | 03h               | 31:24            | 50h  |
| SFDP Revision                             | Minor | 04h               | 7:0              | 06h  |
|                                           | Major | 05h               | 15:8             | 01h  |
| Number of Parameter Headers (NPH)         |       | 06h               | 23:16            | 00h  |
| Unused                                    |       | 07h               | 31:24            | FFh  |
| Parameter ID LSB                          |       | 08h               | 7:0              | 00h  |
| Parameter Minor Revision                  |       | 09h               | 15:8             | 06h  |
| Parameter Major Revision                  |       | 0Ah               | 23:16            | 01h  |
| Parameter Table Length (in DWPRDs)        |       | 0Bh               | 31:24            | 10h  |
| Basic Flash Parameter Table Pointer (PTP) |       | 0Ch               | 7:0              | 30h  |
|                                           |       | 0Dh               | 15:8             | 00h  |
|                                           |       | 0Eh               | 23:16            | 00h  |
| Parameter ID MSB                          |       | 0Fh               | 31:24            | FFh  |

**Table 5.3 JEDEC Basic Flash Parameter Table**

| Description                                                             |       | Address<br>(Byte) | Address<br>(Bit) | Data      |
|-------------------------------------------------------------------------|-------|-------------------|------------------|-----------|
| Minimum Sector Erase Sizes                                              |       | 30h               | 1:0              | 01b       |
| Write Granularity                                                       |       |                   | 2                | 1b        |
| Volatile Status Register Block Protect bits                             |       |                   | 3                | <b>1b</b> |
| Write Enable Instruction Select for writing to Volatile Status Register |       |                   | 4                | <b>0b</b> |
| Unused                                                                  |       |                   | 7:5              | 111b      |
| 4KB Erase Instruction                                                   |       | 31h               | 15:8             | 20h       |
| Supports (1-1-2) Fast Read                                              |       | 32h               | 16               | 1b        |
| Address Bytes                                                           |       |                   | 18:17            | 00b       |
| Supports Double Transfer Rate (DTR) Clocking                            |       |                   | 19               | <b>0b</b> |
| Supports (1-2-2) Fast Read                                              |       |                   | 20               | 1b        |
| Supports (1-4-4) Fast Read                                              |       |                   | 21               | 1b        |
| Supports (1-1-4) Fast Read                                              |       |                   | 22               | 1b        |
| Unused                                                                  |       |                   | 23               | 1b        |
| Reserved                                                                |       | 33h               | 31:24            | FFh       |
| Flash memory Density (bits)                                             |       | 34h               | 7:0              | FFh       |
|                                                                         |       | 35h               | 15:8             | FFh       |
| Flash memory Density (bits)                                             | 4Mb   | 36h               | 23:16            | 3Fh       |
|                                                                         | 2Mb   | 36h               | 23:16            | 1Fh       |
|                                                                         | 1Mb   | 36h               | 23:16            | 0Fh       |
|                                                                         | 512Kb | 36h               | 23:16            | 07h       |
|                                                                         | 256Kb | 36h               | 23:16            | 03h       |
| Flash memory Density (bits)                                             |       | 37h               | 31:24            | 00h       |
| 1-4-4 Fast Read Wait Cycle Count                                        |       | 38h               | 4:0              | 00100b    |
| 1-4-4 Fast Read Mode bit Cycle Count                                    |       |                   | 7:5              | 010b      |
| 1-4-4 Fast Read Instruction                                             |       | 39h               | 15:8             | EBh       |
| 1-1-4 Fast Read Wait Cycle Count                                        |       | 3Ah               | 20:16            | 01000b    |
| 1-1-4 Fast Read Mode bit Cycle Count                                    |       |                   | 23:21            | 000b      |
| 1-1-4 Fast Read Instruction                                             |       | 3Bh               | 31:24            | 6Bh       |
| 1-1-2 Fast Read Wait Cycle Count                                        |       | 3Ch               | 4:0              | 01000b    |
| 1-1-2 Fast Read Mode bit Cycle Count                                    |       |                   | 7:5              | 000b      |
| 1-1-2 Fast Read Instruction                                             |       | 3Dh               | 15:8             | 3Bh       |
| 1-2-2 Fast Read Wait Cycle Count                                        |       | 3Eh               | 20:16            | 00000b    |
| 1-2-2 Fast Read Mode bit Cycle Count                                    |       |                   | 23:21            | 100b      |
| 1-2-2 Fast Read Instruction                                             |       | 3Fh               | 31:24            | BBh       |

**Table 5.3 JEDEC Basic Flash Parameter Table (Continued)**

| Description                                              |             | Address (Byte) | Address (Bit) | Data                  |
|----------------------------------------------------------|-------------|----------------|---------------|-----------------------|
| Supports (2-2-2) Fast Read                               |             | 40h            | 0             | 0b                    |
| Reserved                                                 |             |                | 3:1           | 111b                  |
| Supports (4-4-4) Fast Read                               |             |                | 4             | 1b                    |
| Reserved                                                 |             |                | 7:5           | 111b                  |
| Reserved                                                 |             | 43:41h         | 31:8          | FFFFFFh               |
| Reserved                                                 |             | 45:44h         | 15:0          | FFFFh                 |
| 2-2-2 Fast Read Wait Cycle Count                         |             | 46h            | 20:16         | 00000b                |
| 2-2-2 Fast Read Mode bit Cycle Count                     |             |                | 23:21         | 000b                  |
| 2-2-2 Fast Read Instruction                              |             | 47h            | 31:24         | FFh                   |
| Reserved                                                 |             | 49:48h         | 15:0          | FFFFh                 |
| 4-4-4 Fast Read Wait Cycle Count                         |             | 4Ah            | 20:16         | 00100b                |
| 4-4-4 Fast Read Mode bit Cycle Count                     |             |                | 23:21         | 010b                  |
| 4-4-4 Fast Read Instruction                              |             | 4Bh            | 31:24         | EBh                   |
| Erase Type 1 Size (4KB)                                  |             | 4Ch            | 7:0           | 0Ch                   |
| Erase Type 1 Instruction                                 |             | 4Dh            | 15:8          | 20h                   |
| Erase Type 2 Size (32KB)                                 |             | 4Eh            | 23:16         | 0Fh                   |
| Erase Type 2 Instruction                                 |             | 4Fh            | 31:24         | 52h <sup>(1)</sup>    |
| Erase Type 3 Size (64KB)                                 | 256Kb/512Kb | 50h            | 7:0           | 00h                   |
|                                                          | 1Mb/2Mb/4Mb |                |               | 10h <sup>(2)</sup>    |
| Erase Type 3 Instruction                                 | 256Kb/512Kb | 51h            | 15:8          | FFh                   |
|                                                          | 1Mb/2Mb/4Mb |                |               | D8h <sup>(3)</sup>    |
| Erase Type 4 Size (256KB)                                |             | 52h            | 23:16         | 00h                   |
| Erase Type 4 Instruction                                 |             | 53h            | 31:24         | FFh                   |
| Multiplier from typical erase time to maximum erase time |             | 57:54h         | 3:0           | 0010b                 |
| Sector Type 1 ERASE time (typ)                           |             |                | 8:4           | 00100b                |
|                                                          |             |                | 10:9          | 01b                   |
| Sector Type 2 ERASE time (typ)                           |             |                | 15:11         | 00100b                |
|                                                          |             |                | 17:16         | 01b                   |
| Sector Type 3 ERASE time (typ)                           | 256Kb/512Kb |                | 22:18         | 00000b                |
|                                                          |             |                | 24:23         | 00b                   |
|                                                          | 1Mb/2Mb/4Mb |                | 22:18         | 01100b <sup>(4)</sup> |
|                                                          |             |                | 24:23         | 01b <sup>(4)</sup>    |
| Sector Type 4 ERASE time (typ)                           |             |                | 29:25         | 00000b                |
|                                                          |             |                | 31:30         | 00b                   |

Notes:

1. D8h can also be used for 32KB block erase in 256Kb/512Kb and optional 1Mb (Option C) device.
2. 00h in optional 1Mb (Option C) device. 3. FFh in optional 1Mb (Option C) device
4. [22:18] = 00000b and [24:23] = 00b in optional 1Mb (Option C) device

**4. Table 5.3 JEDEC Basic Flash Parameter Table (Continued)**

| Description                                                           |             | Address<br>(Byte) | Address<br>(Bit) | Data    |
|-----------------------------------------------------------------------|-------------|-------------------|------------------|---------|
| Multiplier from typical time to maximum time for page or byte PROGRAM |             | 58h               | 3:0              | 0001b   |
| Page size                                                             |             |                   | 7:4              | 1000b   |
| Page Program Typical time                                             |             | 5Ah:59h           | 12:8             | 00111b  |
|                                                                       |             |                   | 13               | 1b      |
| Byte Program Typical time, first byte                                 |             |                   | 17:14            | 0111b   |
|                                                                       |             |                   | 18               | 0b      |
| Byte Program Typical time, additional byte                            |             |                   | 22:19            | 0000b   |
|                                                                       |             |                   | 23               | 0b      |
| Chip Erase, Typical time                                              | 4Mb         | 5Bh               | 28:24            | 00101b  |
|                                                                       | 2Mb         |                   |                  | 00010b  |
|                                                                       | 1Mb         |                   |                  | 00001b  |
|                                                                       | 512Kb       |                   |                  | 01111b  |
|                                                                       | 256Kb       |                   |                  | 01000b  |
| Units                                                                 | 4Mb/2Mb/1Mb |                   | 30:29            | 01b     |
|                                                                       | 512Kb/256Kb |                   |                  | 00b     |
| Reserved                                                              |             |                   |                  | 31      |
| Prohibited Operations During Program Suspend                          |             | 5Ch               | 3:0              | 1100b   |
| Prohibited Operations During Erase Suspend                            |             |                   | 7:4              | 1110b   |
| Reserved                                                              |             | 5Eh:5Dh           | 8                | 1b      |
| Program Resume to Suspend Interval                                    |             |                   | 12:9             | 0110b   |
| Suspend in-progress program max latency                               |             |                   | 17:13            | 01100b  |
|                                                                       |             |                   | 19:18            | 10b     |
| Erase Resume to Suspend Interval                                      |             |                   | 23:20            | 0110b   |
| Suspend in-progress erase max latency                                 |             | 5Fh               | 28:24            | 01100b  |
|                                                                       |             |                   | 30:29            | 10b     |
| Suspend /Resume supported                                             |             |                   | 31               | 0b      |
| Program Resume Instruction                                            |             | 60h               | 7:0              | 7Ah     |
| Program Suspend Instruction                                           |             | 61h               | 15:8             | 75h     |
| Resume Instruction                                                    |             | 62h               | 23:16            | 7Ah     |
| Suspend Instruction                                                   |             | 63h               | 31:24            | 75h     |
| Reserved                                                              |             | 64h               | 1:0              | 11b     |
| Status Register Polling Device Busy                                   |             |                   | 7:2              | 111101b |

**Table 5.3 JEDEC Basic Flash Parameter Table (Continued)**

| Description                                                                                    |      | Address<br>(Byte) | Address<br>(Bit) | Data            |
|------------------------------------------------------------------------------------------------|------|-------------------|------------------|-----------------|
| Exit Deep Power-down to next operation delay                                                   | 3V   | 67h:65h           | 12:8             | 00010b          |
|                                                                                                | 1.8V |                   |                  | 00100b          |
| Exit Deep Power-down to next operation delay Units                                             |      |                   | 14:13            | 01b             |
| Exit Deep Power-down Instruction                                                               |      |                   | 22:15            | ABh             |
| Enter Deep Power-down Instruction                                                              |      |                   | 30:23            | B9h             |
| Deep Power-down Supported                                                                      |      |                   | 31               | 0b              |
| 4-4-4 mode disable sequences (QPIDI)                                                           |      | 69h:68h           | 3:0              | 1010b           |
| 4-4-4 mode enable sequences (QPIEN)                                                            |      |                   | 8:4              | 00100b          |
| 0-4-4 Mode Supported                                                                           |      |                   | 9                | 1b              |
| 0-4-4 Mode Exit Method                                                                         |      |                   | 15:10            | 110000b         |
| 0-4-4 Mode Entry Method:                                                                       |      | 6Ah               | 19:16            | 1100b           |
| Quad Enable Requirements (QER)                                                                 |      |                   | 22:20            | 010b            |
| Hold or RESET Disable                                                                          |      |                   | 23               | 0b              |
| Reserved                                                                                       |      | 6Bh               | 31:24            | FFh             |
| Volatile or Non-Volatile Register and Write Enable (WREN)<br>Instruction for Status Register 1 |      | 6Ch               | 6:0              | 1101000b        |
| Reserved                                                                                       |      |                   | 7                | 1b              |
| Soft Reset and Rescue Sequence Support                                                         |      | 6Eh:6Dh           | 13:8             | 110000b         |
| Exit 4-Byte Addressing                                                                         |      |                   | 23:14            | 110000000<br>0b |
| Enter 4-Byte Addressing                                                                        |      | 6Fh               | 31:24            | 10000000b       |

## 6. REGISTERS

The device has four sets of Registers: Status and Function Register.

### 6.1 STATUS REGISTER

Status Register Format and Status Register Bit Definitions are described in Table 6.1 & Table 6.2.

**Table 6.1 Status Register Format**

|         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
|         | SRWD  | QE    | BP3   | BP2   | BP1   | BP0   | WEL   | WIP   |
| Default | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Table 6.2 Status Register Bit Definition**

| Bit   | Name | Definition                                                                                                                                                                               | Read-Write       | Type         |
|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------|
| Bit 0 | WIP  | Write In Progress Bit:<br>"0" indicates the device is ready(default)<br>"1" indicates a write cycle is in progress and the device is busy                                                | R                | Volatile     |
| Bit 1 | WEL  | Write Enable Latch:<br>"0" indicates the device is not write enabled (default)<br>"1" indicates the device is write enabled                                                              | R/W <sup>1</sup> | Volatile     |
| Bit 2 | BP0  | Block Protection Bit:<br>"0" indicates the specific blocks are not write-protected (default)<br>"1" indicates the specific blocks are write-protected                                    | R/W              | Non-Volatile |
| Bit 3 | BP1  |                                                                                                                                                                                          |                  |              |
| Bit 4 | BP2  |                                                                                                                                                                                          |                  |              |
| Bit 5 | BP3  |                                                                                                                                                                                          |                  |              |
| Bit 6 | QE   | Quad Enable bit:<br>"0" indicates the Quad output function disable (default)<br>"1" indicates the Quad output function enable                                                            | R/W              | Non-Volatile |
| Bit 7 | SRWD | Status Register Write Disable: (See Table 7.1 for details)<br>"0" indicates the Status Register is not write-protected (default)<br>"1" indicates the Status Register is write-protected | R/W              | Non-Volatile |

**Note1:** WEL bit can be written by WREN and WRDI commands, but cannot by WRSR command.

The BP0, BP1, BP2, BP3, QE, and SRWD are non-volatile memory cells that can be written by a Write Status Register (WRSR) instruction. The default value of the BP0, BP1, BP2, BP3, QE, and SRWD bits were set to "0" at factory. The Status Register can be read by the Read Status Register (RDSR).

The function of Status Register bits are described as follows:

**WIP bit:** Write In Progress (WIP) is read-only, and can be used to detect the progress or completion of a Program, Erase, or Write/Set Non-Volatile/OTP Register operation. WIP is set to "1" (busy state) when the device is executing the operation. When an operation has completed, WIP is cleared to "0" (ready state) whether the operation is successful or not and the device is ready for further instructions.

**WEL bit:** Write Enable Latch (WEL) indicates the status of the internal write enable latch. When WEL is "0", the internal write enable latch is disabled and the write operations described in Table 6.3 are inhibited. When WEL is "1", the Write operations are allowed. WEL bit is set by a Write Enable (WREN) instruction. Each Write Non-Volatile Register, Program and Erase instruction must be preceded by a WREN instruction. The volatile register related commands such as the Set Volatile Read Register and the Set Volatile Extended Read Register don't require to set WEL to "1". WEL can be reset by a Write Disable (WRDI) instruction. It will automatically reset after the completion of any Write operation.

**Table 6.3 Instructions requiring WREN instruction ahead**

| Instructions must be preceded by the WREN instruction |                        |                                                                   |
|-------------------------------------------------------|------------------------|-------------------------------------------------------------------|
| Name                                                  | Hex Code               | Operation                                                         |
| PP                                                    | 02h                    | Serial Input Page Program                                         |
| PPQ                                                   | 32h/38h                | Quad Input Page Program                                           |
| SER                                                   | D7h/20h                | Sector Erase 4KB                                                  |
| BER32 (32KB)                                          | 52h                    | Block Erase 32KB                                                  |
| BER64 (64KB)                                          | D8h                    | Block Erase 64KB                                                  |
| BER32 (32KB)                                          | 52h/D8h <sup>(2)</sup> | Block Erase 32KB                                                  |
| BER64 (64KB)                                          | NA                     | Block Erase 64KB                                                  |
| CER                                                   | C7h/60h                | Chip Erase                                                        |
| WRSR                                                  | 01h                    | Write Non-Volatile Status Register Status Register <sup>(1)</sup> |
| WRFR                                                  | 42h                    | Write Function Register                                           |
| IRER                                                  | 64h                    | Erase Information Row                                             |
| IRP                                                   | 62h                    | Program Information Row                                           |

**Note:**

1. Optional 1Mb device (Option C) supports only 32KB Block Erase operation with D8h/ 52h command.

**BP3, BP2, BP1, BP0 bits:** The Block Protection (BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 6.4 for the Block Write Protection (BP) bit settings. When a defined combination of BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

**SRWD bit:** The Status Register Write Disable (SRWD) bit operates in conjunction with the Write Protection (WP#) signal to provide a Hardware Protection Mode. When the SRWD is set to “0”, the Status Register is not write-protected. When the SRWD is set to “1” and the WP# is pulled low ( $V_{IL}$ ), the bits of Status Register (SRWD, QE, BP3, BP2, BP1, BP0) become read-only, and a WRSR instruction will be ignored. If the SRWD is set to “1” and WP# is pulled high ( $V_{IH}$ ), the Status Register can be changed by a WRSR instruction.

**QE bit:** The Quad Enable (QE) allows quad operation. When the QE bit is set to “0”, the pin WP# and HOLD# are enabled. When the QE bit is set to “1”, the IO2 and IO3 pins are enabled.

**WARNING:** The QE bit must be set to 0 if WP# or HOLD# pin is tied directly to the power supply.

**Table 6.4 Block (64Kbyte) assignment by Block Write Protect (BP) Bits**

| Status Register Bits |     |     |     | BP Table, Protected Memory Area  |                                  |                                  |                      |
|----------------------|-----|-----|-----|----------------------------------|----------------------------------|----------------------------------|----------------------|
| BP3                  | BP2 | BP1 | BP0 | 4Mb                              | 2Mb                              | 1Mb                              | 512Kb and 256Kb      |
| 0                    | 0   | 0   | 0   | 0 (None)                         | 0 (None)                         | 0 (None)                         | 0 (None)             |
| 0                    | 0   | 0   | 1   | 1(1 block : 7th)                 | 1(1 block : 3rd)                 | 1(1 block : 1st)                 | 1~15<br>(All Blocks) |
| 0                    | 0   | 1   | 0   | 2(2 blocks : 6th – 7th)          | 2(2 blocks : 2nd – 3rd)          | 2~8<br>(2 blocks: All Blocks)    |                      |
| 0                    | 0   | 1   | 1   | 3(4 blocks : 4th – 7th)          | 3(3 blocks : 1st – 3rd)          |                                  |                      |
| 0                    | 1   | 0   | 0   | 4(6 blocks : 2nd – 7th)          | 4~8<br>(4 blocks: All Blocks)    |                                  |                      |
| 0                    | 1   | 0   | 1   | 5(7 blocks : 1st – 7th)          |                                  |                                  |                      |
| 0                    | 1   | 1   | 0   | 6~8<br>(8 blocks: All Blocks)    |                                  |                                  |                      |
| 0                    | 1   | 1   | 1   |                                  |                                  |                                  |                      |
| 1                    | 0   | 0   | 0   |                                  |                                  |                                  |                      |
| 1                    | 0   | 0   | 1   | 9(1 block : 0th)                 | 9(1 block : 0th)                 | 9(1 block : 0th)                 |                      |
| 1                    | 0   | 1   | 0   | 10(2 blocks : 0th – 1st)         | 10(2 blocks : 0th – 1st)         | 10~15<br>(2 blocks : All Blocks) |                      |
| 1                    | 0   | 1   | 1   | 11(4 blocks : 0th – 3rd)         | 11(3 blocks : 0th – 2nd)         |                                  |                      |
| 1                    | 1   | 0   | 0   | 12(6 blocks : 0th – 5th)         | 12~15<br>(4 blocks : All Blocks) |                                  |                      |
| 1                    | 1   | 0   | 1   | 13(7 blocks : 0th– 6th)          |                                  |                                  |                      |
| 1                    | 1   | 1   | 0   | 14~15<br>(8 blocks : All Blocks) |                                  |                                  |                      |
| 1                    | 1   | 1   | 1   |                                  |                                  |                                  |                      |

**Table 6.5 Optional Block (64Kbyte) assignment by Block Write Protect (BP) Bits <sup>(1)</sup>**

| Status Register Bits |     |     |     | Protected Memory Area |                  |                  |                 |
|----------------------|-----|-----|-----|-----------------------|------------------|------------------|-----------------|
| BP3                  | BP2 | BP1 | BP0 | 4Mb                   | 2Mb              | 1Mb              | 512Kb and 256Kb |
| 0                    | 0   | 0   | 0   | None                  | None             | None             | None            |
| 0                    | 0   | 0   | 1   | 1 block : 7           | 1 block : 3      | 1 block : 1      | All Blocks      |
| 0                    | 0   | 1   | 0   | 2 blocks : 6 - 7      | 2 blocks : 2 - 3 | All Blocks       |                 |
| 0                    | 0   | 1   | 1   | 4 blocks : 4 - 7      | 3 blocks : 1 - 3 | 2 blocks : 0 - 1 |                 |
| 0                    | 1   | 0   | 0   | 6 blocks : 2 - 7      | All Blocks       |                  |                 |
| 0                    | 1   | 0   | 1   | 7 blocks : 1 - 7      |                  |                  |                 |
| 0                    | 1   | 1   | 0   | All Blocks            |                  |                  |                 |
| 0                    | 1   | 1   | 1   |                       |                  |                  |                 |
| 1                    | 0   | 0   | 0   |                       |                  |                  |                 |
| 1                    | 0   | 0   | 1   |                       |                  |                  |                 |
| 1                    | 0   | 1   | 0   | 7 blocks 0 - 6        |                  |                  |                 |
| 1                    | 0   | 1   | 1   | 6 blocks 0 - 5        |                  |                  |                 |
| 1                    | 1   | 0   | 0   | 4 blocks 0 - 3        |                  |                  |                 |
| 1                    | 1   | 0   | 1   | 2 blocks : 0 - 1      |                  | 2 blocks : 0 - 1 |                 |
| 1                    | 1   | 1   | 0   | 1 block : 0           | 1 block : 0      | 1 block : 0      |                 |
| 1                    | 1   | 1   | 1   | None                  | None             | None             | None            |

**Note:**

1. Call factory for optional BP Table.

**Table 6.6 Optional Block (32Kbyte) assignment by Block Write Protect (BP) Bits for 1Mb Option C**

| Status Register Bits |     |     |     | BP Table, Protected Memory Area |
|----------------------|-----|-----|-----|---------------------------------|
| BP3                  | BP2 | BP1 | BP0 | 1Mb                             |
| 0                    | 0   | 0   | 0   | 0 (None)                        |
| 0                    | 0   | 0   | 1   | 1(1 block : 3rd)                |
| 0                    | 0   | 1   | 0   | 2(2 blocks : 2nd – 3rd)         |
| 0                    | 0   | 1   | 1   | 3~15<br>(4 blocks: All Blocks)  |
| 0                    | 1   | 0   | 0   |                                 |
| 0                    | 1   | 0   | 1   |                                 |
| 0                    | 1   | 1   | 0   |                                 |
| 0                    | 1   | 1   | 1   |                                 |
| 1                    | 0   | 0   | 0   |                                 |
| 1                    | 0   | 0   | 1   |                                 |
| 1                    | 0   | 1   | 0   |                                 |
| 1                    | 0   | 1   | 1   |                                 |
| 1                    | 1   | 0   | 0   |                                 |
| 1                    | 1   | 0   | 1   |                                 |
| 1                    | 1   | 1   | 0   |                                 |
| 1                    | 1   | 1   | 1   |                                 |

## 6.2 FUNCTION REGISTER

Function Register Format and Bit definition are described in Table 6.5 and Table 6.6.

**Table 6.7 Function Register Format**

|         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1    | Bit 0    |
|---------|-------|-------|-------|-------|-------|-------|----------|----------|
|         | IRL3  | IRL2  | IRL1  | IRL0  | ESUS  | PSUS  | Reserved | Reserved |
| Default | 0     | 0     | 0     | 0     | 0     | 0     | 0        | 0        |

**Table 6.8 Function Register Bit Definition**

| Bit   | Name      | Definition                                                                                                                                   | Read /Write | Type     |
|-------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------|-------------|----------|
| Bit 0 | Reserved  | Reserved                                                                                                                                     | R           | Reserved |
| Bit 1 | Reserved  | Reserved                                                                                                                                     | R           | Reserved |
| Bit 2 | PSUS      | Program suspend bit:<br>"0" indicates program is not suspend<br>"1" indicates program is suspend                                             | R           | Volatile |
| Bit 3 | ESUS      | Erase suspend bit:<br>"0" indicates Erase is not suspend<br>"1" indicates Erase is suspend                                                   | R           | Volatile |
| Bit 4 | IR Lock 0 | Lock the Information Row 0:<br>"0" indicates the Information Row can be programmed<br>"1" indicates the Information Row cannot be programmed | R/W         | OTP      |
| Bit 5 | IR Lock 1 | Lock the Information Row 1:<br>"0" indicates the Information Row can be programmed<br>"1" indicates the Information Row cannot be programmed | R/W         | OTP      |
| Bit 6 | IR Lock 2 | Lock the Information Row 2:<br>"0" indicates the Information Row can be programmed<br>"1" indicates the Information Row cannot be programmed | R/W         | OTP      |
| Bit 7 | IR Lock 3 | Lock the Information Row 3:<br>"0" indicates the Information Row can be programmed<br>"1" indicates the Information Row cannot be programmed | R/W         | OTP      |

**Note:** Once OTP bits of Function Register are written to "1", it cannot be modified to "0" any more.

**PSUS bit:** The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to "1" after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to "0".

**ESUS bit:** The Erase Suspend Status bit indicates when an Erase operation has been suspended. The ESUS bit is "1" after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to "0".

**IR Lock bit 0 ~ 3:** The default is "0" so that the Information Row can be programmed. If the bit set to "1", the Information Row can't be programmed. Once it set to "1", it cannot be changed back to "0" since IR Lock bits are OTP.

## 7. PROTECTION MODE

The device supports hardware and software write-protection mechanisms.

### 7.1 HARDWARE WRITE PROTECTION

The Write Protection (WP#) pin provides a hardware write protection method for BP3, BP2, BP1, BP0, SRWD, and QE in the Status Register. Refer to the section 6.1 STATUS REGISTER.

Write inhibit voltage ( $V_{WI}$ ) is specified in the section 9.8 POWER-UP AND POWER-DOWN. All write sequence will be ignored when  $V_{CC}$  drops to  $V_{WI}$ .

**Table 7.1 Hardware Write Protection on Status Register**

| SRWD | WP#  | Status Register |
|------|------|-----------------|
| 0    | Low  | Writable        |
| 1    | Low  | Protected       |
| 0    | High | Writable        |
| 1    | High | Writable        |

**Note:** Before the execution of any program, erase or write Status Register instruction, the Write Enable Latch (WEL) bit must be enabled by executing a Write Enable (WREN) instruction. If the WEL bit is not enabled, the program, erase or write register instruction will be ignored.

### 7.2 SOFTWARE WRITE PROTECTION

The device also provides a software write protection feature. The Block Protection (BP3, BP2, BP1, BP0) bits allow part or the whole memory area to be write-protected.

## 8. DEVICE OPERATION

The device utilizes an 8-bit instruction register. Refer to Table 8.1. Instruction Set for details on instructions and instruction codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on Serial Data Input (SI) or Serial Data IOs (IO0, IO1, IO2, IO3). The input data on SI or IOs is latched on the rising edge of Serial Clock (SCK) after Chip Enable (CE#) is driven low ( $V_{IL}$ ). Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CE# must be driven high ( $V_{IH}$ ) after the last bit of the instruction sequence has been shifted in to end the operation.

**Table 8.1 Instruction Set<sup>(1)</sup>**

| Instruction Name | Operation               | Mode       | Byte0              | Byte1                | Byte2               | Byte3              | Byte4                       | Byte5         | Byte6         | Byte7         | Byte8 |
|------------------|-------------------------|------------|--------------------|----------------------|---------------------|--------------------|-----------------------------|---------------|---------------|---------------|-------|
| NORD             | Normal Read Mode        | SPI        | 03h                | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | Data out                    |               |               |               |       |
| FRD              | Fast Read Mode          | SPI        | 0Bh                | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | Dummy                       | Data out      |               |               |       |
|                  |                         | QPI        | 0Bh                | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | Dummy                       | Dummy         | Dummy         | Data out      |       |
| FRDIO            | Fast Read Dual I/O      | SPI        | BBh                | A<br><23:16><br>Dual | A<br><15:8><br>Dual | A<br><7:0><br>Dual | Dummy (AXh <sup>(2)</sup> ) | Dual Data out |               |               |       |
| FRDO             | Fast Read Dual Output   | SPI        | 3Bh                | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | Dummy                       | Dummy         | Dual Data out |               |       |
| FRQO             | Fast Read Quad Output   | SPI        | 6Bh                | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | Dummy                       | Quad Data out |               |               |       |
| FRQIO            | Fast Read Quad I/O      | SPI<br>QPI | EBh                | A<br><23:16><br>Quad | A<br><15:8><br>Quad | A<br><7:0><br>Quad | Dummy (AXh <sup>(2)</sup> ) | Dummy         | Dummy         | Quad Data out |       |
| PP               | Input Page Program      | SPI<br>QPI | 02h                | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | PD<br>(256byte)             |               |               |               |       |
| PPQ              | Quad Input Page Program | SPI        | 32h<br>38h         | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         | Quad PD<br>(256byte)        |               |               |               |       |
| SER              | Sector Erase            | SPI<br>QPI | D7h<br>20h         | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         |                             |               |               |               |       |
| BER32<br>(32KB)  | Block Erase<br>32Kbyte  | SPI<br>QPI | 52h <sup>(1)</sup> | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         |                             |               |               |               |       |
| BER64<br>(64KB)  | Block Erase<br>64Kbyte  | SPI<br>QPI | D8h <sup>(1)</sup> | A<br><23:16>         | A<br><15:8>         | A<br><7:0>         |                             |               |               |               |       |
| CER              | Chip Erase              | SPI<br>QPI | C7h<br>60h         |                      |                     |                    |                             |               |               |               |       |
| WREN             | Write Enable            | SPI<br>QPI | 06h                |                      |                     |                    |                             |               |               |               |       |
| WRDI             | Write Disable           | SPI<br>QPI | 04h                |                      |                     |                    |                             |               |               |               |       |
| RDSR             | Read Status Register    | SPI<br>QPI | 05h                | SR                   |                     |                    |                             |               |               |               |       |
| WRSR             | Write Status Register   | SPI<br>QPI | 01h                | WSR<br>Data          |                     |                    |                             |               |               |               |       |

Note: 1. In 256Kb/512Kb, both 52h and D8h command are for 32KB ERASE only.

| Instruction Name | Operation                     | Mode    | Byte0   | Byte1                       | Byte2                      | Byte3                     | Byte4        | Byte5    | Byte6 | Byte7 | Byte8 |
|------------------|-------------------------------|---------|---------|-----------------------------|----------------------------|---------------------------|--------------|----------|-------|-------|-------|
| RDFR             | Read Function Register        | SPI QPI | 48h     | Data out                    |                            |                           |              |          |       |       |       |
| WRFR             | Write Function Register       | SPI QPI | 42h     | WFR Data                    |                            |                           |              |          |       |       |       |
| QPIEN            | Enter QPI mode                | SPI     | 35h     |                             |                            |                           |              |          |       |       |       |
| QPIDI            | Exit QPI mode                 | QPI     | F5h     |                             |                            |                           |              |          |       |       |       |
| PERSUS           | Suspend during program/erase  | SPI QPI | 75h B0h |                             |                            |                           |              |          |       |       |       |
| PERRSM           | Resume program/erase          | SPI QPI | 7Ah 30h |                             |                            |                           |              |          |       |       |       |
| DP               | Deep Power Down               | SPI QPI | B9h     |                             |                            |                           |              |          |       |       |       |
| RDPD             | Release Power Down            | SPI QPI | ABh     |                             |                            |                           |              |          |       |       |       |
| RDID             | Read ID                       | SPI QPI | ABh     | Dummy                       | Dummy                      | Dummy                     | ID7-ID0      |          |       |       |       |
| RDJDID           | Read JEDEC ID Command         | SPI     | 9Fh     | MF7-MF0                     | ID15-ID8                   | ID7-ID0                   |              |          |       |       |       |
|                  |                               | QPI     | AFh     | MF7-MF0                     | ID15-ID8                   | ID7-ID0                   |              |          |       |       |       |
| RDMDID           | Read Manufacturer & Device ID | SPI QPI | 90h     | A<br><23:16> = 00h          | A<br><15:8> = 00h          | 00h                       | MF7-MF0      | ID7-ID0  |       |       |       |
|                  |                               |         |         |                             |                            | 01h                       | ID7-ID0      | MF7-MF0  |       |       |       |
| RDUID            | Read Unique ID                | SPI     | 4Bh     | A <sup>(3)</sup><br><23:16> | A <sup>(3)</sup><br><15:8> | A <sup>(3)</sup><br><7:0> | Dummy        | Data out |       |       |       |
|                  |                               | QPI     | 4Bh     | A <sup>(3)</sup><br><23:16> | A <sup>(3)</sup><br><15:8> | A <sup>(3)</sup><br><7:0> | Dummy        | Dummy    |       |       |       |
| RDSFDP           | SFDP Read                     | SPI     | 5Ah     | A<br><23:16>                | A<br><15:8>                | A<br><7:0>                | Dummy        | Data out |       |       |       |
|                  |                               | QPI     | 5Ah     | A<br><23:16> Quad           | A<br><15:8> Quad           | A<br><7:0> Quad           | Dummy        | Dummy    |       |       |       |
| NOP              | No Operation                  | SPI QPI | 00h     |                             |                            |                           |              |          |       |       |       |
| RSTEN            | Software Reset Enable         | SPI QPI | 66h     |                             |                            |                           |              |          |       |       |       |
| RST              | Software Reset                | SPI QPI | 99h     |                             |                            |                           |              |          |       |       |       |
| IRER             | Erase Information Row         | SPI QPI | 64h     | A<br><23:16>                | A<br><15:8>                | A<br><7:0>                |              |          |       |       |       |
| IRP              | Program Information Row       | SPI QPI | 62h     | A<br><23:16>                | A<br><15:8>                | A<br><7:0>                | PD (256byte) |          |       |       |       |
| IRRD             | Read Information Row          | SPI     | 68h     | A<br><23:16>                | A<br><15:8>                | A<br><7:0>                | Dummy        | Data out |       |       |       |
|                  |                               | QPI     | 68h     | A<br><23:16> Quad           | A<br><15:8> Quad           | A<br><7:0> Quad           | Dummy        | Dummy    |       |       |       |
| STWBR            | Set Wrapped Burst Read        | SPI QPI | C0h     | STWBR Data                  |                            |                           |              |          |       |       |       |

Notes:

1. The number of dummy cycles for read operation is fixed like below.

| Operation                    | Command | Instruction-Address-Data | Dummy Cycles | Comment                                                                   |
|------------------------------|---------|--------------------------|--------------|---------------------------------------------------------------------------|
| Fast Read (SPI mode)         | 0Bh     | 1-1-1                    | 8            | RDUID, IRRD instructions have same dummy cycles with Fast Read operation. |
| Fast Read (QPI mode)         | 0Bh     | 4-4-4                    | <b>6</b>     |                                                                           |
| Fast Read Dual Output        | 3Bh     | 1-1-2                    | 8            |                                                                           |
| Fast Read Dual IO SPI        | BBh     | 1-2-2                    | <b>4</b>     |                                                                           |
| Fast Read Quad Output        | 6Bh     | 1-1-4                    | 8            |                                                                           |
| Fast Read Quad IO (SPI mode) | EBh     | 1-4-4                    | <b>6</b>     |                                                                           |
| Fast Read Quad IO (QPI mode) | EBh     | 4-4-4                    | <b>6</b>     |                                                                           |

2. AXh has to be counted as a part of dummy cycles. X means "don't care".
3. A<23:9> are "don't care" and A<8:4> are always "0".

## 8.1 NORMAL READ OPERATION (NORD, 03h)

The NORMAL READ (NORD) instruction is used to read memory contents at a maximum frequency of 50MHz.

The NORD instruction code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A<sub>VMSB</sub> (Valid Most Significant Bit) - A<sub>0</sub> are decoded. The remaining bits (A23 - A<sub>VMSB+1</sub>) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 8.2 for the related Address Key.

The first byte data (D7 - D0) is shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one NORMAL READ instruction. The address is automatically incremented by one after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH) after the data comes out. When the highest address of the device is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ instruction.

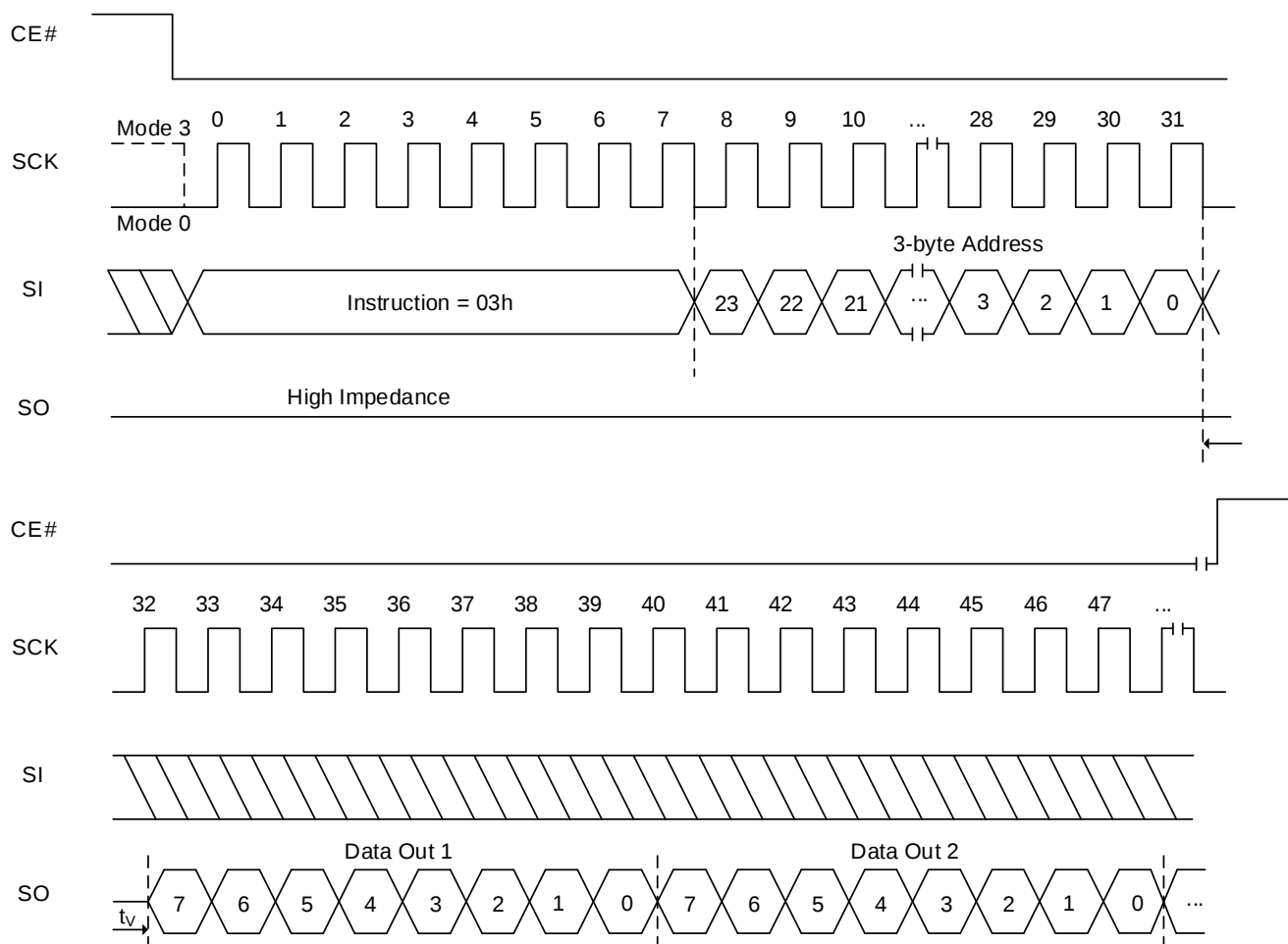
If the NORMAL READ instruction is issued while an Erase, Program or Write operation is in process (WIP=1) the instruction is ignored and will not have any effects on the current operation.

**Table 8.2 Address Key**

| Address                           | 4Mb                | 2Mb                | 1Mb                | 512Kb              | 256Kb              |
|-----------------------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| A <sub>VMSB</sub> -A <sub>0</sub> | A18-A0 (A23-A19=X) | A17-A0 (A23-A18=X) | A16-A0 (A23-A17=X) | A15-A0 (A23-A16=X) | A14-A0 (A23-A15=X) |

**Note: X=Don't Care**

Figure 8.1 Normal Read Sequence



## 8.2 FAST READ OPERATION (FRD, 0Bh)

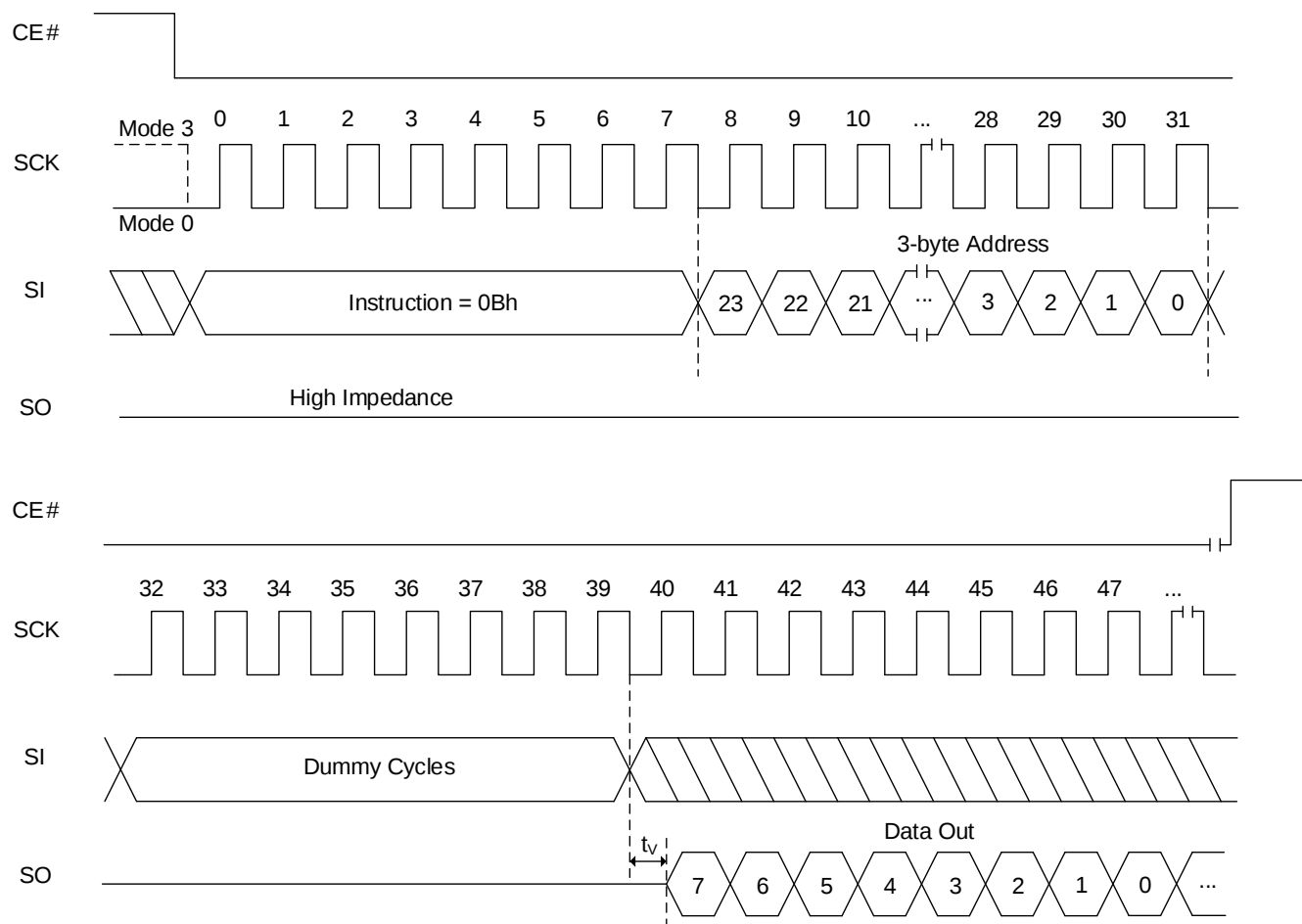
The FAST READ (FRD) instruction is used to read memory data at up to a 104MHz clock.

The FAST READ instruction code is followed by three address bytes (A23 - A0) transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte from the address is shifted out on the SO line after 6 dummy cycles, with each bit shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST READ instruction. The FAST READ instruction is terminated by driving CE# high (VIH).

If the FAST READ instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored without affecting the current cycle.

**Figure 8.2 Fast Read Sequence**



**Note:** Dummy cycles depends on Read Parameter setting. Detailed information in Table 6.11 Read Dummy Cycles.

### FAST READ OPERATION IN QPI MODE (FRD, 0Bh)

The FAST READ (FRD) instruction is used also in QPI mode to read memory data at up to a 104MHz clock.

The FAST READ instruction code (2 clocks) is followed by three address bytes (A23-A0 — 6 clocks), transmitted via the IO3, IO2, IO1 and IO0 lines, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines after 6 dummy cycles, with each bit shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST READ instruction. The FAST READ instruction in QPI mode is terminated by driving CE# high (VIH).

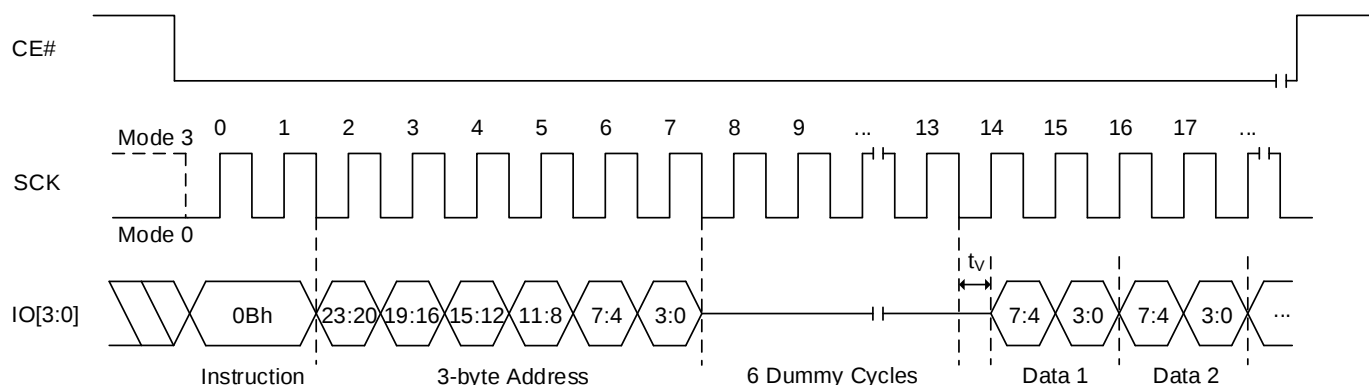
If the FAST READ instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored without affecting the current cycle.

The Fast Read sequence in QPI mode is also applied to the commands in the following table 8.3.

**Table 8.3 Address Key**

| Instruction Name | Operation            | Hex Code |
|------------------|----------------------|----------|
| FRQIO            | Fast Read Quad I/O   | EBh      |
| RDUID            | Read Unique ID       | 4Bh      |
| IRRD             | Read Information Row | 68h      |

**Figure 8.3 Fast Read Sequence In QPI Mode**



**Note:** Number of dummy cycles depends on Read Parameter setting. Detailed information in Table 6.11 Read Dummy Cycles.

### 8.3 HOLD OPERATION

HOLD# is used in conjunction with CE# to select the device. When the device is selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, HOLD# is brought low while the SCK signal is low. To resume serial communication, HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to SI will be ignored while SO is in the high impedance state, during HOLD.

**Note:** HOLD# is not supported with QE=1.

Timing graph can be referenced in AC Parameters Figure 9.4.

### 8.4 FAST READ DUAL I/O OPERATION (FRDIO, BBh)

The FRDIO allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications.

The FRDIO instruction code is followed by three address bytes (A23 – A0) transmitted via the IO1 and IO0 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and this shift pattern continues to alternate between the two lines. Depending on the usage of AX read operation mode, a mode byte may be located after address input.

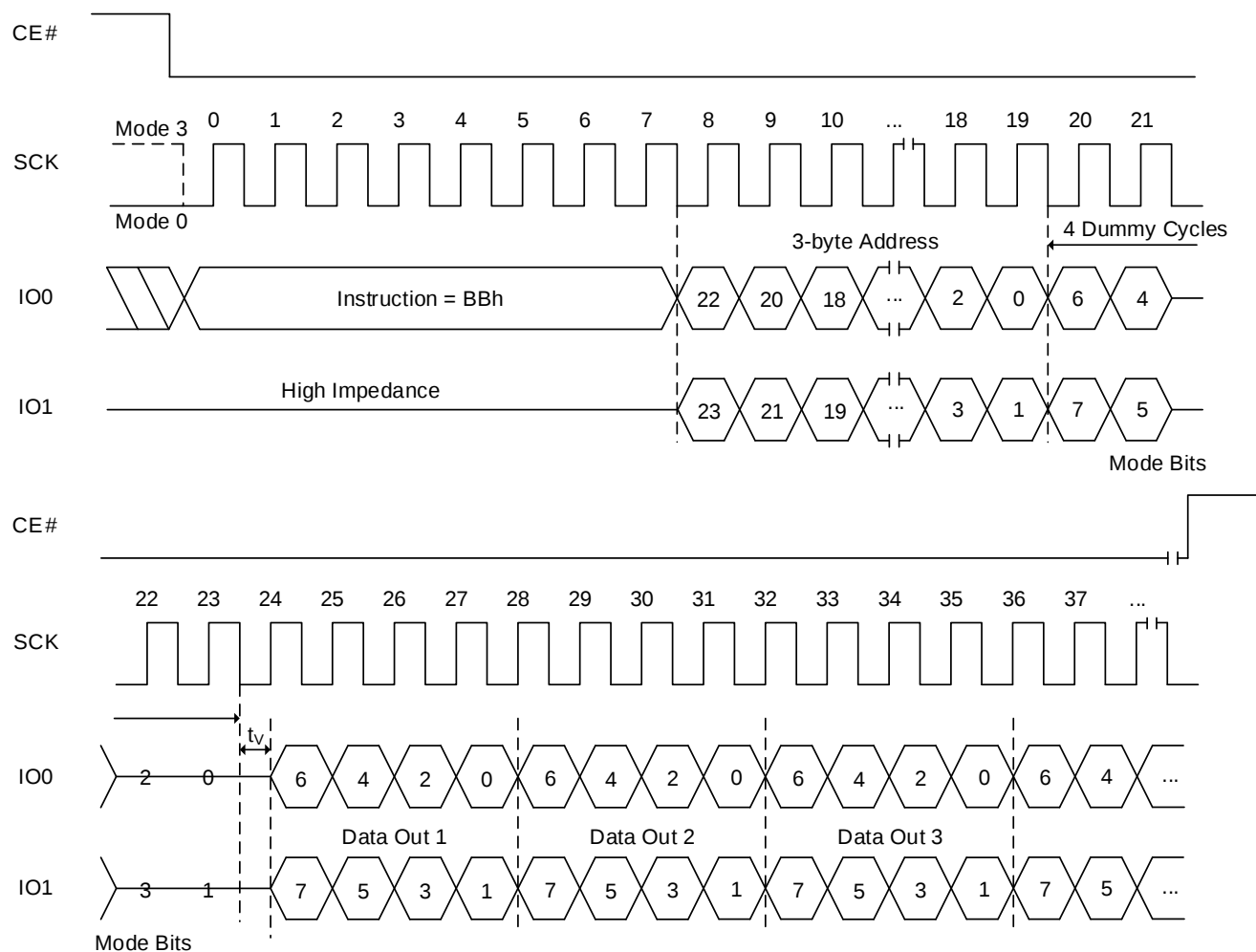
The first data byte addressed is shifted out on the IO1 and IO0 lines after 4 dummy cycles, with each pair of bits shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK. The MSB is output on IO1, while simultaneously the second bit is output on IO0. Figure 8.4 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO instruction. FRDIO instruction is terminated by driving CE# high ( $V_{IH}$ ).

The device supports the AX read operation by applying mode bits during dummy period. Mode bits consist of 8 bits, such as M7 to M0. Four cycles after address input are reserved for Mode bits in FRDIO execution. M7 to M4 are important for enabling this mode. M3 to M0 become don't care for future use. When M[7:4]=1010(Ah), it enables the AX read operation and subsequent FRDIO execution skips command code. It saves cycles as described in Figure 8.5. When the code is different from AXh (where X is don't care), the device exits the AX read operation. After finishing the read operation, device becomes ready to receive a new command. SPI or QPI mode configuration retains the prior setting. Mode bit must be applied during dummy cycles. The dummy cycles are 4 cycles, data output will start right after mode bit is applied.

If the FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not affect the current cycle.

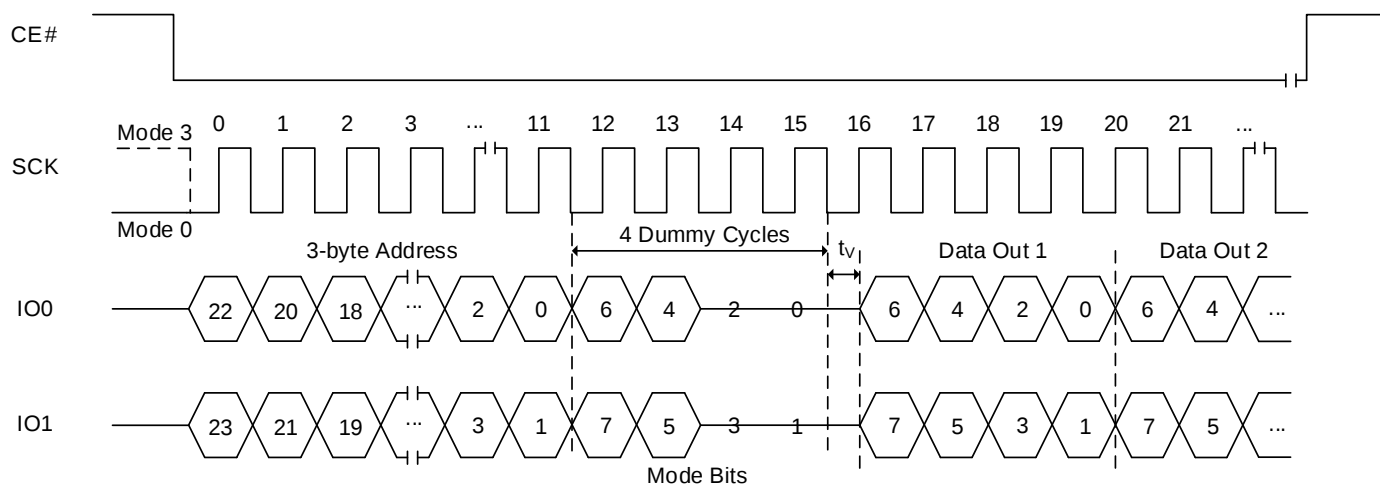
Figure 8.4 Fast Read Dual I/O Sequence (with command decode cycles)



**Notes:**

1. If the mode bits=AXh (where X is don't care), it can execute the AX read mode (without command). When the mode bits are different from AXh, the device exits the AX read operation.
2. Number of dummy cycles depends on clock speed. Detailed information in Table 6.11 Read Dummy Cycles.
3. Sufficient dummy cycles are required to avoid I/O contention. If the number of dummy cycles and AX bit cycles are same, then X should be Hi-Z.

Figure 8.5 Fast Read Dual I/O AX Read Sequence (without command decode cycles)



**Notes:**

1. If the mode bits=AXh (where X is don't care), it will keep executing the AX read mode (without command). When the mode bits are different from AXh, the device exits the AX read operation.

## 8.5 FAST READ DUAL OUTPUT OPERATION (FRDO, 3Bh)

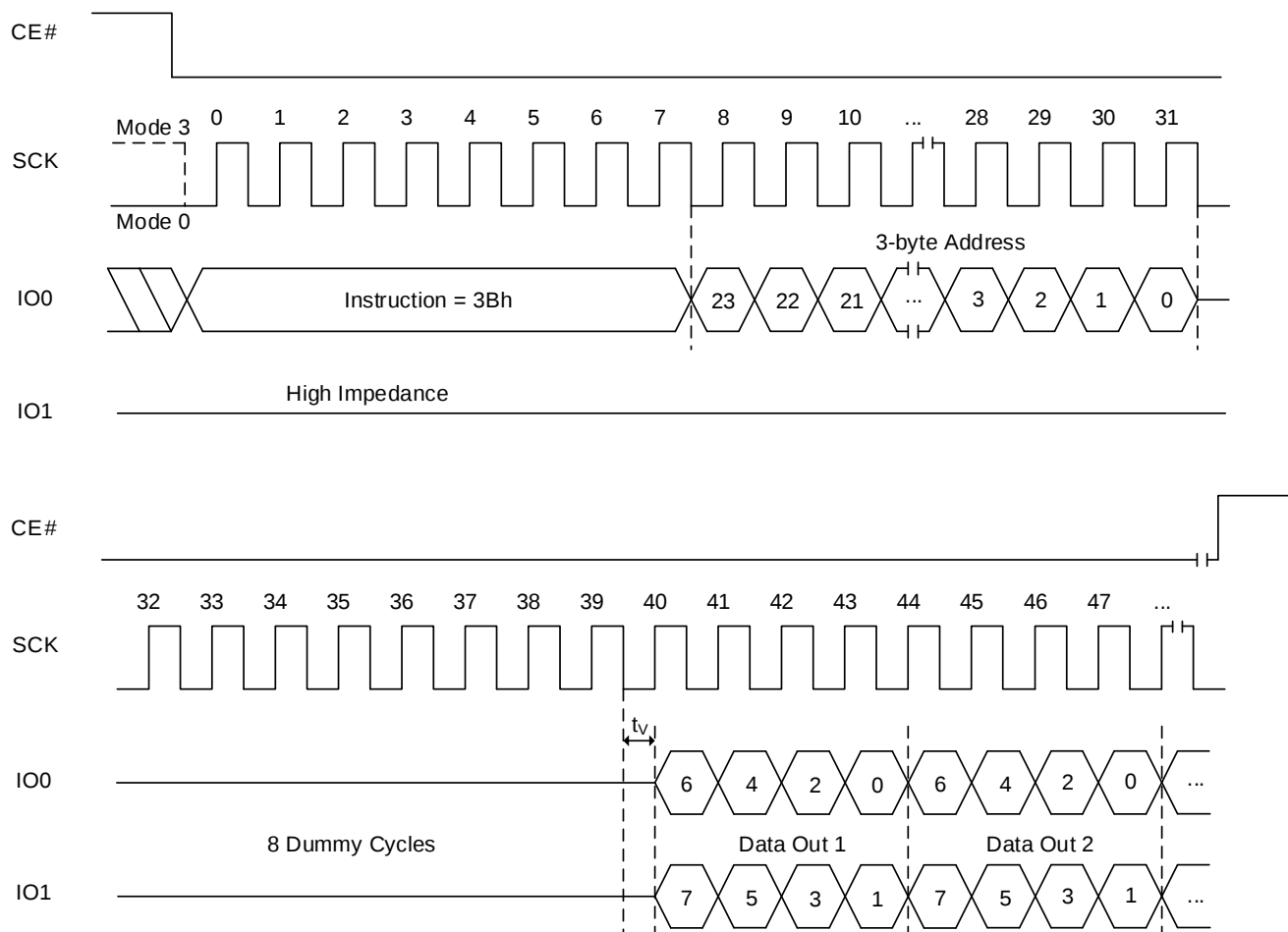
The FRDO instruction is used to read memory data on two output pins each at up to a 104MHz clock.

The FRDO instruction code is followed by three address bytes (A23 – A0) transmitted via the IO0 line, and each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO1 and IO0 lines after 8 dummy cycles, with each pair of bits shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK. The first bit (MSB) is output on IO1. Simultaneously, the second bit is output on IO0.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO instruction. The FRDO instruction is terminated by driving CE# high (VIH).

If the FRDO instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle.

**Figure 8.6 Fast Read Dual Output Sequence**



## 8.6 FAST READ QUAD OUTPUT OPERATION (FRQO, 6Bh)

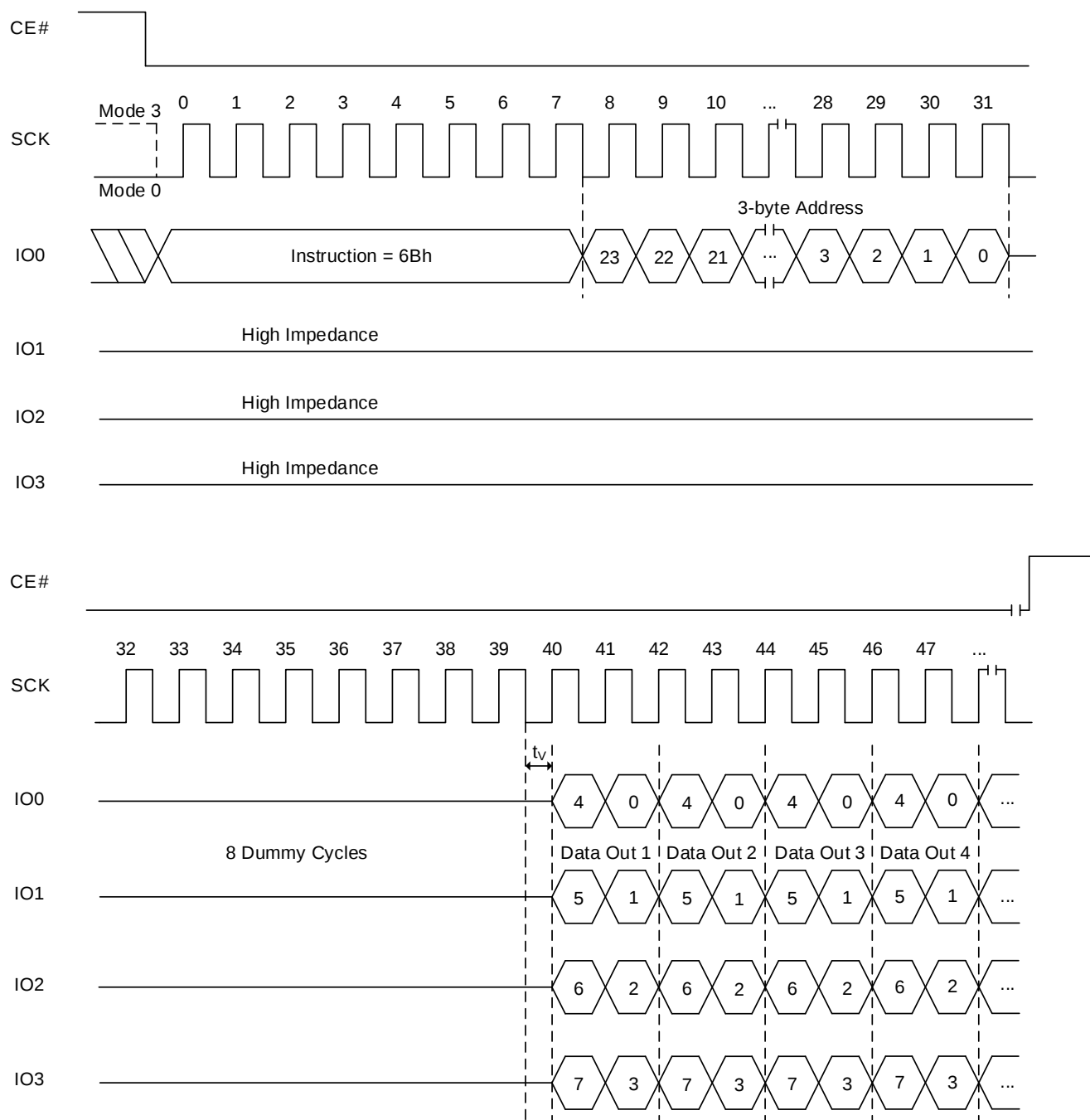
The FRQO instruction is used to read memory data on four output pins each at up to a 104 MHz clock.

The FRQO instruction code is followed by three address bytes (A23 – A0), transmitted via the IO0 line, and each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines after 8 dummy cycles, with each group of four bits shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, the third bit is output on IO1, etc.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQO instruction. FRQO instruction is terminated by driving CE# high (VIH).

If a FRQO instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle.

**Figure 8.7 Fast Read Quad Output Sequence**



### 8.7 FAST READ QUAD I/O OPERATION (FRQIO, EBh)

The FRQIO instruction allows the address bits to be input four bits at a time. This may allow for code to be executed directly from the SPI in some applications.

The FRQIO instruction code is followed by three address bytes (A23 – A0), transmitted via the IO3, IO2, IO1 and IO0 lines, and each group of four bits latched-in during the rising edge of SCK. The address of MSB inputs on IO3, the next bit on IO2, the next bit on IO1, the next bit on IO0, and continue to shift in alternating on the four. Depending on the usage of AX read operation mode, a mode byte may be located after address input.

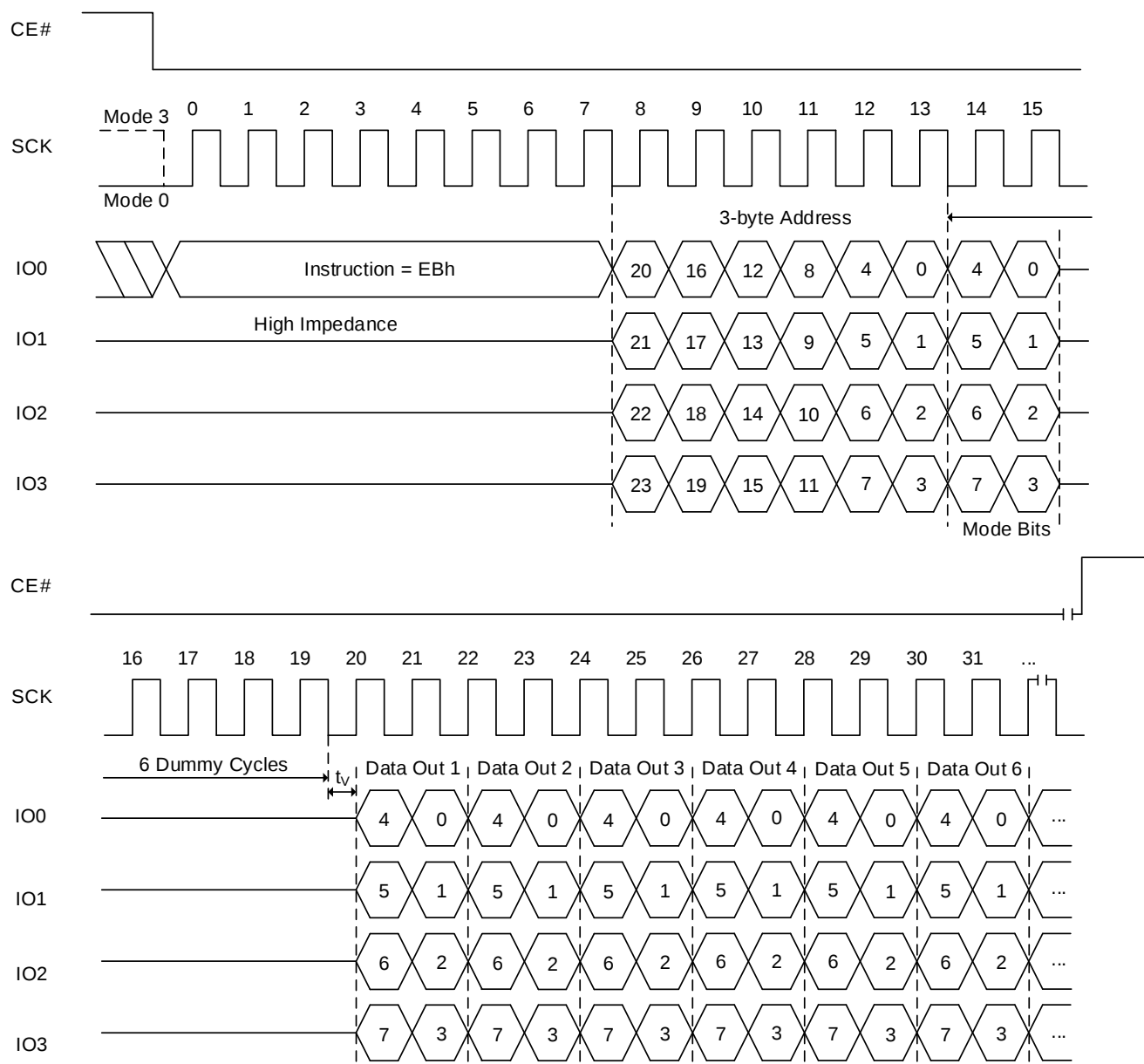
The first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines after 6 dummy cycles, with each group of four bits shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, the third bit is output on IO1, etc. Figure 8.8 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQIO instruction. FRQIO instruction is terminated by driving CE# high ( $V_{IH}$ ).

The device supports the AX read operation by applying mode bits during dummy period. Mode bits consist of 8 bits, such as M7 to M0. Two cycles after address input are reserved for Mode bits in FRQIO execution. M7 to M4 are important for enabling this mode. M3 to M0 become don't care for future use. When M[7:4]=1010(Ah), it enables the AX read operation and subsequent FRQIO execution skips command code. It saves cycles as described in Figure 8.9. When the code is different from AXh (where X is don't care), the device exits the AX read operation. After finishing the read operation, device becomes ready to receive a new command. SPI or QPI mode configuration retains the prior setting.

If the FRQIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

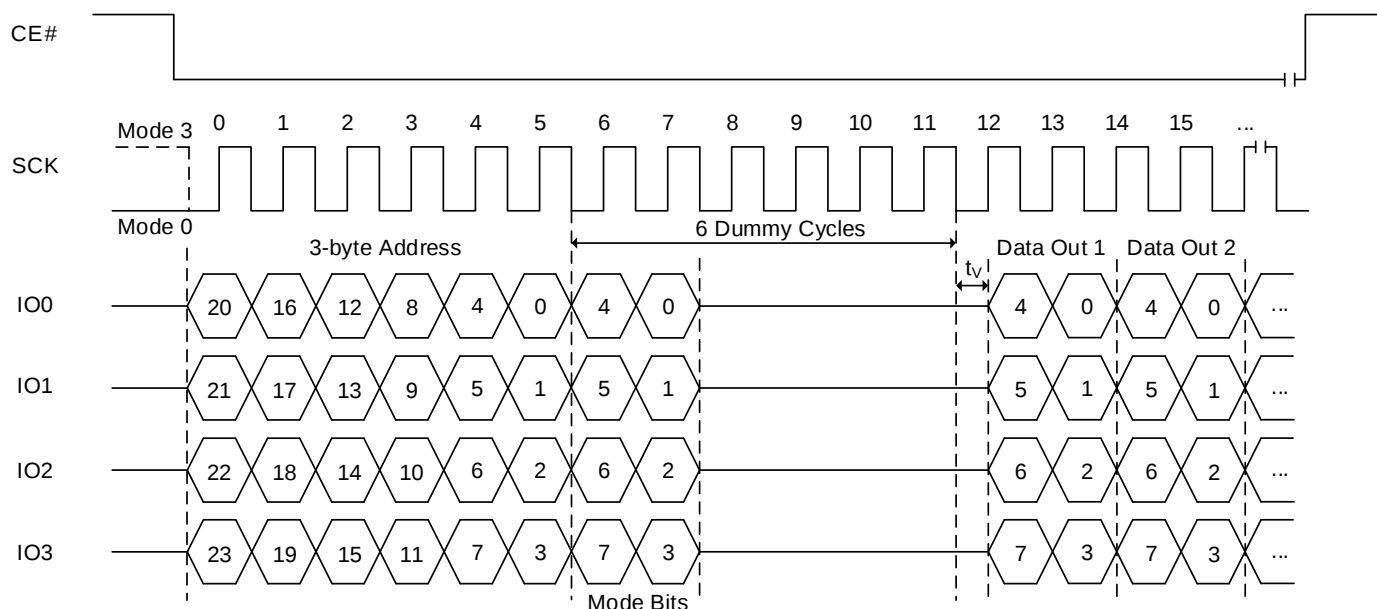
Figure 8.8 Fast Read Quad I/O Sequence (with command decode cycles)



**Note:**

1. If the mode bits=AXh (where X is don't care), it can execute the AX read mode (without command). When the mode bits are different from AXh, the device exits the AX read operation.

Figure 8.9 Fast Read Quad I/O AX Read Sequence (without command decode cycles)



**Note:**

1. If the mode bits=AXh (where X is don't care), it will keep executing the AX read mode (without command). When the mode bits are different from AXh, the device exits the AX read operation.

## FAST READ QUAD I/O OPERATION IN QPI MODE (FRQIO, EBh)

The FRQIO instruction is also used in QPI mode to read memory data at up to a 104MHz clock.

The FRQIO instruction in QPI mode utilizes all four IO lines to input the instruction code so that only two clocks are required, while the FRQIO instruction in SPI mode requires that the byte-long instruction code is shifted into the device only via IO0 line in eight clocks. As a result, 6 command cycles will be reduced by the FRQIO instruction in QPI mode.

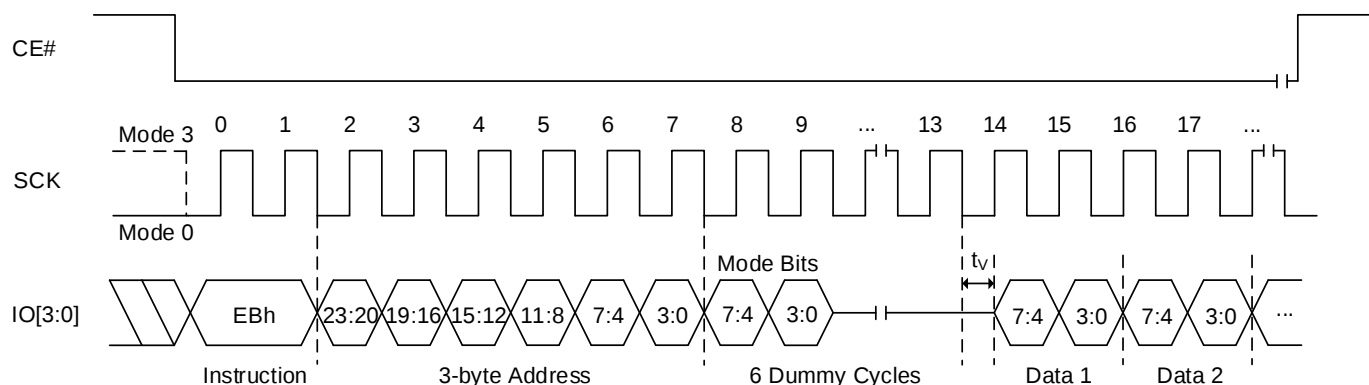
The first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines after 6 dummy cycles, with each group of four bits shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK.

The device supports the AX read operation by applying mode bits during dummy period. Mode bits consist of 8 bits, such as M7 to M0. Two cycles after address input are reserved for Mode bits in FRQIO execution. M7 to M4 are important for enabling this mode. M3 to M0 become don't care for future use. When M[7:4]=1010(Ah), it enables the AX read operation and subsequent FRQIO execution skips command code. When the code is different from AXh (where X is don't care), the device exits the AX read operation.

After finishing the read operation, device becomes ready to receive a new command. SPI or QPI mode configuration retains the prior setting.

If the FRQIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

**Figure 8.10 Fast Read Quad I/O Sequence in QPI Mode**



## 8.8 PAGE PROGRAM OPERATION (PP, 02h)

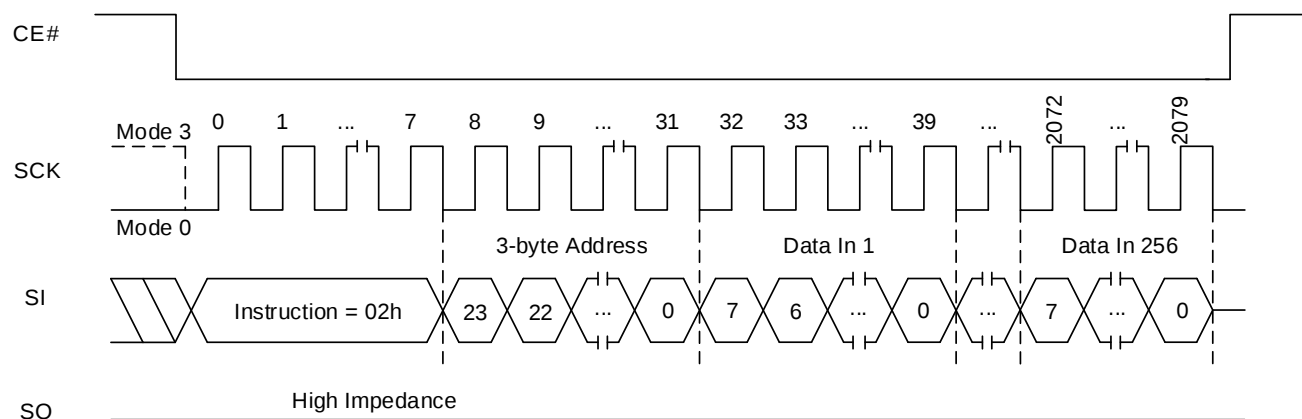
The Page Program (PP) instruction allows up to 256 bytes data to be programmed into memory in a single operation. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A PP instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of PP instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The PP instruction code, three address bytes and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the PP instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is "1", the program operation is still in progress. If WIP bit is "0", the program operation has completed.

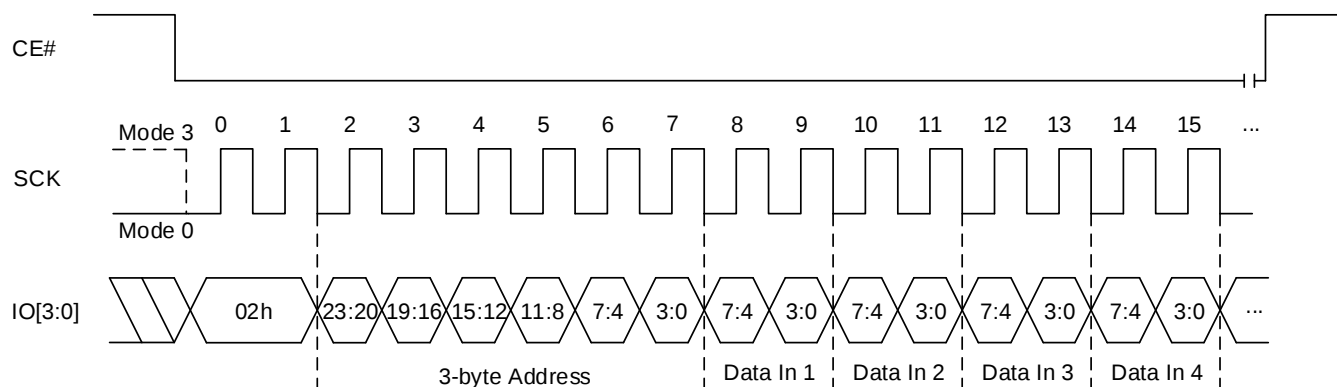
If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

**Note: A program operation can alter "1"s into "0"s. The same byte location or page may be programmed more than once, to incrementally change "1"s to "0"s. An erase operation is required to change "0"s to "1"s.**

**Figure 8.11 Page Program Sequence in SPI Mode**



**Figure 8.12 Page Program Sequence in QPI Mode**



## 8.9 QUAD INPUT PAGE PROGRAM OPERATION (PPQ, 32h/38h)

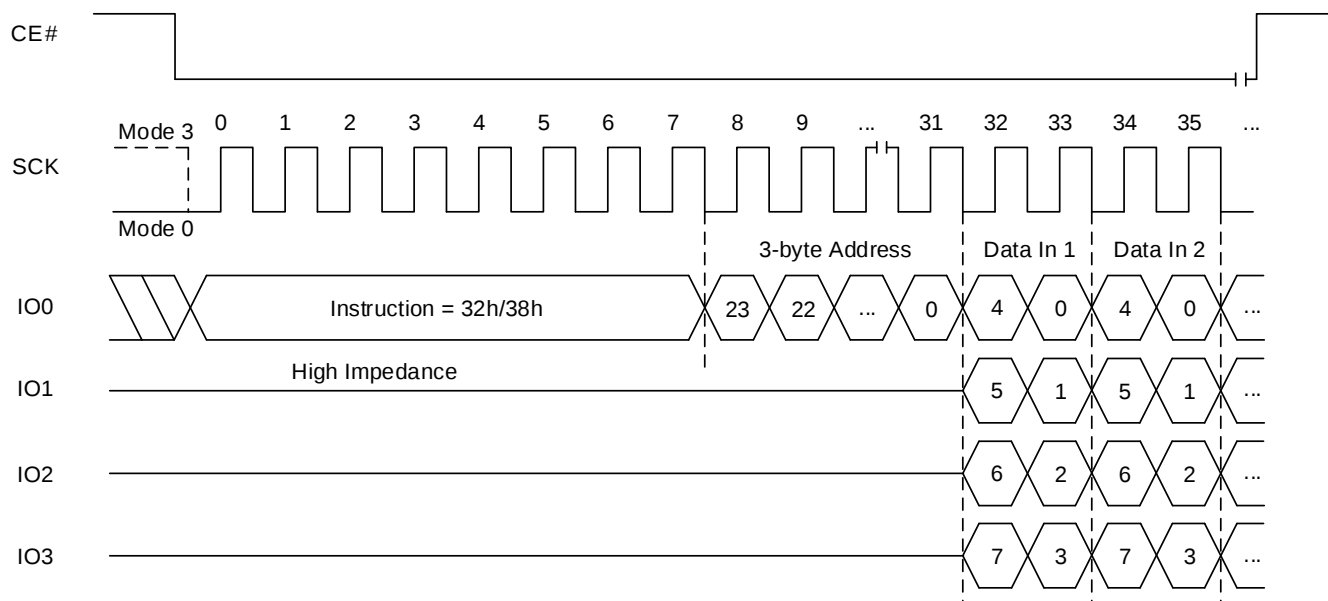
The Quad Input Page Program instruction allows up to 256 bytes data to be programmed into memory in a single operation with four pins (IO0, IO1, IO2 and IO3). The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A Quad Input Page Program instruction which attempts to program into a page that is write-protected will be ignored. Before the execution of Quad Input Page Program instruction, the QE bit in the Status Register must be set to “1” and the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The Quad Input Page Program instruction code, three address bytes and program data (1 to 256 bytes) are input via the four pins (IO0, IO1, IO2 and IO3). Program operation will start immediately after the CE# is brought high, otherwise the Quad Input Page Program instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

**Note:** A program operation can alter “1”s into “0”s. The same byte location or page may be programmed more than once, to incrementally change “1”s to “0”s. An erase operation is required to change “0”s to “1”s.

Figure 8.13 Quad Input Page Program Sequence



## **8.10 ERASE OPERATION**

The Erase command sets all bits in the addressed sector or block to “1”s.

The memory array of the 512Kb/256Kb (IS25LP/WP512E/025E) is organized into uniform 4Kbyte sectors or 32Kbyte uniform blocks (a block consists of eight adjacent sectors).

The memory array of the 4Mb/2Mb/1Mb (IS25LP/WP040E/020E/010E) is organized into uniform 4Kbyte sectors or 32/64Kbyte uniform blocks (a block consists of eight/sixteen adjacent sectors respectively).

In order to erase the device, there are three erase instructions available: Sector Erase (SER), Block Erase (BER) and Chip Erase (CER). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A sector erase, block erase or chip erase operation can be executed prior to any programming operation.

### 8.11 SECTOR ERASE OPERATION (SER, D7h/20h)

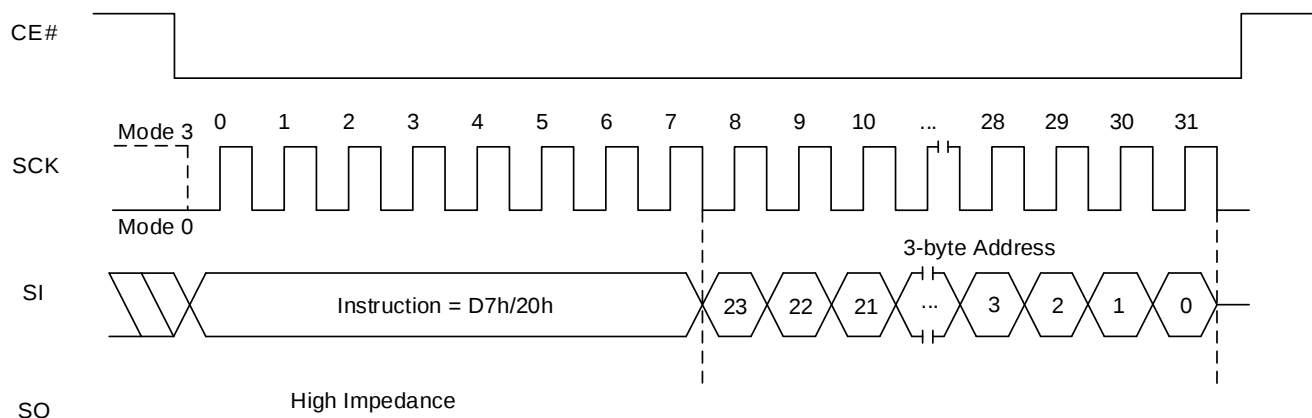
A Sector Erase (SER) instruction erases a 4 Kbyte sector before the execution of a SER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is automatically reset after the completion of Sector Erase operation.

A SER instruction is entered, after CE# is pulled low to select the device and stays low during the entire instruction sequence. The SER instruction code, and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing.

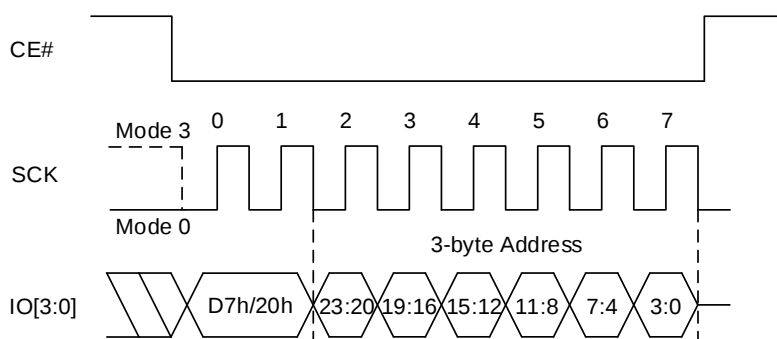
The progress or completion of the erase operation can be determined by reading the WIP bit in the Status Register using a RDSR instruction.

If the WIP bit is "1", the erase operation is still in progress. If the WIP bit is "0", the erase operation has been completed.

**Figure 8.14 Sector Erase Sequence In SPI Mode**



**Figure 8.15 Sector Erase Sequence In QPI Mode**



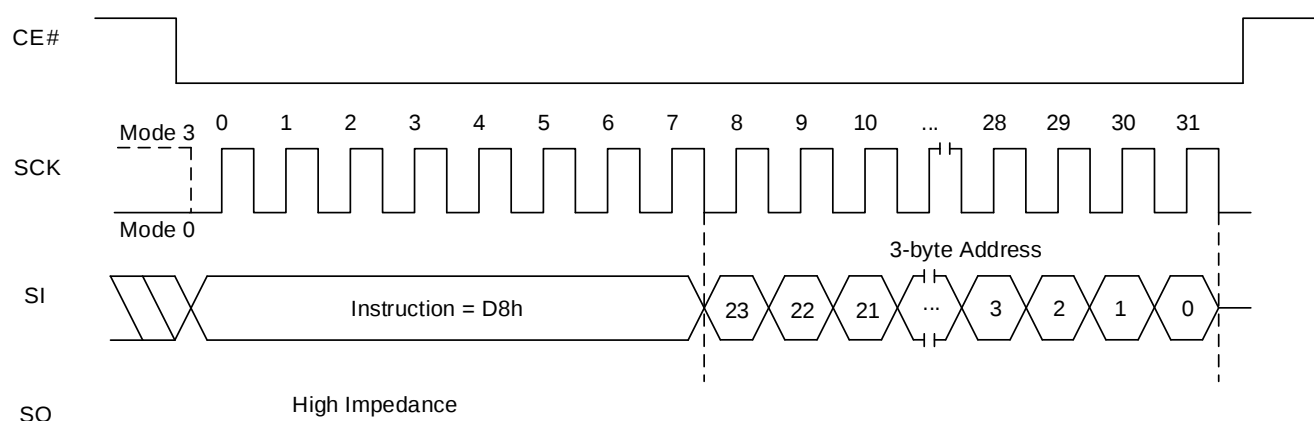
## 8.12 BLOCK ERASE OPERATION (BER32K:52h or 52h/D8h, BER64K:D8h)

A Block Erase (BER) instruction erases a 32/64Kbyte block. Before the execution of a BER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a block erase operation.

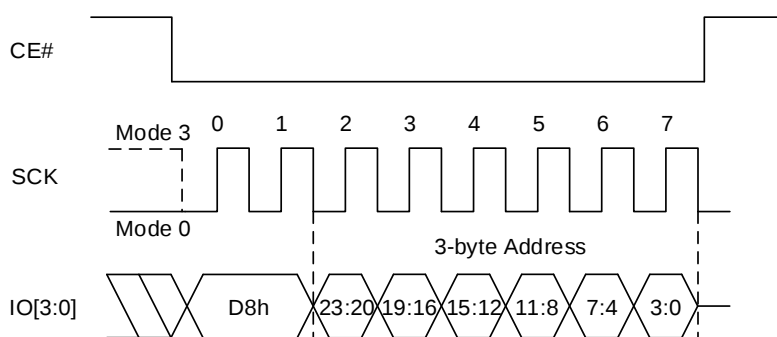
In 256Kb/512Kb (IS25LP/WP512E/025E), there is a 32KB block only, both 52h and D8h are for BER32K command. But in 4Mb/2Mb/1Mb (IS25LP/WP040E/020E/010E), there are 32KB block and 64KB block, so 52h is for BER32K command, and D8h is for BER64K command.

The BER instruction code and three address bytes are input via SI. Erase operation will start immediately after the CE# is pulled high, otherwise the BER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing.

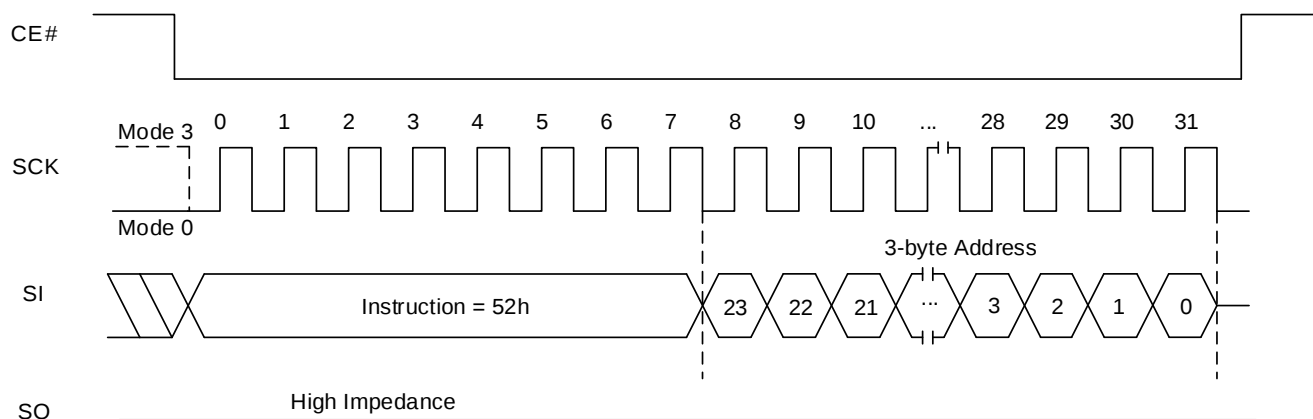
**Figure 8.16 Block Erase (64KB) Sequence In SPI Mode**



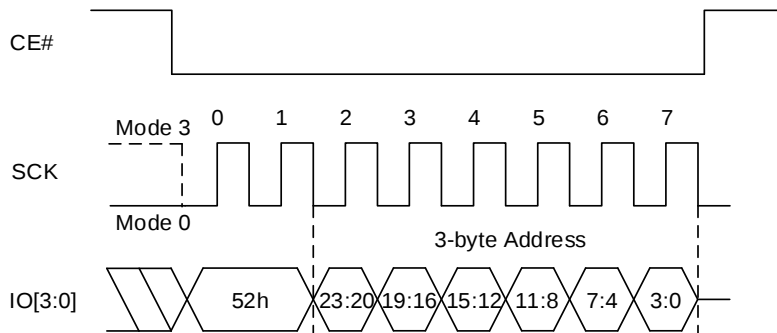
**Figure 8.17 Block Erase (64KB) Sequence In QPI Mode**



**Figure 8.18 Block Erase (32KB) Sequence In SPI Mode**



**Figure 8.19 Block Erase (32KB) Sequence In QPI Mode**

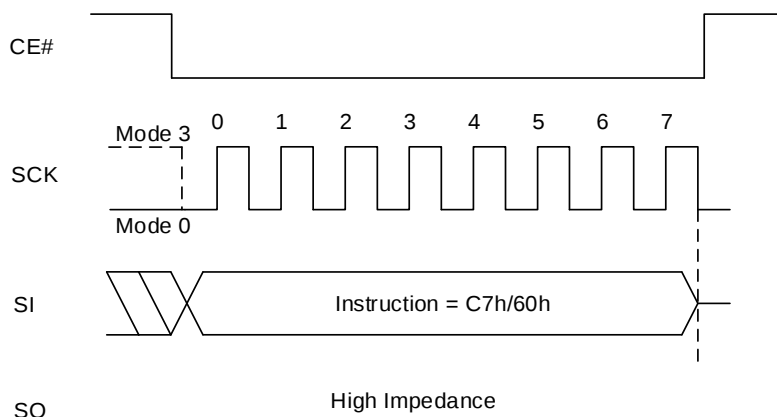


### 8.13 CHIP ERASE OPERATION (CER, C7h/60h)

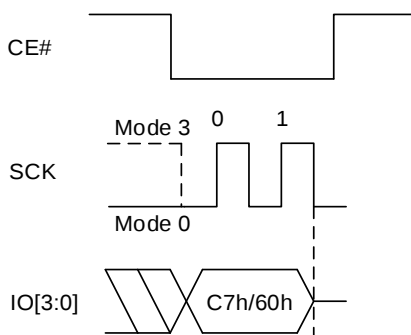
A Chip Erase (CER) instruction erases the entire memory array. Before the execution of CER instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is automatically reset after completion of a chip erase operation.

The CER instruction code is input via the SI. Erase operation will start immediately after CE# is pulled high, otherwise the CER instruction will not be executed. The internal control logic automatically handles the erase voltage and timing.

**Figure 8.20 Chip Erase Sequence In SPI Mode**



**Figure 8.21 Chip Erase Sequence In QPI Mode**

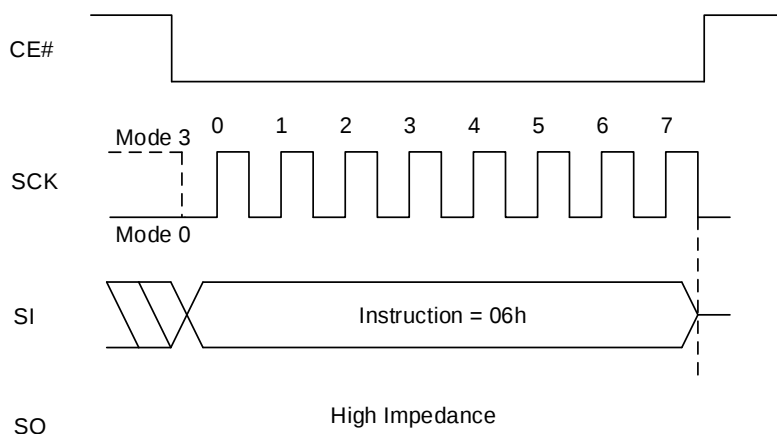


### 8.14 WRITE ENABLE OPERATION (WREN, 06h)

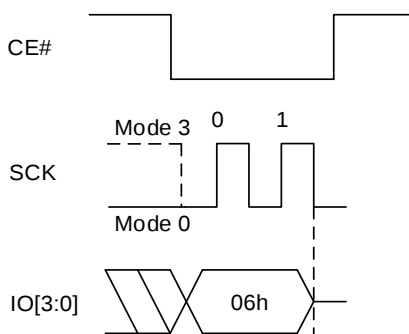
The Write Enable (WREN) instruction is used to set the Write Enable Latch (WEL) bit. The WEL bit is reset to the write-protected state after power-up. The WEL bit must be write enabled before any write operation, including Sector Erase, Block Erase, Chip Erase, Page Program, Program Information Row, Write Non-Volatile Status Register, and Write Function Register operations except for Write Volatile Status Register.

The WEL bit will be reset to the write-protected state automatically upon completion of a write operation. The WREN instruction is required before any above operation is executed.

**Figure 8.22 Write Enable Sequence In SPI Mode**



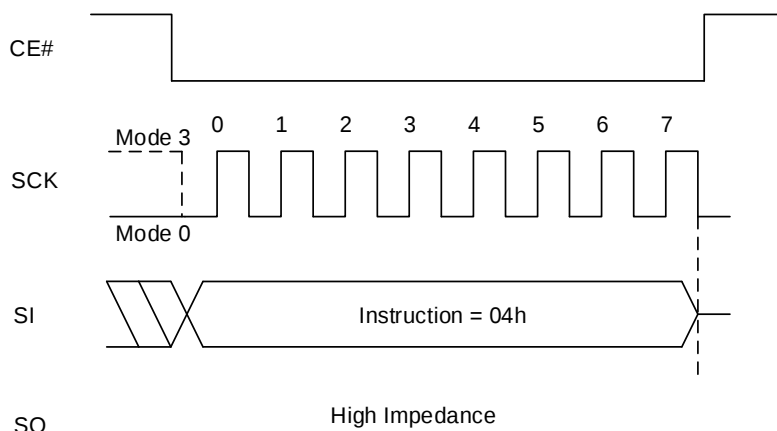
**Figure 8.23 Write Enable Sequence In QPI Mode**



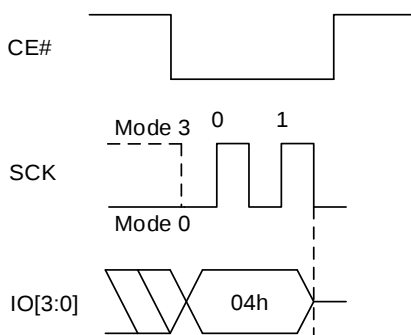
### 8.15 WRITE DISABLE OPERATION (WRDI, 04h)

The Write Disable (WRDI) instruction resets the WEL bit and disables all write instructions. The WRDI instruction is not required after the execution of a write instruction, since the WEL bit is automatically reset.

**Figure 8.24 Write Disable Sequence In SPI Mode**



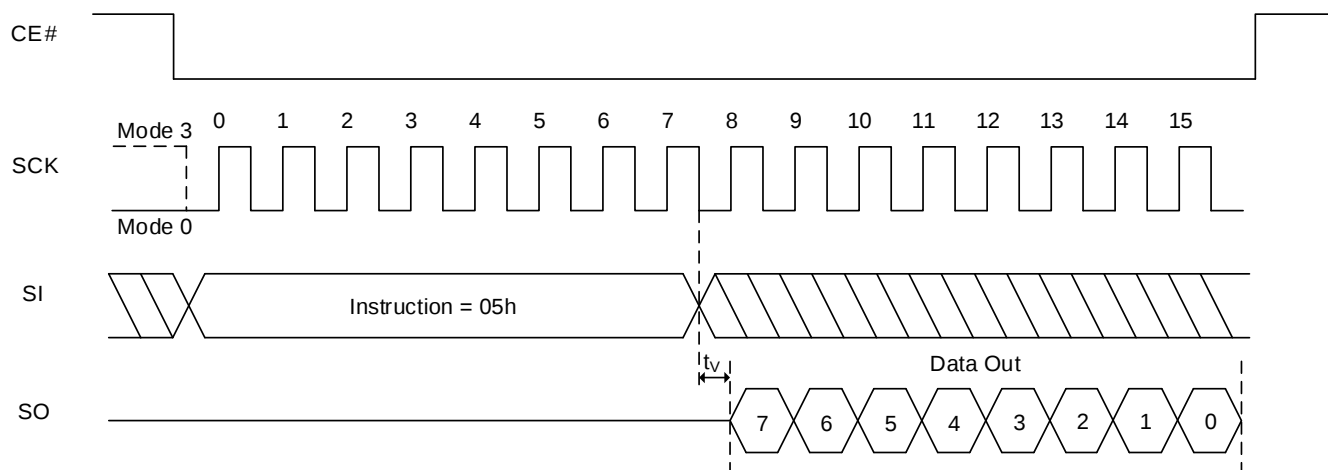
**Figure 8.25 Write Disable Sequence In QPI Mode**



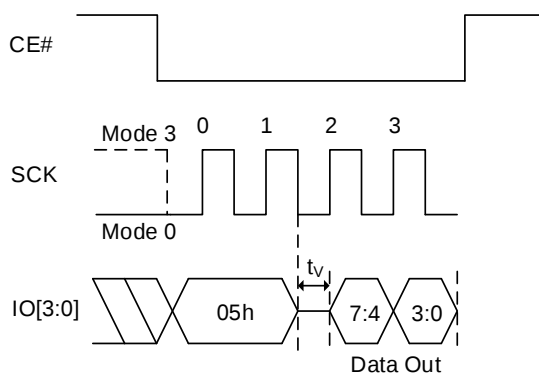
### 8.16 READ STATUS REGISTER OPERATION (RDSR, 05h)

The Read Status Register (RDSR) instruction provides access to the Status Register. During the execution of a program, erase or write Status Register operation, RDSR instruction can be used to check the progress or completion of an operation by reading the WIP bit of Status Register.

**Figure 8.26 Read Status Register Sequence In SPI Mode**



**Figure 8.27 Read Status Register Sequence In QPI Mode**

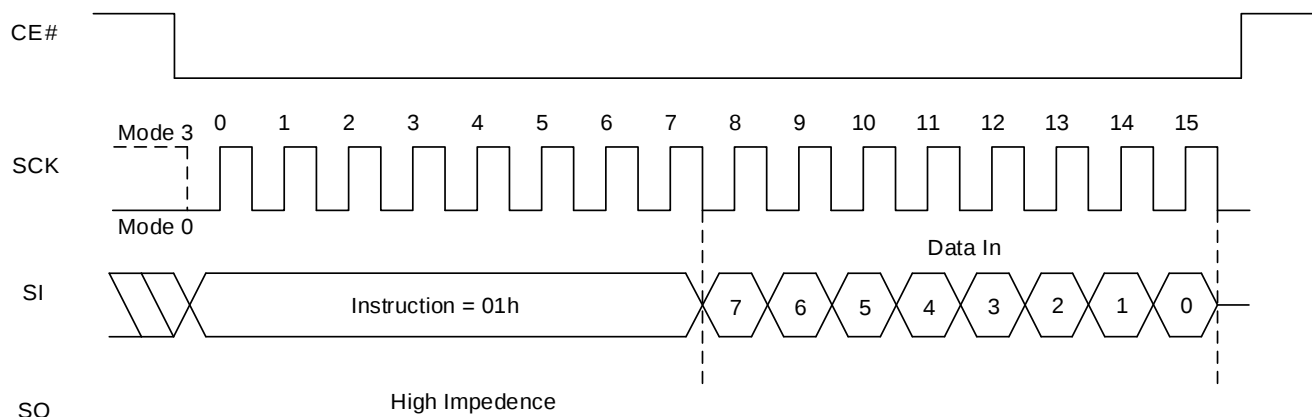


### 8.17 WRITE STATUS REGISTER OPERATION (WRSR, 01h)

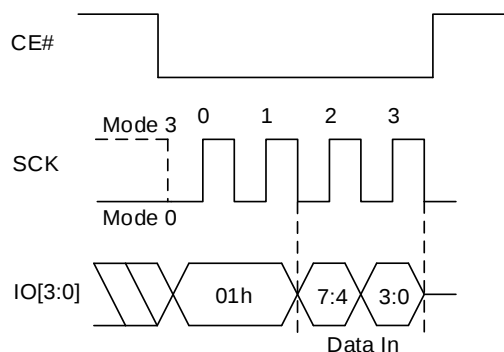
The Write Status Register (WRSR) instruction allows the user to enable or disable the block protection and Status Register write protection features by writing “0”s or “1”s into the volatile/non-volatile BP3, BP2, BP1, BP0, and SRWD bits. Also WRSR instruction allows the user to disable or enable quad operation by writing “0” or “1” into the volatile/non-volatile QE bit.

To write Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept Write Status Register (01h) instruction (Status Register bit WEL must equal 1).

**Figure 8.28 Write Status Register Sequence In SPI Mode**



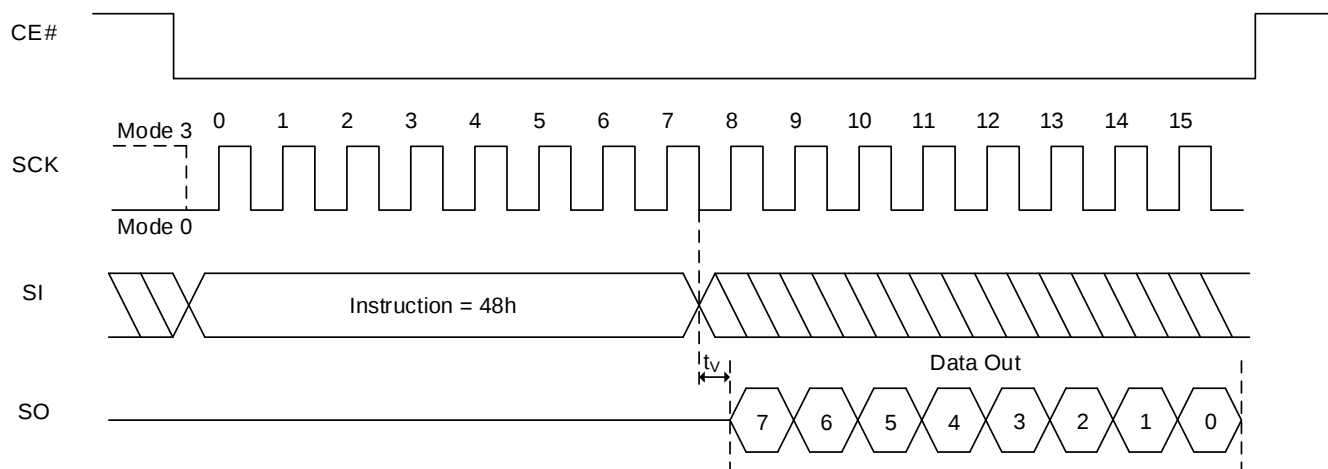
**Figure 8.29 Write Status Register Sequence In QPI Mode**



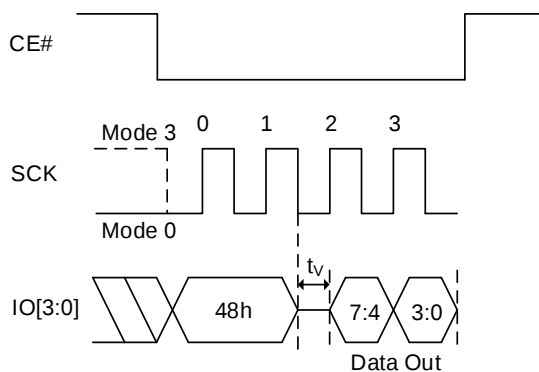
## 8.18 READ FUNCTION REGISTER OPERATION (RDFR, 48h)

The Read Function Register (RDFR) instruction provides access to the Function Register.

**Figure 8.30 Read Function Register Sequence In SPI Mode**



**Figure 8.31 Read Function Register Sequence In QPI Mode**

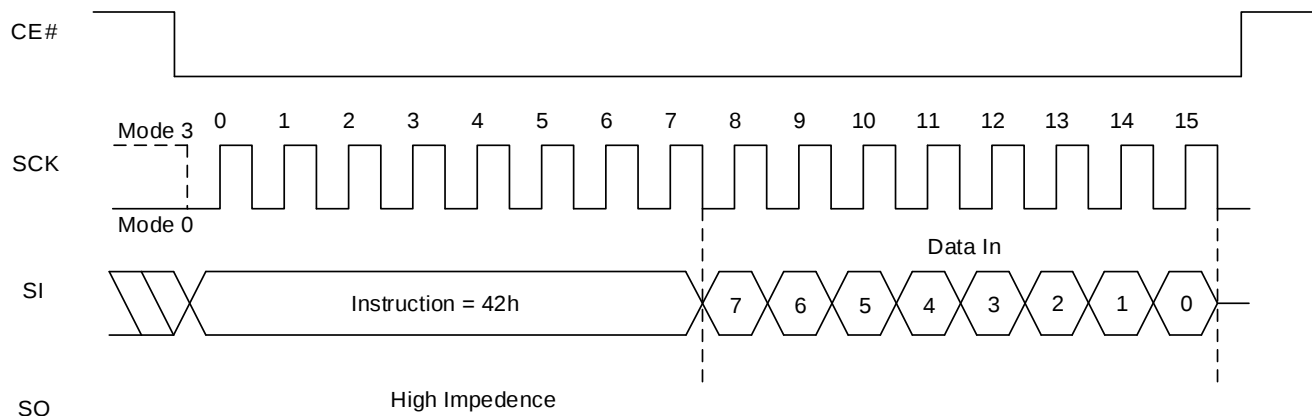


### 8.19 WRITE FUNCTION REGISTER OPERATION (WRFR, 42h)

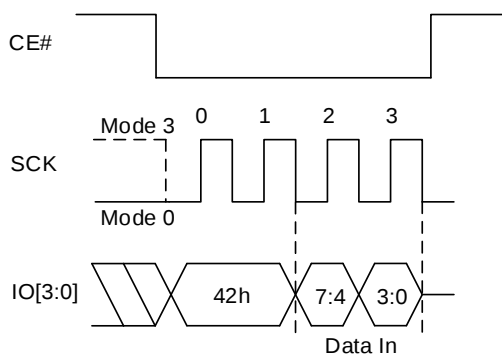
Information Row Lock bits (IRL3~IRL0) can be set to “1” individually by WRFR instruction in order to lock Information Row. Since IRL bits are OTP, once it is set to “1”, it cannot set back to “0” again.

Before the execution of a WRFR instruction, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL is reset automatically after the completion of a write function register operation.

**Figure 8.32 Write Function Register Sequence In SPI Mode**



**Figure 8.33 Write Function Register QPI Sequence In QPI Mode**

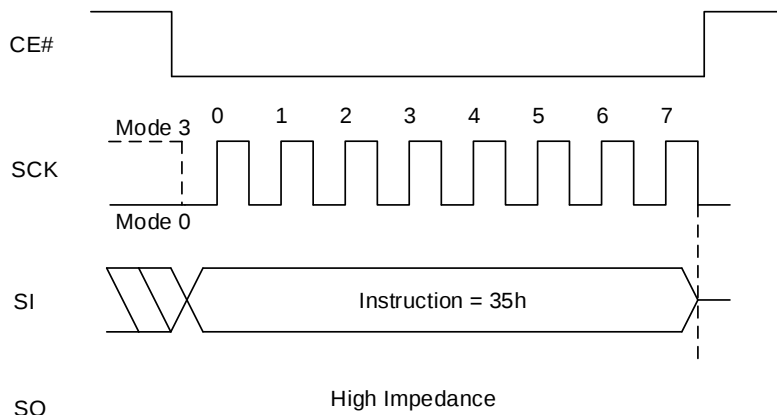


## 8.20 ENTER QUAD PERIPHERAL INTERFACE (QPI) MODE OPERATION (QPIEN, 35h; QPIDI, F5h)

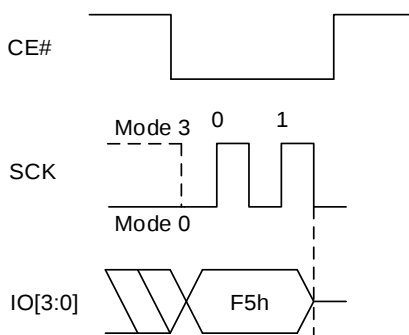
The Enter Quad Peripheral Interface (QPIEN) instruction, 35h, enables the Flash device for QPI bus operation. Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or an Exit Quad Peripheral Interface instruction is sent to device.

The Exit Quad Peripheral Interface (QPIDI) instruction, F5h, resets the device to 1-bit SPI protocol operation. To execute an Exit Quad Peripheral Interface operation, the host drives CE# low, sends the QPIDI instruction, then drives CE# high. The device just accepts QPI (2 clocks) command cycles.

**Figure 8.34 Enter Quad Peripheral Interface (QPI) Mode Sequence**



**Figure 8.35 Exit Quad Peripheral Interface (QPI) Mode Sequence**



## 8.21 PROGRAM/ERASE SUSPEND & RESUME

The device allows the interruption of Sector Erase, Block Erase, or Page Program operations to conduct other operations. 75h/B0h command for suspend and 7Ah/30h for resume will be used. (SPI/QPI all acceptable) Function Register bit2 (PSUS) and bit3 (ESUS) are used to check whether or not the device is in suspend mode.

Suspend to read ready timing ( $t_{SUS}$ ): 100 $\mu$ s (TYP)

Resume to another suspend timing ( $t_{RS}$ ): 80 $\mu$ s (TYP)

### SUSPEND DURING SECTOR-ERASE OR BLOCK-ERASE (PERSUS 75h/B0h)

The Suspend command allows the interruption of Sector Erase and Block Erase operations. But Suspend command will be ignored during Chip Erase operation. After the Suspend command, other commands include array read operation can be accepted.

But Write Status Register command (01h) and Erase instructions are not allowed during Erase Suspend. Also, array read for being erased sector/block is not allowed.

To execute Erase Suspend operation, the host drives CE# low, sends the Suspend command cycle (75h/B0h), then drives CE# high. The Function Register indicates that the Erase has been suspended by setting the ESUS bit from "0" to "1", but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit or wait the specified time  $t_{SUS}$ . When ESUS bit is set to "1", the Write Enable Latch (WEL) bit clears to "0".

### SUSPEND DURING PAGE PROGRAMMING (PERSUS 75h/B0h)

The Suspend command also allows the interruption of all array Program operations. After the Suspend command, other commands include array read operation can be accepted.

But Write Status Register instruction (01h) and Program instructions are not allowed during Program Suspend. Also, array read for being programmed page is not allowed.

To execute the Program Suspend operation, the host drives CE# low, sends the Suspend command cycle (75h/B0h), then drives CE# high. The Function Register indicates that the programming has been suspended by setting the PSUS bit from "0" to "1", but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit or wait the specified time  $t_{SUS}$ . When PSUS bit is set to "1", the Write Enable Latch (WEL) bit clears to "0".

### PROGRAM/ERASE RESUME (PERRSM 7Ah/30h)

The Program/Erase Resume restarts the Program or Erase command that was suspended, and clears the suspend status bit in the Function Register (ESUS or PSUS bits) to "0". To execute the Program/Erase Resume operation, the host drives CE# low, sends the Program/Erase Resume command cycle (7Ah/30h), then drives CE# high. A cycle is two nibbles long, most significant nibble first. To issue another Erase Suspend operation after Erase Resume operation, Erase Resume to another Erase Suspend delay ( $t_{RS}$ ) is required, but it could require longer Erase time to complete Erase operation.

To determine if the internal, self-timed Write operation completed, poll the WIP bit.

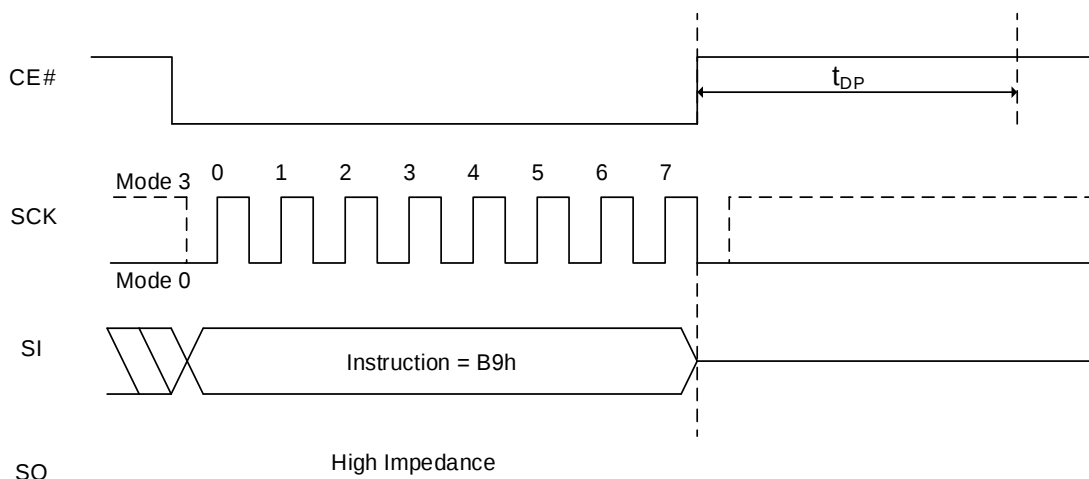
**Table 8.4 Instructions accepted during Suspend**

| Operation Suspended | Instruction Allowed |          |                                                                                            |
|---------------------|---------------------|----------|--------------------------------------------------------------------------------------------|
|                     | Name                | Hex Code | Operation                                                                                  |
| Program or Erase    | NORD                | 03h      | Read Data Bytes from Memory at Normal Read Mode                                            |
| Program or Erase    | FRD                 | 0Bh      | Read Data Bytes from Memory at Fast Read Mode                                              |
| Program or Erase    | FRDIO               | BBh      | Fast Read Dual I/O                                                                         |
| Program or Erase    | FRDO                | 3Bh      | Fast Read Dual Output                                                                      |
| Program or Erase    | FRQIO               | EBh      | Fast Read Quad I/O                                                                         |
| Program or Erase    | FRQO                | 6Bh      | Fast Read Quad Output                                                                      |
| Program or Erase    | WREN                | 06h      | Write Enable                                                                               |
| Program or Erase    | WRDI                | 04h      | Write Disable                                                                              |
| Program or Erase    | WRSR                | 01h      | Write Volatile Status Register                                                             |
| Erase               | PP <sup>(1)</sup>   | 02h      | Serial Input Page Program                                                                  |
| Erase               | PPQ <sup>(1)</sup>  | 32h/38h  | Quad Input Page Program                                                                    |
| Program or Erase    | RDSR                | 05h      | Read Status Register                                                                       |
| Program or Erase    | RDFR                | 48h      | Read Function Register                                                                     |
| Program or Erase    | PERRSM              | 7Ah/30h  | Program/Erase Resume                                                                       |
| Erase               | PERRSM              | 75h/B0h  | Program/Erase Suspend (to suspend program operation in another block during Erase suspend) |
| Program or Erase    | RDID                | ABh      | Read Manufacturer and Product ID                                                           |
| Program or Erase    | RDJDID              | 9Fh      | Read JEDEC ID                                                                              |
| Program or Erase    | RDJDIDQ             | AFh      | Read JEDEC ID in QPI mode                                                                  |
| Program or Erase    | RDMDID              | 90h      | Read Manufacturer and Device ID                                                            |
| Program or Erase    | RDUID               | 4Bh      | Read Unique ID Number                                                                      |
| Program or Erase    | RDSFDP              | 5Ah      | SFDP Read                                                                                  |
| Program or Erase    | NOP                 | 00h      | No Operation                                                                               |
| Program or Erase    | RSTEN               | 66h      | Software reset enable                                                                      |
| Program or Erase    | RST                 | 99h      | Reset (Only along with 66h)                                                                |
| Program or Erase    | IRRD                | 68h      | Read Information Row                                                                       |
| Erase               | SECUNLOCK           | 26h      | Sector Unlock                                                                              |
| Erase               | SECLOCK             | 24h      | Sector Lock                                                                                |
| Program or Erase    | QPIEN               | 35h      | Enter QPI mode                                                                             |
| Program or Erase    | QPIDI               | F5h      | Exit QPI mode                                                                              |
| Program or Erase    | STWBR               | C0h      | Set Wrapped Burst Read                                                                     |

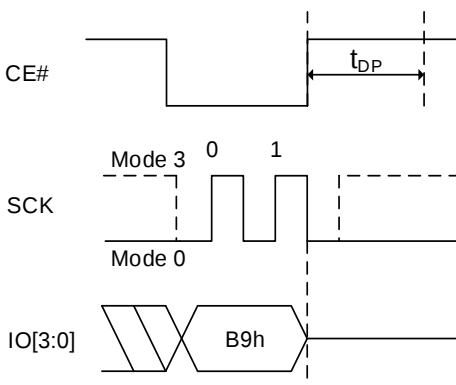
## 8.22 ENTER DEEP POWER DOWN (DP, B9h)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (enter into Power-down mode). During this mode, standby current is reduced from  $I_{sb1}$  to  $I_{sb2}$ . While in the Power-down mode, the device is not active and all Write/Program/Erase instructions are ignored. The instruction is initiated by driving the CE# pin low and shifting the instruction code into the device. The CE# pin must be driven high after the instruction has been latched, or Power-down mode will not engage. Once CE# pin driven high, the Power-down mode will be entered within the time duration of  $t_{DP}$ . While in the Power-down mode only the Release from Power-down/RDID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored, including the Read Status Register instruction which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. It is available in both SPI and QPI mode.

**Figure 8.36 Enter Deep Power Down Mode Sequence In SPI Mode**



**Figure 8.37 Enter Deep Power Down Mode Sequence In QPI Mode**

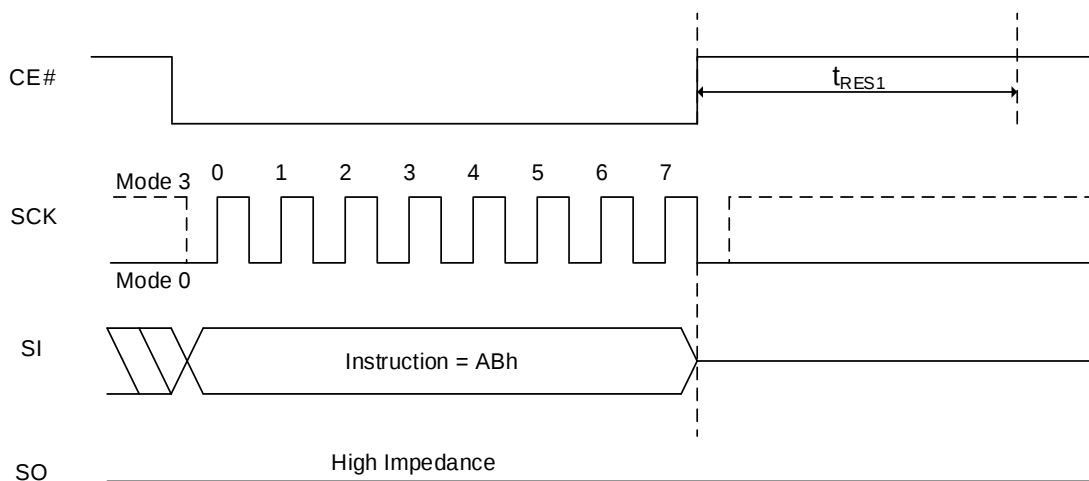


### 8.23 RELEASE DEEP POWER DOWN (RDPD, ABh)

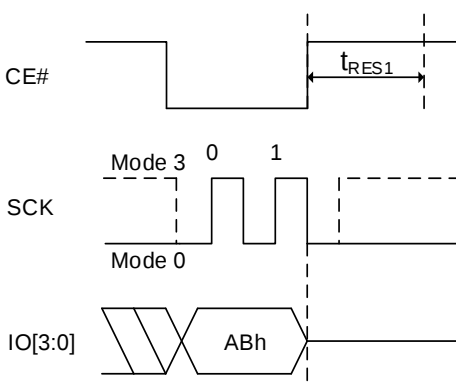
The Release Deep Power-down/Read Device ID instruction is a multi-purpose command. To release the device from the Power-down mode, the instruction is issued by driving the CE# pin low, shifting the instruction code “ABh” and driving CE# high.

Releasing the device from Power-down mode will take the time duration of  $t_{RES1}$  before normal operation is restored and other instructions are accepted. The CE# pin must remain high during the  $t_{RES1}$  time duration. If the Release Deep Power-down/RDID instruction is issued while an Erase, Program or Write cycle is in progress (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

**Figure 8.38 Release Deep Power Down Mode Sequence In SPI Mode**



**Figure 8.39 Release Deep Power Down Mode Sequence In QPI Mode**



## 8.24 SET WRAPPED BURST READ (STWBR, C0h)

The device is capable of wrapped burst read operation in both SPI and QPI mode. Wrapped burst read and the size of burst length are set by using C0h instruction like below:

C0h command is followed by 1 byte data, and wrapped burst and burst length are set like below table:

| Data | Wrap Around | Burst Length |
|------|-------------|--------------|
| 10h  | Yes         | 8-byte       |
| 11h  | Yes         | 16-byte      |
| 12h  | Yes         | 32-byte      |
| 13h  | Yes         | 64-byte      |
| 0Xh  | No          | X            |

By default, address increases by one up through the entire array (Linear Burst). By setting the burst length, the data being accessed can be limited to the length of burst boundary within a 256 byte page, with random initial address. The first output will be the data at the initial address which is specified in the instruction. Following data will come out from the next address within the burst boundary. Once the address reaches the end of boundary, it will automatically move to the first address of the boundary. CE# high will terminate read operation.

For example, if burst length of 8 and initial address being applied is 0h, following byte output will be from address 00h and continue to 01h,...,07h, 00h, 01h... until CE# terminates the operation. If burst length of 8 and initial address being applied is FEh(254d), following byte output will be from address FEh and continue to FFh, F8h, F9h, FAh, FBh, FCh, FDh, and repeat from FEh until CE# terminates the operation.

To exit the wrapped burst mode, it is required to issue another "C0h" command with data = 1Xh. Otherwise, wrapped burst read mode will be maintained until either power down or reset operation.

To change burst length, it is required to issue another "C0h" command with 1 byte data.

**Figure 8.40 Set Wrapped Burst Read Sequence In SPI Mode**

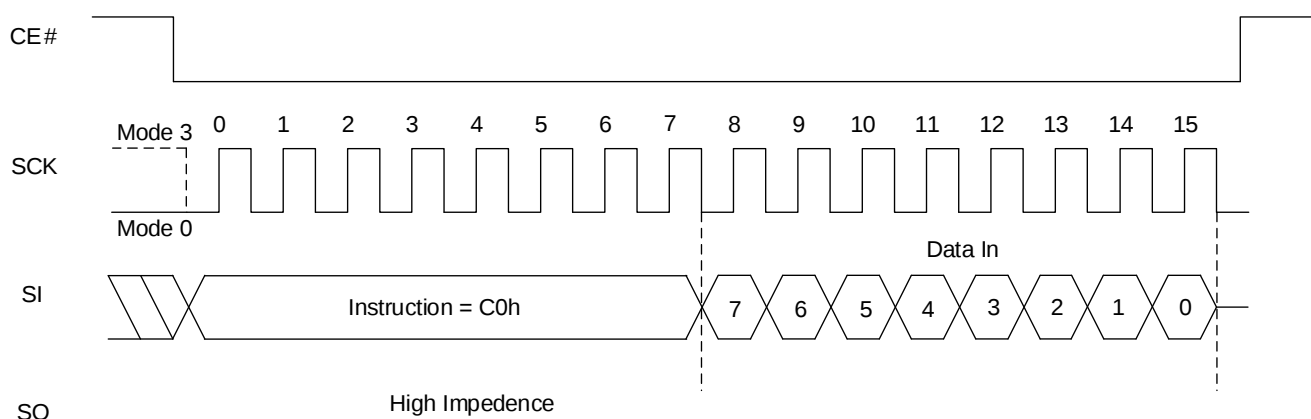
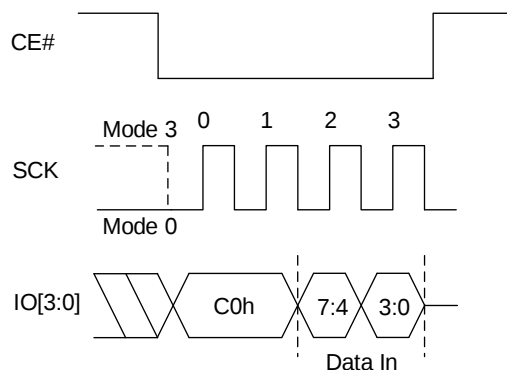


Figure 8.41 Set Wrapped Burst Read Sequence In QPI Mode



## 8.25 READ PRODUCT IDENTIFICATION (RDID, ABh)

The Release from Power-down/Read Device ID instruction is a multi-purpose instruction. It can support both SPI and QPI modes. The Read Product Identification (RDID) instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of Product Identification.

The RDID instruction code is followed by three dummy bytes, each bit being latched-in on SI during the rising SCK edge. Then the Device ID is shifted out on SO with the MSB first, each bit been shifted out during the falling edge of SCK. The RDID instruction is ended by driving CE# high. The Device ID (ID7-ID0) outputs repeatedly if additional clock cycles are continuously sent to SCK while CE# is at low.

**Table 8.5 Product Identification**

| Manufacturer ID   |                     | (MF7-MF0)                         |     |
|-------------------|---------------------|-----------------------------------|-----|
| ISSI Serial Flash |                     | 9Dh                               |     |
| Instruction       | ABh                 | 90h                               | 9Fh |
| Part Number       | Device ID (ID7-ID0) | Memory Type + Capacity (ID15-ID0) |     |
| IS25LP040E        | 12h                 | 4013h                             |     |
| IS25LP020E        | 11h                 | 4012h                             |     |
| IS25LP010E        | 10h                 | 4011h                             |     |
| IS25LP512E        | 05h                 | 4010h                             |     |
| IS25LP025E        | 02h                 | 4009h                             |     |
| IS25WP040E        | 12h                 | 7013h                             |     |
| IS25WP020E        | 11h                 | 7012h                             |     |
| IS25WP010E        | 10h                 | 7011h                             |     |
| IS25WP512E        | 05h                 | 7010h                             |     |
| IS25WP025E        | 02h                 | 7009h                             |     |

Figure 8.42 RDID (Read Product Identification) Sequence In SPI Mode

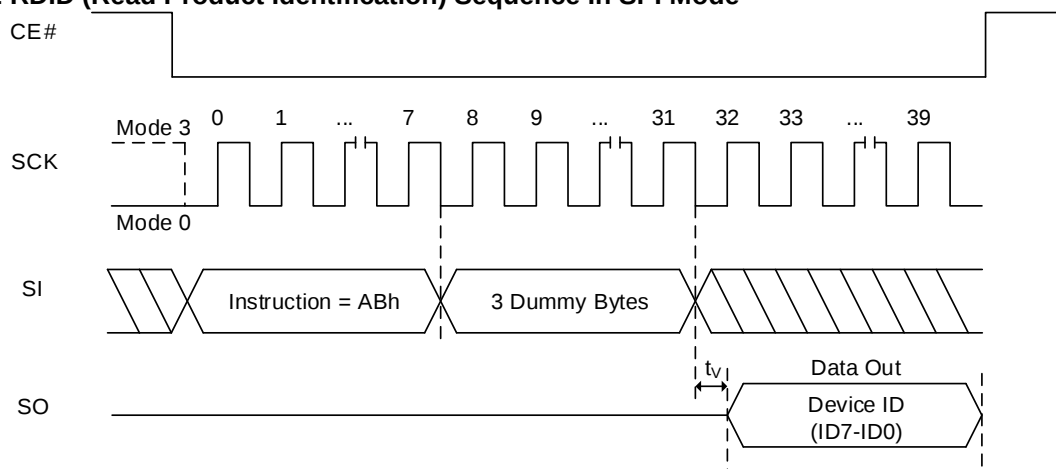
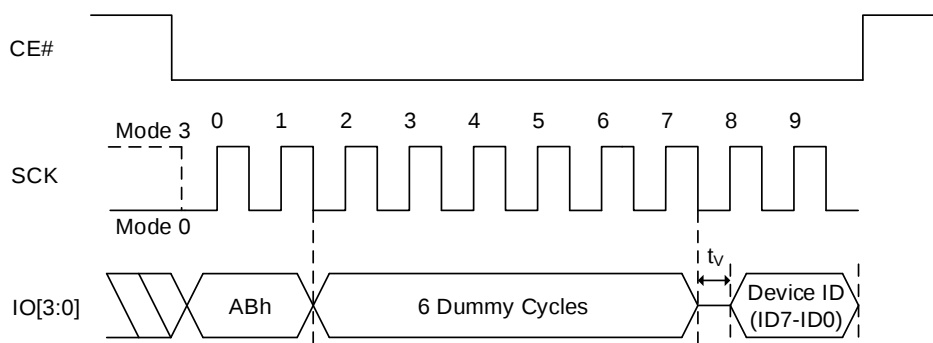


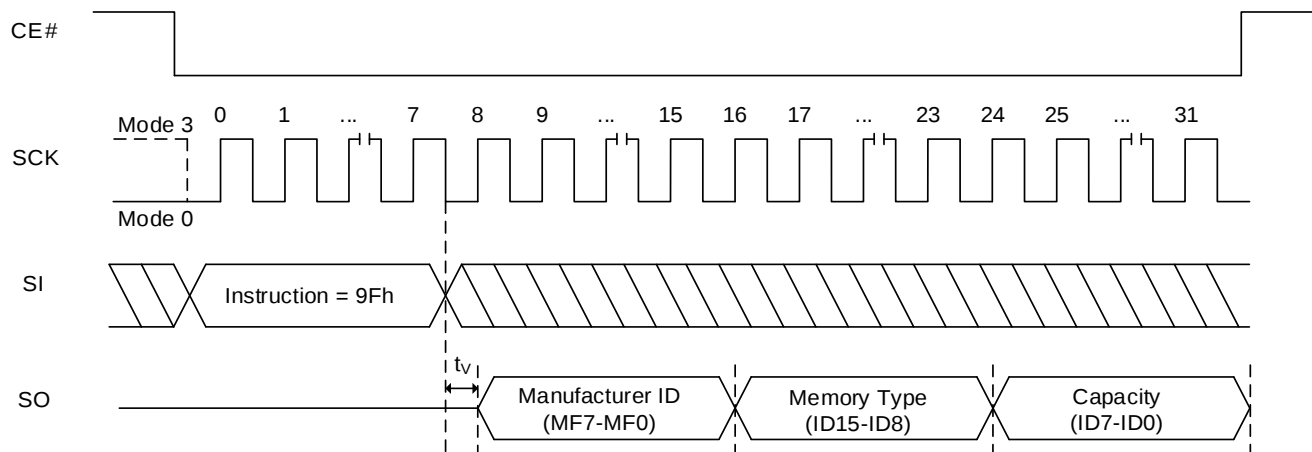
Figure 8.43 RDID (Read Product Identification) Sequence In QPI Mode



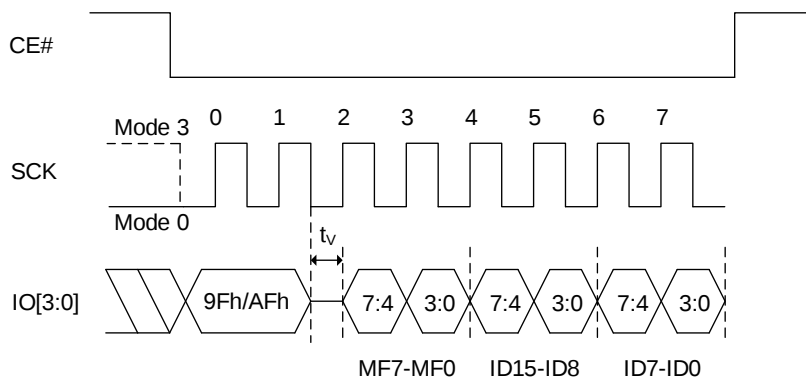
## 8.26 READ PRODUCT IDENTIFICATION BY JEDEC ID OPERATION (RDJDID, 9Fh; RDJDIDQ, AFh)

The JEDEC ID READ instruction allows the user to read the manufacturer and product ID of devices. Refer to Table 8.5 Product Identification for Manufacturer ID and Device ID. After the JEDEC ID READ command (9Fh in SPI mode, AFh in QPI mode) is input, the Manufacturer ID is shifted out MSB first followed by the 2-byte electronic ID (ID15-ID0) that indicates Memory Type and Capacity, one bit at a time. Each bit is shifted out during the falling edge of SCK. If CE# stays low after the last bit of the 2-byte electronic ID, the Manufacturer ID and 2-byte electronic ID will loop until CE# is pulled high.

**Figure 8.44 RDJDID (Read JEDEC ID In SPI Mode) Sequence**



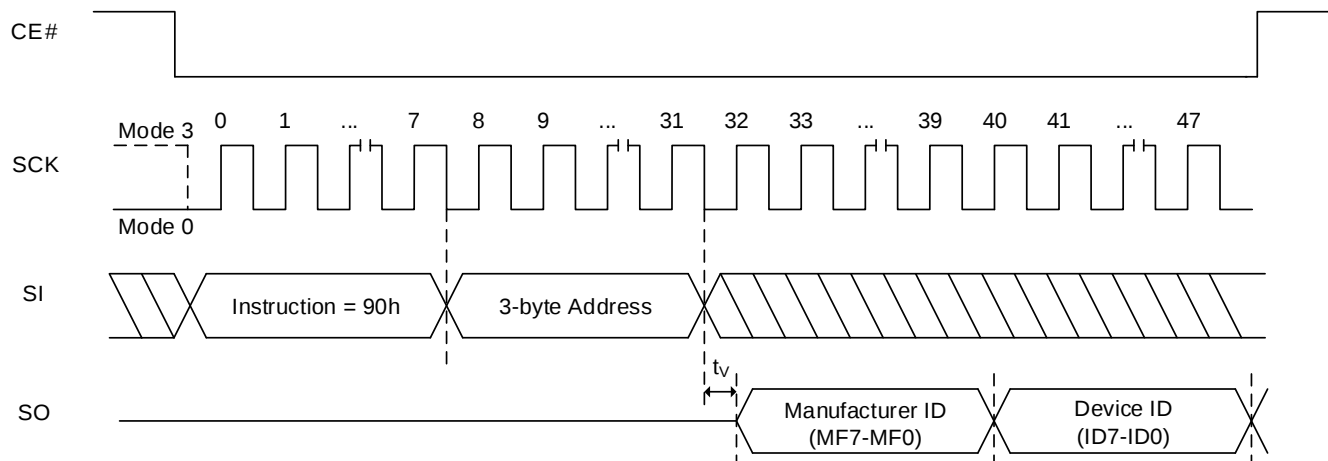
**Figure 8.45 RDJDID and RDJDIDQ DJJDIDQ (Read JEDEC ID In QPI Mode) Sequence**



## 8.27 READ DEVICE MANUFACTURER AND DEVICE ID OPERATION (RDMDID, 90h)

The Read Device Manufacturer and Device ID (RDMDID) instruction allows the user to read the Manufacturer and product ID of devices. Refer to Table 8.5 Product Identification for Manufacturer ID and Device ID. The RDMDID instruction code is followed by two dummy bytes and one byte address (A7~A0), each bit being latched-in on SI during the rising edge of SCK. If one byte address is initially set as A0 = 0, then the Manufacturer ID is shifted out on SO with the MSB first followed by the Device ID (ID7- ID0). Each bit is shifted out during the falling edge of SCK. If one byte address is initially set as A0 = 1, then Device ID will be read first followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously alternating between the two until CE# is driven high.

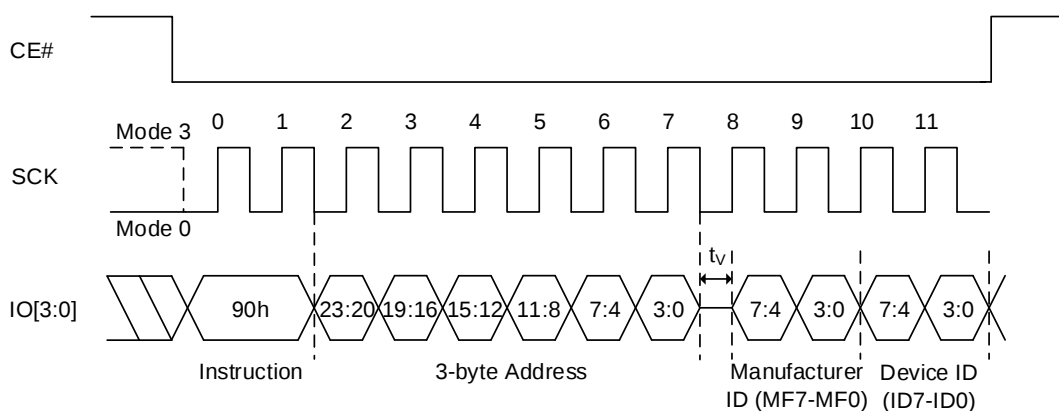
**Figure 8.46 RDMDID (Read Product Identification) Sequence In SPI Mode**



**Notes:**

1. ADDRESS A0 = 0, will output the 1-byte Manufacturer ID (MF7-MF0) → 1-byte Device ID (ID7-ID0)  
ADDRESS A0 = 1, will output the 1-byte Device ID (ID7-ID0) → 1-byte Manufacturer ID (MF7-MF0)
2. The Manufacturer and Device ID can be read continuously and will alternate from one to the other until CE# pin is pulled high.

**Figure 8.47 RDMDID (Read Product Identification) Sequence In QPI Mode**



**Notes:**

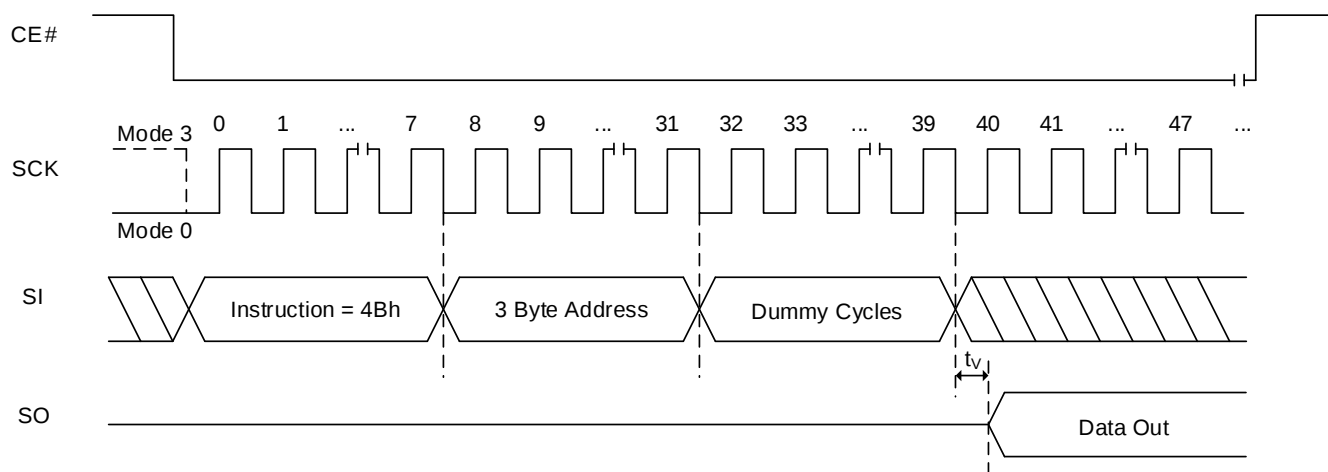
1. ADDRESS A0 = 0, will output the 1-byte Manufacturer ID (MF7-MF0) → 1-byte Device ID (ID7-ID0)  
ADDRESS A0 = 1, will output the 1-byte Device ID (ID7-ID0) → 1-byte Manufacturer ID (MF7-MF0)
2. The Manufacturer and Device ID can be read continuously and will alternate from one to the other until CE# pin is pulled high.

### 8.31 READ UNIQUE ID NUMBER (RDUID, 4Bh)

The Read Unique ID Number (RDUID) instruction accesses a factory-set read-only 16-byte number that is unique to the device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The RDUID instruction is instated by driving the CE# pin low and shifting the instruction code (4Bh) followed by 3 address bytes and dummy cycles (configurable, default is 8 clocks). After which, the 16-byte ID is shifted out on the falling edge of SCK as shown below. As a result, the sequence of RDUID instruction is same as FAST READ. RDUID QPI sequence is also same as FAST READ QPI except for the instruction code. Refer to the FAST READ QPI operation.

**Note:** 16 bytes of data will repeat as long as CE# is low and SCK is toggling.

**Figure 8.48 RDUID Sequence In SPI Mode**



**Table 8.6 Unique ID Addressing**

| A[23:10] | A[9:4] | A[3:0]          |
|----------|--------|-----------------|
| XX       | 00000  | 0h Byte address |
| XX       | 00000  | 1h Byte address |
| XX       | 00000  | 2h Byte address |
| XX       | 00000  | ⋮               |
| XX       | 00000  | Fh Byte address |

**Note:** XX means “don’t care”.

### 8.32 READ SFDP OPERATION (RDSFDP, 5Ah)

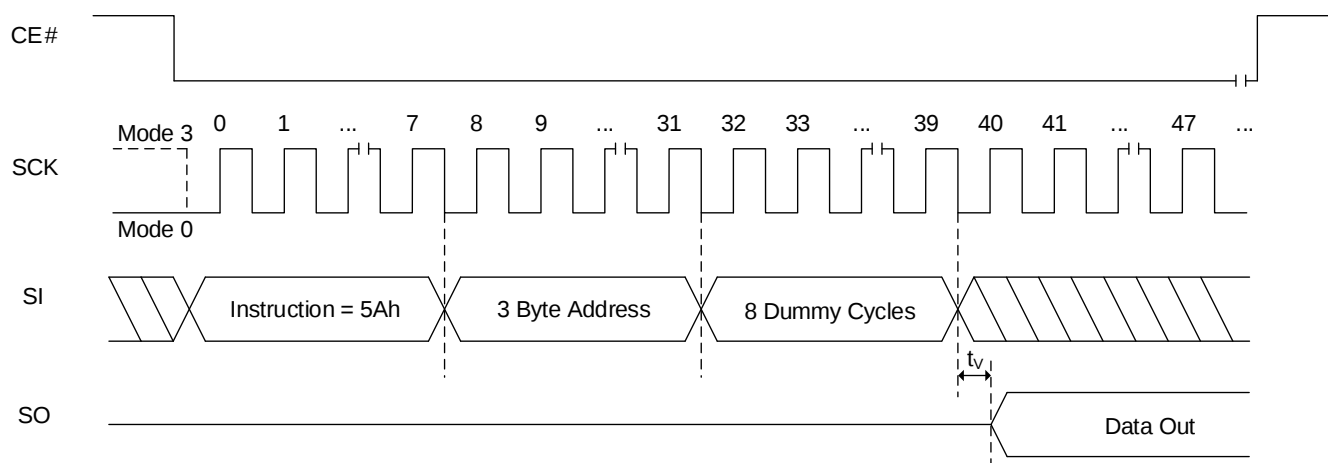
The Serial Flash Discoverable Parameters (SFDP) standard provides a consistent method of describing the functions and features of serial Flash devices in a standard set of internal parameter tables. These parameters can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. For more details please refer to the JEDEC Standard JESD216 (Serial Flash Discoverable Parameters).

The sequence of issuing RDSFDP instruction in SPI mode is:

CE# goes low → Send RDSFDP instruction (5Ah) → Send 3 address bytes on SI pin → 8 dummy cycles on SI pin → Read SFDP code on SO → End RDSFDP operation by driving CE# high at any time during data out. Refer to ISSI's Application note for SFDP table. The data at the addresses that are not specified in SFDP table are undefined.

RDSFDP Sequence in QPI mode, has 8 dummy cycles before SFDP code, too.

**Figure 8.49 RDSFDP (Read SFDP) Sequence In SPI Mode**



### 8.33 NO OPERATION (NOP, 00h)

The No Operation command solely cancels a Reset Enable command and has no impact on any other commands. It is available in both SPI and QPI modes. To execute a NOP, the host drives CE# low, sends the NOP command cycle (00H), then drives CE# high.

### 8.34 SOFTWARE RESET (RESET-ENABLE (RSTEN, 66h) AND RESET (RST, 99h))

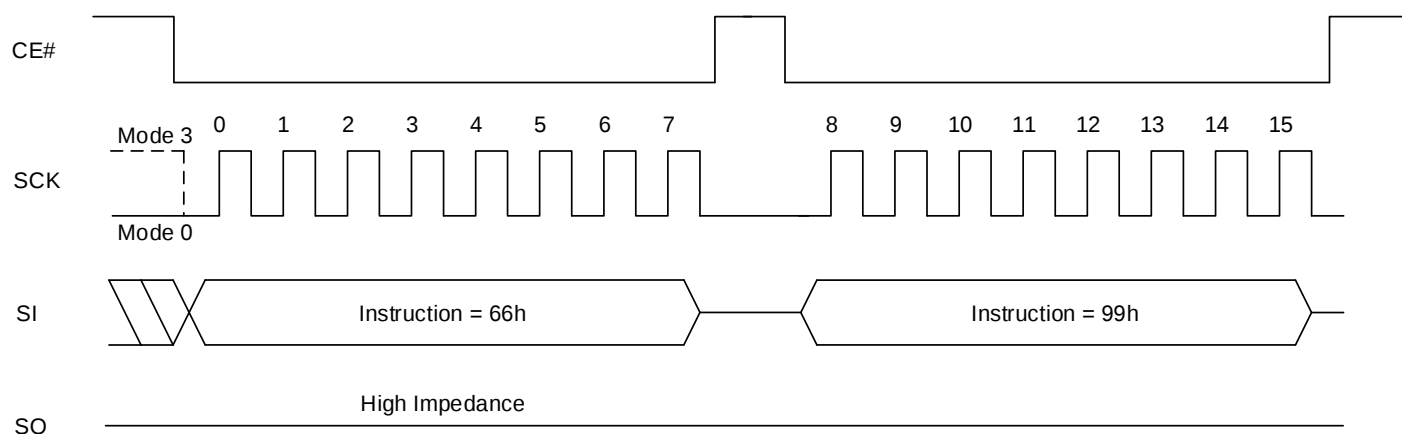
The Reset operation is used as a system (software) reset that puts the device in normal operating mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST). The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

Execute the CE# pin low → sends the Reset-Enable command (66h), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99h), and drives CE# high.

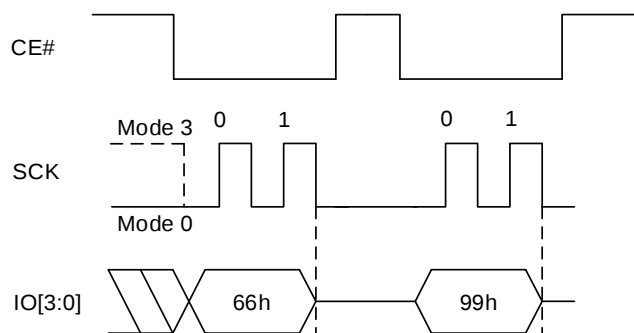
The Software Reset during an active Program or Erase operation aborts the operation, which can result in corrupting or losing the data of the targeted address range. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations.

**Note: The non-volatile Status Register and Function Register remain unaffected by Software RESET.**

**Figure 8.50 Software Reset Enable and Software Reset Sequence In SPI Mode (RSTEN, 66h + RST, 99h)**



**Figure 8.51 Software Reset Enable and Software Reset Sequence In QPI Mode (RSTEN, 66h + RST, 99h)**



### 8.35 SECURITY INFORMATION ROW

The security Information Row is comprised of an additional 4 x 256 bytes of programmable information. The security bits can be reprogrammed by the user. Any program security instruction issued while an erase, program or write cycle is in progress is rejected without having any effect on the cycle that is in progress.

**Table 8.7 Information Row Valid Address Range**

| Address Assignment           | A[23:16] | A[15:8] | A[7:0]       |
|------------------------------|----------|---------|--------------|
| IRL0 (Information Row Lock0) | 00h      | 00h     | Byte address |
| IRL1                         | 00h      | 10h     | Byte address |
| IRL2                         | 00h      | 20h     | Byte address |
| IRL3                         | 00h      | 30h     | Byte address |

Bit 7~4 of the Function Register is used to permanently lock the programmable memory array.

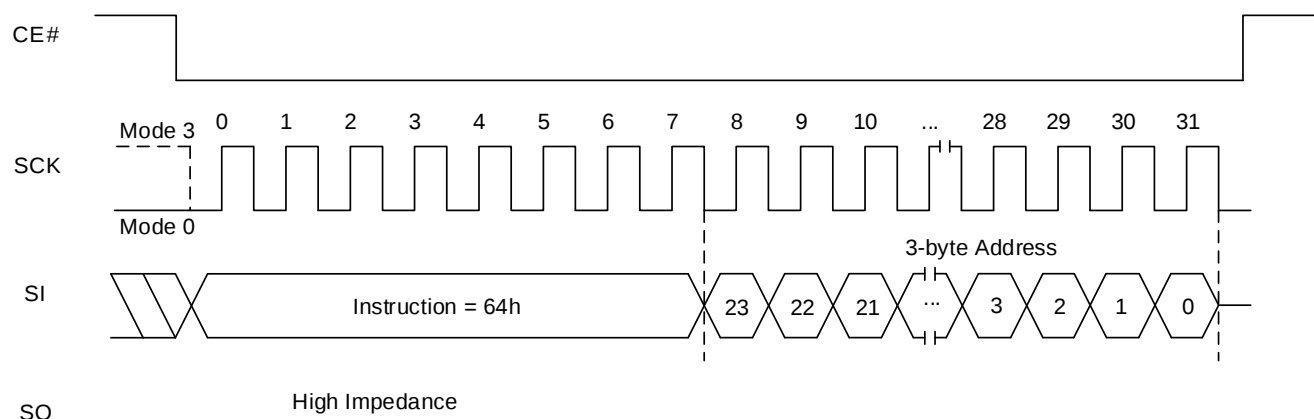
When Function Register bit IRLx = "0", the 256 bytes of the programmable memory array can be programmed.  
 When Function Register bit IRLx = "1", the 256 bytes of the programmable memory array function as read only.

### 8.36 INFORMATION ROW ERASE OPERATION (IRER, 64h)

Information Row Erase (IRER) instruction erases the data in the Information Row x (x: 0~3) array. Prior to the operation, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) instruction. The WEL bit is automatically reset after the completion of the operation.

The sequence of IRER operation: Pull CE# low to select the device → Send IRER instruction code → Send three address bytes → Pull CE# high. CE# should remain low during the entire instruction sequence. Once CE# is pulled high, Erase operation will begin immediately. The internal control logic automatically handles the erase voltage and timing.

**Figure 8.52 IRER (Information Row Erase) Sequence**



### 8.37 INFORMATION ROW PROGRAM OPERATION (IRP, 62h)

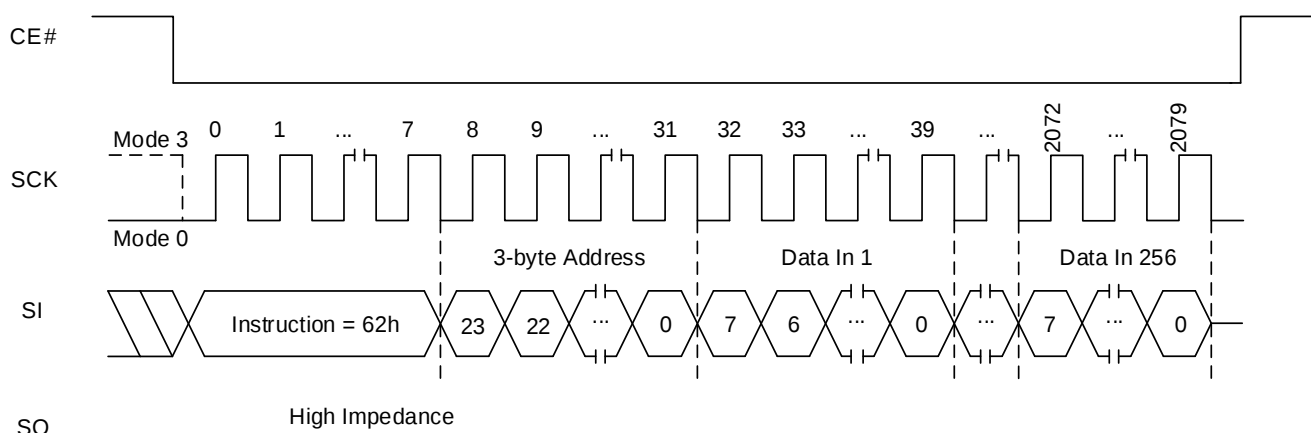
The Information Row Program (IRP) instruction allows up to 256 bytes data to be programmed into the memory in a single operation. Before the execution of IRP instruction, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) instruction.

The IRP instruction code, three address bytes and program data (1 to 256 bytes) should be sequentially input. Three address bytes has to be input as specified in the Table 8.7 Information Row Valid Address Range. Program operation will start once the CE# goes high, otherwise the IRP instruction will not be executed. The internal control logic automatically handles the programming voltages and timing. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR instruction. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page. The previously latched data are discarded and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

**Note:** A program operation can alter “1”s into “0”s, but an erase operation is required to change “0”s back to “1”s. A byte cannot be reprogrammed without first erasing the corresponding Information Row array which is one of IR0~3.

Figure 8.53 IRP (Information Row Program) Sequence



### 8.38 INFORMATION ROW READ OPERATION (IRRD, 68h)

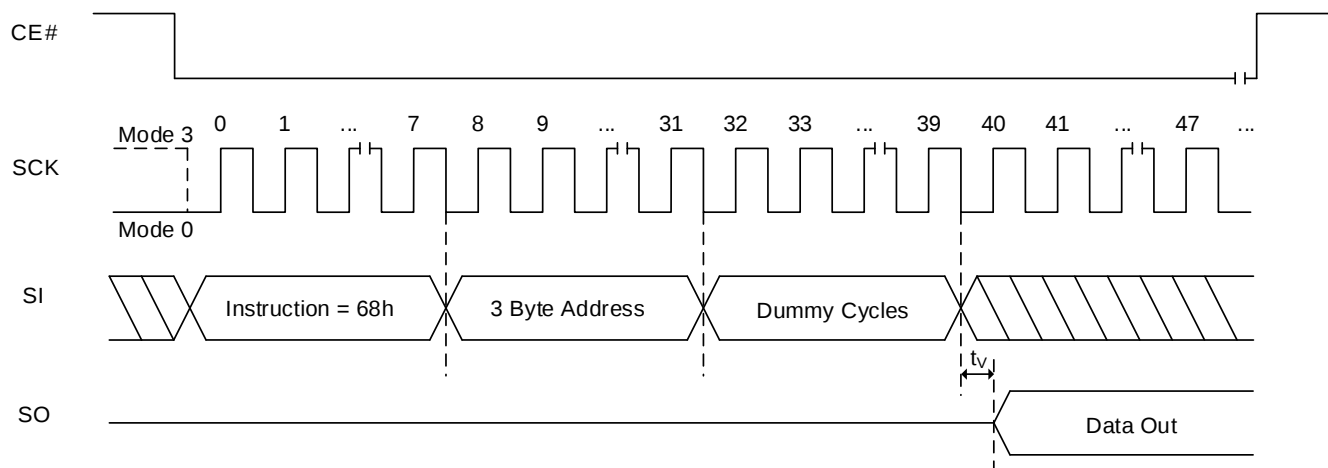
The IRRD instruction is used to read memory data at up to a 104MHz clock.

The IRRD instruction code is followed by three address bytes (A23 - A0), transmitted via the SI line, and each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line after 8 dummy cycles in SPI mode ( 6 dummy cycles in QPI mode), with each bit shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK.

The address is automatically incremented by one after each byte of data is shifted out. Once the address reaches the last address of each 256 byte Information Row, the next address will not be valid and the data of the address will be garbage data. It is recommended to repeat four times IRRD operation that reads 256 byte with a valid starting address of each Information Row in order to read all data in the 4 x 256 byte Information Row array. The IRRD instruction is terminated by driving CE# high (VIH).

If an IRRD instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle.

**Figure 8.54 IRRD (Information Row Read) Sequence**

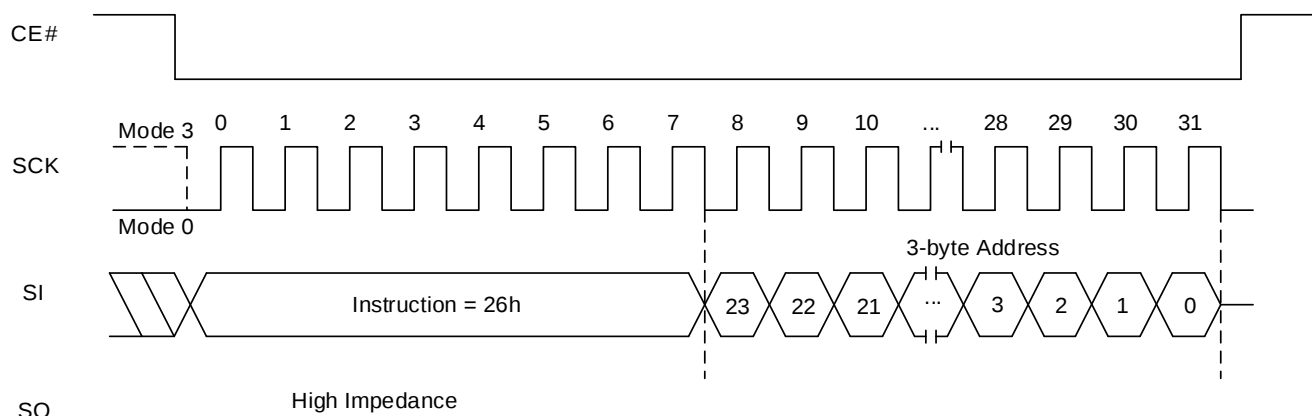


### 8.39 SECTOR LOCK/UNLOCK FUNCTIONS

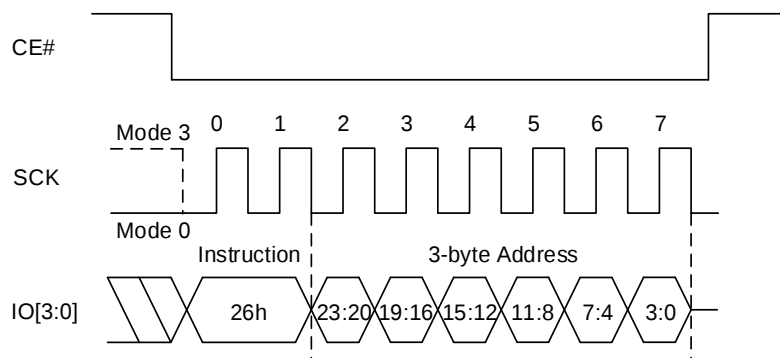
#### SECTOR UNLOCK OPERATION (SECUNLOCK, 26h)

The Sector Unlock command allows the user to select a specific sector to allow program and erase operations. This instruction is effective when the blocks are designated as write-protected through the BP0, BP1, BP2, and BP3 bits in the Status Register. Only one sector can be enabled at any time. To enable a different sector, a previously enabled sector must be disabled by executing a Sector Lock command. The instruction code is followed by a 24-bit address specifying the target sector, but A0 through A11 are not decoded. The remaining sectors within the same block remain as read-only.

**Figure 8.55 Sector Unlock Sequence In SPI Mode**



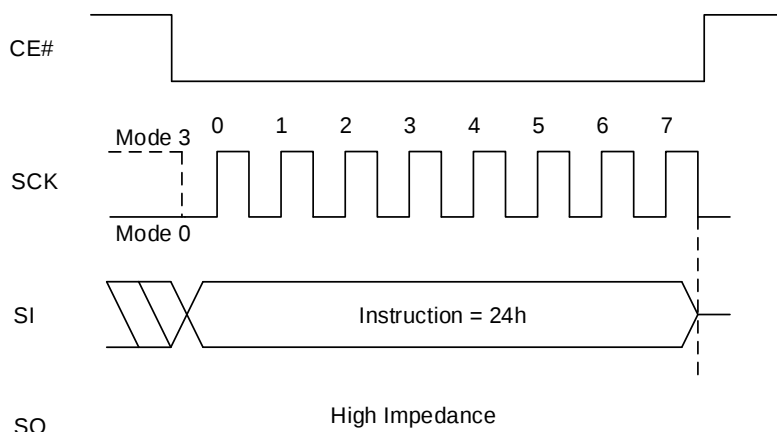
**Figure 8.56 Sector Unlock QPI Sequence In QPI Mode**



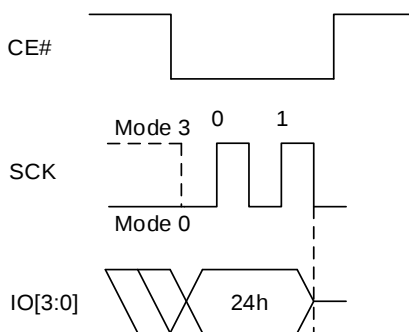
### SECTOR LOCK OPERATION (SECLOCK, 24h)

The Sector Lock command relocks a sector that was previously unlocked by the Sector Unlock command. The instruction code does not require an address to be specified, as only one sector can be enabled at a time. The remaining sectors within the same block remain in read-only mode.

**Figure 8.57 Sector Lock Sequence In SPI Mode**



**Figure 8.58 Sector Lock QPI Sequence In QPI Mode**



## 8.40 IN BAND RESET OPERATION

The device offers an additional feature of In-Band RESET function, which uses existing SPI signals to initiate a hardware reset, which is different from existing software reset/hardware reset (dedicated RESET# pin);

- Existing software reset commands often depend on the Flash being in a particular mode before they are effective. This makes software based reset sequences depend on slave device and mode.
- Dedicated RESET# pin requires additional pin over traditional 8-pins of SPI Flash device. Also it requires 1 more signal for reset operation.

In Band-RESET operation requires 2-signal pins; CE# and IO0.

- CE# is driven active low to select the SPI slave (note1)
- Clock (SCK) remains stable in either a high or low state ....(note 2)
- SI (DQ0) is driven low by the bus master, simultaneously with CE# going active low.....(note 3)
- CE# is driven inactive ... (note 4)
- Repeat the above 4 steps, each time alternating the state of SI (IO0).
- After the fourth CE# pulse, the slave triggers its internal reset.....(note 5)

Note 1 This powers up the SPI slave

Note 2 This prevents any confusion with a command, as no command bits are transferred (clocked)

Note 3 No SPI bus slave drives SI (IO0) during CE# low before a transition of clock. Slave streaming output active is not allowed until after the first edge of clock.

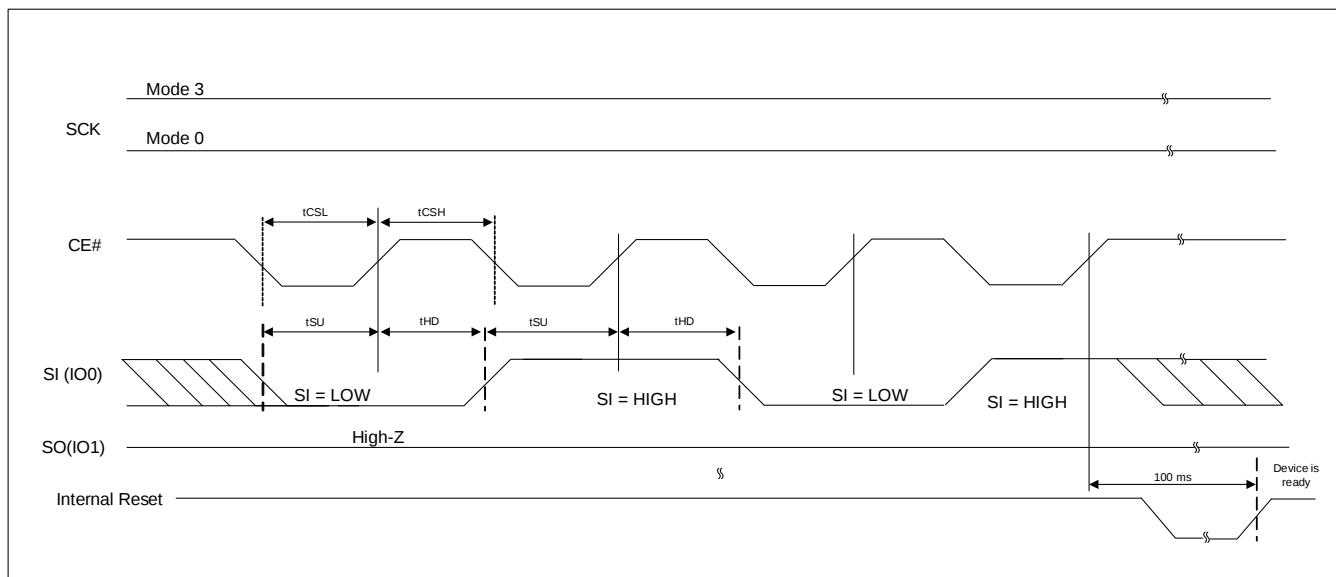
Note 4 The slave captures the state of SI on the rising edge of CE#

Note 5 SI (IO0) is low on the first CE#, high on the second, low on the third, high on the fourth ... (This provides a 5th, unlike random noise)

### NOTE:

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. During the reset process, the device will ignore any chip select (command). Once the sequence is completed the device will respond to normal operation e.g. provide a SFDP response.

Figure 8.59 Timing for In-Band RESET Operation



| Parameter      | Symbol | Min | Max | Units |
|----------------|--------|-----|-----|-------|
| CE# Low Pulse  | tCSL   | 500 | --  | ns    |
| CE# High Pulse | tCSH   | 500 | --  | ns    |
| Setup Time     | tSU    | 5   | --  | ns    |
| Hold Time      | tHD    | 5   | --  | ns    |

## 9. ELECTRICAL CHARACTERISTICS

### 9.1 ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                  |                   |                                 |
|--------------------------------------------------|-------------------|---------------------------------|
| Storage Temperature                              |                   | -65°C to +150°C                 |
| Surface Mount Lead Soldering Temperature         | Standard Package  | 240°C 3 Seconds                 |
|                                                  | Lead-free Package | 260°C 3 Seconds                 |
| Input Voltage with Respect to Ground on All Pins |                   | -0.5V to V <sub>CC</sub> + 0.5V |
| All Output Voltage with Respect to Ground        |                   | -0.5V to V <sub>CC</sub> + 0.5V |
| V <sub>CC</sub>                                  | IS25LP            | -0.5V to +6.0V                  |
|                                                  | IS25WP            | -0.5V to +2.5V                  |

**Notes:**

1. Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. ANSI/ESDA/JEDEC JS-001

### 9.2 OPERATING RANGE

|                               |                     |                                                                  |
|-------------------------------|---------------------|------------------------------------------------------------------|
| Ambient Operating Temperature | Extended Grade E    | -40°C to 105°C                                                   |
|                               | Automotive Grade A3 | -40°C to 125°C                                                   |
| V <sub>CC</sub> Power Supply  | IS25LP              | 2.3V (V <sub>MIN</sub> ) – 3.6V (V <sub>MAX</sub> ); 3.0V (Typ)  |
|                               | IS25WP              | 1.70V (V <sub>MIN</sub> ) –1.95V (V <sub>MAX</sub> ); 1.8V (Typ) |

### 9.3 DC CHARACTERISTICS

(Under operating range)

| Symbol                         | Parameter                                           |                       | Condition                                                           |                           | Min                   | Typ <sup>(2)</sup> | Max                   | Units |
|--------------------------------|-----------------------------------------------------|-----------------------|---------------------------------------------------------------------|---------------------------|-----------------------|--------------------|-----------------------|-------|
| I <sub>CC1</sub>               | V <sub>CC</sub> Active Read current <sup>(3)</sup>  |                       | NORD at 50MHz                                                       |                           |                       | 6                  | 8                     | mA    |
|                                |                                                     |                       | FRD Single at 104MHz                                                |                           |                       | 7                  | 9                     |       |
|                                |                                                     |                       | FRD Dual at 104MHz                                                  |                           |                       | 8                  | 10                    |       |
|                                |                                                     |                       | FRD Quad at 104MHz                                                  |                           |                       | 10                 | 12                    |       |
| I <sub>CC2</sub>               | V <sub>CC</sub> Program Current                     | CE# = V <sub>CC</sub> | 85°C                                                                |                           | 15                    | 20                 |                       |       |
|                                |                                                     |                       | 105°C                                                               |                           |                       | 20                 |                       |       |
|                                |                                                     |                       | 125°C                                                               |                           |                       | 20                 |                       |       |
| I <sub>CC3</sub>               | V <sub>CC</sub> WRSR Current                        | CE# = V <sub>CC</sub> | 85°C                                                                |                           | 15                    | 20                 |                       |       |
|                                |                                                     |                       | 105°C                                                               |                           |                       | 20                 |                       |       |
|                                |                                                     |                       | 125°C                                                               |                           |                       | 20                 |                       |       |
| I <sub>CC4</sub>               | V <sub>CC</sub> Erase Current<br>(SER/BER4K/BER64K) | CE# = V <sub>CC</sub> | 85°C                                                                |                           | 15                    | 20                 |                       |       |
|                                |                                                     |                       | 105°C                                                               |                           |                       | 20                 |                       |       |
|                                |                                                     |                       | 125°C                                                               |                           |                       | 20                 |                       |       |
| I <sub>CC5</sub>               | V <sub>CC</sub> Erase Current (CE)                  | CE# = V <sub>CC</sub> | 85°C                                                                |                           | 15                    | 20                 |                       |       |
|                                |                                                     |                       | 105°C                                                               |                           |                       | 20                 |                       |       |
|                                |                                                     |                       | 125°C                                                               |                           |                       | 20                 |                       |       |
| I <sub>SB1</sub>               | V <sub>CC</sub> Standby Current<br>CMOS             |                       | CE# = V <sub>CC</sub> ,<br>V <sub>IN</sub> = GND or V <sub>CC</sub> | 85°C                      |                       | 17                 | 35 <sup>(4)</sup>     | μA    |
|                                |                                                     |                       |                                                                     | 105°C                     |                       |                    | 40 <sup>(4)</sup>     |       |
|                                |                                                     |                       |                                                                     | 125°C                     |                       |                    | 45                    |       |
| I <sub>SB2</sub>               | Deep power<br>down current                          | IS25LP                | CE# = V <sub>CC</sub> ,<br>V <sub>IN</sub> = GND or V <sub>CC</sub> | 85°C                      |                       | 6                  | 15 <sup>(4)</sup>     |       |
|                                |                                                     |                       |                                                                     | 105°C                     |                       |                    | 18 <sup>(4)</sup>     |       |
|                                |                                                     |                       |                                                                     | 125°C                     |                       |                    | 20                    |       |
|                                |                                                     | IS25WP                | CE# = V <sub>CC</sub> ,<br>V <sub>IN</sub> = GND or V <sub>CC</sub> | 85°C                      |                       | 3                  | 15 <sup>(4)</sup>     |       |
|                                |                                                     |                       |                                                                     | 105°C                     |                       |                    | 18 <sup>(4)</sup>     |       |
|                                |                                                     |                       |                                                                     | 125°C                     |                       |                    | 20                    |       |
| I <sub>LI</sub>                | Input Leakage Current                               |                       | V <sub>IN</sub> = 0V to V <sub>CC</sub>                             |                           |                       |                    | 1                     |       |
| I <sub>LO</sub>                | Output Leakage Current                              |                       | V <sub>IN</sub> = 0V to V <sub>CC</sub>                             |                           |                       |                    | 1                     |       |
| V <sub>IL</sub> <sup>(1)</sup> | Input Low Voltage                                   |                       |                                                                     |                           | -0.5                  |                    | 0.3V <sub>CC</sub>    | V     |
| V <sub>IH</sub> <sup>(1)</sup> | Input High Voltage                                  |                       |                                                                     |                           | 0.7V <sub>CC</sub>    |                    | V <sub>CC</sub> + 0.3 |       |
| V <sub>OL</sub>                | Output Low Voltage                                  |                       | V <sub>MIN</sub> < V <sub>CC</sub> < V <sub>MAX</sub>               | I <sub>OL</sub> = 100 μA  |                       |                    | 0.2                   |       |
| V <sub>OH</sub>                | Output High Voltage                                 |                       |                                                                     | I <sub>OH</sub> = -100 μA | V <sub>CC</sub> - 0.2 |                    |                       |       |

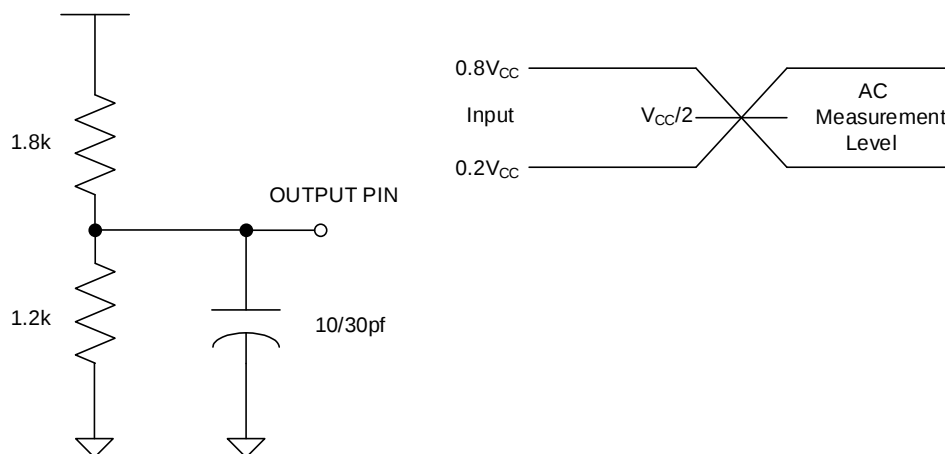
**Notes:**

1. Maximum DC voltage on input or I/O pins is  $V_{CC} + 0.5V$ . During voltage transitions, input or I/O pins may overshoot  $V_{CC}$  by + 2.0V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -2.0V for a period of time not to exceed 20ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC} (Typ)$ ,  $T_A = 25^{\circ}C$ .
3. Outputs are unconnected during reading data so that output switching current is not included.
4. These parameters are characterized and are not 100% tested.

#### 9.4 AC MEASUREMENT CONDITIONS

| Symbol | Parameter                        | Min                                      | Max | Units |
|--------|----------------------------------|------------------------------------------|-----|-------|
| CL     | Load Capacitance                 |                                          | 30  | pF    |
| TR,TF  | Input Rise and Fall Times        |                                          | 5   | ns    |
| VIN    | Input Pulse Voltages             | 0.2V <sub>CC</sub> to 0.8V <sub>CC</sub> |     | V     |
| VREFI  | Input Timing Reference Voltages  | 0.3V <sub>CC</sub> to 0.7V <sub>CC</sub> |     | V     |
| VREFO  | Output Timing Reference Voltages | 0.5V <sub>CC</sub>                       |     | V     |

**Figure 9.1 Output test load & AC measurement I/O Waveform**



#### 9.5 PIN CAPACITANCE

( $T_A = 25^{\circ}C$ ,  $V_{CC} = 3V$  for IS25LP,  $V_{CC} = 1.8V$  for IS25WP, 1MHz)

| Symbol              | Parameter                             | Test Condition           | IS25LP |     | IS25WP |     | Units |
|---------------------|---------------------------------------|--------------------------|--------|-----|--------|-----|-------|
|                     |                                       |                          | Min    | Max | Min    | Max |       |
| C <sub>IN</sub>     | Input Capacitance (CE#, SCK)          | V <sub>IN</sub> = 0V     | -      | 6   | -      | 6   | pF    |
| C <sub>IN/OUT</sub> | Input/Output Capacitance (other pins) | V <sub>IN/OUT</sub> = 0V | -      | 8   | -      | 10  | pF    |

**Note:**

1. These parameters are characterized and are not 100% tested.

## 9.6 AC CHARACTERISTICS

(Under operating range, refer to section 9.4 for AC measurement conditions)

| Symbol                           | Parameter                                  | Min    | Typ <sup>(2)</sup> | Max  | Units |
|----------------------------------|--------------------------------------------|--------|--------------------|------|-------|
| f <sub>CT</sub>                  | Clock Frequency for fast read mode         | 0      |                    | 104  | MHz   |
| f <sub>C</sub>                   | Clock Frequency for read mode              | 0      |                    | 50   | MHz   |
| t <sub>RI</sub>                  | Input Rise Time                            |        |                    | 8    | ns    |
| t <sub>FI</sub>                  | Input Fall Time                            |        |                    | 8    | ns    |
| t <sub>CKH</sub>                 | SCK High Time                              | 4      |                    |      | ns    |
| t <sub>CKL</sub>                 | SCK Low Time                               | 4      |                    |      | ns    |
| t <sub>CEH</sub>                 | CE# High Time                              | 7      |                    |      | ns    |
| t <sub>CS</sub>                  | CE# Setup Time                             | 5      |                    |      | ns    |
| t <sub>CH</sub>                  | CE# Hold Time                              | 5      |                    |      | ns    |
| t <sub>CHSL</sub>                | CE# Not Active Hold Time                   | 5      |                    |      | ns    |
| t <sub>SHCH</sub>                | CE# Not Active Setup Time                  | 5      |                    |      | ns    |
| t <sub>DS</sub>                  | Data In Setup Time                         | 2      |                    |      | ns    |
| t <sub>DH</sub>                  | Data in Hold Time                          | 2      |                    |      | ns    |
| t <sub>V</sub>                   | Output Valid                               |        |                    | 8    | ns    |
| t <sub>OH</sub>                  | Output Hold Time                           | 2      |                    |      | ns    |
| t <sub>DIS</sub> <sup>(1)</sup>  | Output Disable Time                        |        |                    | 8    | ns    |
| t <sub>WHSL</sub> <sup>(3)</sup> | Write Protect Setup Time                   | 20     |                    |      | ns    |
| t <sub>SHWL</sub> <sup>(3)</sup> | Write Protect Hold Time                    | 100    |                    |      | ns    |
| t <sub>HLCH</sub>                | HOLD Active Setup Time relative to SCK     | 5      |                    |      | ns    |
| t <sub>CHHH</sub>                | HOLD Active Hold Time relative to SCK      | 5      |                    |      | ns    |
| t <sub>HHCH</sub>                | HOLD Not Active Setup Time relative to SCK | 5      |                    |      | ns    |
| t <sub>CHHL</sub>                | HOLD Not Active Hold Time relative to SCK  | 5      |                    |      | ns    |
| t <sub>LZ</sub> <sup>(1)</sup>   | HOLD to Output Low Z                       |        |                    | 12   | ns    |
| t <sub>HZ</sub> <sup>(1)</sup>   | HOLD to Output High Z                      |        |                    | 12   | ns    |
| t <sub>EC</sub>                  | Sector Erase Time (4Kbyte)                 |        | 70                 | 300  | ms    |
|                                  | Block Erase Time (32Kbyte)                 |        | 130                | 500  | ms    |
|                                  | Block Erase time (64Kbyte) <sup>(4)</sup>  |        | 200                | 1000 | ms    |
|                                  | Chip Erase Time <sup>(5)</sup>             | 256Kb  | 130                | 500  | ms    |
|                                  |                                            | 512Kb  | 0.25               | 1.0  | s     |
|                                  |                                            | 1Mb    | 0.4                | 1.5  |       |
|                                  |                                            | 2Mb    | 0.75               | 2.0  |       |
|                                  |                                            | 4Mb    | 1.5                | 3.0  |       |
| t <sub>PP</sub>                  | Page Program Time                          |        | 0.45               | 1.2  | ms    |
| t <sub>res1</sub> <sup>(1)</sup> | Release deep power down                    | IS25LP |                    | 3    | μs    |
|                                  |                                            | IS25WP |                    | 5    |       |
| t <sub>DP</sub> <sup>(1)</sup>   | Deep power down                            |        |                    | 3    | μs    |
| t <sub>W</sub>                   | Write Status Register time                 |        | 2                  | 10   | ms    |
| t <sub>SUS</sub> <sup>(1)</sup>  | Suspend to read ready                      |        |                    | 100  | μs    |
| t <sub>RS</sub> <sup>(1)</sup>   | Resume to next suspend                     |        | 80                 | -    | μs    |
| t <sub>SRST</sub> <sup>(1)</sup> | Software Reset cover time                  |        |                    | 100  | μs    |

### Notes:

- These parameters are characterized and not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> (Typ), TA=25°C.
- Only applicable as a constraint for a WRITE STATUS REGISTER command when SRWD is set at 1
- 64Kbyte Block Erase time is not applicable to 256Kb (IS25LP/WP025E) and 512Kb (IS25LP/WP512E).

## 9.7 SERIAL INPUT/OUTPUT TIMING

Figure 9.2 SERIAL INPUT TIMING (STR Mode)

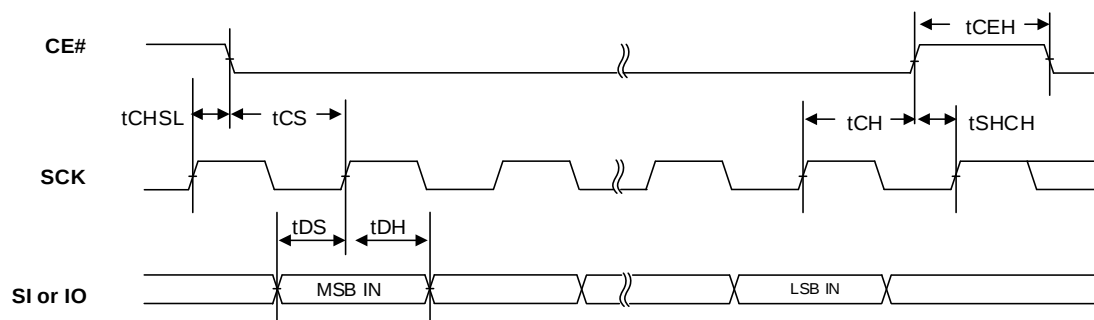


Figure 9.3 SERIAL INPUT TIMING (DTR Mode)

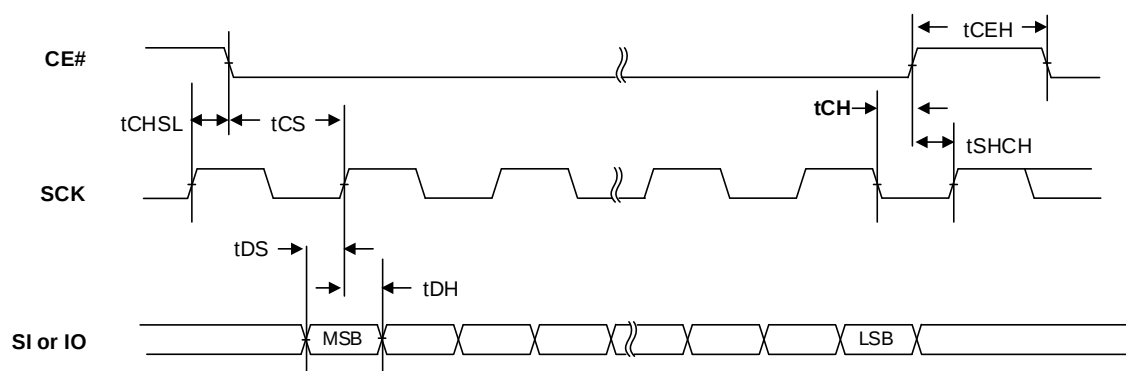


Figure 9.4 OUTPUT TIMING (STR Mode)

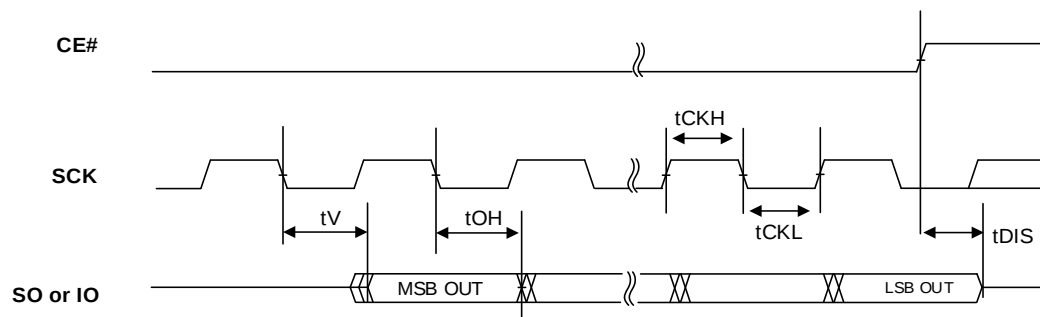


Figure 9.5 OUTPUT TIMING (DTR Mode)

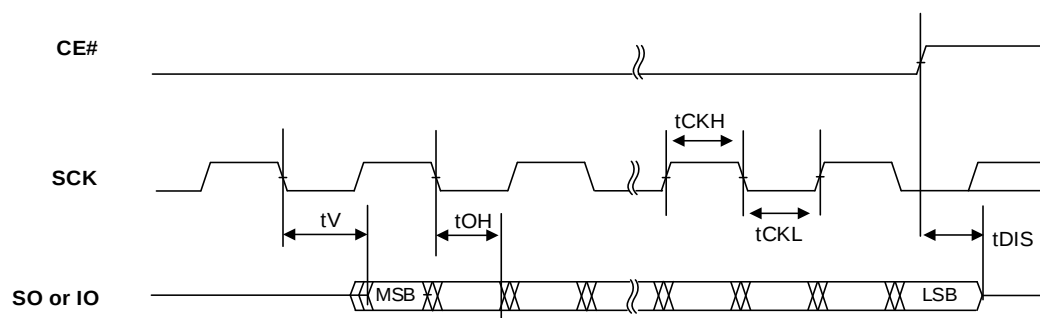


Figure 9.6 HOLD TIMING

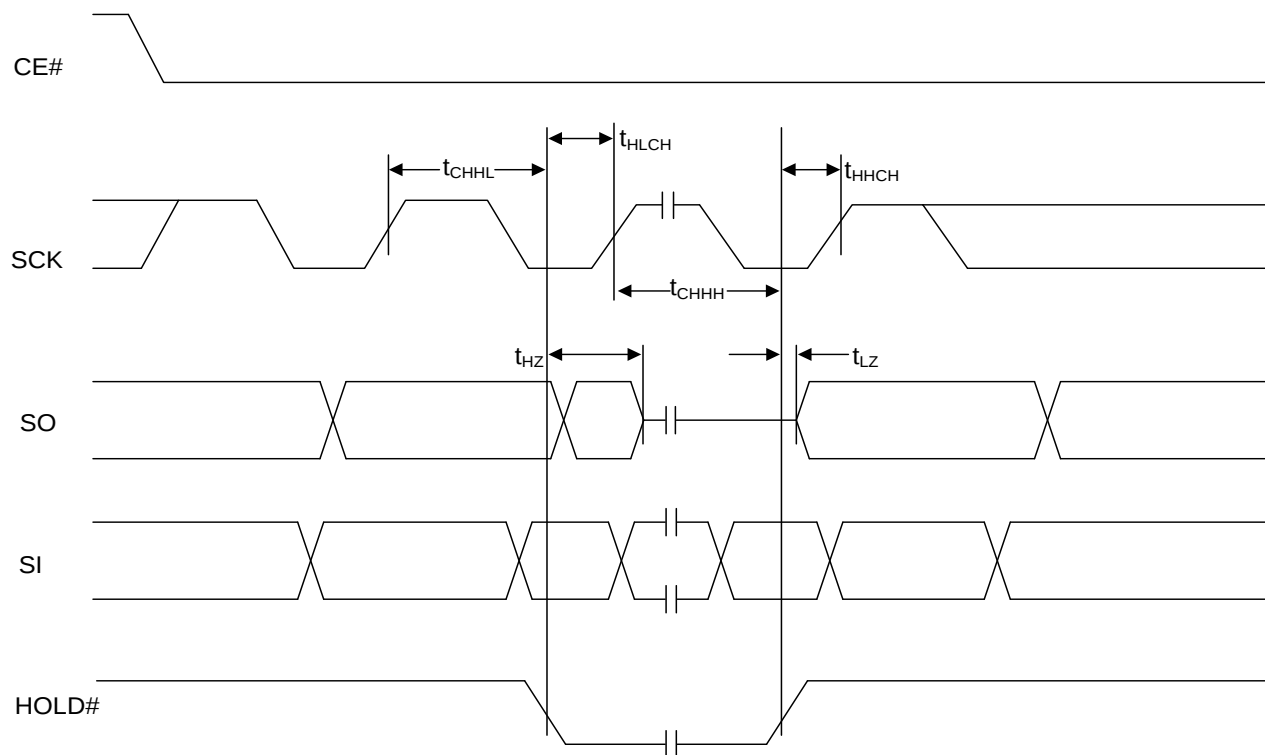
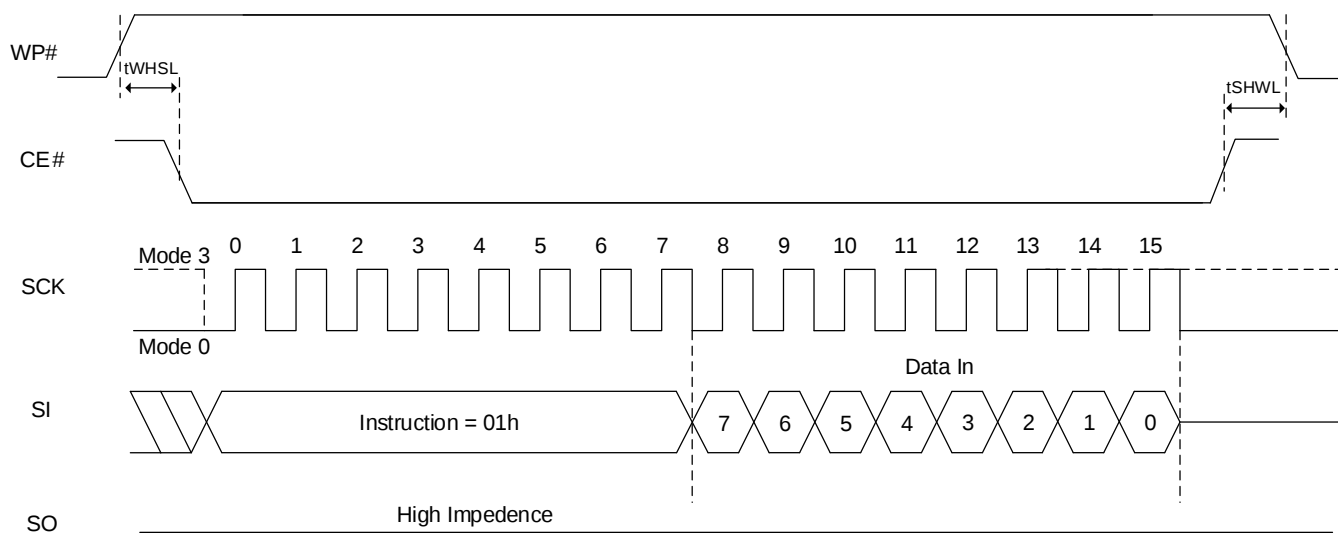


Figure 9.7 WRITE PROTECT SETUP AND HOLD TIMING DURING WRITE STATUS REGISTER (SRWD=1)

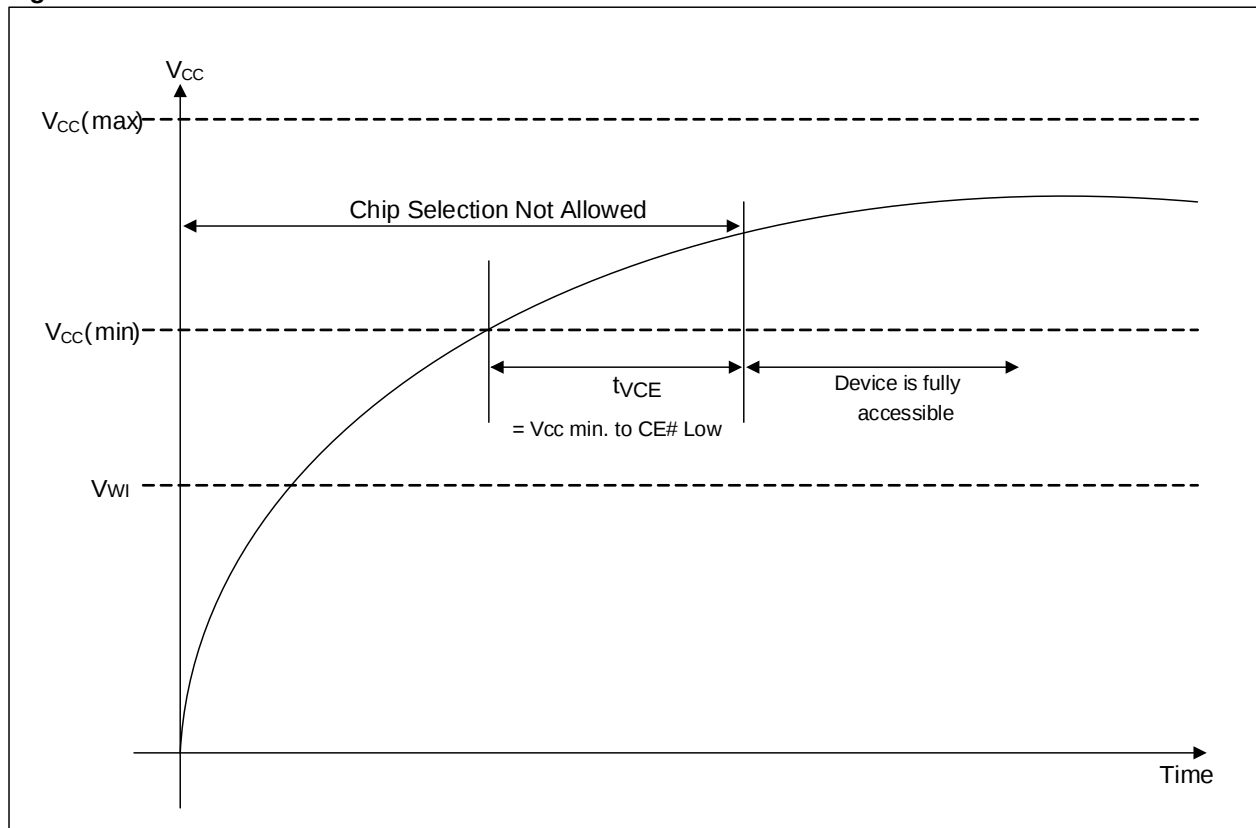


Note: WP# must be kept high until the embedded operation finish.

## 9.8 POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must be NOT SELECTED until Vcc reaches at the right level. (Adding a simple pull-up resistor on CE# is recommended.)

**Figure 9.8 POWER UP TIMING**



| Symbol              | Parameter             |        | Min. | Max | Unit |
|---------------------|-----------------------|--------|------|-----|------|
| tVCE <sup>(1)</sup> | Vcc(min) to CE# Low   |        | 300  |     | us   |
| Vwl <sup>(1)</sup>  | Write Inhibit Voltage | IS25LP |      | 2.1 | V    |
|                     |                       | IS25WP |      | 1.4 |      |

**Note:** These parameters are characterized and not 100% tested.

**9.9 PROGRAM/ERASE PERFORMANCE <sup>(1)</sup>**

| Parameter                              |       | Typ  | Max  | Unit |
|----------------------------------------|-------|------|------|------|
| Sector Erase Time (4KB)                |       | 70   | 300  | ms   |
| Block Erase Time (32KB)                |       | 130  | 500  | ms   |
| Block Erase Time (64KB) <sup>(2)</sup> |       | 200  | 1000 | ms   |
| Chip Erase Time                        | 256Kb | 130  | 500  | ms   |
|                                        | 512Kb | 0.25 | 1.0  | s    |
|                                        | 1Mb   | 0.4  | 1.5  |      |
|                                        | 2Mb   | 0.75 | 2.0  |      |
|                                        | 4Mb   | 1.5  | 3.0  |      |
| Page Programming Time                  |       | 0.45 | 1.2  | ms   |
| Byte Program                           |       | 8    | 40   | μs   |

**Note:**

1. These parameters are characterized and not 100% tested.
2. 64Kbyte Block Erase time is not applicable to 256Kb (IS25LP/WP025E) and 512Kb (IS25LP/WP512E).

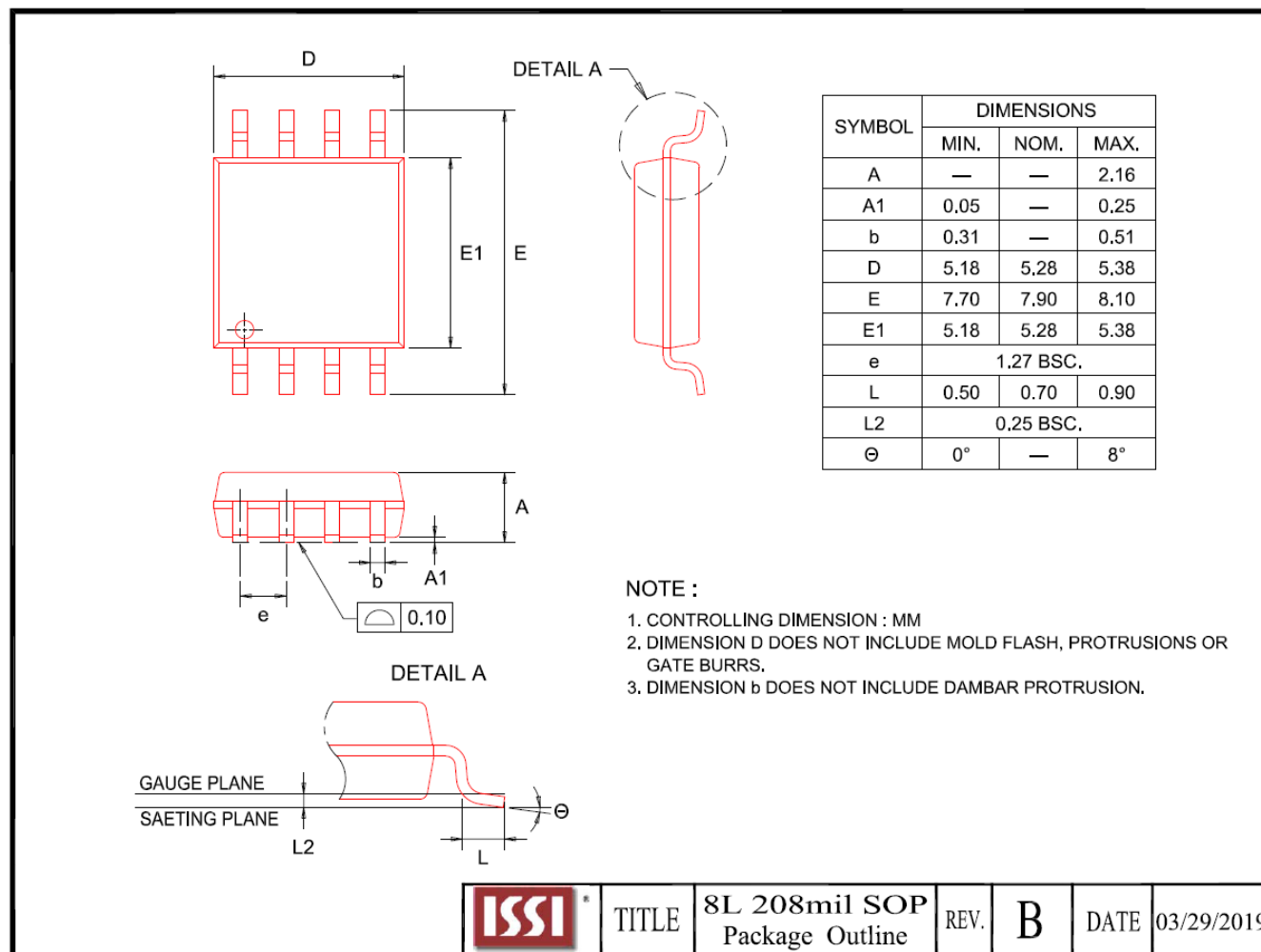
**9.10 RELIABILITY CHARACTERISTICS**

| Parameter      | Min     | Max  | Unit   | Test Method         |
|----------------|---------|------|--------|---------------------|
| Endurance      | 100,000 | -    | Cycles | JEDEC Standard A117 |
| Data Retention | 20      | -    | Years  | JEDEC Standard A117 |
| Latch-Up       | -100    | +100 | mA     | JEDEC Standard 78   |

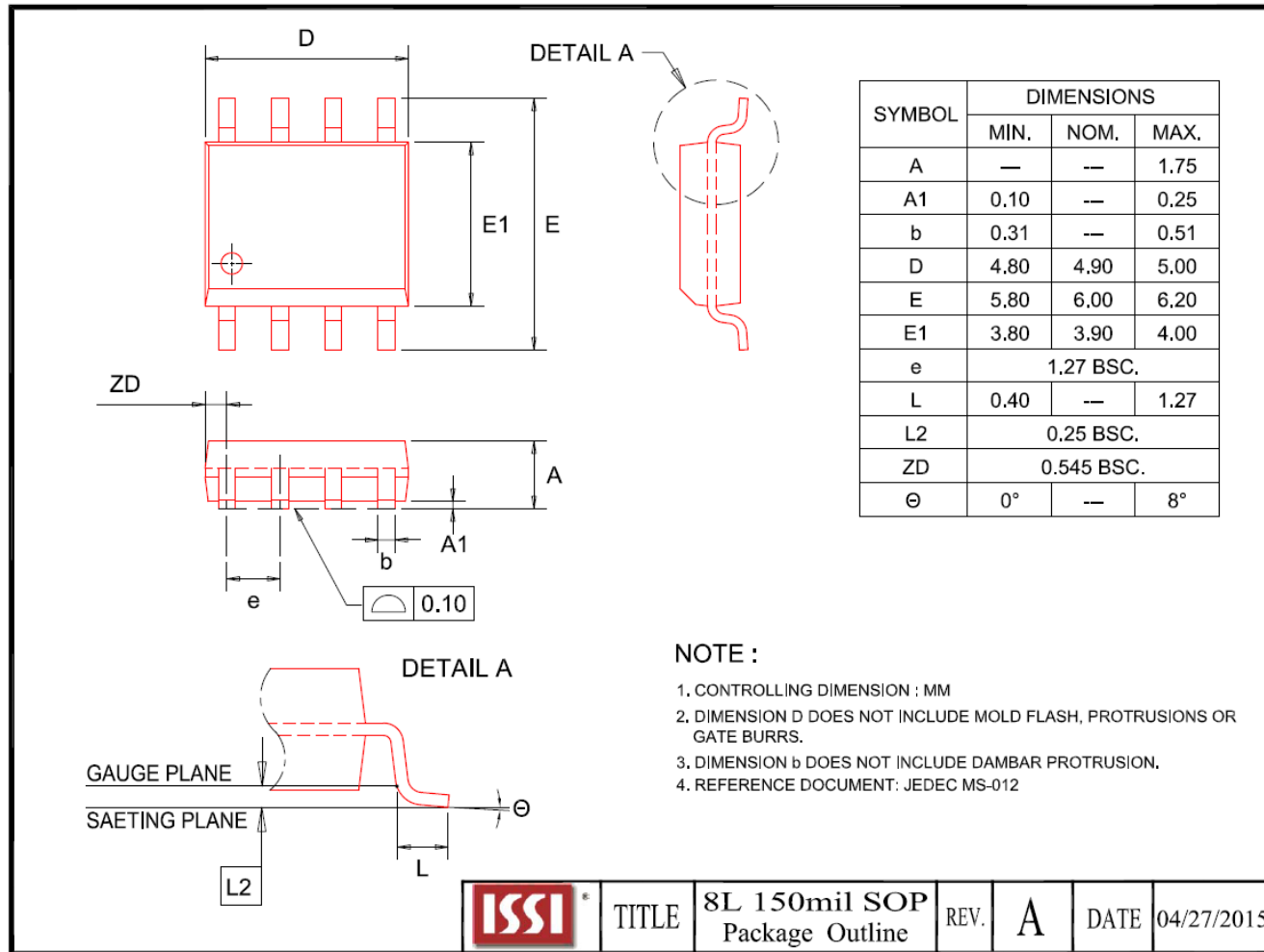
**Note:** These parameters are characterized and not 100% tested.

## 10. PACKAGE TYPE INFORMATION

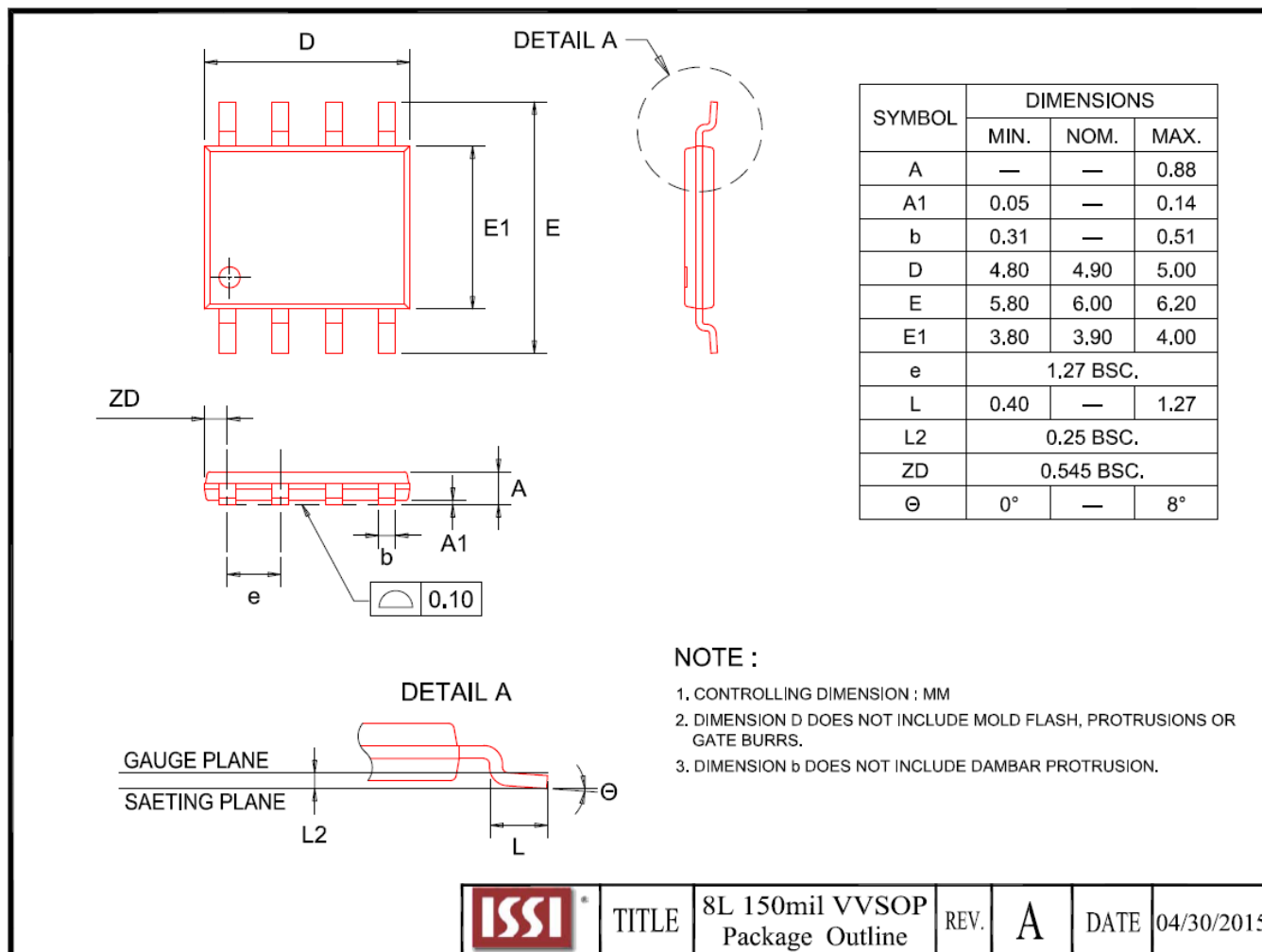
### 10.1 8-PIN JEDEC 208MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (B)



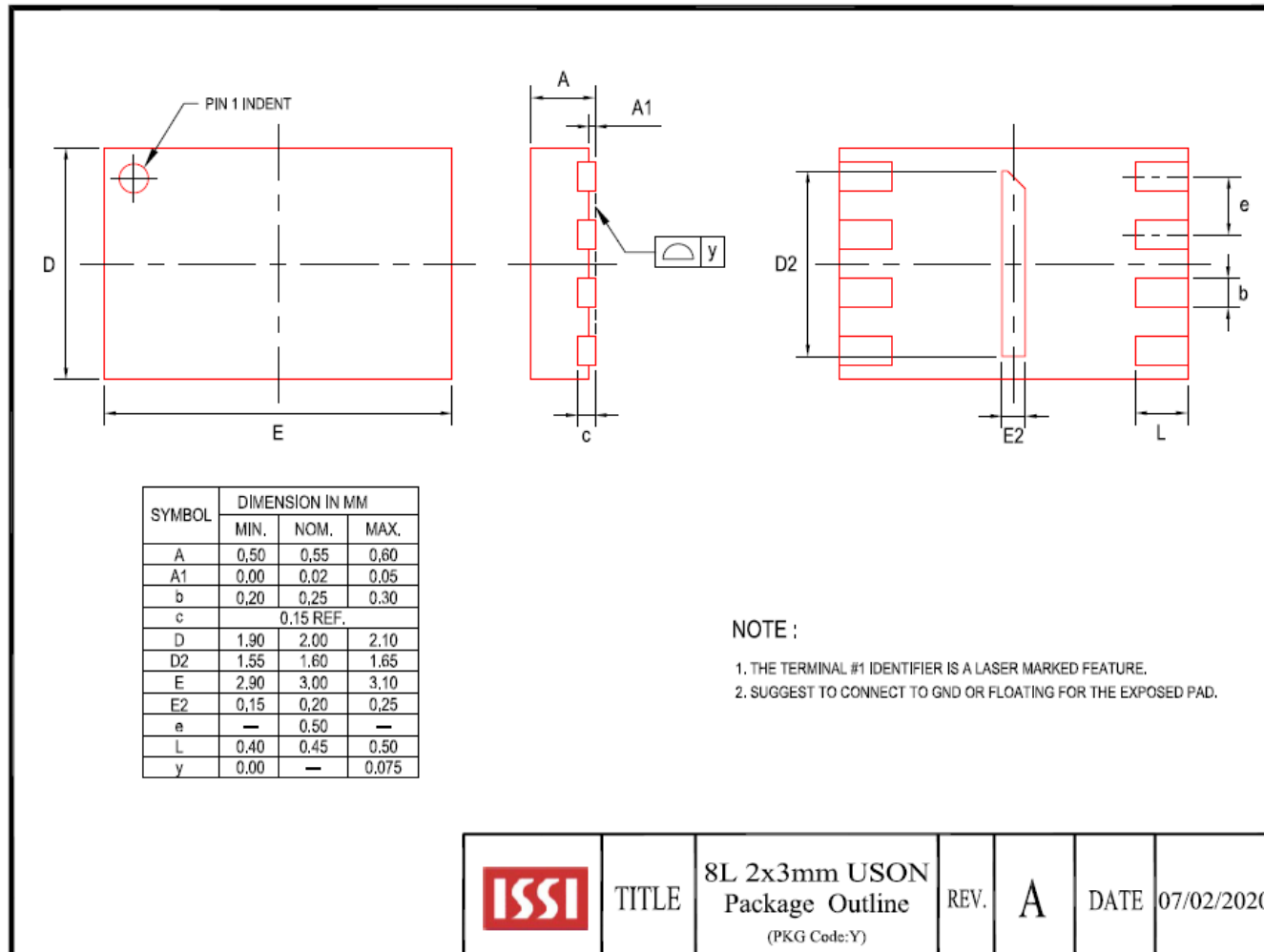
## 10.2 8-PIN JEDEC 150MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (N)



**10.3 8-PIN 150MIL VVSOP PACKAGE (V)**

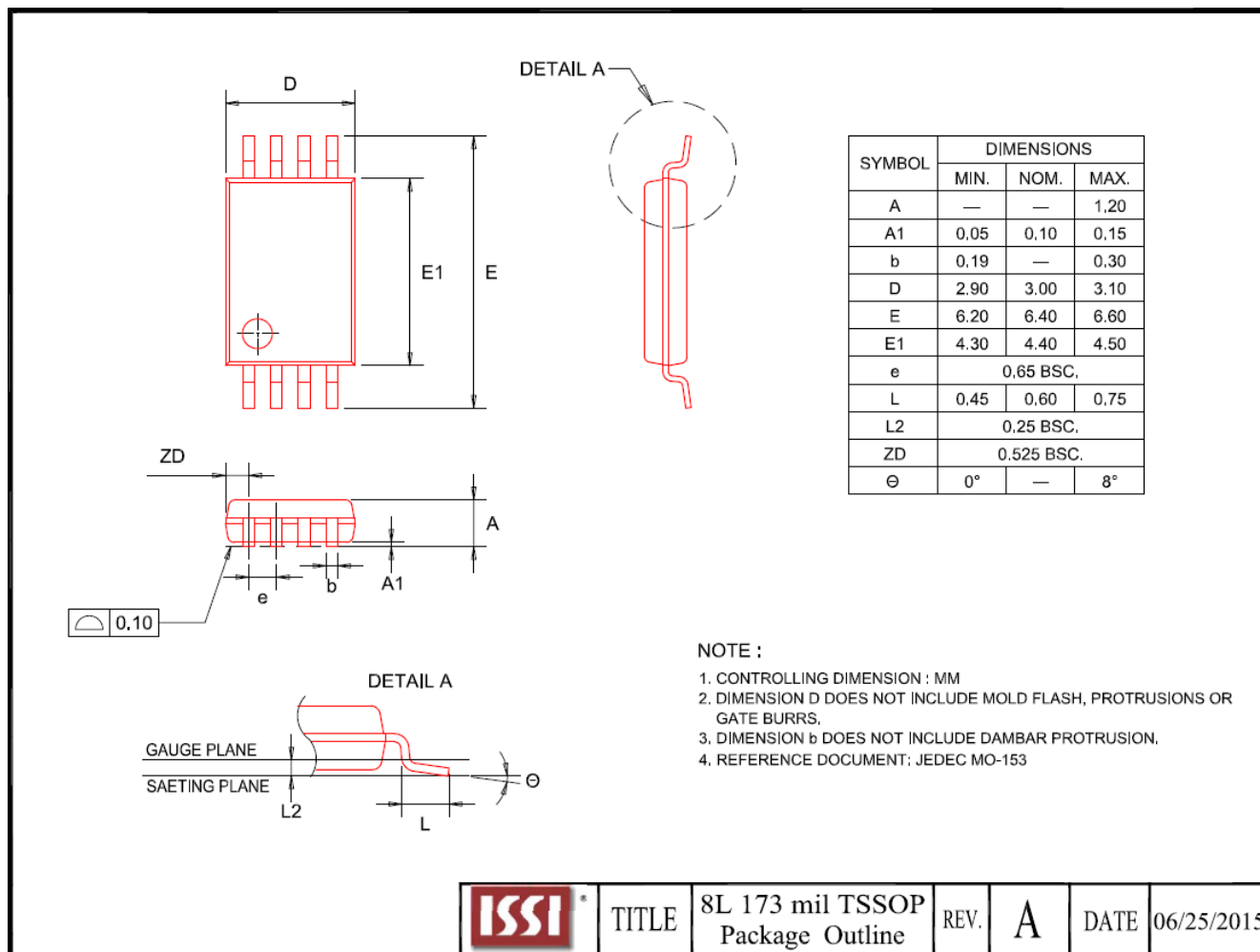


**10.4 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (USON) PACKAGE 2X3MM (Y)**

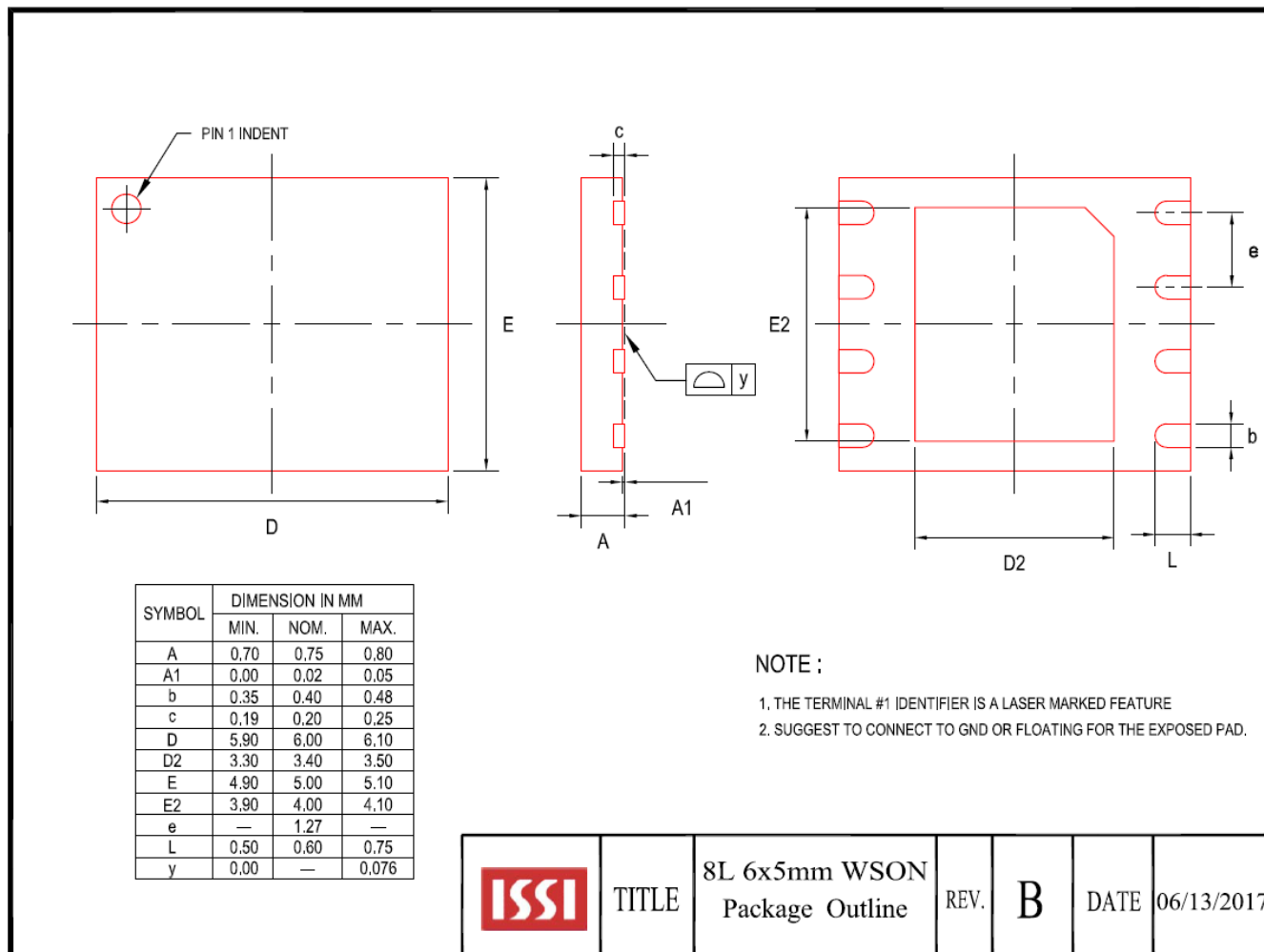


Note: Please [click here](#) to refer to Application Note (AN25D011, Thin USON/WSO/XSON package handling precautions) for assembly guidelines.

# 10.5 8-PIN TSSOP PACKAGE (D)



## 10.6 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 6X5MM (K)



Note: Please [click here](#) to refer to Application Note (AN25D011, Thin USON/WSON/XSON package handling precautions) for assembly guidelines.

## 11. ORDERING INFORMATION - Valid Part Numbers

IS25LP 040 E - J B L E

### TEMPERATURE RANGE

E = Extended (-40°C to +105°C)

A3 = Automotive Grade (-40°C to +125°C)

### PACKAGING CONTENT

L = RoHS compliant

### PACKAGE Type

B = 8-pin SOIC 208mil

N = 8-pin SOIC 150mil

D = 8-pin TSSOP (Call Factory)

V = 8-pin VVSOP 150mil (Call Factory)

Y = 8-contact USON 2x3mm

K = 8-contact WSON 6x5mm (Call Factory)

W = KGD (Call Factory)

### Option

J = Standard

B = Optional BP Table (Call Factory)

C = Optional 1Mb with 32KB Erase only (D8h/52h)

### Die Revision

E = Revision E

### Density

040 = 4 Mbit

020 = 2 Mbit

010 = 1 Mbit

512 = 512Kbit

025 = 256Kbit

### BASE PART NUMBER

IS = Integrated Silicon Solution Inc.

25LP = FLASH, 2.30V ~ 3.60V, QPI

25WP = FLASH, 1.70V ~ 1.95V, QPI



# IS25LP040E/020E/010E/512E/025E IS25WP040E/020E/010E/512E/025E

| Density,<br>Voltage | Frequency<br>(MHz) | Order Part Number <sup>(1, 2)</sup> | Package                             |
|---------------------|--------------------|-------------------------------------|-------------------------------------|
| 4Mb,<br>3V          | 104                | IS25LP040E-JBLE                     | 8-pin SOIC 208mil (Call Factory)    |
|                     |                    | <b>IS25LP040E-JNLE</b>              | <b>8-pin SOIC 150mil</b>            |
|                     |                    | IS25LP040E-JKLE                     | 8-contact WSON 6x5mm (Call Factory) |
|                     |                    | <b>IS25LP040E-JYLE</b>              | <b>8-contact USON 2x3mm</b>         |
|                     |                    | IS25LP040E-JBLA3                    | 8-pin SOIC 208mil (Call Factory)    |
|                     |                    | <b>IS25LP040E-JNLA3</b>             | <b>8-pin SOIC 150mil</b>            |
|                     |                    | IS25LP040E-JKLA3                    | 8-contact WSON 6x5mm (Call Factory) |
|                     |                    | <b>IS25LP040E-JYLA3</b>             | <b>8-contact USON 2x3mm</b>         |
| 2Mb,<br>3V          |                    | <b>IS25LP020E-JNLE</b>              | <b>8-pin SOIC 150mil</b>            |
|                     |                    | <b>IS25LP020E-JYLE</b>              | <b>8-contact USON 2x3mm</b>         |
|                     |                    | <b>IS25LP020E-JNLA3</b>             | <b>8-pin SOIC 150mil</b>            |
|                     |                    | <b>IS25LP020E-JYLA3</b>             | <b>8-contact USON 2x3mm</b>         |
| 1Mb,<br>3V          |                    | IS25LP010E-JBLE                     | 8-pin SOIC 208mil (Call Factory)    |
|                     |                    | <b>IS25LP010E-JNLE</b>              | <b>8-pin SOIC 150mil</b>            |
|                     |                    | <b>IS25LP010E-JYLE</b>              | <b>8-contact USON 2x3mm</b>         |
|                     |                    | IS25LP010E-JNLA3                    | 8-pin SOIC 150mil (Call Factory)    |
|                     |                    | IS25LP010E-JYLA3                    | 8-contact USON 2x3mm(Call Factory)  |
| 512Kb,<br>3V        |                    | IS25LP512E-JNLE                     | 8-pin SOIC 150mil (Call Factory)    |
| 256Kb,<br>3V        |                    | IS25LP025E -JNLE                    | 8-pin SOIC 150mil (Call Factory)    |
| 4Mb,<br>1.8V        |                    | <b>IS25WP040E-JNLE</b>              | <b>8-pin SOIC 150mil</b>            |
|                     |                    | IS25WP040E-JKLE                     | 8-contact WSON 6x5mm (Call Factory) |
|                     |                    | <b>IS25WP040E-JYLE</b>              | <b>8-contact USON 2x3mm</b>         |
|                     |                    | <b>IS25WP040E-JBLE</b>              | <b>8-pin SOIC 208mil</b>            |
|                     |                    | <b>IS25WP040E-JNLA3</b>             | <b>8-pin SOIC 150mil</b>            |
|                     |                    | <b>IS25WP040E-JYLA3</b>             | <b>8-contact USON 2x3mm</b>         |
| 2Mb,<br>1.8V        |                    | IS25WP020E-JBLE                     | 8-pin SOIC 208mil (Call Factory)    |
|                     |                    | <b>IS25WP020E-JNLE</b>              | <b>8-pin SOIC 150mil</b>            |
|                     |                    | <b>IS25WP020E-JYLE</b>              | <b>8-contact USON 2x3mm</b>         |

## Notes:

1. A3 meets AEC-Q100 requirements with PPAP, E1= Extended+ non-Auto qualified

Temp Grades: E= -40 to 105°C, A3= -40 to 125°C

2. Call Factory