

## D/A Converters Series

# D/A Converters 8 bit 2 ch • 3 ch Type

**BD79700FVM-LB BD79701FVM-LB**

### General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

BD79700FVM-LB and BD79701FVM-LB are 8 bit R-2R-type D/A converters with 2 and 3 channels, respectively. A compact package allows for adjacent placement to the adjustment target, thereby eliminating deterioration of the D/A converter due to the board wiring. A broad power supply voltage range (2.7 V to 5.5 V) is available, providing design flexibility.

### Key Specifications

|                                |                   |
|--------------------------------|-------------------|
| ■ Power Source Voltage Range:  | 2.7 V to 5.5 V    |
| ■ Current Consumption:         | 0.6 mA (Typ)      |
| ■ Differential Non Linearity   | ±0.5 LSB (Max)    |
| ■ Integral Non Linearity       | ±0.5 LSB (Max)    |
| ■ Settling Time:               | 4.5 μs (Max)      |
| ■ Max Data Transfer Frequency: | 30 MHz (Max)      |
| ■ Action Temperature Range:    | -40 °C to +125 °C |

### Package

MSOP8

**W (Typ) x D (Typ) x H (Max)**

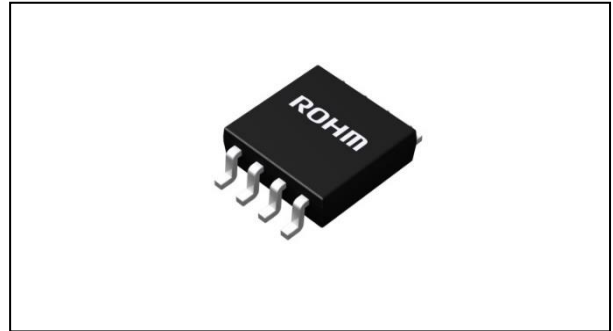
2.9 mm x 4.0 mm x 0.9 mm

### Features

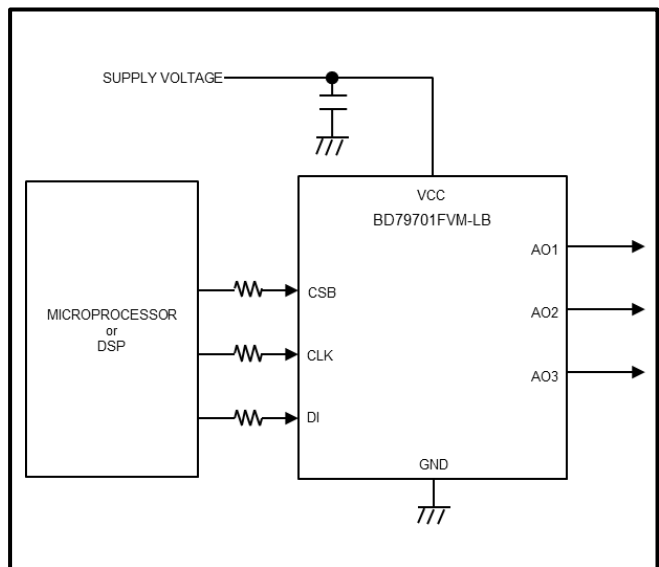
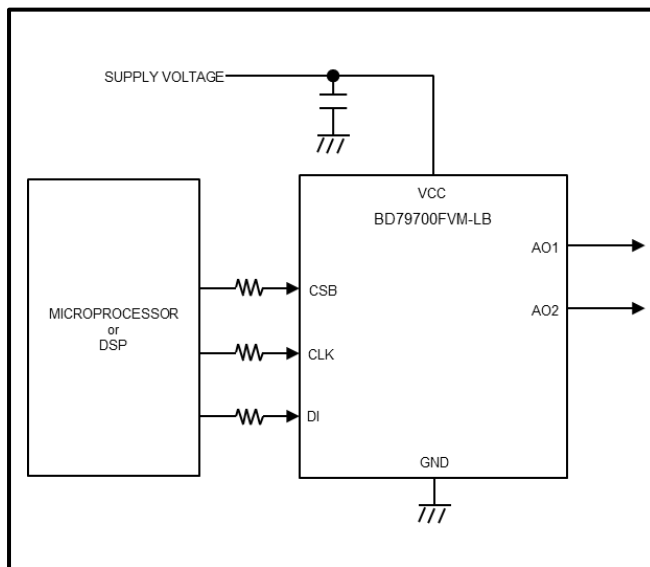
- Compact Package Enabling Adjacent Placement
- Built-in Initial Zero Hold Function
- High Speed Output Response Characteristics
- 3-line Serial Interface

### Applications

- Industrial Equipment
- Battery Operating Equipment
- Digital Gain Adjustment or Offset Adjustment
- Programmable Voltage Source or Current Source
- Programmable Attenuator



### Typical Application Circuit



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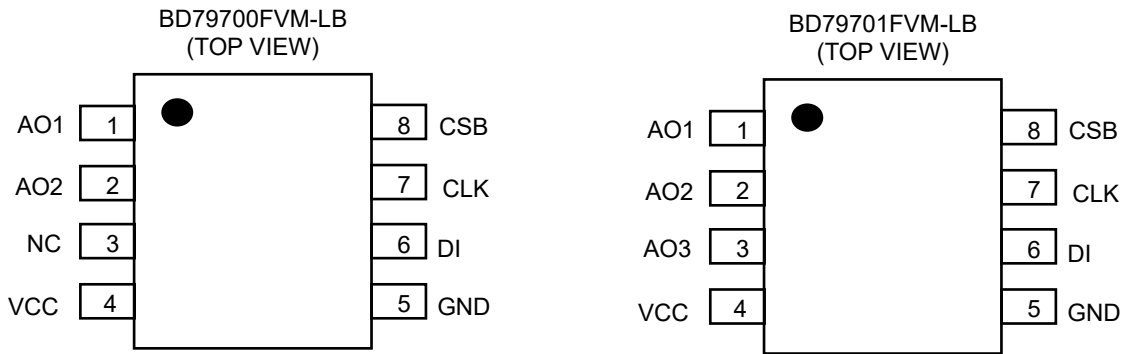
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Pin Configuration



Pin Descriptions

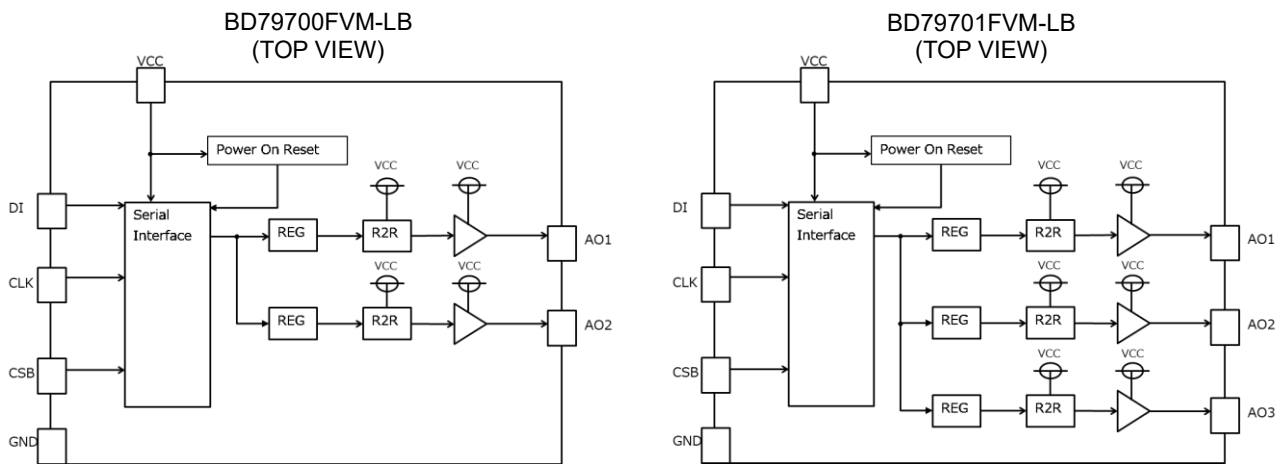
(BD79700FVM-LB)

| Pin No. | Pin Name | Function                 |
|---------|----------|--------------------------|
| 1       | AO1      | Analog output pin 1.     |
| 2       | AO2      | Analog output pin 2.     |
| 3       | NC       | NC.                      |
| 4       | VCC      | Power supply pin.        |
| 5       | GND      | Ground pin.              |
| 6       | DI       | Digital data input pin.  |
| 7       | CLK      | Digital clock input pin. |
| 8       | CSB      | Chip select input pin.   |

(BD79701FVM-LB)

| Pin No. | Pin Name | Function                 |
|---------|----------|--------------------------|
| 1       | AO1      | Analog output pin 1.     |
| 2       | AO2      | Analog output pin 2.     |
| 3       | AO3      | Analog output pin 3.     |
| 4       | VCC      | Power supply pin.        |
| 5       | GND      | Ground pin.              |
| 6       | DI       | Digital data input pin.  |
| 7       | CLK      | Digital clock input pin. |
| 8       | CSB      | Chip select input pin.   |

Block Diagram



## Absolute Maximum Ratings (Ta = 25 °C)

| Parameter                    | Symbol            | Limit                        | Unit |
|------------------------------|-------------------|------------------------------|------|
| Supply Voltage               | V <sub>CC</sub>   | 7.0                          | V    |
| Input Voltage                | V <sub>IN</sub>   | -0.3 to V <sub>CC</sub> +0.3 | V    |
| Maximum Junction Temperature | T <sub>Jmax</sub> | 150                          | °C   |
| Storage Temperature Range    | T <sub>stg</sub>  | -55 to +150                  | °C   |

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance<sup>(Note 1)</sup>

| Parameter                                                      | Symbol        | Thermal Resistance (Typ) |                        | Unit |
|----------------------------------------------------------------|---------------|--------------------------|------------------------|------|
|                                                                |               | 1s <sup>(Note 3)</sup>   | 4s <sup>(Note 4)</sup> |      |
| MSOP8                                                          |               |                          |                        |      |
| Junction to Ambient                                            | $\theta_{JA}$ | 284.1                    | 135.4                  | °C/W |
| Junction to Top Characterization Parameter <sup>(Note 2)</sup> | $\Psi_{JT}$   | 21                       | 11                     | °C/W |

(Note 1) Based on JESD51-2A (Still-Air),

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

| Layer Number of Measurement Board | Material | Board Size                    |
|-----------------------------------|----------|-------------------------------|
| Single                            | FR-4     | 114.3 mm x 76.2 mm x 1.57 mmt |

| Top                   |           |
|-----------------------|-----------|
| Copper Pattern        | Thickness |
| Footprints and Traces | 70 μm     |

| Layer Number of Measurement Board | Material | Board Size                   |
|-----------------------------------|----------|------------------------------|
| 4 Layers                          | FR-4     | 114.3 mm x 76.2 mm x 1.6 mmt |

| Top                   |           | 2 Internal Layers |           | Bottom            |           |
|-----------------------|-----------|-------------------|-----------|-------------------|-----------|
| Copper Pattern        | Thickness | Copper Pattern    | Thickness | Copper Pattern    | Thickness |
| Footprints and Traces | 70 μm     | 74.2 mm x 74.2 mm | 35 μm     | 74.2 mm x 74.2 mm | 70 μm     |

Recommended Operating Conditions

| Parameter              | Symbol            | Min | Typ | Max             | Unit |
|------------------------|-------------------|-----|-----|-----------------|------|
| Supply Voltage         | V <sub>CC</sub>   | 2.7 | -   | 5.5             | V    |
| Input Voltage          | V <sub>IN</sub>   | 0   | -   | V <sub>CC</sub> | V    |
| Operating Temperature  | T <sub>opr</sub>  | -40 | +25 | +125            | °C   |
| Serial Clock Frequency | f <sub>SCLK</sub> | -   | 10  | 30              | MHz  |
| Load Capacitance Limit | C <sub>L</sub>    | -   | -   | 1500            | pF   |

**Electrical Characteristics**(Unless otherwise specified  $V_{CC} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $f_{SCLK} = 30\text{ MHz}$ )

| Parameter                      | Symbol    | Min         | Typ             | Max         | Unit          | Conditions                                                 |
|--------------------------------|-----------|-------------|-----------------|-------------|---------------|------------------------------------------------------------|
| <Current Consumption>          |           |             |                 |             |               |                                                            |
| Power Down Current             | $I_{PD}$  | -           | 0.3             | -           | $\mu\text{A}$ | Power Down Hi-Z, CLK = 0 V, CSB = $V_{CC}$ , DI = $V_{CC}$ |
| Current Consumption            | $I_{CC}$  | -           | 0.6             | 0.9         | mA            | 780h setting                                               |
| <Logic Interface>              |           |             |                 |             |               |                                                            |
| L Input Voltage                | $V_{IL}$  | GND         | -               | $0.2V_{CC}$ | V             |                                                            |
| H Input Voltage                | $V_{IH}$  | $0.8V_{CC}$ | -               | $V_{CC}$    | V             |                                                            |
| Input Current                  | $I_{IN}$  | -10         | -               | +10         | $\mu\text{A}$ |                                                            |
| <Buffer Amplifier>             |           |             |                 |             |               |                                                            |
| Zero Scale Output Voltage      | $V_{ZSO}$ | -           | 10              | -           | mV            | $V_{CC} = 5\text{ V}$ , $I_{OH} = 1\text{ mA}$             |
| Full Scale Output Voltage      | $V_{FSO}$ | -           | $V_{CC} - 0.05$ | -           | V             | $V_{CC} = 5\text{ V}$ , $I_{OL} = 1\text{ mA}$             |
| <D/A Converter Precision>      |           |             |                 |             |               |                                                            |
| Differential Non Linearity     | DNL       | -0.5        | -               | +0.5        | LSB           | Input range is 3 to 252                                    |
| Integral Non Linearity         | INL       | -0.5        | -               | +0.5        | LSB           | Input range is 3 to 252                                    |
| Power Source Voltage Rise Time | $t_{VCC}$ | 100         | -               | -           | $\mu\text{s}$ |                                                            |
| Power On Reset Release Voltage | $V_{POR}$ | -           | 1.2             | -           | V             |                                                            |

Timing Specifications

(Unless otherwise specified V<sub>CC</sub> = 2.7 V to 5.5 V, Ta = 25 °C, f<sub>SCLK</sub> = 30 MHz)

| Parameter                | Symbol            | Min | Typ | Max | Unit | Conditions                                                                       |
|--------------------------|-------------------|-----|-----|-----|------|----------------------------------------------------------------------------------|
| CLK L Level Time         | t <sub>CLKL</sub> | 10  | -   | -   | ns   |                                                                                  |
| CLK H Level Time         | t <sub>CLKH</sub> | 10  | -   | -   | ns   |                                                                                  |
| DI Setup Time            | t <sub>sDI</sub>  | 3.5 | -   | -   | ns   |                                                                                  |
| DI Hold Time             | t <sub>hDI</sub>  | 3.5 | -   | -   | ns   |                                                                                  |
| CSB Setup Time           | t <sub>sCSB</sub> | 10  | -   | -   | ns   |                                                                                  |
| CSB Hold Time            | t <sub>hCSB</sub> | 10  | -   | -   | ns   |                                                                                  |
| CSB H Level Time         | t <sub>CSBH</sub> | 10  | -   | -   | ns   |                                                                                  |
| D/A Output Settling Time | t <sub>OUT</sub>  | -   | -   | 4.5 | μs   | C <sub>L</sub> = 200 pF, R <sub>L</sub> = 2 kΩ<br>Set-up Time<br>from 40h to C0h |

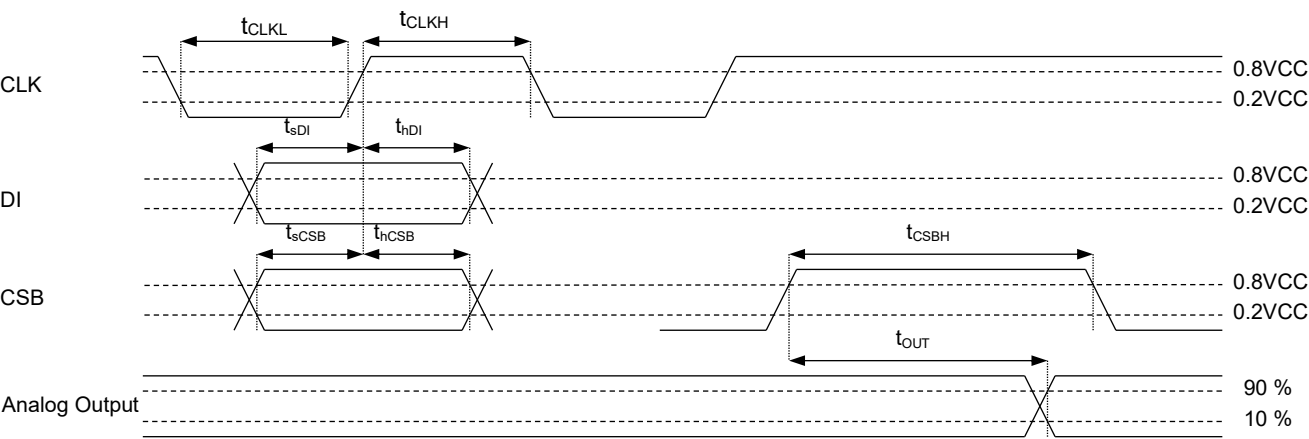
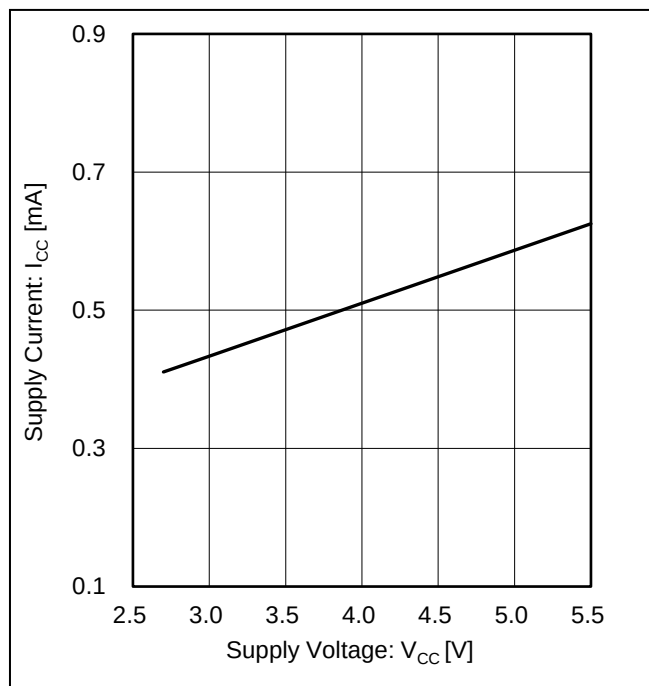
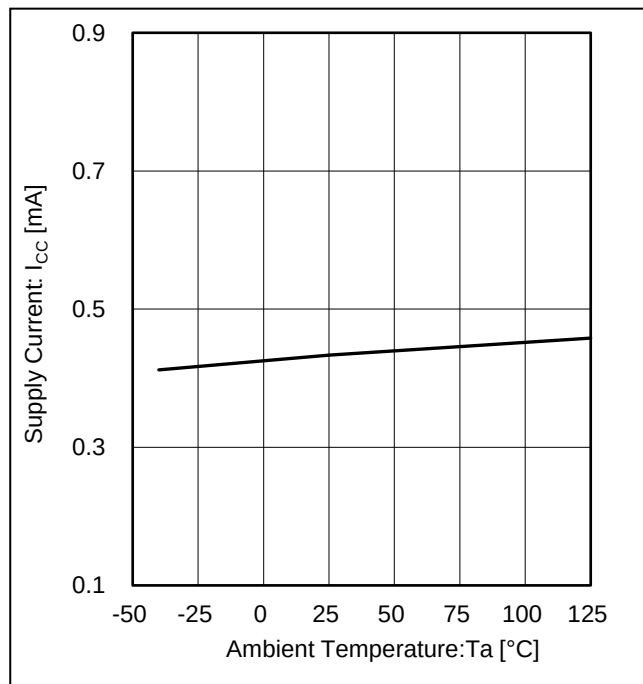
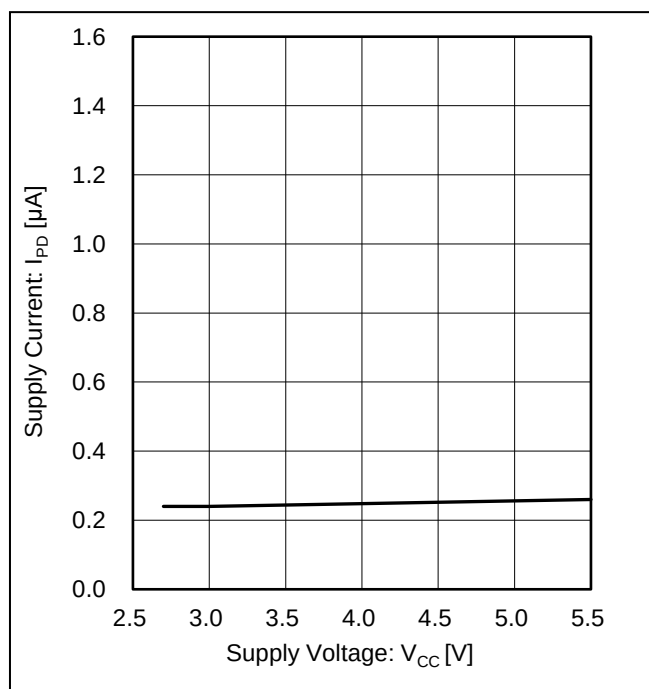
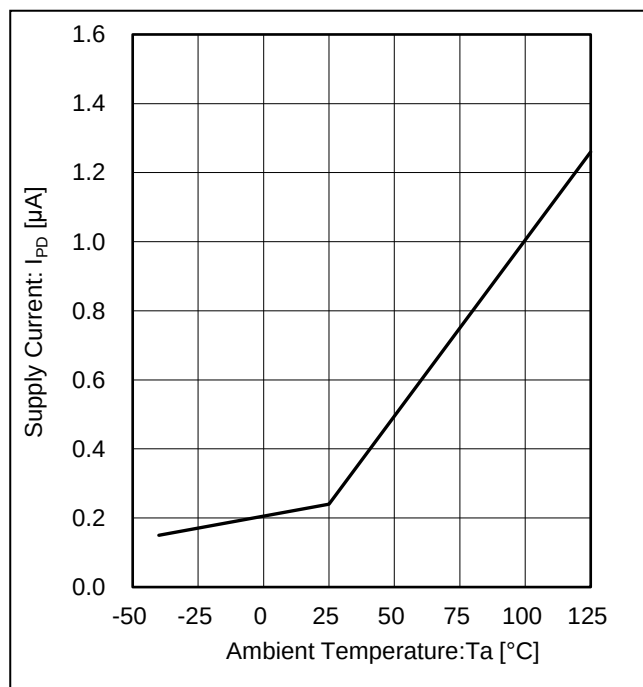


Figure 1. 3-line Serial Bus and Analog Output Timing Chart

## Typical Performance Curves

(Reference Data)

Unless otherwise specified  $V_{CC} = 3\text{ V}$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $f_{SCLK} = 30\text{ MHz}$ Figure 2. Supply Current vs Supply Voltage  
( $V_{CC}$  Current Consumption)Figure 3. Supply Current vs Ambient Temperature  
( $V_{CC}$  Current Consumption)Figure 4. Supply Current vs Supply Voltage  
(Power-down Current)Figure 5. Supply Current vs Ambient Temperature  
(Power-down Current)



## Typical Performance Curves – continued

(Reference Data)

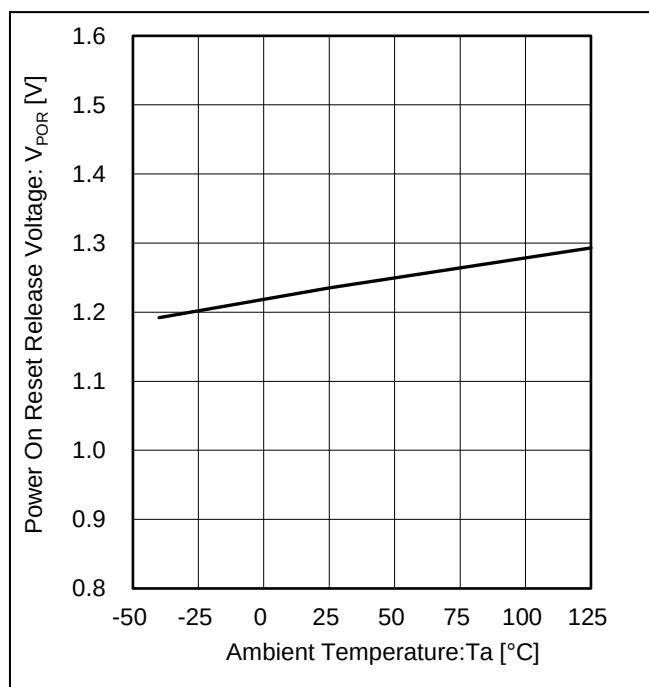
Unless otherwise specified  $V_{CC} = 3\text{ V}$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $f_{SCLK} = 30\text{ MHz}$ 

Figure 6. Power On Reset Release Voltage vs Ambient Temperature

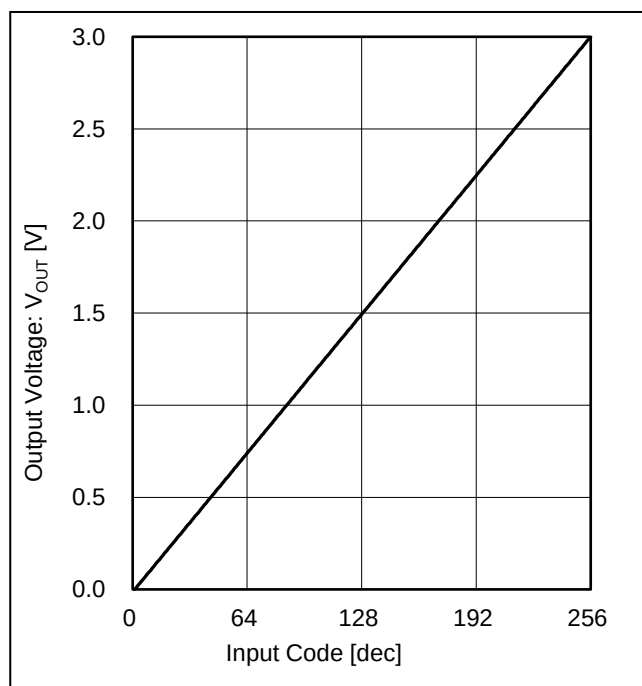


Figure 7. Output Voltage vs Input Code

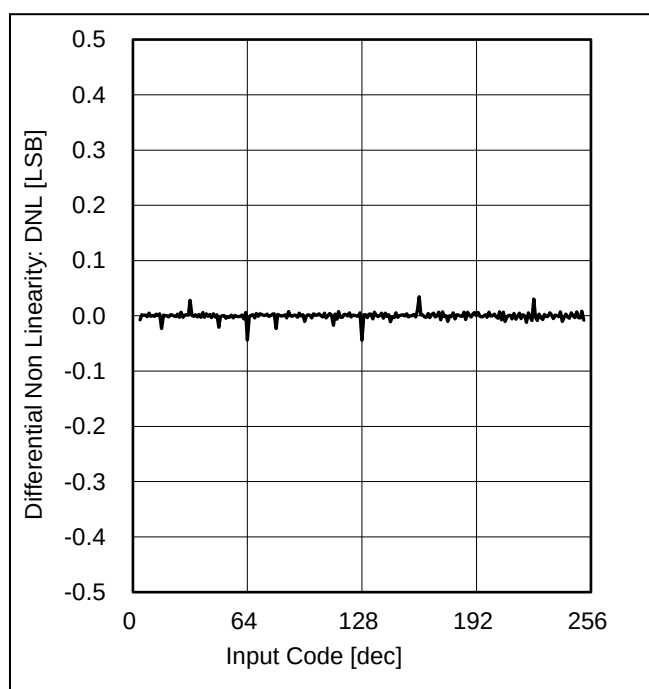


Figure 8. Differential Non Linearity vs Input Code

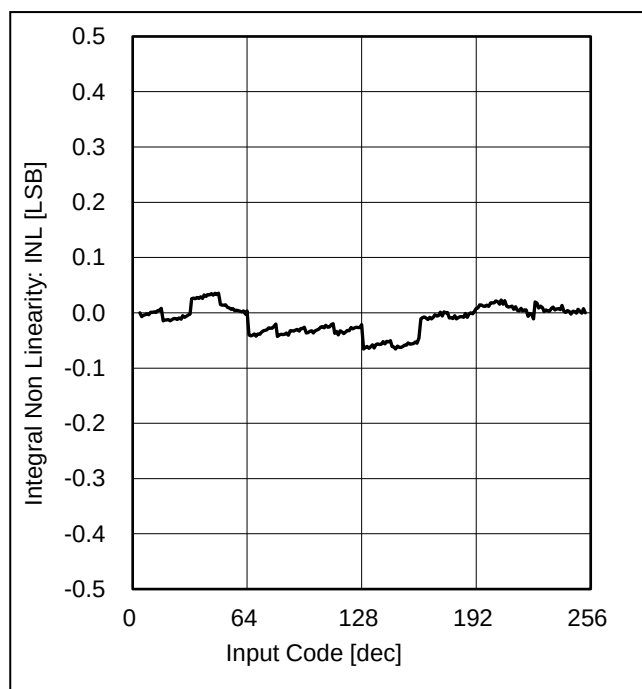


Figure 9. Integral Non Linearity vs Input Code

Typical Performance Curves – continued  
(Reference Data)  
Unless otherwise specified  $V_{CC} = 3\text{ V}$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $f_{SCLK} = 30\text{ MHz}$

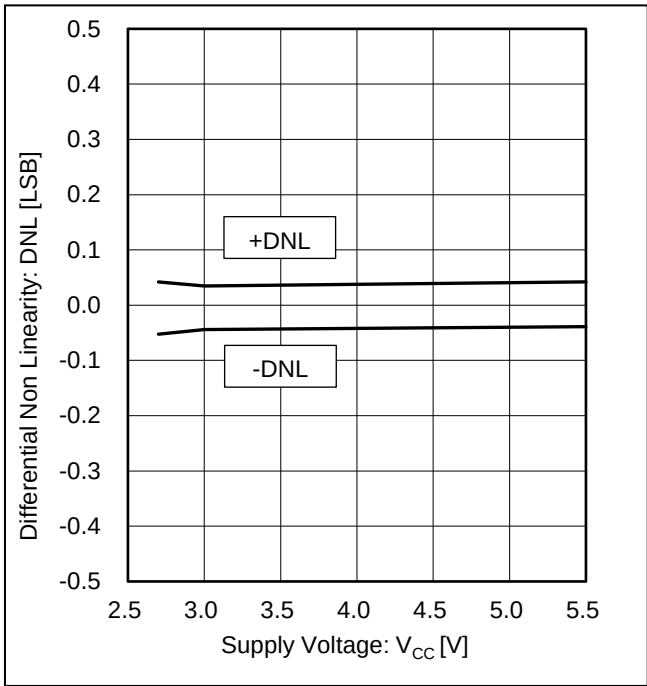


Figure 10. Differential Non Linearity vs Supply Voltage

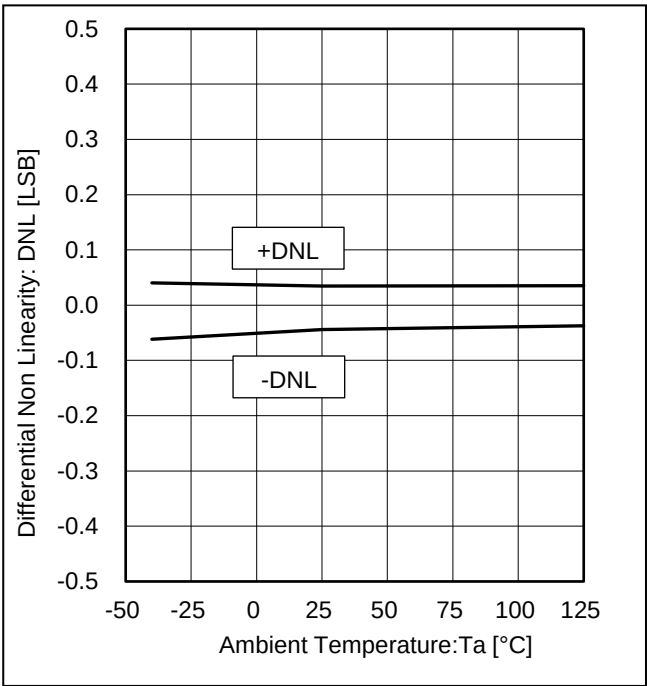


Figure 11. Differential Non Linearity vs Ambient Temperature

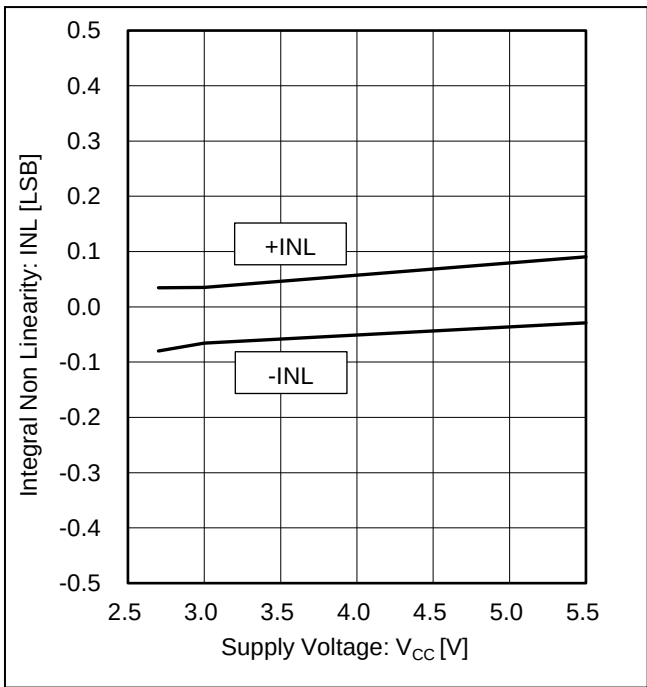


Figure 12. Integral Non Linearity vs Supply Voltage

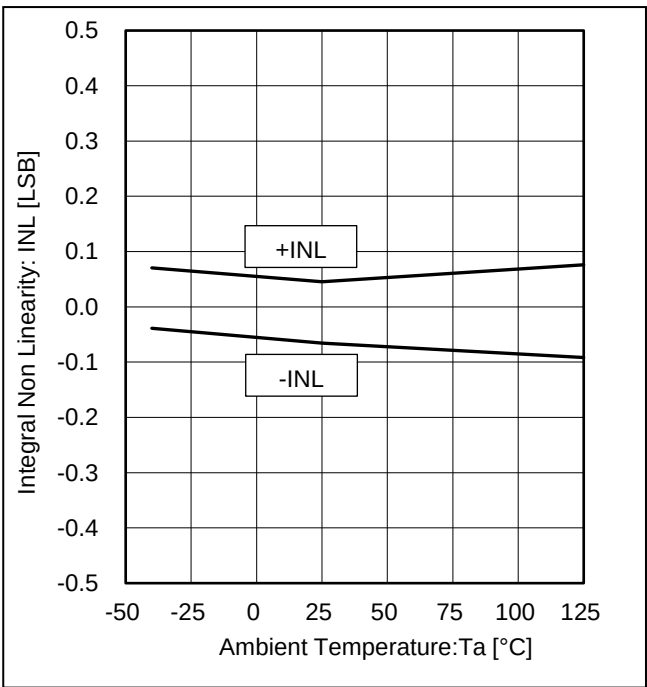


Figure 13. Integral Non Linearity vs Ambient Temperature

Typical Performance Curves – continued

(Reference Data)

Unless otherwise specified  $V_{CC} = 3\text{ V}$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $f_{SCLK} = 30\text{ MHz}$

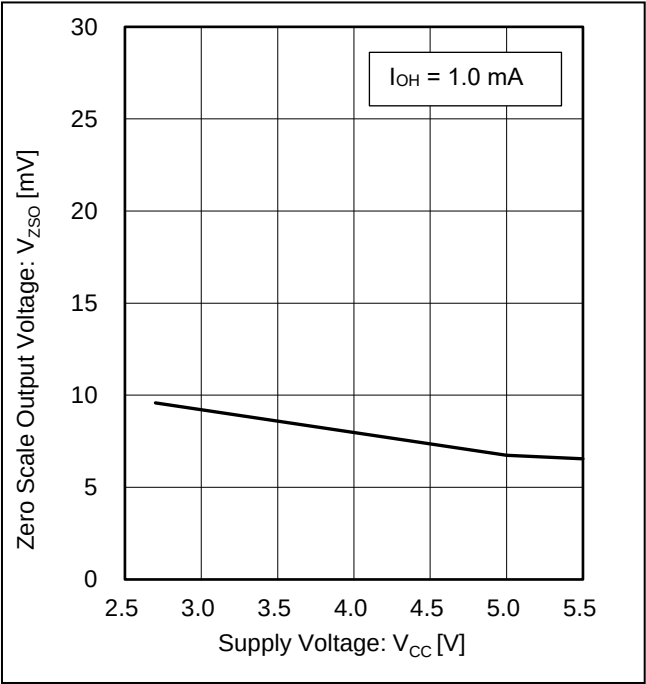


Figure 14. Zero Scale Output Voltage vs Supply Voltage

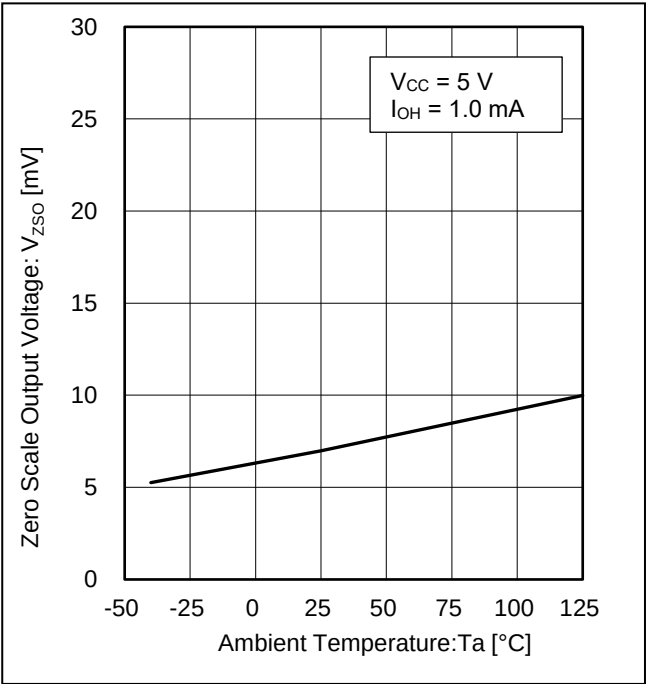


Figure 15. Zero Scale Output Voltage vs Ambient Temperature

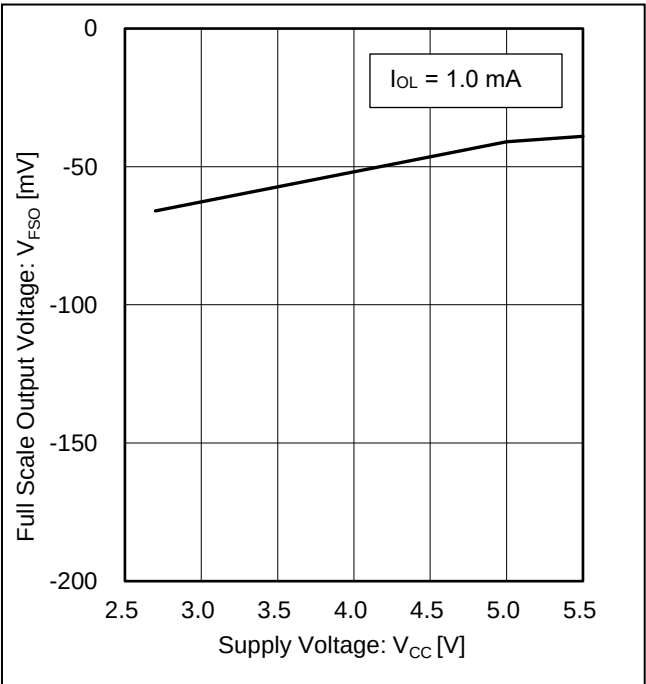


Figure 16. Full Scale Output Voltage vs Supply Voltage

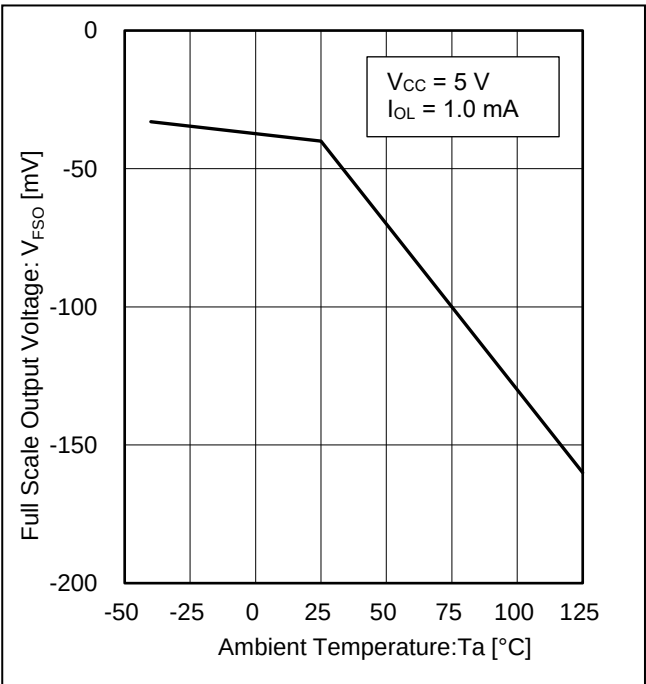


Figure 17. Full Scale Output Voltage vs Ambient Temperature

Typical Performance Curves – continued  
(Reference Data)  
Unless otherwise specified  $V_{CC} = 3\text{ V}$ ,  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $f_{SCLK} = 30\text{ MHz}$

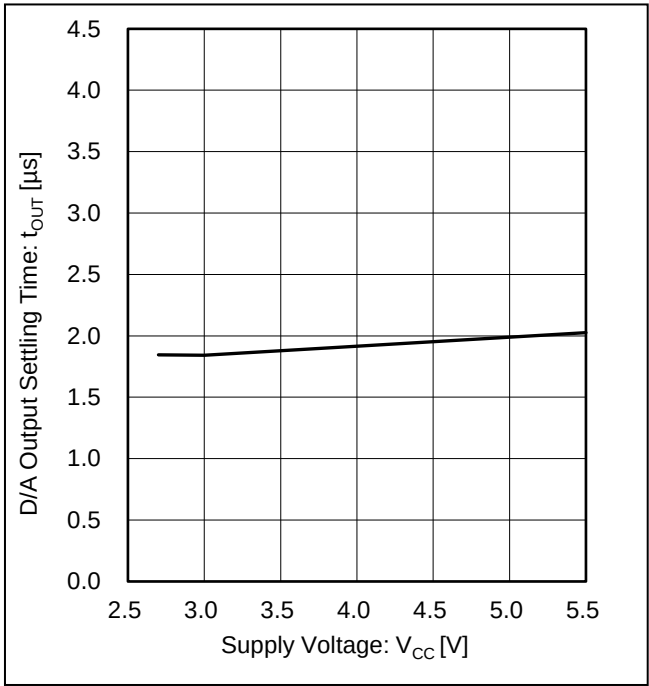


Figure 18. D/A Output Settling Time vs Supply Voltage

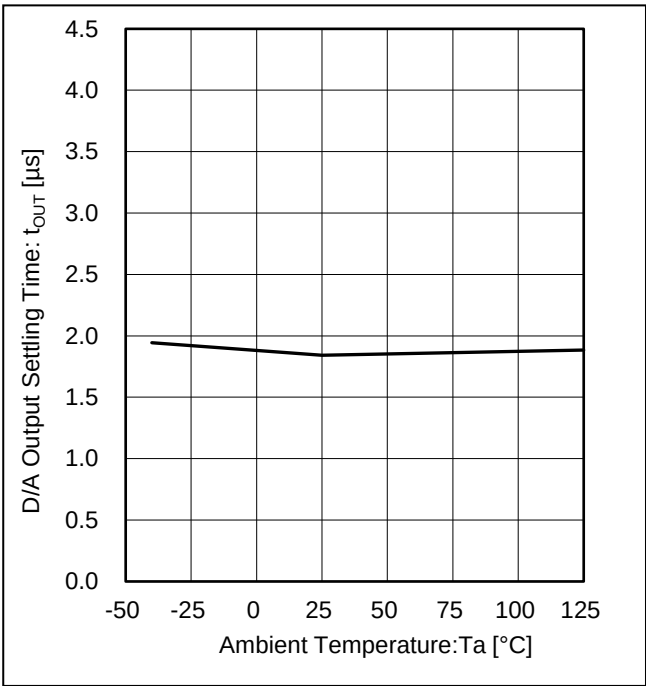


Figure 19. D/A Output Settling Time vs Ambient Temperature

**Communication Format**

The Serial Control Interface is 3-line 12 bit serial interface (MSB first).

DI data is read every rising edge of the CLK.

Last 12 bits of data are latched when CSB goes HIGH.

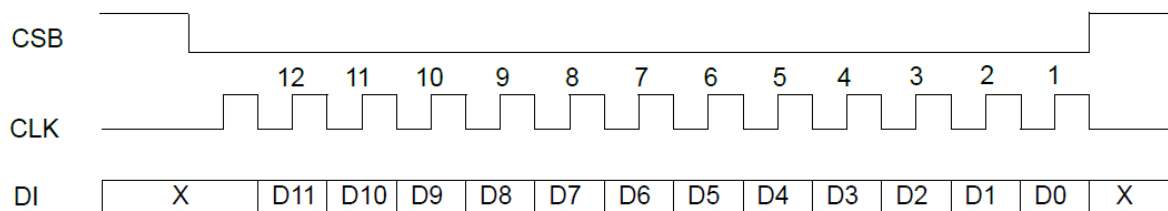


Figure 20. Communication Format

**Register Map** (Note 5)

## Channel setting

| D11 | D10 | D9 | D8 | D7 to D0       | BD79700FVM-LB                  | BD79701FVM-LB                  |
|-----|-----|----|----|----------------|--------------------------------|--------------------------------|
| 0   | 0   | 0  | 0  | 0000_0000      | Power Down 100 kΩ              | Power Down 100 kΩ              |
| 0   | 0   | 0  | 1  | D/A DATA [7:0] | AO1 Data Setting and Output    | AO1 Data Setting and Output    |
| 0   | 0   | 1  | 0  | D/A DATA [7:0] | AO2 Data Setting and Output    | AO2 Data Setting and Output    |
| 0   | 0   | 1  | 1  | D/A DATA [7:0] | Not used                       | AO3 Data Setting and Output    |
| 0   | 1   | 0  | 0  | 0000_0000      | Not used                       | Not used                       |
| 0   | 1   | 0  | 1  | 0000_0000      | Not used                       | Not used                       |
| 0   | 1   | 1  | 0  | 0000_0000      | Not used                       | Not used                       |
| 0   | 1   | 1  | 1  | D/A DATA [7:0] | All Channel Setting and Output | All Channel Setting and Output |
| 1   | 0   | 0  | 0  | 0000_0000      | Power Down 2.5 kΩ              | Power Down 2.5 kΩ              |
| 1   | 0   | 0  | 1  | D/A DATA [7:0] | AO1 Data Setting Only          | AO1 Data Setting Only          |
| 1   | 0   | 1  | 0  | D/A DATA [7:0] | AO2 Data Setting Only          | AO2 Data Setting Only          |
| 1   | 0   | 1  | 1  | D/A DATA [7:0] | Not used                       | AO3 Data Setting Only          |
| 1   | 1   | 0  | 0  | 0000_0000      | Not used                       | Not used                       |
| 1   | 1   | 0  | 1  | 0000_0000      | Not used                       | Not used                       |
| 1   | 1   | 1  | 0  | 0000_0000      | Not used                       | Not used                       |
| 1   | 1   | 1  | 1  | 0000_0000      | Power Down Hi-Z                | Power Down Hi-Z                |

## Data Setting

| D/A DATA [7:0] |    |    |    |    |    |    |    | Setting             |
|----------------|----|----|----|----|----|----|----|---------------------|
| D7             | D6 | D5 | D4 | D3 | D2 | D1 | D0 |                     |
| 0              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | GND                 |
| 0              | 0  | 0  | 0  | 0  | 0  | 0  | 1  | (Vcc - GND)/256x1   |
| 0              | 0  | 0  | 0  | 0  | 0  | 1  | 0  | (Vcc - GND)/256x2   |
| 0              | 0  | 0  | 0  | 0  | 0  | 1  | 1  | (Vcc - GND)/256x3   |
| 0              | 0  | 0  | 0  | 0  | 1  | 0  | 0  | (Vcc - GND)/256x4   |
| 1              | 1  | 1  | 1  | 1  | 1  | 1  | 0  | (Vcc - GND)/256x254 |
| 1              | 1  | 1  | 1  | 1  | 1  | 1  | 1  | (Vcc - GND)/256x255 |

(Note 5) Do not write '1' to the fields in which value is '0' in above table.

## Resister Map – continued

BD79700FVM-LB, BD79701FVM-LB common  
(000h, 800h, F00h) Power Down Enable

|                         |                                                             |
|-------------------------|-------------------------------------------------------------|
| 000h, Power Down 100 kΩ | All channel are power down mode. Output is 100 kΩ pulldown. |
| 800h, Power Down 2.5 kΩ | All channel are power down mode. Output is 2.5 kΩ pulldown. |
| F00h, Power Down Hiz    | All channel are power down mode. Output is Hiz state.       |

Default value 0x800

BD79700FVM-LB

(1xxh to 7xxh) DAC Output

|                          |                                                     |
|--------------------------|-----------------------------------------------------|
| 1xxh, AO1 Output         | Output AO1 with setting data from D7 to D0.         |
| 2xxh, AO2 Output         | Output AO2 with setting data from D7 to D0.         |
| 3xxh, Not used           | Not used                                            |
| 4xxh, Not used           | Not used                                            |
| 5xxh, Not used           | Not used                                            |
| 6xxh, Not used           | Not used                                            |
| 7xxh, All Channel Output | Output All channel with setting data from D7 to D0. |

Default value 0x000

(9xxh to Exxh) DAC Data Setting Only

|                             |                                                                            |
|-----------------------------|----------------------------------------------------------------------------|
| 9xxh, AO1 Data Setting Only | Set ch1 DAC code with setting data from D7 to D0.<br>Output is no changed. |
| Axxh, AO2 Data Setting Only | Set ch2 DAC code with setting data from D7 to D0.<br>Output is no changed. |
| Bxxh, Not used              | Not used                                                                   |
| Cxxh, Not used              | Not used                                                                   |
| Dxxh, Not used              | Not used                                                                   |
| Exxh, Not used              | Not used                                                                   |

Default value 0x000

BD79701FVM-LB

(1xxh to 7xxh) DAC Output

|                          |                                                     |
|--------------------------|-----------------------------------------------------|
| 1xxh, AO1 Output         | Output AO1 with setting data from D7 to D0.         |
| 2xxh, AO2 Output         | Output AO2 with setting data from D7 to D0.         |
| 3xxh, AO3 Output         | Output AO3 with setting data from D7 to D0.         |
| 4xxh, Not used           | Not used                                            |
| 5xxh, Not used           | Not used                                            |
| 6xxh, Not used           | Not used                                            |
| 7xxh, All Channel Output | Output All channel with setting data from D7 to D0. |

Default value 0x000

(9xxh to Exxh) DAC Data Setting Only

|                             |                                                                            |
|-----------------------------|----------------------------------------------------------------------------|
| 9xxh, AO1 Data Setting Only | Set ch1 DAC code with setting data from D7 to D0.<br>Output is no changed. |
| Axxh, AO2 Data Setting Only | Set ch2 DAC code with setting data from D7 to D0.<br>Output is no changed. |
| Bxxh, AO3 Data Setting Only | Set ch3 DAC code with setting data from D7 to D0.<br>Output is no changed. |
| Cxxh, Not used              | Not used                                                                   |
| Dxxh, Not used              | Not used                                                                   |
| Exxh, Not used              | Not used                                                                   |

Default value 0x000

Resister Map – continued

Example Send Command DAC Output

|          | Send Command | Command details    | AO1                              | AO2                              |
|----------|--------------|--------------------|----------------------------------|----------------------------------|
| Power On | -            | -                  | Power Down 2.5 kΩ                | Power Down 2.5 kΩ                |
| Step1    | 780h         | Output All channel | Output (V <sub>CC</sub> - GND)/2 | Output (V <sub>CC</sub> - GND)/2 |
| Step2    | 1FFh         | Output AO1         | Output V <sub>CC</sub>           | Output (V <sub>CC</sub> - GND)/2 |

Example Send Command DAC Data Setting Only

|          | Send Command | Command details                                | AO1                              | AO2                              |
|----------|--------------|------------------------------------------------|----------------------------------|----------------------------------|
| Power On | -            | -                                              | Power Down 2.5 kΩ                | Power Down 2.5 kΩ                |
| Step1    | 780h         | Output All channel                             | Output (V <sub>CC</sub> - GND)/2 | Output (V <sub>CC</sub> - GND)/2 |
| Step2    | A00h         | Set ch2 DAC data<br>Output is no changed       | Output (V <sub>CC</sub> - GND)/2 | Output (V <sub>CC</sub> - GND)/2 |
| Step3    | 1FFh         | Output AO1<br>All channel update<br>DAC output | Output V <sub>CC</sub>           | Output GND                       |

Application Example

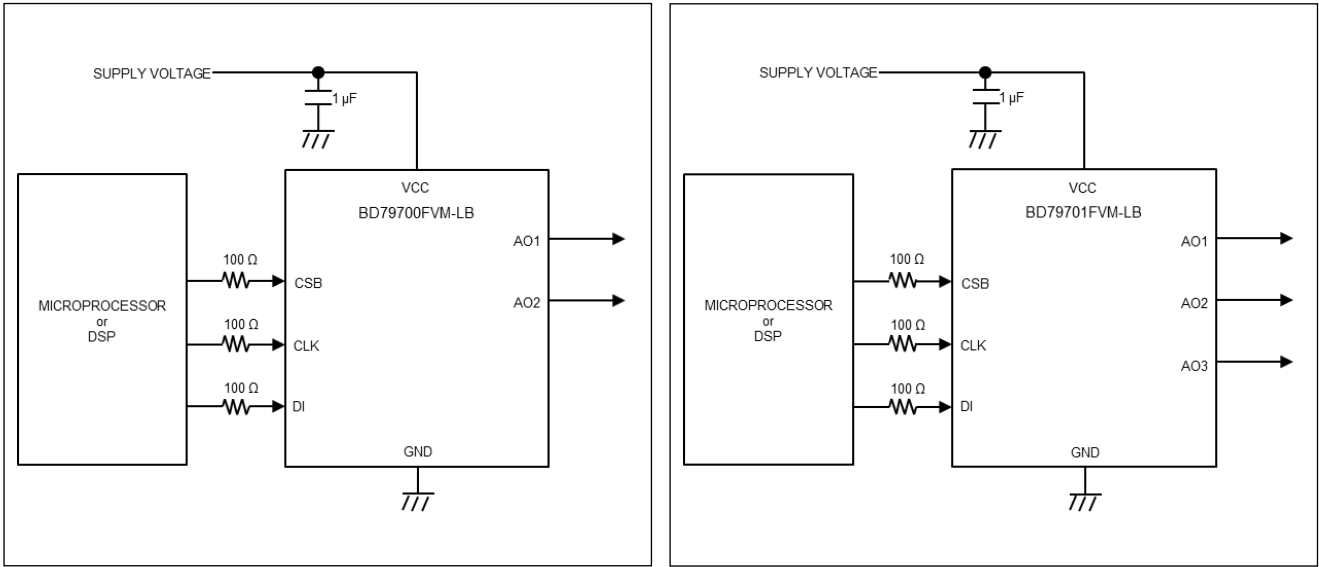


Figure 21. Application Circuit

I/O Equivalence Circuit

| Pin Name          | Equivalent Circuit Diagram | Pin Name         | Equivalent Circuit Diagram |
|-------------------|----------------------------|------------------|----------------------------|
| AO1<br>AO2<br>AO3 |                            | DI<br>CLK<br>CSB |                            |

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.



## Operational Notes – continued

**10. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin\ A$  and  $GND > Pin\ B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin\ B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

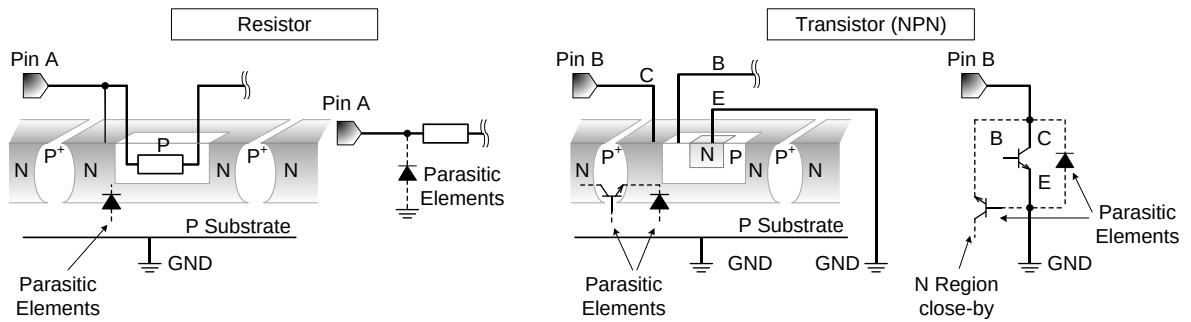
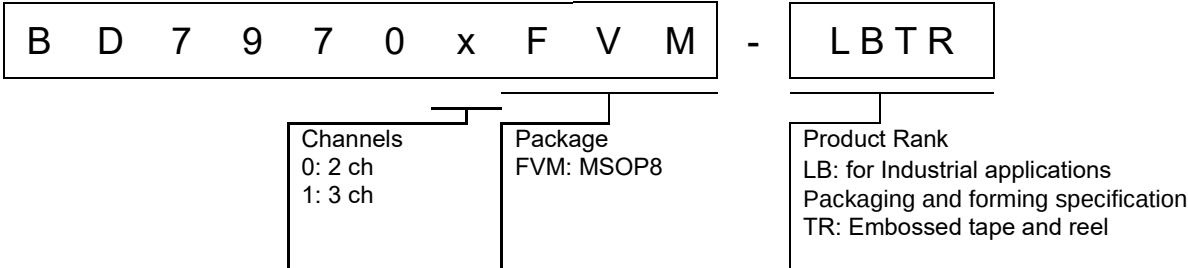


Figure 22. Example of Monolithic IC Structure

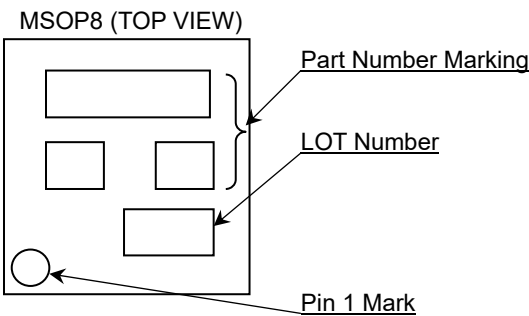
**11. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

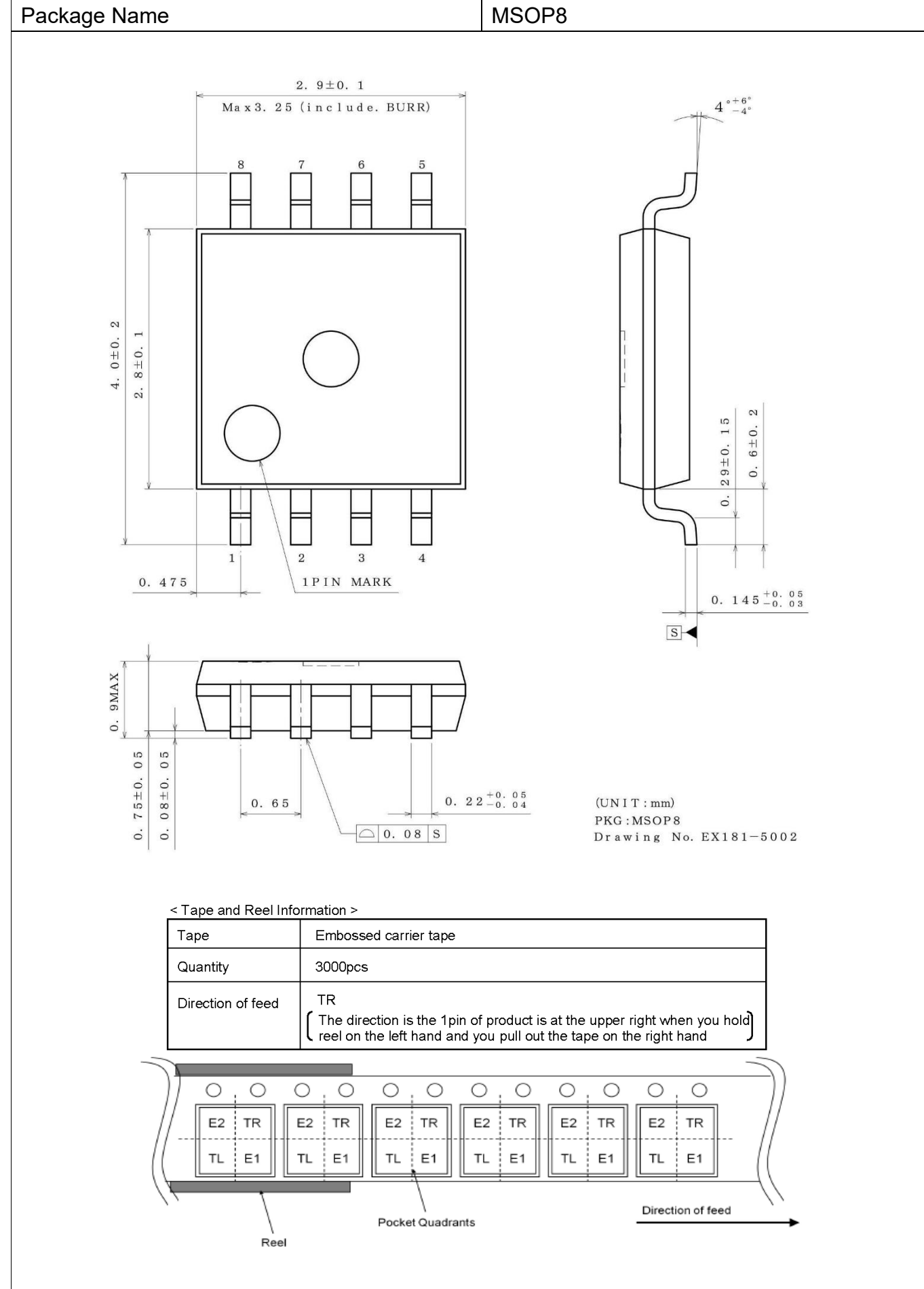


Marking Diagram



| Part Number Marking | Package | Orderable Part Number |
|---------------------|---------|-----------------------|
| 79700               | MSOP8   | BD79700FVM-LBTR       |
| 79701               |         | BD79701FVM-LBTR       |

Physical Dimension and Packing Information



Revision History

| Date        | Revision | Changes     |
|-------------|----------|-------------|
| 05.Mar.2024 | 001      | New Release |

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(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN     | USA       | EU         | CHINA     |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

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  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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