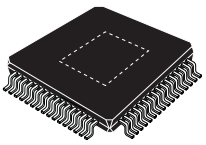
L9396

Automotive multiple power supply IC

Datasheet - Production data



TQFP64 (exposed pad down)

GAPGPS00129

Features



- AEC-Q100 qualified
- FFull ISO26262 compliant, ASIL-D systems ready
- Integrated boost regulator, 9 V, 300 mA, 2 MHz (opt. populated diode & inductor) for deep cranking pulse (Stop&Start) & weak battery conditions
- Integrated buck pre-regulator, 6.5 V / 7.2 V, 1 A, 465 kHz
- Integrated LDO, 5 V, 250 mA for µC I/O and ADC supply
- Integrated configurable LDO, 3.3 V / 5 V, 100 mA for µC I/O supply
- Configurable and programmable regulator with external FET, 0.8 V to 5 V for µC core supply
  - up to 1 A in buck configuration
  - up to 750 mA in linear configuration
- Spread spectrum approach to reduce EMC emissions
- Four channels configurable remote sensor interface
  - wheel speed sensor protocol
  - tracking regulator supply (3.3 V - 5 V)
  - reverse battery protection and integrated digital decoding
- High-side pre-drivers for fail safe (On/off control) and for motor pump (PWM control)
- SPI communication bus
- Configurable 3.3 V / 5 V I/O level
- Configurable and programmable double watchdog (Q&A WD and time-windowed WD)
- Double voltage reference for regulated rail reference and monitoring
- Configurable Fail-Safe Functionality (Mode / Safe Delay)
- Fail-Safe Output (FSN)
- Wake-up input
- Low-side general purpose output with programmable PWM control
- Integrated 10-bits ADC with system diagnostics
- Discrete analog inputs for integrated ADC measurement (3 ch.)
- Voltage monitoring UV/OV on all regulated rails
- Temperature monitoring and thermal shutdown
- Operating voltage: VBATP: 4.5 V to 19 V with boost; 6 V to 19 V without boost
- Ambient temperature range: -40 °C to 135 °C
- Package: TQFP64EP (10x10x1mm)

Table 1. Device summary

Order code	Package	Packing
L9396	TQFP64 10 x 10 x 1 mm (exposed pad down)	Tray
L9396-TR		Tape & Reel

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Contents

1 **Description** 8

2 **Overall description** 9

2.1 Block diagram 9

2.2 Pins description 10

2.3 Absolute maximum ratings 13

2.4 Operating range 16

3 **Power supply** 18

3.1 Battery range 18

3.2 Boost regulator 19

3.3 Internal supply 21

3.4 Wake-up input 22

3.5 Charge pump 23

3.6 VPREREG buck regulator 24

3.7 VCORE regulator 27

3.8 VCC5 regulator 32

3.9 VCC regulator 33

3.10 Protected battery switch 34

3.11 Power up and power down sequences 35

4 **Pre-drivers** 37

4.1 Fail safe pre-driver 37

4.2 Pump motor pre-driver 38

4.3 Pump motor diagnostics 38

5 **Remote sensor interface** 43

5.1 Active wheel speed sensor 43

5.1.1 Wheel speed data register formats 46

5.1.2 Testmode 46

5.1.3 Wheel Speed SPI Registers 46

5.2 Tracking regulation 58

5.3 Remote sensor interface fault protection 58

Downloaded from Arrow.com.

5.4 Electrical characteristics 59

6 General purpose output (GPO) driver 62

7 System functional safety implementations 64

7.1 General functional safety implementations 64

7.2 System monitoring and reset handling 64

7.2.1 Analog to Digital algorithmic converter 64

7.2.2 Voltage measurement 65

7.2.3 Reset output 68

7.2.4 Oscillator 69

7.3 Fault output 70

7.4 Watchdog control 71

7.4.1 Watchdog (WD1) 72

7.4.2 Second Watchdog (WD2) 83

7.4.3 Watchdog Timer Disable Input (WDTDIS) 84

7.5 Fail safe output 85

7.6 Temperature sensor 87

7.7 Over temperature protection 87

7.8 Bist 87

7.8.1 Logic Bist 87

7.8.2 Analog Bist 88

7.8.3 OTP check 88

8 Serial Peripheral Communication 89

8.1 CRC Field Details 89

8.2 SPI frame 89

8.3 SPI registers 91

8.4 SPI parameters 102

8.4.1 DC Electrical Parameters 102

8.4.2 AC electrical parameters 103

9 Package information 104

9.1 TQFP64 (10x10x1 mm exp. pad down) package information 104

9.2 TQFP64 (10x10x1 mm exp. pad down) marking information 107

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10 Revision history 108

Downloaded from Arrow.com.

List of tables

Table 1. Device summary . . . 1
Table 2. Pins description . . . 9
Table 3. Pin absolute maximum ratings . . . 12
Table 4. Pin operating range . . . 15
Table 5. Configuration and control DC specifications . . . 17
Table 6. Boost regulator electrical characteristics . . . 19
Table 7. Internal supply electrical characteristics . . . 21
Table 8. Wake-up input electrical characteristics . . . 22
Table 9. Charge pump electrical characteristics . . . 23
Table 10. VPREREG buck regulator . . . 24
Table 11. Vcore configuration . . . 27
Table 12. VCORE regulator electrical characteristics . . . 27
Table 13. VCC5 regulator electrical characteristics . . . 31
Table 14. VCC regulator electrical characteristics . . . 32
Table 15. Protected battery switch electrical characteristics . . . 33
Table 16. Power up and power down . . . 35
Table 17. Fail Safe pre-driver electrical characteristics . . . 37
Table 18. Logical operation definition . . . 38
Table 19. Pump motor diagnostics electrical characteristics . . . 40
Table 20. WSS_TEST register . . . 46
Table 21. WSS_TEST register bit description . . . 47
Table 22. RS_CFG_0_1 register . . . 47
Table 23. RS_CFG_0_1 register bit description . . . 47
Table 24. RS_CFG_2_3 register . . . 49
Table 25. RS_CFG_2_3 register bit description . . . 49
Table 26. RS_CTRL register . . . 51
Table 27. RS_CTRL register bit description . . . 51
Table 28. RS_AUX_CFG register . . . 52
Table 29. RS_AUX_CFG register bit description . . . 52
Table 30. RS_DATA_RSDR_0-3 registers . . . 53
Table 31. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 0] . . . 53
Table 32. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 1] . . . 54
Table 33. RS_DATA_RSDR_4-7 registers . . . 56
Table 34. RS_DATA_RSDR_4-7 registers bit description . . . 56
Table 35. RS_DATA_RSDR_8-11 registers . . . 57
Table 36. RS_DATA_RSDR_8-11 registers bit description . . . 57
Table 37. RS_DATA_RSDR_12 register . . . 57
Table 38. RS_DATA_RSDR_12 register bit description . . . 57
Table 39. RSU_STATUS register . . . 58
Table 40. RSU_STATUS register bit description . . . 58
Table 41. WSS configuration . . . 59
Table 42. Tracking regulation configuration . . . 60
Table 43. Assignment matrix configured via SPI . . . 62
Table 44. GPO electrical characteristics . . . 62
Table 45. Analog to digital converter . . . 65
Table 46. Conversion time . . . 66
Table 47. Divider ratios vary by measurement are summarized by function . . . 66
Table 48. Voltage measurement electrical characteristics . . . 67

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Table 49. Reset electrical characteristics . . . 69
Table 50. Oscillator electrical characteristics . . . 70
Table 51. Masking bits and fault sources . . . 71
Table 52. Fault characteristics . . . 71
Table 53. Description of the timing parameter . . . 73
Table 54. WD2 characteristics . . . 84
Table 55. WDTDIS characteristics . . . 85
Table 56. Masking bits and fault sources . . . 85
Table 57. Fail safe output . . . 86
Table 58. Temperature sensor . . . 87
Table 59. Logic Bist . . . 88
Table 60. Registers summary . . . 92
Table 61. DC electrical characteristics . . . 102
Table 62. SPI timing characteristics . . . 103
Table 63. TQFP64 (10x10x1 mm exp. pad down) package mechanical data . . . 105
Table 64. Document revision history . . . 108

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List of figures

Figure 1. Block diagram . . . 9
Figure 2. Pins connection diagram (top view) . . . 10
Figure 3. Boost regulator block diagram . . . 19
Figure 4. Charge pump block diagram . . . 23
Figure 5. VCORE configuration diagram (buck regulator - top, linear regulator - bottom) . . . 27
Figure 6. Power up sequence from wake up input . . . 35
Figure 7. Power down sequence from wake up input . . . 36
Figure 8. Standstill operation diagram . . . 44
Figure 9. Wheel speed sensor protocol types . . . 45
Figure 10. ADC conversion time . . . 65
Figure 11. Reset input logic diagram . . . 68
Figure 12. Reset output logic diagram . . . 69
Figure 13. WD1 block diagram . . . 72
Figure 14. Mono-directional timing check evolution . . . 72
Figure 15. Bidirectional timing check evolution . . . 73
Figure 16. Timing State evolution depending on WD_TO_RST_EN and WD_REQ_CHECK_EN . . . 74
Figure 17. WD1 state machine . . . 75
Figure 18. WD1_RESET & DRIVERS ENABLE versus WD_CNT value . . . 76
Figure 19. Seed generation algorithm block diagram . . . 77
Figure 20. Seed selection and elaboration flow . . . 77
Figure 21. Answer check generation algorithm block diagram . . . 77
Figure 22. WD2 timing diagram . . . 83
Figure 23. WD2 diagram . . . 84
Figure 24. GSW[8..0] bits . . . 90
Figure 25. SPI timing diagram . . . 103
Figure 26. TQFP64 (10x10x1 mm exp. pad down) package outline . . . 104
Figure 27. TQFP64 (10x10x1 mm exp. pad down) marking information . . . 107

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1 Description

The L9396 is an integrated power management System Basis Chip targeting a large spectrum of automotive electronics applications, in particular ABS, EPS and Transmission, compatible with single (12 V) battery system.

It combines a switched mode power supply for pre-regulation along with 3 independent integrated linear regulators and a powerful configurable regulator for µC supply that can operate either in buck or linear mode with an external FET.

The device also integrates a 4-channel flexible interface for Wheel Speed Sensor or tracking regulation, 2 configurable pre-drivers for fail safe and motor pump, 1 configurable general purpose outputs, wake-up detection circuitry, advanced fail-safe functionality, watchdog control and system monitoring.

The boost regulator (optionally enabled) is intended to sustain cold cranking pulses, stop & start and weak battery conditions, while the buck pre-regulator drastically improves the power efficiency and CO2 emissions.

Different combinations enable to supply the system microcontroller and external peripheral loads and sensors with wide current ranges and adjustable voltage levels.

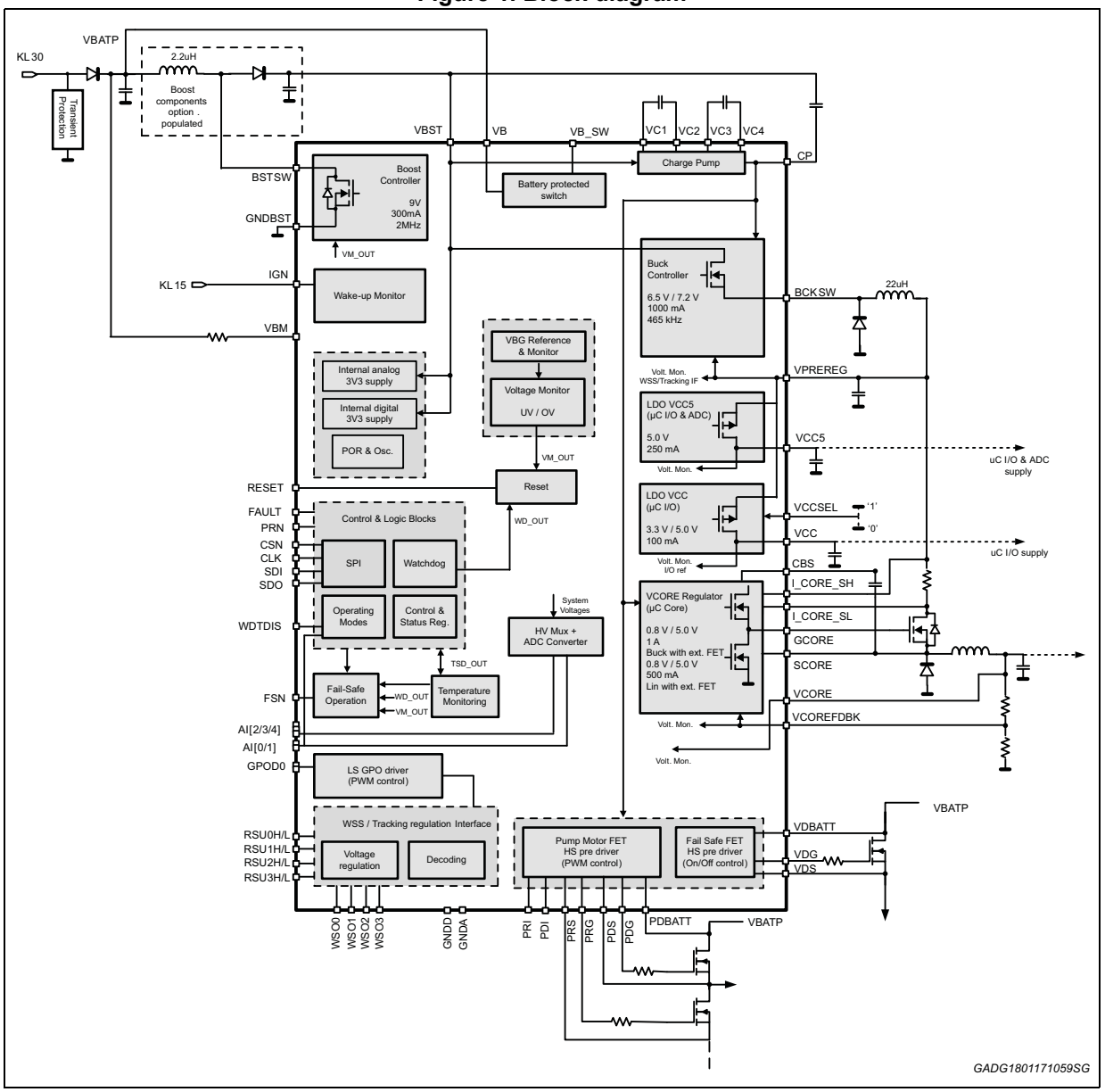
In addition, the L9396 provides enhanced system standby functionalities.

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2 Overall description

2.1 Block diagram

Figure 1. Block diagram



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2.2 Pins description

Figure 2. Pins connection diagram (top view)

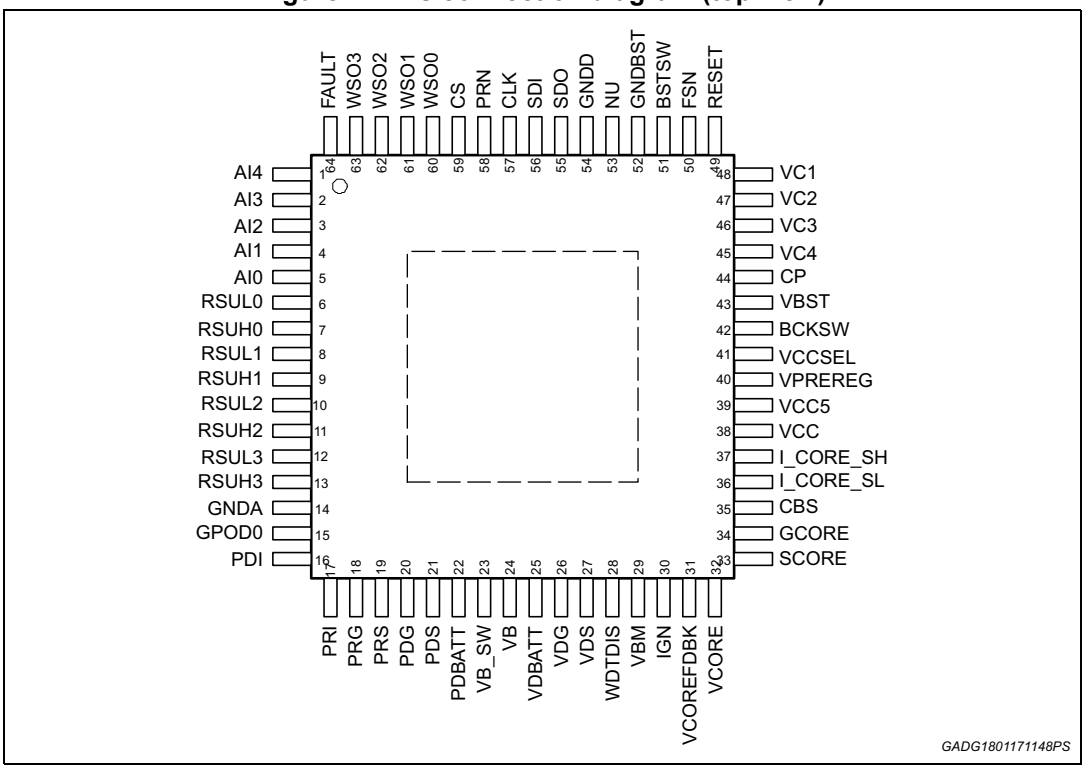


Table 2. Pins description

Pin	Name	Description	Pin type	
1	AI4	Analog input to ADC converter	I	Local
2	AI3	Analog input to ADC converter	I	Local
3	AI2	Analog input to ADC converter	I	Local
4	AI1	Input 1 to select VCORE function	I	Local
5	AI0	Input 0 to select VCORE function	I	Local
6	RSUL0	WSS ground return	I/O	Global
7	RSUH0	WSS / tracking regulated output	I/O	Global
8	RSUL1	WSS ground return	I/O	Global
9	RSUH1	WSS / tracking regulated output	I/O	Global
10	RSUL2	WSS ground return	I/O	Global
11	RSUH2	WSS output	I/O	Global
12	RSUL3	WSS ground return	I/O	Global
13	RSUH3	WSS output	I/O	Global
14	GNDA	Analog ground	Supply	Local
15	GPOD0	GPO driver drain terminal	I/O	Global

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Table 2. Pins description (continued)

Pin	Name	Description	Pin type	
16	PDI	Motor Pump HS FET control pin	I	Local
17	PRI	Motor Pump recirculation FET control pin	I	Local
18	PRG	Motor Pump recirculation FET gate control	O	Local
19	PRS	Motor Pump recirculation FET source pin	I	Local
20	PDG	Motor Pump HS FET gate control	O	Local
21	PDS	Motor Pump HS FET source pin	I	Local
22	PDBATT	Battery sense for Motor Pump FET pre-driver	I	Global
23	VB_SW	Battery protected output	I/O	Local
24	VB	Battery line input	Supply	Global
25	VDBATT	Battery sense for Fail Safe FET pre-driver	I	Global
26	VDG	Fail Safe FET gate control	O	Local
27	VDS	Fail Safe FET source pin	I	Local
28	WDTDIS	Watchdog disable	I	Local
29	VBM	Battery sense	I	Local
30	IGN	Wake up pin for battery connection	I	Global
31	VCOREFDBK	VCORE voltage feedback	I	Local
32	VCORE	µC core voltage supply	I	Local
33	SCORE	Source pin for VCORE regulator external FET	I/O	Local
34	GCORE	Gate control for VCORE regulator external FET	I/O	Local
35	CBS	VCORE bootstrap capacitor	I/O	Local
36	I_CORE_SL	Shunt input for current sensing on VCORE regulator	I	Local
37	I_CORE_SH	Shunt input for current sensing on VCORE regulator	I	Local
38	VCC	3.3 V / 5 V µC I/O supply	Supply	Local
39	VCC5	5 V µC I/O and ADC supply	O	Local
40	VPREREG	Pre-regulator output	Supply	Local
41	VCCSEL	Voltage selection for VCC regulator	I	Local
42	BCKSW	Switched pre-regulator output	I/O	Local
43	VBST	Device battery line input or boost regulated output	Supply	Global
44	CP	Charge pump output	Supply	Local
45	VC4	Charge pump 2nd cap high terminal	I/O	Local
46	VC3	Charge pump 2nd cap low terminal	I/O	Local
47	VC2	Charge pump 1st cap high terminal	I/O	Local
48	VC1	Charge pump 1st cap low terminal	I/O	Local
49	RESET	Reset output pin	O	Local
50	FSN	Fail safe negated digital output	O	Local

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Table 2. Pins description (continued)

Pin	Name	Description	Pin type	
51	BSTSW	Switched boost regulator output	I/O	Local
52	GNDBST	Boost regulator ground	Supply	Local
53	NU	Not used. To be connected to ground voltage.	I	Local
54	GNDD	Digital Ground	Supply	Local
55	SDO	SPI data digital output	O	Local
56	SDI	SPI data digital input	I	Local
57	CLK	SPI clock	I	Local
58	PRN	MCU clock signal	I/O	Local
59	CS	Chip select digital input	I	Local
60	WSO0	WSS pass-through output	O	Local
61	WSO1	WSS pass-through output	O	Local
62	WSO2	WSS pass-through output	O	Local
63	WSO3	WSS pass-through output	O	Local
64	FAULT	General fault output	O	Local

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2.3 Absolute maximum ratings

Within the maximum ratings, no damage to the component shall occur. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

All maximum ratings can occur at the same time.

All analog and digital voltages are related to the potential at substrate ground GNDA.

Table 3. Pin absolute maximum ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply						
ABS_VB	-	-	-0.3	-	40	V
ABS_VBST	-	-	-0.3	-	40	V
ABS_VBM	-	-	-0.3	-	40	V
ABS_VB_SW	-	-	-18	-	40	V
ABS_BSTSW	-	-	-0.3	-	40	V
ABS_VPREREG	-	-	-0.3	-	40	V
ABS_I_CORE_SH	-	-	-0.3	-	40	V
ABS_I_CORE_SL	-	-	-0.3	-	40	V
ABS_BCKSW	-	-	-1	-	40	V
ABS_SCORE	-	-	-1	-	40	V
ABS_VC4	-	-	VBST-0.6	-	VBST+13 ≤ 51	V
ABS_VC2	-	-	VBST-0.3	-	VBST+13 ≤ 51	V
ABS_CP	-	-	VBST-0.3	-	VBST+13 ≤ 51	V
ABS_VC1	-	-	-0.3	-	40	V
ABS_VC3	-	-	-0.3	-	40	V
ABS_CBS	-	-	-0.3	-	SCORE+ 20≤40	V
ABS_GCORE	-	-	-0.3	-	SCORE+ 20≤40	V
ABS_NU	-	-	-0.3	-	4.6	V
ABS_VCC5	-	-	-0.3	-	40	V
ABS_VCC	-	-	-0.3	-	40	V
ABS_VCOREFDBK	-	-	-0.3	-	40	V
ABS_VCORE	-	-	-0.3	-	40	V
ABS_VCCSEL	-	-	-0.3	-	40	V
ABS_IGN	-	-	-0.3	-	40	V
ABS_GNDA	-	-	-0.3	-	0.3	V
ABS_GNDD	-	-	-0.3	-	0.3	V
ABS_GNDBST	-	-	-0.3	-	0.3	V

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Table 3. Pin absolute maximum ratings (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Interfaces						
ABS_VDBATT	-	-	-18	-	40	V
ABS_PDBATT	-	-	-18	-	40	V
ABS_VDG	-	IC in sleep mode (IGN low)	-0.3	-	VDS+12≤51	V
	-	IC in operative mode (IGN high)	-18	-	VDS+12≤51	V
ABS_PDG	-	IC in sleep mode (IGN low)	-0.3	-	PDS+12≤51	V
	-	IC in operative mode (IGN high)	-18	-	PDS+12≤51	V
ABS_PRG	-	IC in sleep mode (IGN low)	-0.3	-	PRS+12≤51	V
	-	IC in operative mode (IGN high)	-18	-	PRS+12≤51	V
ABS_VDS	-	IC in sleep mode (IGN low)	-0.3	-	40	V
	-	IC in operative mode (IGN high)	-18	-	40	V
ABS_PDS	-	IC in sleep mode (IGN low)	-0.3	-	40	V
	-	IC in operative mode (IGN high)	-18	-	40	V
ABS_PRS	-	IC in sleep mode (IGN low)	-0.3	-	40	V
	-	IC in operative mode (IGN high)	-18	-	40	V

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Table 3. Pin absolute maximum ratings (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ABS_WDTDIS	-	-	-0.3	-	7	V
ABS_AI0	-	-	-0.3	-	40	V
ABS_AI1	-	-	-0.3	-	40	V
ABS_AI2	-	-	-0.3	-	40	V
ABS_AI3	-	-	-0.3	-	40	V
ABS_AI4	-	-	-0.3	-	40	V
ABS_FSN	-	-	-0.3	-	40	V
ABS_FAULT	-	-	-0.3	-	40	V
ABS_PRN	-	-	-0.3	-	40	V
ABS_RESET	-	-	-0.3	-	40	V
ABS_WSO0	-	-	-0.3	-	40	V
ABS_WSO1	-	-	-0.3	-	40	V
ABS_WSO2	-	-	-0.3	-	40	V
ABS_WSO3	-	-	-0.3	-	40	V
ABS_CS	-	-	-0.3	-	40	V
ABS_CLK	-	-	-0.3	-	40	V
ABS_SDI	-	-	-0.3	-	40	V
ABS_SDO	-	-	-0.3	-	40	V
ABS_PRI	-	-	-0.3	-	40	V
ABS_PDI	-	-	-0.3	-	40	V
ABS_GPOD0	-	-	-18	-	40	V
ABS_RSUH0	-	-	-18	-	40	V
ABS_RSUH1	-	-	-18	-	40	V
ABS_RSUH2	-	-	-18	-	40	V
ABS_RSUH3	-	-	-18	-	40	V
ABS_RSUL0	-	-	-18	-	40	V
ABS_RSUL1	-	-	-18	-	40	V
ABS_RSUL2	-	-	-18	-	40	V
ABS_RSUL3	-	-	-18	-	40	V
ESD requirements						
ESD according to the Human Body Model (HBM), Q100-002 for global pins; (100pF/1.5kΩ)	-	-	-	-	±4000	V
ESD according to the Human Body Model (HBM), Q100-002 for all other pins; (100pF/1,5kΩ)	-	-	-	-	±2000	V

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Table 3. Pin absolute maximum ratings (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ESD according to the Charged Device Model (CDM), Q100-011 Corner pins	-	-	-	-	±750	V
ESD according to the Charged Device Model (CDM), Q100-011 Non-corner pins	-	-	-	-	±500	V
Temperature requirements						
T_a	-	-	-40	-	135	°C
$T_{storage}$	-	-	-55	-	150	°C
T_j	-	-	-40	-	175	°C
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	With 2s2p PCB std Jedec. Natural convenction. Standard Jedec best JESD51-7	-	26	-	°C/W
$R_{th\ j\text{-}c}$	Thermal resistance junction to case	Bottom cold plate in contact with package bottom case (e-pad side). JESD51 best practice guidlines.	-	-	2.9	°C/W

2.4 Operating range

Within the operating ratings the part operates as specified and without parameter deviations. Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each specification table.

Table 4. Pin operating range

Pin name	Condition	Min	Max	Unit
Power supply				
VB, VBST, VBM	-	-0.1	19	V
VB_SW	-	-1	19	V
BSTSW, VPREREG, I_CORE_SH, I_CORE_SL	-	-0.1	19	V

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Table 4. Pin operating range (continued)

Pin name	Condition	Min	Max	Unit
BCKSW, SCORE	-	-1	19	V
VC4	-	VBST-0.6	VBST+10	V
VC2, CP	-	VBST-0.3	VBST+10	V
VC1, VC3	-	-0.1	19	V
CBS, GCORE	-	-0.1	SCORE+8	V
VCC5, VCC, VCOREFDBK, VCORE	-	-0.1	5.5	V
VCCSEL, IGN	-	-0.1	19	V
GNDA, GNDD, GNDBST, NU	-	-0.1	0.1	V
Interfaces				
VDBATT, PDBATT	-	-0.1	19	V
VDG	IC in sleep mode (IGN low)	-0.3	VDS+10	V
	IC in operative mode (IGN high)	-7	VDS+10	V
PDG	IC in sleep mode (IGN low)	-0.3	PDS+10	V
	IC in operative mode (IGN high)	-7	PDS+10	V
PRG	IC in sleep mode (IGN low)	-0.3	PRS+10	V
	IC in operative mode (IGN high)	-7	PRS+10	V
VDS, PDS, PRS	IC in sleep mode (IGN low)	-0.3	19	V
	IC in operative mode (IGN high)	-7	19	V
WDTDIS	-	-0.1	5.5	V
AI[0..4]	-	-0.1	19	V
FSN, FAULT, PRN, RESET, WSO[0..3]	-	-0.1	5.5	V
CS, CLK, SDI, SDO, PRI, PDI	-	-0.1	5.5	V
RSUH/L[0..3], GPOD0	-	-0.1	19	V

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3 Power supply

3.1 Battery range

The device operates on 12 V system. Transient operation for these systems can reach 40 V maximum. Particular care is to be taken in PCB manufacturing to keep thermal dissipation to a reasonable level.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C.

Table 5. Configuration and control DC specifications

Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
$VBATP_{NOV_OB}$	Normal Operating Voltage without boost	Design Info	6	13	19	V
$VBATP_{NOV_WB}$	Normal Operating Voltage with boost	Design Info	4.5 (6 to start-up)	-	19	V

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3.2 Boost regulator

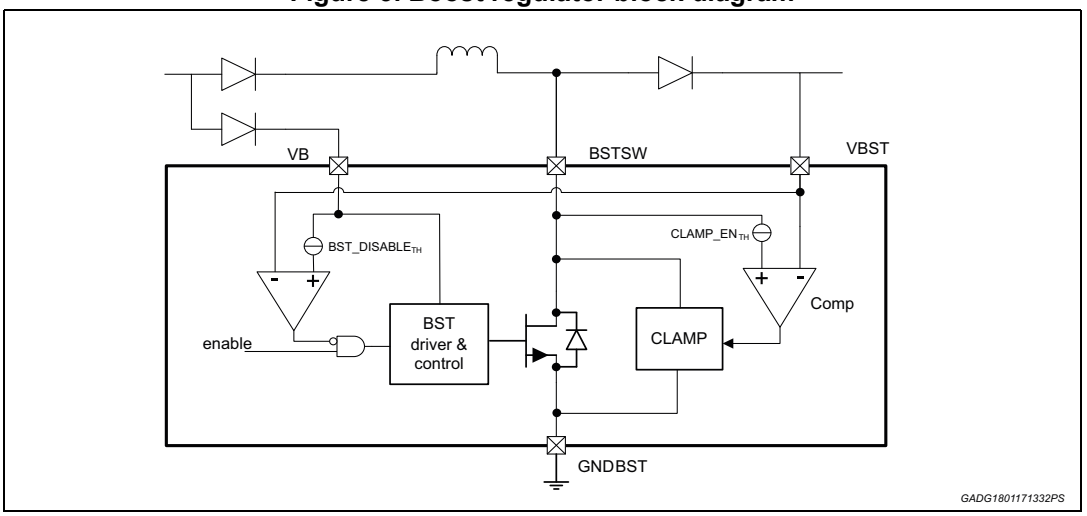
The boost regulator can be enabled or disabled via SPI depending on the needs of the application with respect to the operating battery level. It features an integrated power stage and operates at 2 MHz to allow the use of external low cost 2.2 µH inductor. The current capability should be enough to grant full I/O pin supply and minimal µC operation.

When not used, BSTSW pin can be connected to ground and VBST directly to the protected battery line. The device enables or keeps disabled the boost converter at start-up depending on the external circuitry: if BSTSW pin is shorted to ground, the boost is disabled at power up and kept disabled; in case the BSTSW experiences a high voltage at power up, given by battery connection through the inductor, the boost is enabled. This condition is reported via SPI with bit BOOST_KEPT_OFF of SUPPLY_CONTROL_2 register (it means that boost has been kept off and will not operate).

Boost converter diagnostics include under voltage, reported via SPI and FAULT pin (if the regulator is enabled). The integrated FET featuring the boost switch is protected against short to battery by means of a thermal shutdown circuit. When thermal fault is detected the FET is switched off and latched in this state until the related fault flag is read. In case of loss of ground the FET is switched off and automatically reactivated as soon as ground connection is restored. Over-voltage protection from load-dump and inductive flyback is provided via an active clamp and a disable circuitry. A dedicated circuitry is implemented to keep the boost off at start-up till the voltage difference between VB and VBST pins is lower than BST_DISABLETH in order to reduce in-rush current and diagnose VBST pin loss condition or diode loss. An SPI bit is present to report output of this comparator (bit BOOST_READY of SUPPLY_CONTROL_2 register goes high when VBST>=VB-BST_DISABLETH).

State of boost regulator is reported via SPI bit BOOST_ON_FLAG in register SUPPLY_CONTROL_2. In case boost is disabled due to diagnostic or battery voltage above output regulation voltage this bit is cleared to 0.

Figure 3. Boost regulator block diagram



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All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ T_j ≤ +175 °C; 4.5 V ≤ VBATP ≤ 19 V

Table 6. Boost regulator electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VBST_{NOV}$	Normal Operating Voltage at VBST	Design Info With boost, VBST is more than minimum boost output (> 6 V); Without boost, VBST is shorted to VBATP	6	13	19	V
$VBST_{UV_UP}$	VBST under voltage release threshold	VBST rising. VBST under-voltage release leads to charge pump switch on	6.5	-	7.1	V
$VBST_{UV_DN}$	VBST under voltage detection threshold	VBST falling. VBST under-voltage detection leads to charge pump shut down.	5.6	-	6	V
$t_{flt_VBST_UV}$	Under voltage filter time	-	-	12	-	µs
VBST	Boost Output Voltage	Across all line and load (steady state)	8.55	-	9.6	V
I_{O_BST}	Boost Output Current	Excluding current on analog and digital 3.3V	20	-	300	mA
dV_{SR_ac}	Line Transient Response	All line, load; dt = 100 µs	-8%	-	8%	%
dV_{LR_ac}	Load Transient Response	All line, load; dt = 100 µs	-8%	-	8%	%
L_{BST}	Output Inductance	2.2 µH nominal tolerance ±30% Design Information	1.6	-	2.8	µH
R_{LBST}	Output Inductance Impedance	Design Information	-	-	0.1	Ω
C_{BST}	Output Bulk Capacitance	Design Information	1.76	-	-	µF
R_{BST}	Bulk Capacitor ESR	Design Information	-	-	0.1	Ω
C_{BSTF}	Output Filter Capacitance	Min 100 nF nominal Design Information	80	-	-	nF
I_{OC}	Over Current Detection	-	1.2	-	2	A
R_{DSon}	Switch R_{DSon}	-	-	-	0.8	Ω

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Table 6. Boost regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BSTSW}	BSTSW Voltage Clamp	Active when not in load dump ($VB_{LOADDUMP}$)	30	-	36	V
$BST_DISABLE_{TH}$	Voltage difference between VB and VBST to deactivate the Boost regulator	VB – VBST	1.6	-	2.6	V
$CLAMP_EN_{TH}$	Voltage difference between BSTSW and VBST to activate the Boost CLAMP	BSTSW – VBST	1.5	-	4.5	V
f_{BSTSW}	Operating Frequency	-	-	f_{OSCINT}/8.5(1.88)	-	MHz
t_{BSTSW}	BSTSW Transition Time	VB = 4.5 V, I_{O_BST} = 300 mA	8	-	50	ns
T_{JSDBST}	Thermal Shutdown	-	175	-	200	°C
T_{HYS_TSDBST}	Thermal Shutdown hysteresis	-	5	-	15	°C
$I_{BSTSW_LO_OFF}$	BSTSW current consumption when BOOST is OFF	BSTSW - VBST<1.5V	3	-	20	µA
$I_{BSTSW_HI_OFF}$	BSTSW current consumption when BOOST is OFF	BSTSW – VBST>4.5V	30	-	70	µA
$V_{TH_BST_KEEP_OFF}$	Voltage threshold to deactivate the Boost regulator when not used	-	0.5	-	1	V

3.3 Internal supply

The internal analog and digital part is supplied by the supply voltage VBST through integrated voltage regulators. The generated voltage is monitored. In case of under/over-voltage, the device performs a power on reset (POR).

An undervoltage condition on VBST will lead to an internal reset of the IC. Above this undervoltage threshold, full functionality is granted.

The device integrates two separated instances of Bandgap voltage regulators; one of these bandgaps is used as voltage reference for the internal regulators, while the other one is used for monitoring the voltage levels.

GNDD ground line is protected against ground loss scenarios. In case GNDD line would be at least $GNDD_{OPEN}$ above the reference ground line GNDA, a POR is asserted.

GNDD is used for digital logic and charge pump while GNDA is used for analog blocks. GNDBST is used for boost regulator only.

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The device returns to normal operation with full functionality as soon as the POR is released.

Table 7. Internal supply electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$GNDD_{OPEN}$	GNDD threshold	GNDx = 0	180	300	420	mV
$T_{FLT_GNDD_OPEN}$	GNDD Open deglitch filter time	-	-	10	-	µs
$GNDBST_{OPEN}$	GNDBST threshold	GNDx=0	200	300	400	mV
$GNDBST_{PU}$	GNDBST pull-up current	Boost OFF	50	-	200	µA
$T_{FLT_GNDBST_OPEN}$	GNDBST Open deglitch filter time	-	7.5	-	11	µs
VDD	VDD Output Voltage	-	3.15	3.3	3.4	V
VDD_{OV}	VDD Over-voltage threshold	-	3.47	-	3.7	V
VDD_{UV}	VDD Under-voltage threshold	-	2.7	-	2.9	V
$T_{FLT_VDD_OV_UV}$	VDD Over-voltage / Under-voltage deglitch filter time	-	-	10	-	µs
VINTA	VINTA Output Voltage	-	3.2	3.3	3.4	V
$VINTA_{OV}$	VINTA Over-voltage threshold	-	3.47	-	3.7	V
$VINTA_{UV}$	VINTA Under-voltage threshold	-	2.95	-	3.13	V
$T_{FLT_VINTA_OV_UV}$	VINTA Over-voltage / Under-voltage deglitch filter time	-	-	10	-	µs

3.4 Wake-up input

The input pin IGN can be used as a wake up source connection. In case the voltage on IGN pin raises above $WAKE_{high_th}$ for an interval longer than $WAKE_{flt_up}$, the device wakes up. The device moves to sleep in case IGN falls below $WAKE_{high_th}$ - $WAKE_{hys}$ for an interval longer than $WAKE_{flt_down}$. This input can be connected to ignition battery switches or transceiver inhibit outputs. A filter time is implemented to reject spurious glitches. The filter time is started when the input signal exceeds the specified threshold.

The IGN signal must rise with a minimum slew rate of 0.1 V/µs.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; 4.5 V ≤ VBATP ≤ 19 V.

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Table 8. Wake-up input electrical characteristics

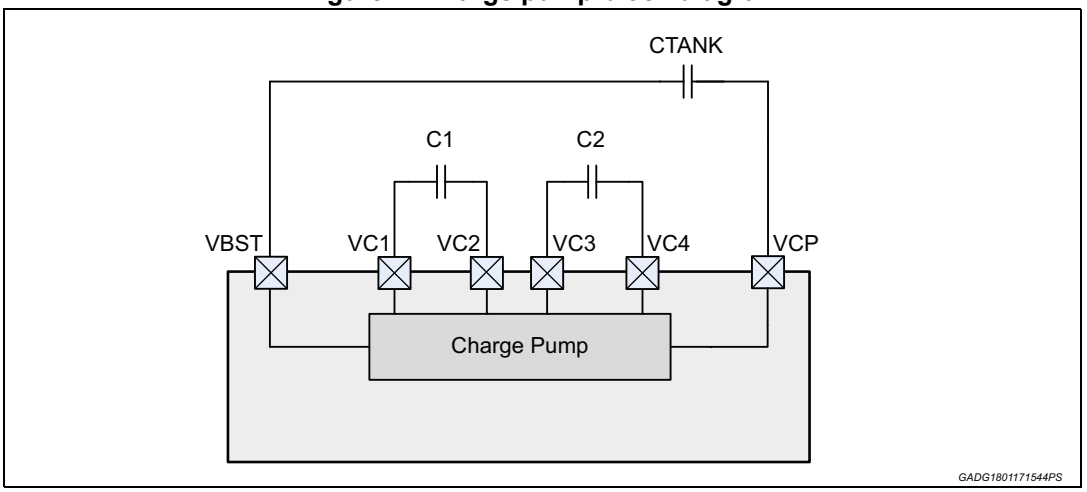
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VB_{stby_cur}	Battery standby current consumption	VBATP = 19 V Wake disable Sum of leakage currents from BSTSW, VBST, VB and VBM	-	-	30	µA
$WAKE_{high_th}$	Wake-up high voltage threshold	-	3.5	-	-	V
$WAKE_{low_th}$	Wake-up low voltage threshold	-	-	-	1.5	V
$WAKE_{hys}$	Wake-up voltage hysteresis	-	0.5	-	1.5	V
$WAKE_{pd}$	Wake-up pull down	IGN = 14 V	300	-	900	kΩ
$WAKE_{flt_up}$	Wake up ON deglitch	-	-	10	-	µs
$WAKE_{flt_down}$	Wake up OFF deglitch	-	-	10	-	µs
KA_period	Keep-alive period	-	-	200	-	ms
IGN_{slew_rate}	IGN rise time	-	0.1	-	-	V/µs

3.5 Charge pump

A two-stage charge pump is integrated to supply the high voltage circuit in the VPREREG and VCORE regulators and in the pump motor and fail safe pre-drivers.

The charge pump is supplied by the rail connected to VBST pin. External charging capacitors are used to achieve a high current capability.

Figure 4. Charge pump block diagram



It features a current limitation protection when either C1 or C2 is being charged up. The charge pump is protected against over temperature with dedicated thermal sensor. In standby mode the charge pump is disabled.

In case the CP output voltage remains too low for longer than tfCP the CP LOW bit is latched, which leads to shutdown of VPREREG, pump motor driver and fail safe driver. In turn, under voltage of VPREREG leads to shutdown of VCC, VCC5 and VCORE regulators.

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A second undervoltage threshold is present (V_{CPLOW2}) with a higher value. It can be used together with PDG turn-on threshold voltage to detect that low charge pump voltage is responsible for low PDG ON voltage.

Table 9. Charge pump electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CP_5V6}	Charge pump output voltage	VBST > 5.6 V Iload_ext = 8 mA	VBST+7.0	-	VBST+11	V
V_{CP_8V}	Charge pump output voltage	VBST >8V Iload_ext=10mA	VBST+8.9	-	VBST+11	V
V_{CP_8V55}	Charge pump output voltage	VBST >8.55V Iload_ext=1mA	VBST+9.1	-	VBST+11	V
I_{CP_5V6}	Charge pump output current	VBST>5.6V	-	-	8	mA
I_{CP_8V}	Charge pump output current	VBST>8V	-	-	10	mA
f_{CP}	Charge pump frequency	-	-	f_{OSCINT}/34(0.470)	-	MHz
V_{CPLOW}	Charge pump low voltage threshold	-	VBST+5.6	VBST+6	VBST+6.8	V
V_{CPLOW2}	Charge pump second low voltage threshold	-	VBST+7.85	VBST+8.35	VBST+8.85	V
t_{fCP}	Low voltage filter time	-	-	10	-	µs
C_{TANK}	Output capacitor	Design Info	-	220	-	nF
C_{CP1}, C_{CP2}	Switching capacitor	Design Info	-	68	-	nF
T_{JSDCP}	Thermal Shutdown	-	175	-	200	°C
T_{HYS_TSDCP}	Thermal Shutdown hysteresis	-	5	-	15	°C

3.6 VPREREG buck regulator

The integrated buck regulator provides a reduced voltage supply to the remaining regulators and to the WSS / tracking interface. Its default output level 6.5 V can be further increased to 7.2 V via register of BUCK VOLTAGE SELECTION in SPI.

This regulator is protected against short circuits and over temperature with dedicated thermal sensor, and an over/under voltage monitor is implemented. VPREREG itself is not shut down in case of over/under voltage at its output. VPREREG itself is not shut down in case of overcurrent, only in case of over temperature the regulator is switched off.

This regulator is not protected against diode loss and the IC may be irreparably damaged due to diode loss.

Under voltage of VPREREG (VPREREG_UV) leads to shutdown of VCC, VCC5 and VCORE regulators.

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Note: In particular corner conditions, the VPREREG output could be affected by transient overvoltage (clamped to VBST) once the Wake-up input is lowered. In these conditions the integrated high-side regulator FET is kept OFF through a passive switch OFF, that may lead the output to bounce. For this reason, it is not recommended the VPREREG to supply eventual external circuits, unless properly protected.

It is recommended to start the power-up sequence with a residual bias on VPREREG close to 0 V, as described in AN5702.

This can be achieved with a discharge resistor of 4.7 kOhm between VPREREG and GND.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; 6 ≤ VBST ≤ 19 V.

Table 10. VPREREG buck regulator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PREREG_H}	Output Voltage	VBST > 8.2 V	6.984	7.2	7.416	V
V_{PREREG_L}	Output Voltage	VBST > 7.5 V	6.305	6.5	6.695	V
V_{PREREG_UV}	Under voltage threshold	-	5.05	5.21	5.32	V
$t_{flt_VPREREG_UV}$	Under voltage filter time	-	-	12	-	µs
V_{PREREG_OV}	Over voltage threshold	-	$V_{PREREG_}$ x +5%	-	$V_{PREREG_}$ x +10%	V
$t_{flt_VPREREG_OV}$	Over voltage filter time	-	-	12	-	µs
$I_{VPREREG_HI}$	Output load current	SYS_CONFIG_1[9]=1	0.01	-	1	A
$I_{VPREREG_LO}$	Output load current	SYS_CONFIG_1[9]=0 (default)	0.01	-	0.5	A
$L_{VPREREG}$	Buck inductor	-	17.6	22	26.4	µH
$C_{VPREREG}$	Output capacitor	-	14.3	22	29.7	µF
dV_{SR_ac}	Line Transient Response	All line, load; dt = 10 µs VBST> V_{PREREG}(Typ)+3V	-8%	-	8%	%
dV_{LR_ac}	Load Transient Response	All line, load; dt = 10 µs VBST> V_{PREREG}(Typ)+3V	-8%	-	8%	%
$I_{OC_VPREREG_HI}$	High_Over current detection	SYS_CONFIG_1[9]=1	1.8	-	3	A
$I_{OC_VPREREG_LO}$	Low Over current detection	SYS_CONFIG_1[9]=0 (default)	0.9	-	1.6	A
-	High side t_{on}	-	-	-	40	ns
-	High side t_{off}	-	-	-	40	ns
$Fv_{preregsw}$	Operating Frequency	-	-	f_{OSCINT}/ 34 (0.470)	-	MHz

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Table 10. VPREREG buck regulator (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{DSon}	High side Rds_ON	T_j = 25 °C	-	-	0.4	Ω
		T_j = 175 °C	-	-	0.44	Ω
$t_{softstart}$	Softstart time	From 10% to 90% of nominal output voltage	130	-	390	µs
$T_{JSDVPRE}$	Thermal Shutdown	-	175	-	200	°C
$T_{HYS_TSDVPRE}$	Thermal Shutdown hysteresis	-	5	-	15	°C

The status of the VPREREG regulator can be read via SPI in SUPPLY_CONTROL_1 register.

The Buck overcurrent flag in the SUPPLY_CONTROL_1 register cannot be cleared after the fault condition is removed if the regulator load current remains above a defined threshold. After the fault is removed, the flag is expected to clear when read by the microcontroller. However, if the load current remains above 300 mA (low overcurrent threshold selected), the flag does not clear.

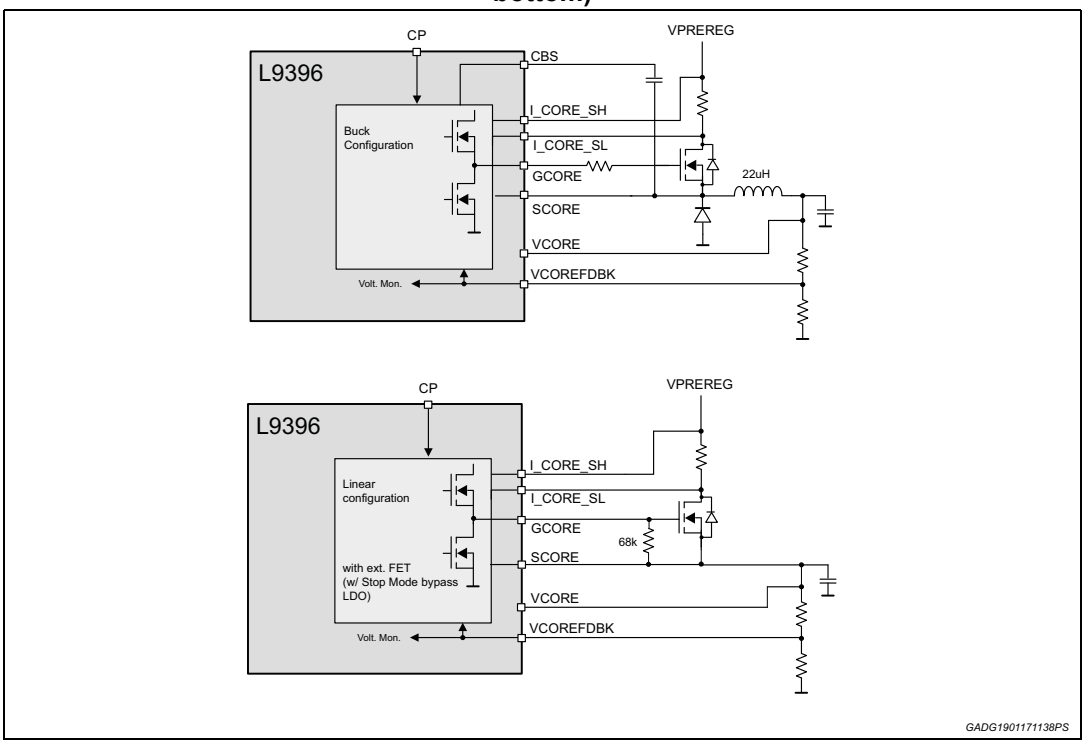
The flag behavior during fault detection is correct: it is asserted when an overcurrent fault is present and remains deasserted during normal operation.

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3.7 VCORE regulator

This regulator provides the supply to the µC core. The flexible approach with the external voltage divider allows the rail to be regulated from 0.8 V to 5 V. It can also be configured either as a buck controller or as a linear controller, driving an external FET in both cases.

Figure 5. VCORE configuration diagram (buck regulator - top, linear regulator - bottom)



Typically 2.2 Ω resistor has to be inserted between GCORE pin and gate of the external FET for buck configuration. For buck configuration, the source of the external FET should be connected to the SCORE pin, and the output tank capacitor should be connected to the VCORE pin. For linear configuration, the output tank capacitor should be connected with the source of the external FET and the SCORE pin, while VCORE pin should be either tied to ground or shorted to SCORE.

The operating mode (Linear, Buck) is selected when the regulator is enabled; mode recognition assumes that VCORE capacitance is fully discharged at each power-up. Some residual VCORE voltage, lower than 2.6 V, is allowed as reported in the relevant Application Note AN5702.

The mode selected for VCORE operation can be read via SPI in SUPPLY_CONTROL_1 register.

Note: When linear mode is selected for VCORE, in order to guarantee the right functionality it is recommended to tie VCORE to GND or eventually realize the short between SCORE and VCORE at device pin level, minimizing the parasitic path coming from the PCB routing.

The VCORE regulator has over and under voltage detections and the VCORE is not shut down in case of over or under voltage. It is also protected against short to ground by monitoring regulation loop for VCORE buck or over current for VCORE linear. When short to ground is detected and lasts more than the filter time of tflt_oc_vcore, the vcore is shut down

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and the restart is automatic in tflt_restart. No thermal protection is implemented for VCORE because the power MOS is external.

Both VPREREG and VCORE regulators could be disabled by connecting I_CORE_SH pin to ground. In this case, VPREREG pin should be connected to VBST pin.

Moreover two pins (AI0 and AI1) are used to configure additional features of VCORE regulator. It's possible to disable only VCORE regulator leaving VPREREG enabled. It's possible to change the monitor of regulated voltage (monitor on VCORE pin or monitor on VCOREFDBK pin). All the possibilities are listed in the following table.

Table 11. Vcore configuration

AI0	AI1	I_CORE_SH	VCORE state	VPREREG state	VCORE monitor
Low	Low	High	Enabled	Enabled	VCORE_UV_L, VCORE_OV_L
Low	High	High	Enabled	Enabled	VCORE_UV_H, VCORE_OV_H
High	Low	High	Enabled	Enabled	VCOREFDBK_UV, VCOREFDBK_OV
High	High	High	Disabled	Enabled	Disabled
Don’t care	Don’t care	Low	Disabled	Disabled	Disabled

The state of configuration pins (AI0, AI1 and I_CORE_SH) is latched at power up when VPREREG voltage exceeds the V_{PREREG}_UV threshold and stays latched until next POR event.

Microcontroller can monitor the voltage of AI0 and AI1 pins using embedded ADC converter and latched configuration is available via SPI bits.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; V_{PREREG}_L(Min) ≤ VPREREG ≤ V_{PREREG}_H(Max).

Table 12. VCORE regulator electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{SH_HI_CURR}$	Shunt resistor high current	-	99	100	101	mΩ
$R_{SH_LO_CURR}$	Shunt resistor low current	Only in linear mode	327	330	333	mΩ
VCORE FDBK_RES	Feedback resistor range	-	10	-	100	kΩ
VCOREFDBK_UV	Undervoltage threshold	Excluding external voltage divider accuracy	VCOREFDBK – 10%	-	VCOREFDBK – 5%	V
VCOREFDBK_OV	Overvoltage threshold	Excluding external voltage divider accuracy	VCOREFDBK + 5%	-	VCOREFDBK + 10%	V

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Table 12. VCORE regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCORE_UV_L	VCORE low Undervoltage threshold	-	2.97	-	3.135	V
VCORE_OV_L	VCORE low Overvoltage threshold	-	3.465	-	3.63	V
VCORE_UV_H	VCORE high Undervoltage threshold	-	4.5	-	4.75	V
VCORE_OV_H	VCORE high Overvoltage threshold	-	5.25	-	5.5	V
$t_{flt_VCORE_VCOREFDBK_UVOV}$	Under/overvoltage filter time	-	-	12	-	µs
VICORESH_IH	I_CORE_SH input high voltage	-	1.75	-	-	V
VICORESH_IL	I_CORE_SH input low voltage	-	-	-	0.75	V
VICORESH_Ihys	I_CORE_SH input hysteresis	-	100	-	1000	mV
Ipd_ICORESH_L	I_CORE_SH input Pull down current	VCORE linear mode, I_CORE_SH=3.3V	5	-	20	µA
Ipd_ICORESH_B	I_CORE_SH input Pull down current	VCORE buck mode, I_CORE_SH=3.3V	100	-	300	µA
V_AI0_IH	AI0 input high voltage	-	1.75	-	-	V
V_AI0_IL	AI0 input low voltage	-	-	-	0.75	V
V_AI0_Ihys	AI0 input hysteresis	-	100	-	1000	mV
Ipd_AI0	AI0 input Pull down current	AI0=3.3V	10	-	100	µA
V_AI1_IH	AI1 input high voltage	-	1.75	-	-	V
V_AI1_IL	AI1 input low voltage	-	-	-	0.75	V
V_AI1_Ihys	AI1 input hysteresis	-	100	-	1000	mV
Ipd_AI1	AI1 input Pull down current	AI1 = 3.3 V	10	-	100	µA
$t_{softstart}$	Softstart time	From 10% to 90% of nominal output voltage	240	-	720	µs

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Table 12. VCORE regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Buck configuration						
VCORE	Output voltage	Nominal 0.8V to 5V Excluding external voltage divider accuracy	0.776	-	5.15	V
I_{VCORE}	Output load current	$R_{SH_HI_CURR}$	0.01	-	1	A
C_{VCORE}	Output capacitor	VCORE > 1.2 V	-35%	22	+35%	µF
C_{VCORE}	Output capacitor	VCORE ≤ 1.2V	-35%	47	+35%	µF
L_{VCORE}	Buck inductor	VCORE > 1.2 V	-20%	22	+20%	µH
L_{VCORE}	Buck inductor	VCORE ≤ 1.2 V	-20%	12	+20%	µH
R_{LVCORE}	Buck inductor resistance	-	-	-	105	mΩ
C_{FET}	External FET gate charge	-	-	-	30	nC
C_{BS}	Bootstrap capacitor	-	-	100	-	nF
VCOREFDBK	Feedback voltage	Excluding external voltage divider accuracy	0.8 -3%	-	0.8 +3%	V
dV_{SR_ac}	Line Transient Response	All line, load; dt = 10 µs	-8%	-	8%	%
dV_{LR_ac}	Load Transient Response	All line, load; dt = 10 µs	-8%	-	8%	%
VCORE ripple	Ripple voltage	-	-20	-	+20	mV
$I_{OC_VCORE_BUCK}$	Over current detection	$R_{SH_HI_CURR}$	1.6	-	2.6	A
Rdson_hs	High side on resistance	-	-	-	28	Ω
Rdson_ls	Low side on resistance	-	-	-	8.3	Ω
tflt_oc_vcore	Shut down filter time for short to ground	Filter time starts to count from when current in power MOS is more than I_{O_LIM}	85	100	115	µs
tflt_restart	restart filter time for short to ground	Filter time starts to count from when core buck is disabled	1.7	2	2.3	ms
Sw_fr	Switching frequency	-	-	f_{OSCINT} /34 (0.470)	-	MHz

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Table 12. VCORE regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR	Power supply rejection ratio	VPREREG = 6.5 V, V_{noise} = 1 Vpp f_{noise} = 20 kHz, C_{VCORE} = 22 µF L_{VCORE} = 22 µH	40	-	-	dB
Linear configuration						
VCORE	Output voltage	Nominal 0.8 V to 5 V Excluding external voltage divider accuracy	0.78	-	5.125	V
I_{VCORE_HI}	Output load current high	$R_{SH_HI_CURR}$	0.07	-	0.75	A
I_{VCORE_LO}	Output load current low	$R_{SH_LO_CURR}$	0.07	-	0.25	A
C_{VCORE}	Output capacitor	-	5	-	40	µF
R_{CVCORE}	Output capacitor ESR	-	0.01	-	0.1	Ω
C_{VCORE_EMI}	Drain output stability capacitor	-	0.1	-	-	µF
C_{FET}	External FET gate charge	-	-	-	50	nC
VCOREFDBK	Feedback voltage	Excluding external voltage divider accuracy	0.8 -2.5%	-	0.8 + 2.5%	V
dV_{SR_ac}	Line Transient Response	All line, load; dt = 10 µs	-5%	-	5%	%
dV_{LR_ac}	Load Transient Response	All line, load; dt = 10 µs	-5%	-	5%	%
GCORE_pd	Gate internal pull down	Not tested, guaranteed by design.	100	-	-	kΩ
GCORE_Vclamp	Gate voltage clamp	-	8	-	12	V
I_{COREL_HI} Ilim	High Current limitation	-	0.8	-	1.6	A
I_{COREL_HI}_OC	High Overcurrent threshold	-	0.8	-	1.6	A
I_{COREL_LO} Ilim	Low Current limitation	-	0.26	-	0.48	A
I_{COREL_LO}_OC	Low Overcurrent threshold	-	0.26	-	0.48	A

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Table 12. VCORE regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tflt_oc_vcore	Shut down filter time for short to ground	Filter time starts to count from when current in power MOS is more than I_{COREL} Ilimx	85	100	115	µs
tflt_restart	restart filter time for short to ground	Filter time starts to count from when core buck is disabled	1.7	2	2.3	ms
PSRR	Power supply rejection ratio	VPREREG = 6.5V, V_{noise} = 1Vpp f_{noise} = 20 kHz, C_{VCORE} = 22µF L_{VCORE} = 22µH	40	-	-	dB

3.8 VCC5 regulator

This regulator provides a fixed 5V rail to supply µC I/Os and ADC. The VCC5 regulator has over and under voltage detections and is also protected against short circuits and over temperature with shared thermal sensor with VCC regulator.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; V_{PREREG}_L(Min) ≤ VPREREG ≤ V_{PREREG}_H(Max).

Table 13. VCC5 regulator electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC5	Regulated output voltage	0mA ≤ I_{VCC5} ≤ 250mA	4.88	5	5.12	V
VCC5_UV	Undervoltage threshold	-	VCC5 - 10%	-	VCC5 - 5%	V
VCC5_OV	Overvoltage threshold	-	VCC5 + 5%	-	VCC5 + 10%	V
$t_{flt_VCC5_UVOV}$	Under/overvoltage filter time	-	-	12	-	µs
I_{VCC5}	Output load current	-	0	-	250	mA
C_{VCC5}	Output capacitor	-	2.2	4.7	20	µF
C_{VCC5} ESR	Output capacitor ESR	-	0.01	-	0.1	Ω
dV_{SR_ac}	Line Transient Response	All line, load; dt = 10 µs	-5%	-	5%	%
dV_{LR_ac}	Load Transient Response	All line, load; dt = 10 µs	-5%	-	5%	%
R_{DSon}	High side Rds_ON	-	-	-	4	Ω
VCC5_cur lim	Current limitation	-	300	-	600	mA

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Table 13. VCC5 regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC5_oc	Overcurrent threshold	-	300	-	600	mA
VCC5_ilim_oc_delta	Delta_Ilim_Oc	VCC5_cur_lim – VCC5_oc	0.1	-	100	mA
$t_{softstart}$	Softstart time	From 10% to 90% of nominal output voltage	345	-	1035	µs
$T_{JSDVCCx}$	Thermal Shutdown	-	175	-	200	°C
$T_{HYS_TSDVCCx}$	Thermal Shutdown hysteresis	-	5	-	15	°C

3.9 VCC regulator

This regulator provides a dedicated rail to supply µC I/Os. It can be configured via VCCSEL pin to output either 3.3 V or 5 V. The VCC regulator has over and under voltage detections and is also protected against short to ground and over temperature with shared thermal sensor with VCC5.

The state of VCCSEL pin is latched at power up when VPREREG voltage exceeds the VPREREG_UV threshold and stays latched until next POR event.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; V_{PREREG}_L(Min) ≤ VPREREG ≤ V_{PREREG}_H(Max).

Table 14. VCC regulator electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC_L	Regulated output voltage	0mA ≤ I_{VCC} ≤ 100mA; VCCSEL = ‘0’	3.220	3.3	3.380	V
VCC_H	Regulated output voltage	VPREREG ≥ 6V, 0mA ≤ I_{VCC} ≤ 100mA; VCCSEL = ‘1’	4.88	5	5.12	V
VCCSEL_IH	VCCSEL input high voltage	-	1.75	-	-	V
VCCSEL_IL	VCCSEL input low voltage	-	-	-	0.75	V
VCCSEL_Ihys	VCCSEL input hysteresis	-	100	-	1000	mV
Ipd_VCCSEL	VCCSEL input Pull down current	VCCSEL=3.3V	1	-	10	µA
VCC_UV	Undervoltage threshold	-	VCC_x - 10%	-	VCC_x - 5%	V
VCC_OV	Overvoltage threshold	-	VCC_x + 5%	-	VCC_x + 10%	V
$t_{flt_VCC_UVOV}$	Under/overvoltage filter time	-	-	12	-	µs

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Table 14. VCC regulator electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VCC}	Output load current	-	0	-	100	mA
C_{VCC}	Output capacitor	-	2.2	4.7	20	µF
C_{VCC} ESR	Output capacitor ESR	-	0.01	-	0.1	Ω
dV_{SR_ac}	Line transient response	All line, load; dt = 10 µs	-5%	-	5%	%
dV_{LR_ac}	Load transient response	All line, load; dt = 10 µs	-5%	-	5%	%
R_{DSon}	High side Rds_ON	-	-	-	12	Ω
VCC_cur lim	Current limitation	-	125	-	240	mA
VCC_oc	Overcurrent threshold	-	125	-	240	mA
VCC_ilim_oc_delta	Delta_Ilim_Oc	VCC_cur_lim – VCC_oc	0.1	-	100	mA
$t_{softstart}$	Softstart time	From 10% to 90% of nominal output voltage	345	-	1035	µs

3.10 Protected battery switch

The device provides a fully protected switched battery output VB_SW, always active when the device is not in stand-by mode and WD1 is correctly served. This functionality can be used as further battery supply, e.g. for external sensors requiring battery level, or as a pull-up voltage rail.

The output can be disabled through SPI. Should the VB_SW diagnostics detect an over current condition, the output is turned off and the over current SPI fault is set. Once an over-current condition is detected, the output can only be re-enabled through SPI command, when the fault disappears, writing the bit PROTECTED BATTERY SWITCH COMMAND at 1 after the related OVER CURRENT flag is cleared on read.

All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; 4.5 ≤ VB = VBATP ≤ 19 V.

Table 15. Protected battery switch electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
-	Saturation voltage	VB – VB_SW @ max. current	-	-	0.5	V
-	Operating current	-	-	-	150	mA
VB_SW_oc	Overcurrent shutdown	-	165	-	250	mA
VB_SW _cur lim	Current limitation	-	165	-	250	mA
VB_SW _ilim_oc_delta	Delta_Ilim_Oc	VB_SW_cur_lim – VB_SW_oc	0.1	-	20	mA

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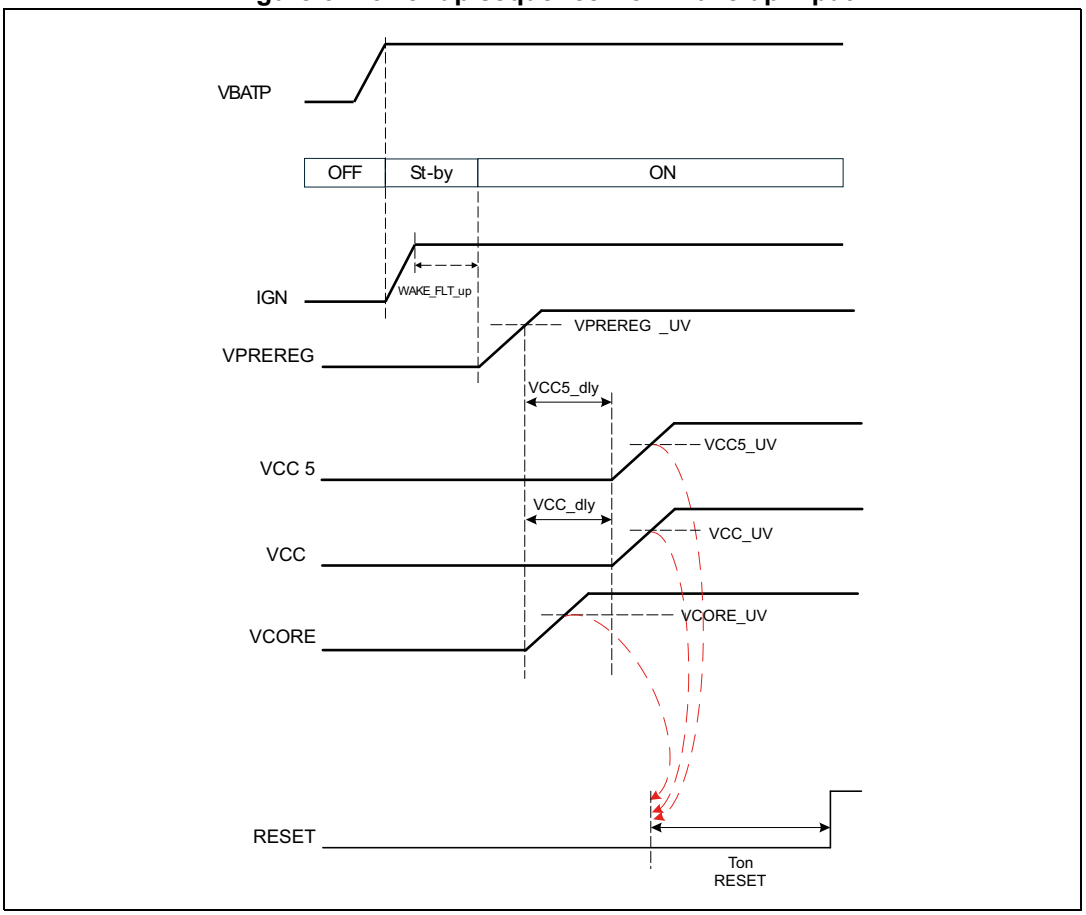
Table 15. Protected battery switch electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
-	Shutdown delay time	-	90	-	110	µs
Ileak	Off state leakage current	VB_SW off	-1	-	1	µA

3.11 Power up and power down sequences

Wake-up signal turns on the device and initiates the regulator power up sequence as in the figure below.

Figure 6. Power up sequence from wake up input



At power-up, the IGN signal must rise only after the battery voltage has reached its final value. Therefore, the IGN pin cannot be tied directly to the battery pin and moved together. In addition, the IGN signal must ramp up with a minimum slew rate of 0.1 V/µs.

All unused regulators should be turned-off whenever possible. If disabling them is not feasible, a minimum load, typically around 1 mA, should be applied.

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The device provides three different possibilities to stay in ON state:

- a persistent high signal on IGN pin,
- the setting of the POWERHOLD bit through SPI,
- the refreshing of the KEEPALIVE bit through SPI within a specified time frame.

At each transition H->L on the wake-up pin the device enters the keep-alive mode for one keep-alive period (KA_period).
If the device receives an SPI command to set the POWERHOLD bit within the first keep-alive period the device remains awake. Similarly, if the device receives an SPI command to refresh the KEEPALIVE bit within the first keep-alive period the device remains awake. Once the KEEPALIVE bit is refreshed a new KA_period starts and so forth. To stay on the keep-alive bit should be refreshed at each KA_period.
Should the KA_period elapse without any of the above 3 conditions, the device exits the keep-alive mode and enters in power down.
The power down sequence depends on the keep alive choice being done.
A new power up sequence should start only with a residual bias on VPREREG close to 0 V.

In the following figure, the power down sequence related to a H->L transition on the wake-up input pin without SPI conditioning is shown.

Figure 7. Power down sequence from wake up input

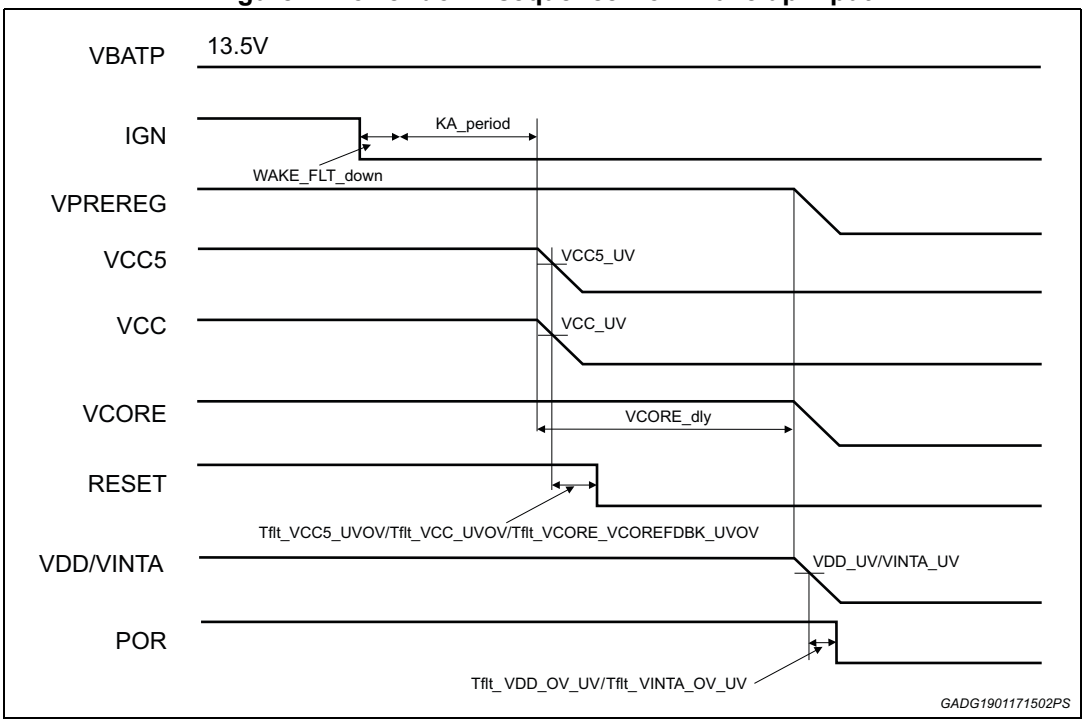


Table 16. Power up and power down

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC5_dly	VCC5 delay at power-up	From VPREREG_UV to VCC5 start	-	200	-	µs
VCC_dly	VCC delay at power-up	From VPREREG_UV to VCC start	-	200	-	µs
VCORE_dly	VCORE delay at power-down	From end of KA_period to VCORE switch off	-	200	-	µs
Ton_RESET	RESET hold time	From regulators in range to RESET High	11	12	13	ms

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4 Pre-drivers

4.1 Fail safe pre-driver

The device integrates a pre-driver of an external FET for fail safe purposes. It can be used as a HS pre-driver in case the external FET is used as a switch. The device controls the fail safe pre-driver in On/Off via SPI. The function remains active while no internal voltage faults or watchdog faults are detected.

This pre-driver implements a monitor against over current thanks to the diagnostics on drain-source monitoring of the external FET (in case of overcurrent SPI bit 15 of DRV_CONTROL_1 register goes high). If charge pump level goes below the disable voltage, the pre-driver is turned off. When the level returns above the disable voltage, the pre-driver returns to normal operation.

Table 17. Fail Safe pre-driver electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDG_ON	VDG On voltage	(VDG-VDS)@-0.1mA	5.2	-	12	V
VDG_OFF	VDG Off voltage	(VDG-VDS)@0.1 mA	-	-	1	V
Rpd_VDG_VDS	Pull down resistor at VDG-VDS	-	130	-	270	kΩ
VDG_Isource	VDG current source	V(VDG)=V(VDS) V(CP)– V(VDG)=2V	0.2	1	2	mA
VDG_Isink	VDG current sink	V(VDG)-V(VDS)=1V	1	5	9	mA
QFS_turn-on_00	QFS turn-on threshold voltage	V(VDBATT) – V(VDS) VDS_TH='00'	0.25	-	0.75	V
QFS_turn-on_01	QFS turn-on threshold voltage	V(VDBATT) – V(VDS) VDS_TH='01'	0.75	-	1.25	V
QFS_turn-on_10	QFS turn-on threshold voltage	V(VDBATT) – V(VDS) VDS_TH='10'	1.25	-	1.8	V
QFS_turn-on_11	QFS turn-on threshold voltage	V(VDBATT) – V(VDS) VDS_TH='11'	1.75	-	2.4	V
IVDBATT_ds	VDBATT leakage current for drain-source monitor	FAIL SAFE DRIVER ENABLE=0	7	-	67	µA
t_{QFS_ON}	Filter time of QFS turn-on	guaranteed by scan	-	12	-	µs

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4.2 Pump motor pre-driver

The device can drive a pump motor through this pre-driver for external FETs. It provides pre-driver circuitry for the motor high-side FET and the motor recirculation FET.

The PDG gate drive signal is referenced to PDS, and the pre-driver pair shall be able to float below the logic ground voltage, while keeping full on/off control on the external FET. This is required to prevent the FET from being partially turned on in the case of a ground offset between ECU and motor ground, or in case of loss of ECU ground.

Similarly, the PRG gate drive signal shall be referenced to PRS, and the pre-driver pair shall be able to float below the logic ground voltage, while keeping full on/off control on the external recirculation FET.

The motor FET pre-drivers shall be controlled by logic level input pins PDI and PRI, with logical operation defined as:

Table 18. Logical operation definition

PDI	PRI	PDG	PRG	High-side FET	Recirculation FET
L	L	L	L	OFF	OFF
H	L	H	L	ON	OFF
L	H	L	H	OFF	ON
H	H	H	L	ON	OFF

The state of the PDI and PRI pins can be observed via SPI.

The device is able to generate software selectable dead time between PDG and PRG transitions, to prevent cross-conduction on the external FETs.

In order to enable either PDG or PRG the following conditions must be met:

- the watchdog reset must not be asserted,
- the Enable Motor FET Driver SPI bit must be set,
- no device faults preventing PDG or PRG operation must be present.

When disabled, PDG and PRG are driven to their low states.

4.3 Pump motor diagnostics

To enable MCU diagnostics, the device provides an internal pull-up current (IPDS) on PDS and the PDS voltage can be read by the ADC and available over SPI.

After PDG is turned on, the device monitors the rising differential voltage between PDG and PDS. If the differential voltage does not exceed the PDG turn-on voltage threshold within the PDG switching time, the device disables the PDG pre-driver and sets the PDG Turn-On Fault SPI bit. The device automatically re-enables the PDG pre-driver on the next rising PDI edge.

After PDG is turned off, the device monitors the falling differential voltage between PDG and PDS. If the differential voltage does not drop below the PDG turn-off voltage threshold within the PDG switching time, the device disables both the PDG and PRG pre-drivers, sets the PDG Turn-Off Fault SPI bit and clears the Enable Motor FET Driver SPI bit. The PDG and

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PRG pre-drivers remain disabled until the Enable Motor FET Driver SPI bit is re-set over SPI. The PDG Turn-On/off Fault SPI bits are latched until read.

In case the negative flyback voltage on PDS drops below the open flyback voltage threshold for longer than the open flyback debounce time after PDG is turned off, the device disables both the PDG and PRG pre-drivers, sets the Open Flyback Fault SPI bit and clears the Enable Motor FET Driver SPI bit. The PDG and PRG pre-drivers remain disabled until the Enable Motor FET Driver SPI bit is re-set over SPI. The Open Flyback Fault SPI bit is latched until read.

After PDG is turned on, the device monitors the falling differential voltage between PDBATT and PDS. If the differential voltage does not drop below the QPD turn-on voltage threshold within the QPD switching time, the device disables the PDG pre-driver and sets the QPD Turn-On Fault SPI bit. The device automatically re-enables the PDG pre-driver on the next rising PDI edge. The QPD Turn-On Fault SPI bit is latched until read.

After PDG is turned off, the device monitors the falling PDS voltage. If the voltage does not drop below the QPD turn-off voltage threshold within the QPD switching time, the device disables both the PDG and PRG pre-drivers, sets the QPD Turn-Off Fault SPI bit and clears the Enable Motor FET Driver SPI bit. The PDG and PRG pre-drivers remain disabled until the Enable Motor FET Driver SPI bit is re-set over SPI. The QPD Turn-Off Fault SPI bit is latched until read.

After PRG is turned on, the device monitors the rising differential voltage between PRG and PRS. If the differential voltage does not exceed the PRG turn-on voltage threshold within the PRG switching time, the device sets the PRG Turn-On Fault SPI bit. The device continues to drive the current limited PRG pin. The PRG Turn-On Fault SPI bit is latched until read.

After PRG is turned off, the device monitors the falling differential voltage between PRG and PRS. If the differential voltage does not drop below the PRG turn-off voltage threshold within the PRG switching time, the device disables both the PDG and PRG pre-drivers, sets the PRG Turn-Off Fault SPI bit and clears the Enable Motor FET Driver SPI bit. The PDG and PRG pre-drivers remain disabled until the Enable Motor FET Driver SPI bit is re-set over SPI. The PRG Turn-On Fault SPI bit is latched until read.

All the OFF diagnostic comparators (PDG_OFF, open flyback, QPD_OFF, PRG_OFF) are active during the entire OFF state until FETs are switched on. Output of comparators is masked when Enable Motor FET Driver SPI bit is high while is not masked when Enable bit is low and FETs are in off state. There is no masking of OFF diagnostic when there is transition of Enable Motor FET Driver SPI bit from low to high. Masking time is only applied during the transitions of FETs gate command.

In case of a device ground loss while the motor is enabled, the device disables both external FETs. These FETs remain disabled until the device returns to the active mode.

If battery level goes below the disable voltage, the pre-driver is turned off after the delay disable time has elapsed. When the level returns above the disable voltage, the pre-driver returns to normal operation.

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Table 19. Pump motor diagnostics electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PDG_ON_5V6	PDG On voltage	(V(PDG)-V(PDS))@-1mA@VBST>5.6V assuming PDBATT=VBST	6.8	-	12	V
PDG_ON_8V	PDG On voltage	(V(PDG)-V(PDS))@-10mA@VBST>8V assuming PDBATT=VBST	7.8	-	12	V
PDG_ON_8V55	PDG On voltage	(V(PDG)-V(PDS))@-1mA@VBST>8.55V assuming PDBATT=VBST	8.9	-	12	V
PDG_OFF	PDG Off voltage	(V(PDG)-V(PDS))@1mA	-	-	0.5	V
-	PDG turn-on threshold voltage	V(PDG) – V(PDS)	5.1	6	6.8	V
-	PDG turn-off threshold voltage	V(PDG) – V(PDS)	0.5	-	1	V
Rpd_PDG_PDS	Pull down resistor at PDG-PDS	-	130	-	270	kΩ
-	PDG switching time	guaranteed by scan	-	6	-	µs
-	PDG filter time	guaranteed by scan	-	3	-	µs
QPD_turn-on_00	QPD turn-on threshold voltage	V(PDBATT) – V(PDS) PUMP_VDS_TH='00'	0.25	-	0.75	V
QPD_turn-on_01	QPD turn-on threshold voltage	V(PDBATT) – V(PDS) PUMP_VDS_TH='01'	0.75	-	1.25	V
QPD_turn-on_10	QPD turn-on threshold voltage	V(PDBATT) – V(PDS) PUMP_VDS_TH='10'	1.25	-	1.8	V
QPD_turn-on_11	QPD turn-on threshold voltage	V(PDBATT) – V(PDS) PUMP_VDS_TH='11'	1.75	-	2.4	V
IPDBATT_ds	PDBATT leakage current for drain-source monitor	PUMP MOTOR PRE DRIVER ENABLE=0	7	-	67	µA
QPD_turn-off_th	QPD turn-off threshold voltage	V(PDBATT) – V(PDS)	-	QPD_turn-on_th	-	V
-	QPD switching time	guaranteed by scan	-	6	-	µs

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Table 19. Pump motor diagnostics electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
-	QPD filter time	guaranteed by scan	-	3	-	µs
-	Open flyback threshold	-	-11	-	-7.5	V
-	Open flyback filter time	-	-	3	-	µs
PDG_Isource	PDG current source	V(PDG)=V(PDS) V(CP)-V(PDG) = 2 V	15	25	35	mA
PDG_Isink	PDG current sink	V(PDG) – V(PDS) = 1 V	15	25	35	mA
PRG_ON	PRG On voltage	(V(PRG)-V(PRS))@- 1 mA@VBST>5.6 V	6.8	-	12	V
PRG_OFF	PRG Off voltage	(V(PRG)-V(PRS))@1 mA	-	-	0.5	V
-	PRG turn-on threshold voltage	V(PRG)-V(PRS)	5.1	-	6.8	V
-	PRG turn-off threshold voltage	V(PRG)-V(PRS)	0.5	-	1	V
Rpd_PRG_PRS	Pull down resistor at PRG-PRS	-	130	-	270	kΩ
-	PRG switching time	guaranteed by scan	-	6	-	µs
-	PRG filter time	guaranteed by scan	-	3	-	µs
PRG_Isource	PRG current source	V(PRG)=V(PRS) V(CP)-V(PRG)=2V	15	25	35	mA
PRG_Isink	PRG current sink	V(PRG) – V(PRS)=1V	15	25	35	mA
-	PDI propagation delay	From PDI rising edge to PDG at turn-on threshold voltage	-	2	-	µs
-	PRI propagation delay	From PRI rising edge to PRG at turn-on threshold voltage	-	2	-	µs
PDI _IH	PDI input high voltage	-	1.75	-	-	V
PDI _IL	PDI input low voltage	-	-	-	0.75	V
PDI _Ihys	PDI input hysteresis	-	100	-	1000	mV
Ipd_PDI	PDI input Pull down current	PDI=3.3V	10	-	100	µA

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Table 19. Pump motor diagnostics electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PRI _IH	PRI input high voltage	-	1.75	-	-	V
PRI _IL	PRI input low voltage	-	-	-	0.75	V
PRI _Ihys	PRI input hysteresis	-	100	-	1000	mV
Ri_pd_PRI	PRI input Pull down current	PRI=3.3V	10	-	100	µA
-	Non overlap timing	Programmable in 24 steps	-	0.25	6	µs

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5 Remote sensor interface

The device contains 4 remote sensor interfaces, capable of supporting active wheel speed sensors or operating as an independent 2-channel tracking regulation supply.

The interface supply is internally connected to the VPREREG pin. The circuitry consists of a power interface delivering a dedicated output voltage on RSUHx pins. This output could be voltage regulated in case of operation as tracking supply (pins RSUH0 and RSUH1). When WSS operation is selected, the function mirrors the current flowing in the external sensor and transmits this current information to the decoder, which produces a digital value for each sensor channel. RSULx pins are used as ground returns from the sensors and current sense is carried out in low side.

Data are then output through SPI registers. Received signals can be processed to the corresponding discrete logic output pin WSO0-WSO3.

5.1 Active wheel speed sensor

The remote sensor interface circuit conditions and interprets active wheel speed sensor signals with various pulse widths and output currents. The following sensor types are supported and selected through SPI configuration:

- Standard active 2-level wheel speed sensors (7/14 mA);
- A three-level (7/14/28 mA) VDA compliant sensor with direction and air gap information ("Requirement Specification for Standardized Interface for Wheel Speed Sensor with Additional Information", Version 4.0);
- PWM encoded 2-level sensors with 2 edges per tooth (see data sheet Infineon IC TLE4942/BOSCH DF11);
- PWM encoded 2-level sensors with 1 edge per tooth (see data sheet Allegro ATS651LSH/BOSCH DF11).

Received wheel speed frames from all the above sensors are decoded into signals suitable for the microcontroller through SPI or the four WSOx output pins. For all sensors, other than the standard active 2- level sensor, additional sensor data (diagnostics, etc…) are decoded and available within SPI registers. The user may select to have all sensor data processed on WSOx pins through the microcontroller by selecting pass through mode. In pass through mode, the remote sensor interface simply conditions the incoming sensor current pulses to digital pulses, no decoding is performed.

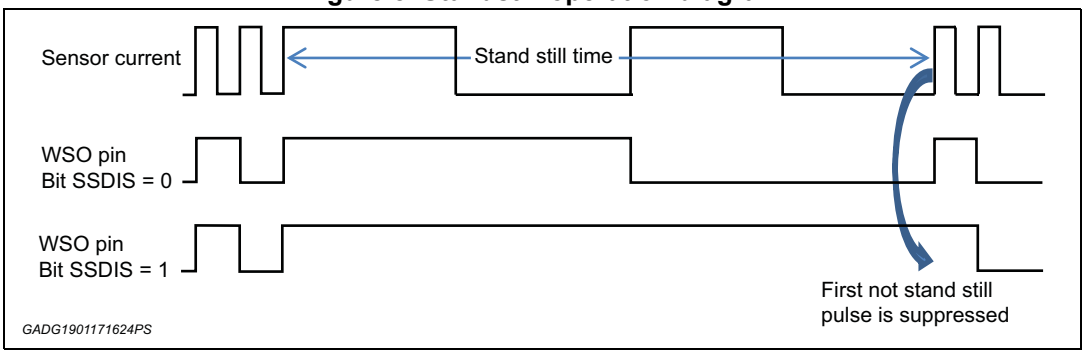
The sensor input filter time, deglitch filter, (delay until a threshold crossing is detected) can be configured (from 8 µs to 50 µs). Filters can be selected individually for each channel, through the RS_CFG_x_y registers, bits [9:6].

For PWM encoded sensors with 2 edges per tooth not in pass through mode, the standstill signal can be processed directly to the WSOx output pins. This is done in the RS_CFG_x_y registers, bit [4].

Since the decoder has to measure the pulses in order to determine whether they are stand-still pulses or not, the first standstill pulse will always be seen on the WSOx output pins and the first not stand-still pulse after a stand-still period will be suppressed.

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Figure 8. Standstill operation diagram



Data from the sensor are not latched: last incoming frame overwrites the previous one once validated. Faults coming from diagnostic (i.e. over current, short to ground or battery) are latched until the microcontroller reads them.

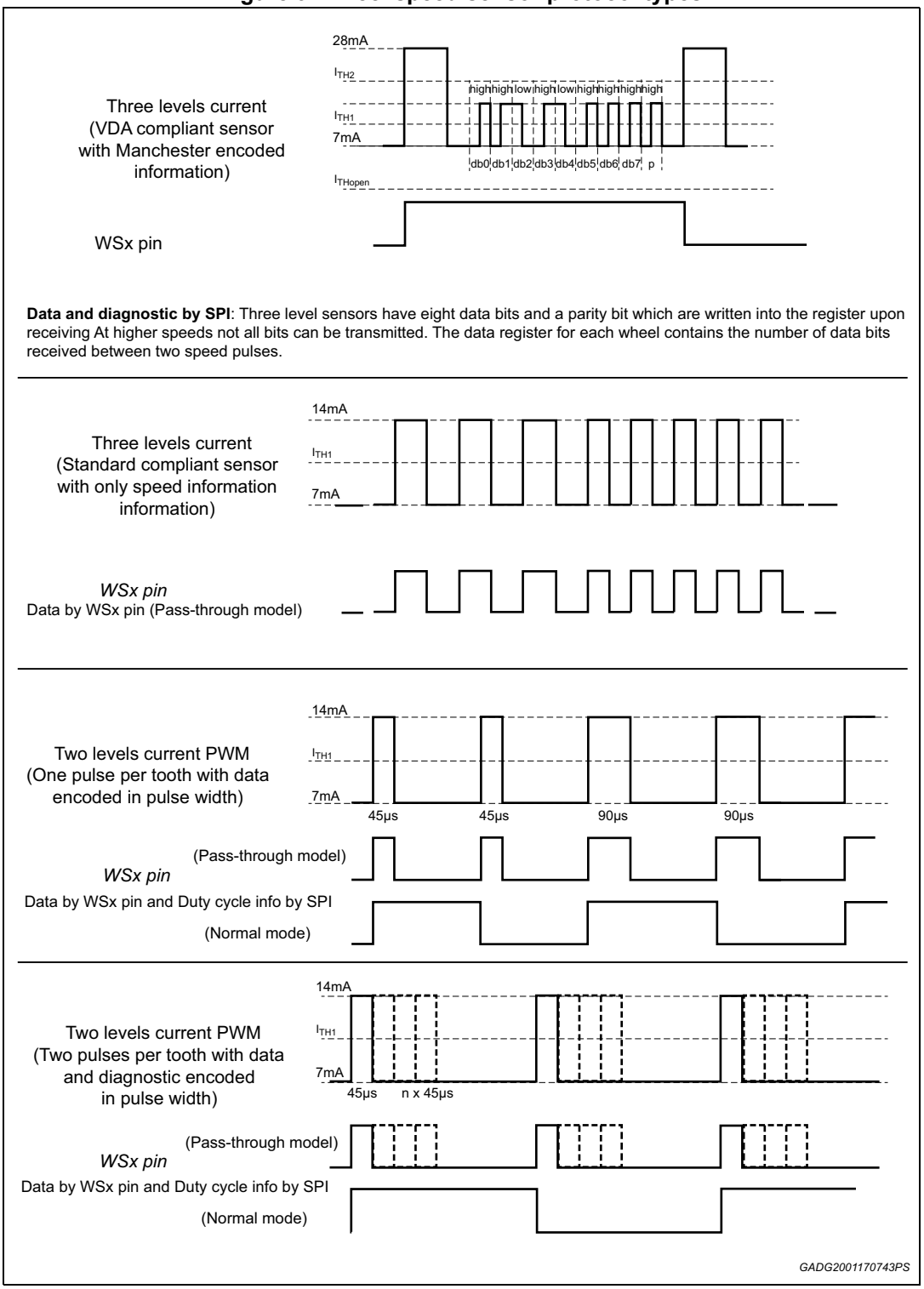
We have two different digital algorithms:

- Auto-adjusting current trip points. With this option, the IC is able to find sensor base current value (named IB0). Range of base current can be configured via SPI. The IC is also able to detect the current value of the data pulse and compute the first threshold (named Ith1): Ith1 = IB0 + (ΔIth1)/2 where ΔIth1 range is also configurable via SPI.

  Besides, in case of VDA selected, the IC is also able to recognize the current value of the speed pulse by computing a second threshold (named Ith2): Ith2 = IB0 + ΔIth1 + (ΔIth2)/2 where ΔIth2 range is configurable via SPI.
- Fixed current trip points where the thresholds are set by SPI. To avoid the risk of wrong settings (inverted thresholds, thresholds outside WSI limits and similar) only the first threshold can be directly programmed while, to determine the second one, an offset vs. the first threshold must be provided. Both values, threshold and offset, can be specified through an 8-bit word (range 0x00 → 0xFF). A fixed offset of 54 (0x36) is also added to determine the actual thresholds in order to prevent any potential wrong setting out or range. Complete formulas for threshold computation are the following:
  - First threshold (typ.) = 93.75 µA*(54 +WSI_FIRST_TH)
  - Second threshold rising edge (typ.) = 93.75 µA*(108+WSI_FIRST_TH+WSI_OFFS_TH)
  - Second threshold falling edge (typ.) = 93.75 µA*(108+WSI_FIRST_TH+WSI_OFFS_TH)*0.6865
  - WSI_FIRST_TH: SPI programmable from 0x00 to 0xFF (default = 0x33)
  - WSI_OFFS_TH: SPI programmable from 0x00 to 0xFF (default = 0x34)

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Figure 9. Wheel speed sensor protocol types



Data and diagnostic by SPI: Three level sensors have eight data bits and a parity bit which are written into the register upon receiving At higher speeds not all bits can be transmitted. The data register for each wheel contains the number of data bits received between two speed pulses.

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5.1.1 Wheel speed data register formats

In the wheel speed sensor interface four data registers are used (Remote Sensor Data Register RS_DATA_RSDR_0- RS_DATA_RSDR_3).

Independent data registers are defined for each wheel speed channel and their contents are determined by sensor type. Three-level VDA sensors have eight data bits and parity as shown in the table below. At fast speed not all bits may be transmitted by the sensor: the IC is able both to process normal or either truncated frames by providing together with data, a 4-bit counter to inform the microcontroller about the number of received valid bits.

For PWM encoded sensors, each pulse length is written to the sensor data register with a typical resolution of 5 µs per bit. In case of pulse width duration equal to or higher than 1.045 ms, the standstill condition will be recognized and bit 16 in the corresponding register will be set.

The register is updated when a PWM falling edge is detected; in case of stuck-at 1 of the PWM signal the register is updated when the counter reaches the overflow value (0x1FF): in this case the standstill bit not set and the counter in overflow will signal a fault to the microcontroller.

5.1.2 Testmode

In order to test the input structures of the connected microcontroller, the device features a wheel speed test mode that allows test patterns to be applied on the four wheel speed outputs WSOx. The test mode can be entered via SPI and the test patterns can also be controlled via SPI commands. Test patterns can be composed only of static high or low signals, which can be selected via SPI. For safety reasons only one channel at a time can be switched into test mode.

In order to enable testmode it is necessary to write to '1' bit DIAG (bit 4) of register RS_CTRL. After that the bits of WSS_TEST register select the channel under test and the state of output pin.

To exit this testmode it is not sufficient to clear to '0' the DIAG bit but, before that, also bits 8:2 of WSS_TEST register (Config range field) must be changed in order not to select any of the four available outputs.

5.1.3 Wheel Speed SPI Registers

WSI test

Table 20. WSS_TEST register

Addr	Name	Type	Bits = 9
0001111	WSS_TEST	RW	Config Range= 8:2, X:1, TestBit = 0;

WSS_TEST register stores Static Test configurator bit-field.

This register configures a static test for WSI interface. Test consists in transferring TestBit value on a selected (by Config range) WSI output.

TestBit: Test input value.

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Table 21. WSS_TEST register bit description

Data Field	Description	Reset value	Reset Event
Bit 8:2	Config range: selects one WSI output according to the following range: 1010011 => DOUT4 output; 1010101 => DOUT3 output; 1011001 => DOUT2 output; 1010110 => DOUT1 output; all others: test mode disabled	0	SSM_RESET LBIST
Bit 1	DON'T CARE	0	SSM_RESET LBIST
Bit 0	WSSTP: DOUTx Output Test Value 0 => Output for selected DOUTx set 'high' 1 => Output for selected DOUTx set 'low'	0	SSM_RESET LBIST

WSI configuration

Table 22. RS_CFG_0_1 register

ADDR	Name	Type	Bits = 20
0001100	RS_CFG_0_1	RW	Config1 Range ch1 = 19:10, Config0 Range ch0 = 9:0;

Any WSI interface is configured by a 10-bit field according to the following format.

Table 23. RS_CFG_0_1 register bit description

Data Field	Description	Reset value	Reset Event
Bit 19:16	WSFILT[3:0]: Wheel Speed filter time selection (500nsec per bit) If WSFILT_CONF=0: 0000 => 8 µs ----- => 500 ns per bit 1111 => 15.5 µs If WSFILT_CONF=1: => 30 µs, xx11 => 50 µs	0010	SSM_RESET LBIST
Bit 15	WSIPTEN: Pass Through mode enable (valid only for PWM encoded sensors) 0 => Off 1 => On	0	SSM_RESET LBIST

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Table 23. RS_CFG_0_1 register bit description (continued)

Data Field	Description	Reset value	Reset Event
Bit 14	SSDIS: DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor) 0 => DOUTx enabled during standstill 1 => DOUTx disabled during standstill	0	SSM_RESET LBIST
Bit 13	WSI_FIX_THRESH: WSI selection of fixed or auto adaptive thresholds 0 => auto adaptive thresholds 1 => fixed thresholds	0	SSM_RESET LBIST
Bit 12	WSFILT_CONF (see bits 16 to 19)	0	SSM_RESET LBIST
Bit 11:10	STS: Sensor Type Selection 00 => Two level, Standard 01 => Three level, VDA 10 => PWM Encoded, 2 level, 2 edges/tooth 11 => PWM Encoded, 2 level, 1 edge/tooth	0	SSM_RESET LBIST
Bit 9:6	WSFILT[3:0]: Wheel Speed filter time selection (500 ns per bit) If WSFILT_CONF=0: 0000 => 8 µs ----- => 500 ns per bit 1111 => 15.5 µs If WSFILT_CONF=1: xx00 => 8 µs, xx01 ≥15 µs, xx10 => 30 µs, xx11 ≥50 µs	0010	SSM_RESET LBIST
Bit 5	WSIPTEN: Pass Through mode enable (valid only for PWM encoded sensors) 0 => Off 1 => On	0	SSM_RESET LBIST
Bit 4	SSDIS: DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor) 0 => DOUTx enabled during standstill 1 => DOUTx disabled during standstill	0	SSM_RESET LBIST

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Table 23. RS_CFG_0_1 register bit description (continued)

Data Field	Description	Reset value	Reset Event
Bit 3	WSI_FIX_THRESH: WSI selection of fixed or auto adaptive thresholds 0 => auto adaptive thresholds 1 => fixed thresholds	0	SSM_RESET LBIST
Bit 2	WSFILT_CONF (see bits 6 to 9)	0	SSM_RESET LBIST
Bit 1:0	STS: Sensor Type Selection 00 => Two level, Standard 01 => Three level, VDA 10 => PWM Encoded, 2 level, 2 edges/tooth 11 => PWM Encoded, 2 level, 1 edge/tooth	0	SSM_RESET LBIST

Table 24. RS_CFG_2_3 register

ADDR	Name	Type	Bits = 20
0001101	RS_CFG_2_3	RW	Config3 Range ch3= 19:10, Config2 Range ch2 = 9:0;

Any WSI interface is configured by a 10-bit field according to the following format.

Table 25. RS_CFG_2_3 register bit description

Data Field	Description	Reset Value	Reset Event
Bit 19:16	WSFILT[3:0]: Wheel Speed filter time selection (500 ns per bit) If WSFILT_CONF=0: 0000 => 8 µs ----- => 500 ns per bit 1111 => 15.5 µs If WSFILT_CONF=1: xx00 => 8 µs, xx01 =>15 µs, xx10 => 30 µs, xx11 => 50 µs	0	SSM_RESET LBIST
Bit 15	WSIPTEN: Pass Through mode enable (valid only for PWM encoded sensors) 0 => Off 1 => On	0	SSM_RESET LBIST

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Table 25. RS_CFG_2_3 register bit description (continued)

Data Field	Description	Reset Value	Reset Event
Bit 14	SSDIS: DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor) 0 => DOUTx enabled during standstill 1 => DOUTx disabled during standstill	0	SSM_RESET LBIST
Bit 13	WSI_FIX_THRESH: WSI selection of fixed or auto adaptive thresholds 0 => auto adaptive thresholds 1 => fixed thresholds	0	SSM_RESET LBIST
Bit 12	WSFILT_CONF (see bits 16 to 19)	0	SSM_RESET LBIST
Bit 11:10	STS: Sensor Type Selection 00 => Two level, Standard 01 => Three level, VDA 10 => PWM Encoded, 2 level, 2 edges/tooth 11 => PWM Encoded, 2 level, 1 edge/tooth	0	SSM_RESET LBIST
Bit 9:6	WSFILT[3:0]: Wheel Speed filter time selection (500 ns per bit) If WSFILT_CONF=0: 0000 => 8 µs ----- => 500 ns per bit 1111 => 15.5 µs If WSFILT_CONF=1: xx00 => 8 µs, xx01 =>15 µs, xx10 => 30 µs, xx11 => 50 µs	0	SSM_RESET LBIST
Bit 5	WSIPTEN: Pass Through mode enable (valid only for PWM encoded sensors) 0 => Off 1 => On	0	SSM_RESET LBIST
Bit 4	SSDIS: DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor) 0 => DOUTx enabled during standstill 1 => DOUTx disabled during standstill	0	SSM_RESET LBIST

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Table 25. RS_CFG_2_3 register bit description (continued)

Data Field	Description	Reset Value	Reset Event
Bit 3	WSI_FIX_THRESH: WSI selection of fixed or auto adaptive thresholds 0 => auto adaptive thresholds 1 => fixed thresholds	0	SSM_RESET LBIST
Bit 2	WSFILT_CONF (see bits 6 to 9)	0	SSM_RESET LBIST
Bit 1:0	STS: Sensor Type Selection 00 => Two level, Standard 01 => Three level, VDA 10 => PWM Encoded, 2 level, 2 edges/tooth 11 => PWM Encoded, 2 level, 1 edge/tooth	0	SSM_RESET LBIST

Table 26. RS_CTRL register

ADDR	NAME	TYPE	BITS = 10
0001011	RS_CTRL	RW	9: WSS_EN_SAT_FLAGS, 8: WSS_READ_CURRENT, 5: INIT, 4:DIAG, 3:0 WSIENA

WSICTRL register stores Remote sensor control field.

Bits 3 down to 0 of this register are used to enable WSS interfaces. These bits can be written only when INIT bit (bit 5) of this register is '1'. When INIT is cleared to 0, also bits 3 down to 0 are cleared to 0. Enable/Disable state of interfaces is maintained and it can be monitored by reading back RS_DATA_RSDR registers.

Bits 8 and 9 of this register can be changed only when INIT bit is '1'. When INIT is cleared to '0' these bits maintain their values.

Table 27. RS_CTRL register bit description

Data Field	Description	Reset Value	Reset Event
Bit 9	WSS EN SAT FLAGS: Allow to read WSS current saturation flags available in RS_DATA_RSDR_12 0 => disable flags 1 => enable flags	0	SSM_RESET LBIST
Bit 8	WSS READ CURRENT: Allow to read instantaneous converted current in bit [9:0] of RS_DATA_RSDR_4/5/6/7 0 => reading base current 1 => reading instantaneous current	0	SSM_RESET LBIST

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Table 27. RS_CTRL register bit description (continued)

Data Field	Description	Reset Value	Reset Event
Bit 5	INIT: Allow access to RS_CFG_x registers, RS_CTRL register bits 3 down to 0 and RS_AUX_CFG register. 0 => Off 1 => On	0	SSM_RESET LBIST
Bit 4	DIAG: Allow access to WSS test reg 0 => Off 1 => On	0	SSM_RESET LBIST
Bit 3:0	CHxEN: Channel x Output enable, updated by Reset Event or SPI write 0 => Off 1 => On	0	SSM_RESET LBIST

Table 28. RS_AUX_CFG register

Addr	Name	Type	Bits = 20
0001110	RS_AUX_CFG	RW	Offset Thr Range= 19:10, Lo Thr Range = 9:0

RS_AUX_CFG register stores WSI Thresholds for fixed current trip-point method.

Table 29. RS_AUX_CFG register bit description

Data Field	Description	Reset Value	Reset Event
Bit 19:18	SECOND_RANGE_SEL: (valid only for adaptive thresholds): 00 => $\Delta Ith2_{MIN}$= 12.5 mA, $\Delta Ith2_{MAX}$ = 15.5 mA; 01 => $\Delta Ith2_{MIN}$=11.0mA, $\Delta Ith2_{MAX}$=17.0mA; 10 => $\Delta Ith2_{MIN}$=9.5mA, $\Delta Ith2_{MAX}$=18.5mA; 11 => $\Delta Ith2_{MIN}$=8.0mA, $\Delta Ith2_{MAX}$=20.0mA;	01	SSM_RESET LBIST
Bit 17:10	WSI_OFFS_TH[7:0]: In case of fixed thresholds this represents offset from low threshold to calculate the high threshold (see formula in *Section 4.1*). In case of adaptive thresholds this is the offset to calculate maximum value of base current IB0: $IB0_{MAX}$= $IB0_{MIN}$ + OFFSET_IB0. In both cases LSB=93.75 µA typ.	0x34	SSM_RESET LBIST

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Table 29. RS_AUX_CFG register bit description (continued)

Data Field	Description	Reset Value	Reset Event
Bit 9:8	FIRST_RANGE_SEL (valid only for adaptive thresholds): 00 ==> $\Delta Ith1_{MIN}$=6.25mA, $\Delta Ith1_{MAX}$=7.75mA; 01 ==> $\Delta Ith1_{MIN}$=5.5mA, $\Delta Ith1_{MAX}$=8.5mA; 10 ==> $\Delta Ith1_{MIN}$=4.75mA, $\Delta Ith1_{MAX}$=9.25mA; 11 ==> $\Delta Ith1_{MIN}$=4.0mA, $\Delta Ith1_{MAX}$=10.0mA;	01	SSM_RESET LBIST
Bit 7:0	WSI_FIRST_TH[7:0]: In case of fixed thresholds this is used to calculate low threshold (see formula in 4.1). In case of adaptive thresholds this is the minimum value of IB0 ($IB0_{MIN}$ range from 0 to 24 mA). In both cases LSB=93.75 µA typ.	0x33	SSM_RESET LBIST

WSI remote sensor data/fault register

Table 30. RS_DATA_RSDR_0-3 registers

ADDR	Name	Type	Bits = 20
0010000	RS_DATA_RSDR_0	RO	See description
0010001	RS_DATA_RSDR_1	RO	See description
0010010	RS_DATA_RSDR_2	RO	See description
0010011	RS_DATA_RSDR_3	RO	See description

RS_DATA_RSDR_x register stores status bits of WSS interface. Output format depends on the status of bit 15.

No Fault condition:

Table 31. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 0]

Data Field	Description	Reset Value	Reset Event
Bit 19:17	CRC [2:0]: CRC based on bits [16:0] Update based on bits [16:0]	-	SSM_RESET LBIST
Bit 16	STDSTL: Standstill indication (only for VDA sensor or PWM 2 edges) 0 => Valid sensor signal 1 => Standstill	0	SSM_RESET LBIST

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Table 31. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 0] (continued)

Data Field	Description	Reset Value	Reset Event
Bit 15	FLT: Fault Status, depending on fault status the DATA bits are defined differently. Cleared when all the fault bits are 0, set when one of the fault bits is 1 0 => No fault 1 => Fault	1	SSM_RESET LBIST
Bit 14	Latch_D0: Latched D0, set when previous message contains a '1' in bit0, cleared on read (only for VDA sensor) 0 => no prior bit0 faults 1 => prior message(s) contained bit0 fault	0	SSM_RESET LBIST
Bit 13:12	LCID[1:0]: Logical Channel ID 00 => ch1 01 => ch2 10 => ch3 11 => ch4	-	SSM_RESET LBIST
Bit 11:0	12-bit data from wheel speed decoder VDA Data Format: DATA[7:0] Data bits DATA[11:8] Counter bits PWM Data Format: DATA[8:0] Pulse Data bits STD Data Format: All zeros, data bits not used	0	SSM_RESET LBIST

Fault condition:

Table 32. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 1]

Data Field	Description	Reset Value	Reset Event
Bit 19:17	CRC [2:0]: CRC based on bits [16:0] Update based on bits [16:0]	-	SSM_RESET LBIST
Bit 16	NOT USED	0	-
Bit 15	FLT: Fault Status, depending on fault status the DATA bits are defined differently. Cleared when all the fault bits are 0, set when one of the fault bits is 1 0 => No fault 1 => Fault	1	SSM_RESET LBIST

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Table 32. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 1] (continued)

Data Field	Description	Reset Value	Reset Event
Bit 14	On/Off: Channel on/off status, cleared by Reset Event or when the channel is commanded OFF via SPI WSICTRL or when the STG bit is set or WSITEMP bit is set 0 => Off 1 => On	0	SSM_RESET LBIST
Bit 13:12	LCID[1:0]: Logical Channel ID 00 => ch1 01 => ch2 10 => ch3 11 => ch4	-	SSM_RESET LBIST
Bit 11:10	NOT USED	0	-
Bit 9	STG: Short to ground of RSUHx (over current condition of RSUHx) 0 => no fault 1 => fault	0	SSM_RESET LBIST
Bit 8	STB: Short to battery of RSUHx ($V_{RSUHx} > V_{PREREG} + V_{RSUHxSTB}$) 0 => no fault 1 => fault	0	SSM_RESET LBIST
Bit 7	CURRENT HI: Set when channel current measured in RSULx exceeds $I_{THVBATP}$ for a time determined by an up/down counter 0 => no fault 1 => fault	0	SSM_RESET LBIST
Bit 6	OPENDET: Open Sensor detected. Set when channel current in RSULx is below I_{THOPEN} for a time determined by an up/down counter 0 => no fault 1 => fault	0	SSM_RESET LBIST
Bit 5	WSITEMP: Overtemperature detected 0 => no fault 1 => fault	0	SSM_RESET LBIST
Bit 4	INVALID: Invalid data, set when parity error is detected (when this check is feasible), valid only for VDA sensor. 0 => no fault 1 => fault	0	SSM_RESET LBIST

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Table 32. RS_DATA_RSDR_0-3 registers bit description [Bit 15 = 1] (continued)

Data Field	Description	Reset Value	Reset Event
Bit 3	NODATA: No data in buffer (valid also for two level STD sensors but in this case, where data bits are not expected, this bit is high during normal communication) 0 => no fault 1 => fault	1	SSM_RESET LBIST
Bit 2	PULSE OVERFLOW: Pulse duration counter overflow_ (available only for PWM encoded WSS) 0 => no fault 1 => fault	0	SSM_RESET LBIST
Bit 1:0	NOT USED	0	SSM_RESET LBIST

Table 33. RS_DATA_RSDR_4-7 registers

Addr	Name	Type	Bits = 20
0010100	RS_DATA_RSDR_4	RO	For channel 0, See description
0010101	RS_DATA_RSDR_5	RO	For channel 1, See description
0010110	RS_DATA_RSDR_6	RO	For channel 2, See description
0010111	RS_DATA_RSDR_7	RO	For channel 3, See description

Table 34. RS_DATA_RSDR_4-7 registers bit description

Data Field	Description	Reset Value	Reset Event
Bit 19:10	the content of this register is value of first delta (ΔIth1) LSB=93.75 µA typ.	0x4B	SSM_RESET LBIST
Bit 9:0:	In case WSS_READ_CURRENT bit = 0 the content of this register is value of base current (IB0); in case WSS_READ_CURRENT bit = 1 the content of the register is value of instantaneous current in RSULx pin. In both cases LSB=93.75 µA typ.	0x4A	SSM_RESET LBIST

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Table 35. RS_DATA_RSDR_8-11 registers

Addr	Name	Type	Bits = 10
0011000	RS_DATA_RSDR_8	RO	For channel 0, See description
0011001	RS_DATA_RSDR_9	RO	For channel 1, See description
0011010	RS_DATA_RSDR_10	RO	For channel 2, See description
0011011	RS_DATA_RSDR_11	RO	For channel 3, See description

Table 36. RS_DATA_RSDR_8-11 registers bit description

Data Field	Description	Reset Value	Reset Event
Bit 9:0:	the content of this register is value of second delta (ΔIth2) LSB = 93.75 µA typ.	0x96	SSM_RESET

Table 37. RS_DATA_RSDR_12 register

Addr	Name	Type	Bits = 12
0011100	RS_DATA_RSDR_12	RO	See description

Table 38. RS_DATA_RSDR_12 register bit description

Data Field	Description	Reset Value	Reset Event
Bit 11:9	(2nd range saturation flag, 1st range saturation flag, Base current saturation flag) related to channel 3. Enabled only when WSS_EN_SAT_FLAGS (bit 9 of RSCTRL register) is 1.	0x0	SSM_RESET
Bit 8:6	(2nd range saturation flag, 1st range saturation flag, Base current saturation flag) related to channel 2. Enabled only when WSS_EN_SAT_FLAGS (bit 9 of RSCTRL register) is 1.	0x0	SSM_RESET
Bit 5:3	(2nd range saturation flag, 1st range saturation flag, Base current saturation flag) related to channel 1. Enabled only when WSS_EN_SAT_FLAGS (bit 9 of RSCTRL register) is 1.	0x0	SSM_RESET
Bit 2:0	(2nd range saturation flag, 1st range saturation flag, Base current saturation flag) related to channel 0. Enabled only when WSS_EN_SAT_FLAGS (bit 9 of RSCTRL register) is 1.	0x0	SSM_RESET

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Table 39. RSU_STATUS register

ADDR	NAME	TYPE	BITS = 8
0001010	RSU_STATUS	R	LS Over Current and Short to ground Status

Table 40. RSU_STATUS register bit description

Data Field	Description	Reset Value	TYPE
Bit 7:4	LS OVER CURRENT channels 3:0. (Active if the wss LS are ON) 0 => NO FAULT 1 => FAULT	0	SSM_RESET LBIST
Bit 3:0	LS Short To Ground channels 3:0. (Active if the wss LS are OFF) 0 => NO FAULT 1 => FAULT	0	SSM_RESET LBIST

5.2 Tracking regulation

RSUH0 and RSUH1 output pins can be configured as independent tracking regulators; this is the default configuration at start-up. Each regulator tracks the voltage reference given by the VCC (default) or VCC5 rail, depending on the user selection via SPI command. The 2 channels can be activated or deactivated independently (default state is off). Over/under voltage and over current monitoring are applied to RSU0/1 channels when in tracking regulator configuration and result bits are available via SPI.

5.3 Remote sensor interface fault protection

Each output is short circuit protected by an independent current limit and a thermal detection circuit. Current limit and overcurrent detection are present for both RSUHx and RSULx and they are independent of RSUHx and RSULx. In case RSUHx overcurrent is detected the output stage is disabled after filter time while in case of RSULx overcurrent it's not disabled. In any case if the thermal protection (shared between RSUH and RSUL) is triggered the output stage is disabled. In case the thermal warning level would not be reached, the current limitation circuitry will prevent damages on the channel, while operating the output. This fault condition does not interfere with the normal operation of the IC or with the operation of the other channels.

All RSUHx(x=0,1,2,3) are independently protected against a short to battery condition. Short to battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The channel in short to battery is not shutdown by this condition. Other channels are not affected in case of short of one output pin.

The sensor interface of RSULx(x=0,1,2,3) also offers open condition (only in ON state) and short to ground detection (only in OFF state). The channel in this condition is not shutdown. If there is open circuit for RSUHx, it will be detected by open detection of corresponding RSULx if the sensor is still connected to RSULx.

The short to ground detection is implemented with a pull-up current (IRSUL_PU) and a voltage comparator (V_{STGTH}) on RSULx (x=0,1,2,3). Requirement is that external short to

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ground with a resistance ≤ 7 kΩ will be detected as short condition while a short with a resistance ≥ 19 kΩ will not be detected. This kind of diagnostic is present only when channel is in OFF state.

The current sense is carried out in the low side through RSULx(x=0,1,2,3). The sensor interface implements either the detection of a leakage to battery or RSUHx condition, that will possibly raise the sensor current level. The channel in this condition is not shutdown.

5.4 Electrical characteristics

Table 41. WSS configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{RSUHx}	RSUHx load capacitance	Design Information	6	-	-	nF
C_{RSULx}	RSULx capacitance	Design Information	-	-	30.8	nF
R_{RSUx}	Output resistance	High side + low side Up to I_{LIMTH}	4.75	-	30	Ω
I_{BO}	Base Current	Auto-adjusting option (default value)	-9%	7	+9%	mA
I_{TH1}	7 mA / 14 mA detection	-	-9%	9.8	+9%	mA
I_{TH2_RISE}	14 mA / 28 mA rising edge detection	-	-9%	19.8	+9%	mA
I_{TH2_FALL}	14 mA / 28 mA falling edge detection	-	-9%	13.6	+9%	mA
I_{THOPEN}	Open sensor detection	$V_{RSULx=OPEN}$	1.0	-	3.5	mA
t_{OPEN_DET}	Open sensor detection filter time	-	11	-	15	µs
$I_{THVBATP}$	RSUL leakage to VBATP or RSUHx threshold	$V_{RSULx=}$ $V_{RSUHx,}$	-15%	23	+15%	mA
$t_{LEAKBAT_DET}$	RSUL leakage to VBATP or RSUHx filter time	-	97	-	110	µs
$I_{LIMTHHS}$	Output Current Limit	High side	-80	-	-33	mA
$t_{ILIMTHHS}$	HS overcurrent detection filter time	-	350	-	650	µs
I_{OCTHHS}	Overcurrent threshold	High side	-80	-	-31	mA
$I_{LIMTHLS}$	Output Current Limit	Low side	35	-	80	mA
$t_{ILIMTHLS}$	LS overcurrent detection filter time	-	350	-	650	µs
I_{OCTHLS}	Overcurrent threshold	Low side	35	-	80	mA
$t_{RSUHxSTB}$	RSUHx short to Battery detection filter time	-	11	-	15	µs
$V_{RSUHxSTB}$	Output Short to Battery Threshold	Versus VPREREG	10.0	-	100	mV

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Table 41. WSS configuration (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{STBTH}	Static reverse current into VPREREG	$V_{RSUHx} > V_{VPREREG} + V_{RSUHxSTB}$	0.0	-	1	mA
I_{RSUL_PU}	RSULx pull-up current	RSULx=OFF $0V < V_{RSULx} < V_{STGTH}$	80	-	180	µA
V_{STGTH}	LS short to ground threshold voltage	Off state	1.35	1.65	1.95	V
t_{STGTH}	LS short to ground detection filter time	Off state	500	-	600	µs
t_{BLNKHS}	HS diagnostics blanking time	-	240	-	360	µs
V_{OH}	WSOx Output Voltage	Ioh = -1 mA	VCC-0.5	-	-	V
V_{OL}	WSOx Output Voltage	Iol = 1 mA	-	-	0.4	V
I_{LKG}	WSOx Output Leakage	Tri-state leakage	-10	-	10	µA
$t_{deglitch}$	WS deglitch filter time	Configurable by SPI (4bits)	8	-	15.5	µs
-	Latency time between receiving sensor data @RSULx pin and reaching V_{OH} on WSOx pin	Trigger point 80% of RSux modulated current)	-	-	3.625 + $t_{deglitch}$	µs
-	Jitter on Latency time	-	-	-	125	ns
T_{JSD}	Thermal Shutdown	-	175	-	200	C
T_{HYS_TSD}	-	-	5	10	15	°C

Table 42. Tracking regulation configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{RSUH0}	RSUHx current capability	RSUH0	0	-	120	mA
I_{RSUH1}	RSUHx current capability	RSUH1	0	-	120	mA
C_{RSUHx}	RSUH load capacitance	Design Information	-25%	2.2	+25%	µF
R_{C_RSUHx}	Output capacitor ESR	Design Information	0.01	-	1	Ω
C_{RSUHx_EXT}	External sensor capacitor	Design Information	-	-	150	µF
V_{RSUHx_VCC}	Regulated output voltage	-	-20	VCC	+20	mV
$V_{RSUHx_VCC_UV}$	Undervoltage threshold	-	VCC - 10%	-	VCC - 5%	V
$V_{RSUHx_VCC_OV}$	Overvoltage threshold	-	VCC + 5%	-	VCC + 10%	V
V_{RSUHx_VCC5}	Regulated output voltage	-	-20	VCC5	+20	mV

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Table 42. Tracking regulation configuration (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{RSUHx_VCC5_UV}$	Undervoltage threshold	-	VCC5 - 10%	-	VCC5 - 5%	V
$V_{RSUHx_VCC5_OV}$	Overvoltage threshold	-	VCC5 + 5%	-	VCC5 + 10%	V
-	Line regulation	V(VPREREG) = 6V to 19V, I_{RSUHx} = 10mA, 100mA	-10	-	+10	mV
-	Load regulation	I_{RSUHx} = 10mA to 100mA, V(VPREREG) = 6V, 19V	-10	-	+10	mV
-	Transient line regulation	V(VPREREG) = 6 V to 19 V, dV/dt = 3 V/µs C_{RSUHx} = 2.2 µF	-5	-	+5	%
-	Transient load regulation	I_{RSUHx} = 10 mA to 100 mA, dI/dt = 100 mA/µs C_{RSUHx} = 2.2 µF	-5	-	+5	%
PSRR	Power supply rejection ratio	V(VPREREG) = 6.5 V, V_{noise} = 1Vpp f_{noise} = 20 kHz, C_{RSUHx} = 2.2 µF	40	-	-	dB
I_{LIMTH}	Output Current Limit	V(RSUHx) = -2 V	-340	-	-140	mA
I_{OCTH}	Overcurrent threshold	-	-340	-	-140	mA
$V_{RSUHxSTB}$	Output Short to Battery Threshold	-	10.0	-	100	mV
I_{STBTH}	Static reverse current into VPREREG	$V_{RSUHx} > V_{VPREREG} + V_{RSUHxSTB}$	0.0	-	1	mA
-	Soft start control	I_{RSUHx} = 10 mA C_{RSUHx} = 2.2 µF	5	-	25	V/ms

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6 General purpose output (GPO) driver

The device integrates one GPO driver operating in low-side mode. GPO driver can be used in multiple ways, depending on application needs.

Default configuration uses the GPO output interface to map the internal RSUHx signal on the GPOD0 pin. In this way, the decoded signal from the RSUHx sensor channel can be output as voltage information on the GPO output, even without intervention of the microcontroller. The following assignment matrix can be configured via SPI.

Table 43. Assignment matrix configured via SPI

-	RSUH0	RSUH1	RSUH2	RSUH3	GPOD0_RSU_SEL
GPOD0	√	-	-	-	00 (default)
	-	√	-	-	01
	-	-	√	-	10
	-	-	-	√	11

GPO driver can also be configured to operate in ON-OFF mode or in PWM mode setting the desired duty cycle and frequency (128 Hz nominal) values through SPI register.

The default state of the driver is off. The driver can be activated via SPI.

The driver output structure is designed to stand -1V on its terminals and a +1V reverse voltage across source and drain. The GPO driver is protected against short circuits and thermal overload conditions. The driver is switched off if SSM_reset is asserted and the driver automatically restarts when the fault is cleared.

The device also offers an open load diagnostics while in ON state.

Table 44. GPO electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{sat}	Output saturation voltage	$V_{sat} = V_{GPOD0} – GND$; $I_{GPO0} = 70mA$	-	-	0.5	V
IGPO_LIM	Current Limit	$V_{GPOD0} – GND = 1.5V$	80	-	145	mA
I_{GPO_OC}	Overcurrent	$V_{GPOD0} – GND = 1.5V$	80	-	145	mA
$GPO_{ilim_oc_delta}$	Delta_Ilim_Oc	$I_{GPO_LIM} – I_{GPO_OC}$	0.1	-	20	mA
$I_{OpenLoad}$	Open load current threshold	ON condition	-	-	3	mA
I_{LKG_GPODx}	GPO Output Leakage Current	Vbattery=V_{GPOD0}=19V; GPO in OFF condition	-10	-	10	µA
$I_{reverse}$	Reverse current	V_{GPOD0} = -1V OFF condition	-	-	1	mA
T_{JSD}	Thermal Shutdown	-	175	-	200	C
T_{HYS_TSD}	-	All states off	5	10	15	°C
C_{GPO}	Load capacitor	Design info	60	100	140	nF

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Table 44. GPO electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{LKG_GPODx_DEV_OFF}$	GPO Leakage in Power-Off	V_{GPOD0} = 19V; VBST=0V	-10	-	10	µA
dV/dt_{led_BLow}	Output Voltage Slew Rate	30% - 70%; R_{Load} = 273Ω, C_{GPO} = 100nF; 4.5 ≤ VBATP ≤ 14 V	0.1	0.25	0.55	V/µs
dV/dt_{led_BHigh}	Output Voltage Slew Rate	30% - 70%; R_{Load} = 273Ω, C_{GPO} = 100nF; 4.5 ≤ VBATP ≤ 19 V	0.01	-	0.55	V/µs
t_{ilim}	Current Limit Filter Time	-	8	-	15	µs
t_{open_load}	Open load filter time	-	-	-	12.5	µs
t_{mask}	Diagnostic mask delay after switch ON	C_{GPO} = 100 nF typ; R_{Load} = 273 Ω; VBATP = 14 V	30	50	70	µs
t_{JSDF}	Thermal Shutdown Filter Time	-	-	-	12.5	µs
f_{PWM}	PWM frequency	Programmable by SPI	64	-	521	Hz

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7 System functional safety implementations

7.1 General functional safety implementations

The device comes with a set of analog and digital design implementations:

- Double independent voltage reference;
- Oscillator clock monitoring;
- Battery monitoring;
- ECU supply voltage monitoring;
- Internal (more than 30 channels) and external (up to 7 channels) analog voltage measurements;
- Double watchdog control;
- Pump motor driver diagnostics;
- Reset output pin;
- Fault output pin;
- Fail-safe configurable output pin;
- Analog BIST on all analog voltage monitors;
- Digital BIST;
- Over temperature protection;
- Temperature sensor

7.2 System monitoring and reset handling

7.2.1 Analog to Digital algorithmic converter

The device hosts an integrated 10-bit Analog to Digital converter, running at a clock frequency of 16MHz. The ADC output is processed by a D to D converter with the following functions:

- Use of trimming bits to recover additional gain error due to resistor dividers mismatch;
- Digital low-pass filtering;
- Conversion from 12 to 10 bits.

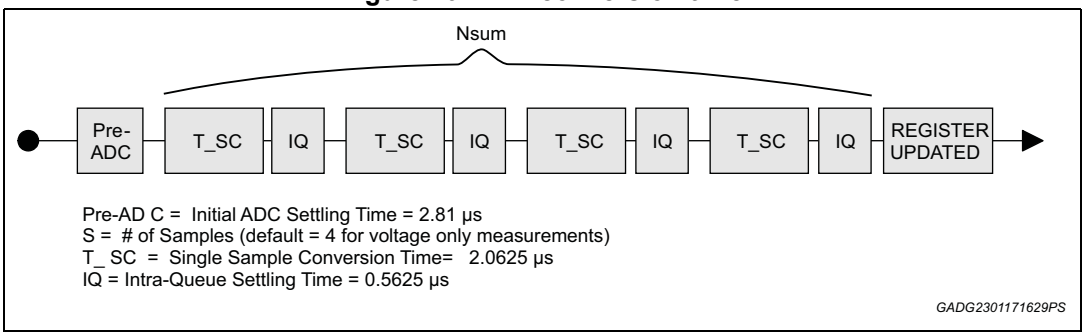
10-bit data are filtered inside the digital section. The number of samples that are filtered vary depending on the chosen conversion. The sample number can be configured by accessing the ADC_CFG register. After low pass filter, the residual total error is +/-5 LSB. This error figure applies to the case of a precise reference voltage: the spread of reference voltage causes a proportional error in the conversion output.

The reference voltage of the ADC VREFH is set to 2.5 V and VREFL set to 0.1 V. Therefore the voltage range is 2.4 V.

The conversion time is comprised of several factors: the number of measurements loaded into the queue, the number of samples taken for any measurement, and the various settling times. An example of conversion time calculation for a full ADC request queue is reported in *Figure 10*. The timings reported in *Figure 10* are nominal ones, min/max values can be obtained by considering the internal oscillator frequency variation reported in the DC characteristics section.

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Figure 10. ADC conversion time



All electrical characteristics are valid for the following conditions unless otherwise noted:

-40 °C ≤ T_j ≤ +175 °C; 6 ≤ VBST ≤ 19 V

Table 45. Analog to digital converter

Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
V_{ADC_RANGE}	ADC input voltage range	-	0.1	-	2.5	V
$V_{ADC_REF_H}$	ADC Reference voltage	-	-3%	2.5	+3%	V
ADC_RES	ADC resolution(1)	Design Info	-	10	-	bit
-	Differential non linearity error (DNL)	-	-2	-	+2	LSB
-	Integral non linearity error (INL)	-	-3.5	-	+3.5	LSB
-	Total error	Not including reference voltage error	-5	-	+5	LSB
-	Internal BG reference readout	-	480	492	504	LSB
-	Internal BG monitor readout	-	480	492	504	LSB

1. LSB = (2.5 V / 1024) = 2.44 mV.

7.2.2 Voltage measurement

The device includes a 10-bit ADC converter with high voltage multiplexer stage to report any of the relevant internal voltage levels through SPI.

It further includes 3 discrete analog input pins AI2, AI3, AI4, 0.2V to 5V range, for external generic measurements.

All the channels are acquired cyclically after the SSM reset is released and the values are available on the ADC CONV REG x registers. A digital programmable filter is implemented in order to reduce the noise.

Setting the ADC CONFIG NSUM [2:0] bits in ADC_CFG register the filter will return the average values calculated on N samples acquired for each channel to be converted. The conversion time of the cycle depends on N following this table:

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Table 46. Conversion time

ADC CONFIG NSUM	N	Con. time (all channels)
“000”	1 sample	445 µs
“001”	2 samples	539 µs
“010”	4 samples	728 µs
“011”	8 samples	1106 µs
“100” to “111”	16 samples	1862 µs

Proper scaling is necessary for various voltage measurements. The divider ratios vary by measurement and are summarized by function in the table below.

Table 47. Divider ratios vary by measurement are summarized by function

Measurements	Divider ratio						
	22:1	15:1	10:1	7:1	4:1	2:1	1:1
CP	√	-	-	-	-	-	-
VBST	-	√	-	-	-	-	-
GPOD0	-	-	√	-	-	-	-
VB	-	-	√	-	-	-	-
VB_SW	-	-	√	-	-	-	-
VBM	-	-	√	-	-	-	-
VDBATT	-	-	√	-	-	-	-
VDS	-	-	√	-	-	-	-
PDS	-	-	√	-	-	-	-
IGN	-	-	√	-	-	-	-
WDTDIS	-	-	-	√	-	-	-
RSUH/L	-	-	-	-	√	-	-
VPREREG	-	-	-	-	√	-	-
VCC5	-	-	-	-	√	-	-
VCC	-	-	-	-	√	-	-
VCORE	-	-	-	-	√	-	-
SCORE	-	-	-	-	√	-	-
VDD	-	-	-	-	√	-	-
VINTA	-	-	-	-	√	-	-
AI[0..4]	-	-	-	-	-	√	-
Bandgap reference (BGR/BGM)	-	-	-	-	-	-	√
Temperature sensor	-	-	-	-	-	-	√

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Table 48. Voltage measurement electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Ratio_1	Divider Ratio	Guaranteed by design	-	1	-	V/V
Ratio_2	Divider Ratio	Vinput_range_2 = 0.2 V … 5 V	-0.8%	2	0.8%	V/V
Ratio_4	Divider Ratio	Vinput_range_4a = 0.4 V … 10 V for VCORE, SCORE; Vinput_range_4b = 1.5 V … 10 V for the other	-3%	4	3%	V/V
Ratio_7	Divider Ratio	Vinput_range_7 = 1.5 V … 17.5 V	-3%	7	3%	V/V
Ratio_10	Divider Ratio	Vinput_range_10 = 2 V … 25 V	-3%	10	3%	V/V
Ratio_15	Divider Ratio	Vinput_range_15 = 5.5 V … 35 V	-3%	15	3%	V/V
Ratio_22	Divider Ratio	Vinput_range_22 = 5.5 V … 51 V	-3%	22	3%	V/V
offset	Divider Offset	High impedance	-10	-	10	mV
Rratio2	Divider impedance	Multiplexer input to GNDA	200	-	800	kΩ
Rratio4	Divider impedance	Multiplexer input to GNDA	80	-	170	kΩ
Rratio7	Divider impedance	Multiplexer input to GNDA	120	-	300	kΩ
Rratio10	Divider impedance	Multiplexer input to GNDA	160	-	420	kΩ
Rratio15	Divider impedance	Multiplexer input to GNDA	200	-	630	kΩ
Rratio22	Divider impedance	Multiplexer input to GNDA	440	-	930	kΩ
$I_{leak_mux_on}$	Multiplexer On-state input leakage current	For all divider ratio except Ratio_1	-	-	60	µA

Note: For more information about L9396 ADC accuracy, please locate the "L9396 ADC Conversion Error" calculator in the attachment section.

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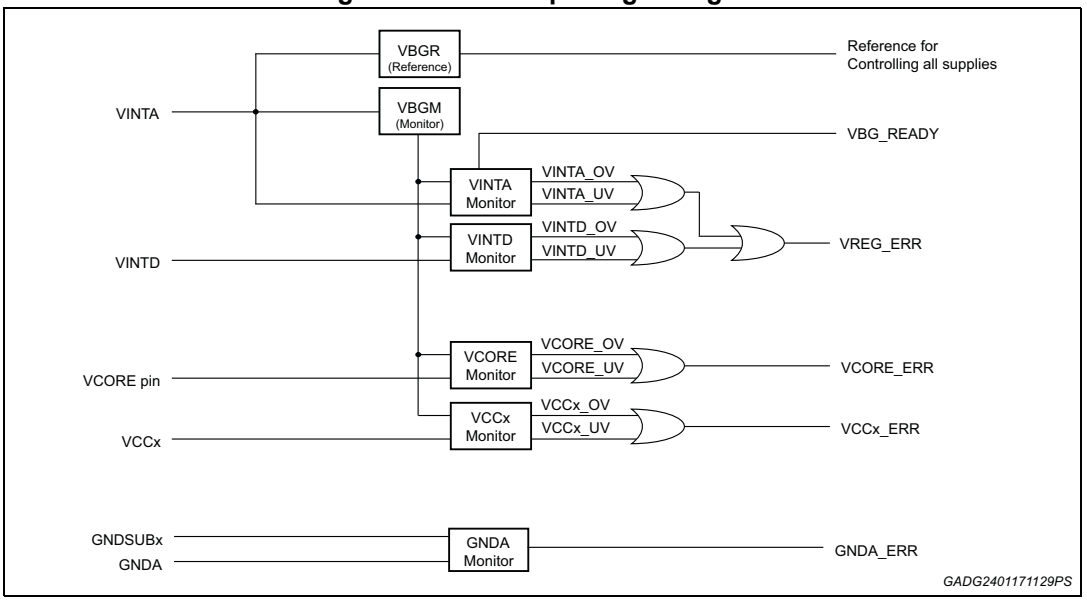
7.2.3 Reset output

RESET output pin conveys the active low reset signal generated by the device in case of over / under voltage conditions on the µC supply rails or when a watchdog error (either from WD1 or WD2) is asserted.

It is implemented as an open drain output, therefore an external source can be connected to this output. An external 5 kΩ typ pull-up is recommended to ensure the proper functionality.

RESET output is able to operate and force output low also in standby mode only if VBST supply is present.

Figure 11. Reset input logic diagram



Three internal reset signals are generated by the device:

- POR: Power On Reset - This reset is asserted when GNDD is open or a failure is detected in the internal supplies or bandgap circuits. When active, all other resets are asserted.
- WSM_RESET: Watchdog State Machine Reset - This reset is generated when the POR is active or when a failure is detected in the VCCx or VCORE supply.
- SSM_RESET: System State Machine Reset - This reset is asserted when the POR or the WSM_RESET are active, or when a failure is detected in either Watchdog state machine.

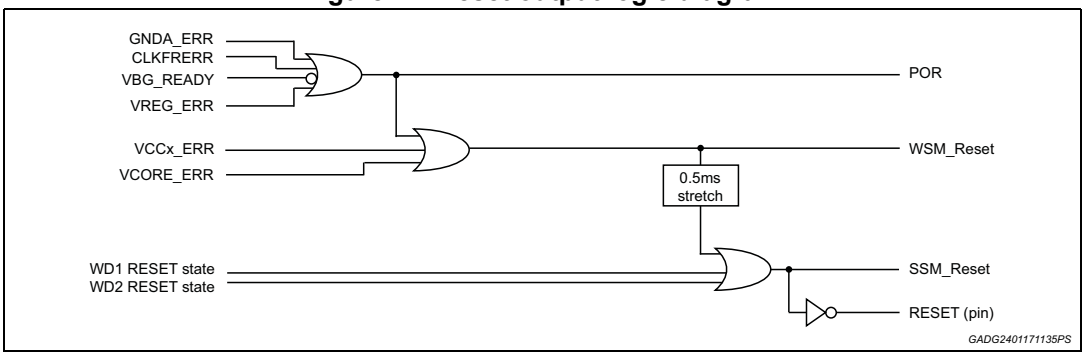
The RESET pin is the active-low signal driven on the output pin, and is an inverted form of SSM_RESET.

The cause of a RESET activation is latched and reported into the SUPPLY CONTROL REGISTERS and cleared upon SPI reading.

The reset logic shall be controlled as shown in the diagram below:

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Figure 12. Reset output logic diagram



-40°C ≤ T_j ≤ 175 °C; 3 V ≤ VCC ≤ 5.5 V, 5.6 ≤ VBST ≤ 19 V unless otherwise specified.

Table 49. Reset electrical characteristics

Symbol	Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
V_{OL}	RESET Logic Output Low Voltage	5 kΩ tied to VCC	-	-	0.4	V
V_{OH}	RESET Logic Output High Voltage	5 kΩ tied to VCC	VCC-0.05	-	-	V
t_r	Rise time	Load = 50 pF; 20%-80%	-	-	1	µs
t_f	Fall time	Load = 50 pF; 20%-80%	-	-	1	µs
$Ileak_{_RESET}$	RESET leakage current	RESET output off 0<RESET<VCC	-2	-	2	µA

7.2.4 Oscillator

The IC implements a clock frequency validation circuit. CLK ERR flag is the error signal reporting a problem with the integrated oscillator source. If the frequency of the integrated oscillator moves away from the desired one, the error flag is set. The check is performed by comparing the main oscillator with a secondary one; in case the frequency of the main oscillator shifts out of the specified range (in case of a stuck oscillator the CLOCK TIMEOUT ERROR is activated), the secondary oscillator source will recognize it, asserting the CLK ERROR flag.

The Clock monitor check is performed also comparing the second oscillator to the first one. The CLK ERROR flag is asserted also in case the frequency of the second oscillator shifts out of the specified range. To reduce the emissions of the main logic core and of the switching circuits in general, spread spectrum is operating on the main oscillator: the central 16 MHz frequency is varied by a triangular modulation at 125 kHz. Spread spectrum is always active and can be disabled setting the SPREAD SPECTRUM DISABLE MODE bit in the POWER_ON register.

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6 V ≤ VBST ≤ 19 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise noted.

Table 50. Oscillator electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
f_{OSCINT}	Internal Oscillator main frequency	-	15.1	16	16.9	MHz
$f_{OSCINT_mod_freq}$	Spread spectrum modulation frequency	Guaranteed by scan	-	125	-	kHz
$f_{OSCINT_mod_id_min}$	Spread spectrum minimum modulation index	-	-5	-	-2	%
$f_{OSCINT_mod_id_max}$	Spread spectrum maximum modulation index	-	2	-	5	%
$f_{OSCINT2}$	Internal second oscillator frequency	-	1.7	2	2.3	MHz

7.3 Fault output

The device provides a digital push-pull output. In its default configuration, the output is controlled low when the watchdogs are properly served and controlled high in case of watchdog errors. The meaning of watchdog error for WD1 is different in interrupt mode respect to warning lamp mode. In the first case it will be considered as a fault an event that causes a WD COUNTER decrease, while in the second case, the fault considered is a WD1 reset (so the most critical fault for WD1). About WD2 error, all faults will be considered, generating a reset.

This output can be used as a pre-driver for a passive warning lamp using the proper SPI Bit.

With a proper SPI configuration, FAULT output pin can act as an interrupt signal to the µC in case of:

- status change on wake-up input (IGN),
- over / under-voltage detections (see table below),
- thermal warnings (see table below).

Feedbacks can be programmed as mask-able via SPI register ADV_CONFIG (see *Table 51*).

In case of the above faulty conditions, with FAULT output configured in Interrupt mode, the FAULT output is driven high for t_{FAULT_ACT} in case of IGN status change and Watchdogs errors, while it is driven high for other faults (OT and over/under voltage detections) until the faults disappear and t_{FAULT_ACT} expires.

In case of faulty conditions, with FAULT output configured as passive warning lamp driver, the output is driven high until the faults disappear and the related flags are read.

FAULT output is enabled (exit of high impedance state) only at the end of power up cycle. This happens only when undervoltage of regulators (VPREREG, VCC, VCC5, VCORE) is no more present after power up.

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After that FAULT stays enabled until power down by wake-up is triggered or undervoltage of VPREREG is generated.

Here the table of masking bits and fault sources

Table 51. Masking bits and fault sources

-	FAILSAFE / FAULT OUTPUT WD1 and WD2 FAULT MASK	FAILSAFE / FAULT OUTPUT THERMAL WARNING MASK	FAILSAFE / FAULT OUTPUT µC VOLTAGE FAULT MASK	FAILSAFE / FAULT OUTPUT BOOST FAULT MASK
WD Q/A ERR	MASKED	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP
WD PRUN ERR	MASKED	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP
BOOST OT	INTERRUPT / WARNING LAMP	MASKED	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP
BUCK OT	INTERRUPT / WARNING LAMP	MASKED	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP
CP OT	INTERRUPT / WARNING LAMP	MASKED	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP
VCORE UV/OV	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP	MASKED	INTERRUPT / WARNING LAMP
VCC5 UV/OV	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP	MASKED	INTERRUPT / WARNING LAMP
BOOST UV	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP	INTERRUPT / WARNING LAMP	MASKED
IGN EDGE	INTERRUPT	INTERRUPT	INTERRUPT	INTERRUPT

40°C ≤ T_j ≤ 175°C; 3 V ≤ VCC ≤ 5.5 V, unless otherwise specified.

Table 52. Fault characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Fault logic output low voltage	I_{source} = 1 mA	-	-	0.4	V
V_{OH}	Fault logic output high voltage	I_{sink} = 1 mA	VCC-0.4	-	-	V
t_{FAULT_ACT}	Fault actuation time	-	35	48	60	µs

7.4 Watchdog control

This device offers a 2-level watchdog control approach. The first control level is given by means of a query & answer watchdog (WD1). The second control level controls the PRN input pin to assert the proper frequency is delivered by the microcontroller (WD2).

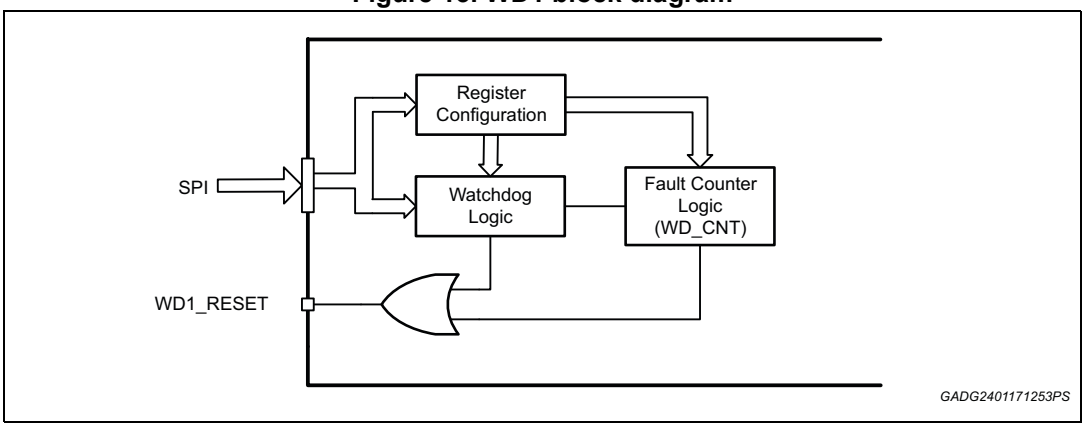
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7.4.1 Watchdog (WD1)

The device and the microcontroller exchange queries and answers on a defined timing base. An internal watchdog logic is implemented to inhibit load actuation such as to send reset signal, while it can disable directly these drivers through a second switch-off path:

1. Pump Motor Pre-Driver
2. GPO Driver
3. Fail Safe Pre Driver
4. VBAT Switch

Figure 13. WD1 block diagram

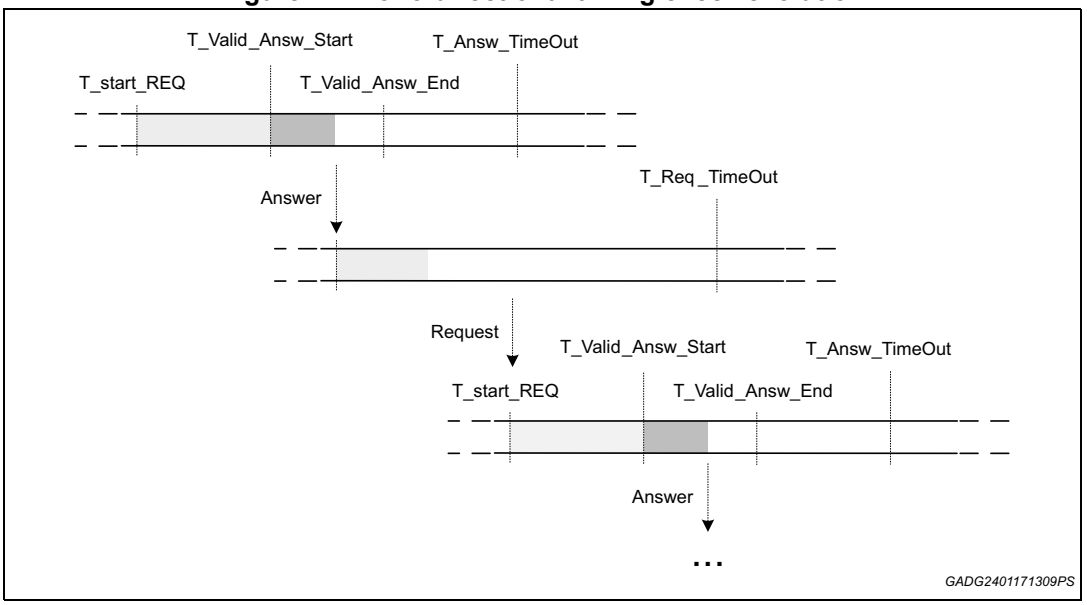


Two modes of timing checks are provided:

- Mono-directional: timing check based only on answers. Microcontroller must send queries (without timing window check) and answers on a defined time window;
- Bidirectional: timings are bidirectionally checked. L9396 must receive queries on a defined time window. Microcontroller must send answers on a defined time window.

In case time windows are not respected an error is generated.

Figure 14. Mono-directional timing check evolution



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Figure 15. Bidirectional timing check evolution

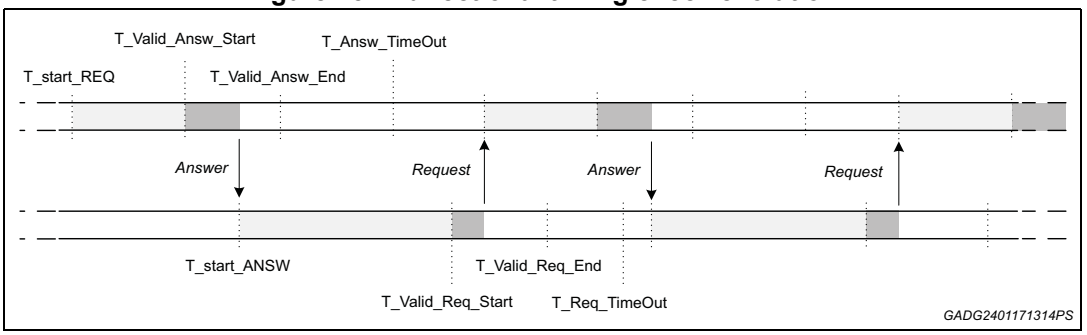


Table 53. Description of the timing parameter

Timing parameter	Description
T_start_REQ	Micro reads, through SPI register seed to be elaborated
T_Valid_Answ_Start	Starting time interval for Valid answers
T_Valid_Answ_End	Ending time interval for Valid answers
T_Answ_TimeOut	Time out for answer
T_start_ANSW	Micro sends, through SPI register answer to the IC
T_Valid_Req_Start	Starting time interval for next following request
T_Valid_Req_End	Ending time interval for next following request
T_Req_TimeOut	Time out for request

Both the request and the answer must be sent on a predefined timing interval.

When the microcontroller finishes its boot procedures, it will send the first seed sending request to the device. In this moment all the timing counters will start and never stop.

In order to detect a fast event, such as two consequent SPI frames, the time base is based on the WD frequency of 250 kHz, which is obtained from the device clock period (16 MHz). The obtained clock period WD_CLK is 4 µs. The clock used for the timing windows is a divided version of that in order to obtain a timing resolution of WD_CLK equal to 64 µs or 256 µs depending on the WD_CLK_DIV settings.

When the microcontroller sends the request of a new seed to the device (T_start_REQ) the WD_REQ_TMR timer starts to count. The microcontroller must send a valid answer inside the timing interval defined by the two SPI programmable parameters T_Valid_Answ_Start and T_Valid_Answ_End. In case the microcontroller sends an answer before T_Valid_Answ_Start or after T_Valid_Answ_End an error will be generated.

In case the WD_TO_RST_EN is set:

If no answer will arrive before T_Answ_TimeOut has elapsed, a WD1_RESET will be generated and the flag WD_RST_ TO_Answ will be set.

When the microcontroller sends the answer to the device (T_start_ANSW) the WD_ANSW_TMR timer starts to count. Microcontroller must send a new seed request inside the timing interval defined by the two SPI programmable parameters T_Valid_Req_Start and T_Valid_Req_End. In case the Micro sends the request before T_Valid_Req_Start or after T_Valid_Req_End an error will be generated. If no request will

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arrive before T_Req_TimeOut has elapsed, a WD1_RESET will be generated and the flag WD_RST_TO_Req will be set.

In case the WD_TO_RST_EN is not set:

The error event counter, WD_CNT, will be decreased and the device starts to wait again for the answer with the same timing procedure.

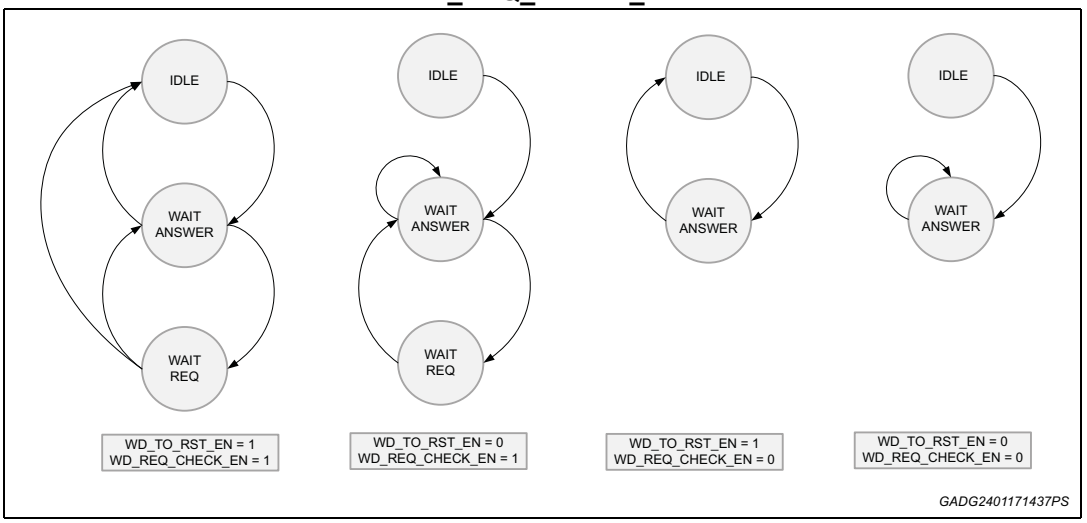
L9396 starts the WD evolution state machine in IDLE mode in which it is waiting for the first seed request from microcontroller through SPI. In this way the starting period is completely under the control of the microcontroller allowing to safely conclude boot procedure before starting the WD seed request/answer mechanism. During this period WD configuration registers can be programmed. The first seed request acts when a WD state machine start. After this event the WD will never stop and WD configuration registers become read only and cannot be changed. The only exception is about the T_Valid_Answ_Start and the T_Valid_Req_Start. In case one of these parameters is changed, the timing window restarts and WD_CNT will be decremented by a WD_cnt_bad_step number of steps.

WD_CNT is a 4-bit counter used to collect good and bad events provided by the microcontroller.

A good event is a Request coming in the correct timing window if a Request is expected in the FSM, or a correct Answer coming in the correct timing window when expected.

A bad event is a wrong Answer or an answer in a wrong timing window, a Request in a wrong timing window (in bidirectional mode), a timeout event, a Request when an Answer is expected or an Answer when a Read is expected.

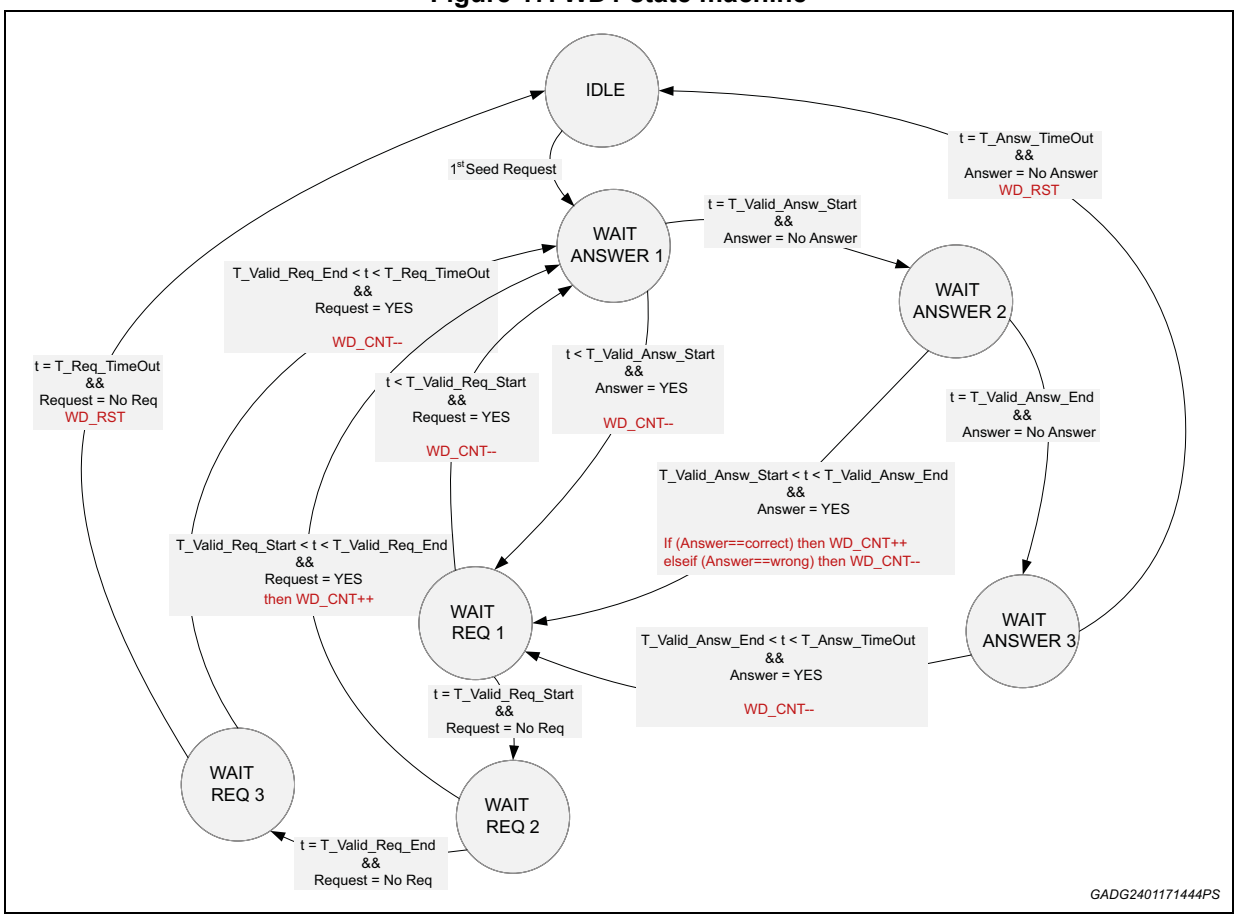
Figure 16. Timing State evolution depending on WD_TO_RST_EN and WD_REQ_CHECK_EN



Note: Also in mono-directional mode the FSM is waiting a Query after an Answer in order to send a new seed to µC but in this configuration the Timing check on Queries is not performed and WD_CNT is not decremented in case of request timing error except for Timeout.

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Figure 17. WD1 state machine



Depending on the value of the WD_CNT counter the device will stop the drivers, will send the WD1_RESET or will enable the drivers.

The WD_CNT will be incremented by a number of steps as defined through the SPI configurable parameter WD_cnt_good_step each time a correct answer is given in the right time interval or a Query arrives in the right time interval. In all the other cases, as defined in the WD state machine, the WD_CNT will be decremented by a number of steps as defined through the SPI configurable parameter WD_cnt_bad_step.

If WD_CNT reaches the value of zero two different behaviors are possible depending on the value of WD_RST_EN. If WD_RST_EN is set to 1 then a WD_RST will be sent by the device and the flag WD_RST_CNT will be set; else if WD_RST_EN is set to 0 then the WD_RST will not be sent by the device but the flag WD_RST_CNT will be set.

Two different thresholds are defined (both programmable through SPI): WD_th_low and WD_th_high.

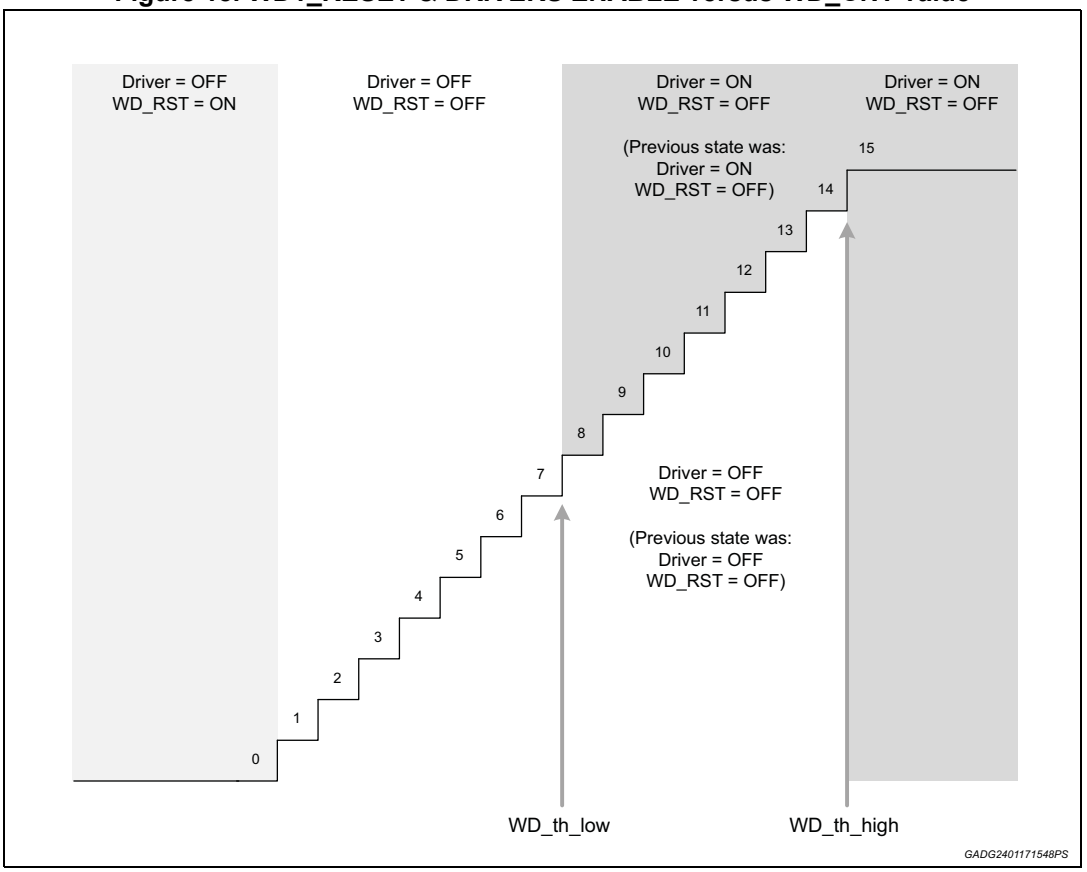
If WD_CNT value is lower than WD_th_low, but greater than zero, the drivers are disabled such as any WD_RST. If WD_CNT is greater than WD_TH_LOW and lower than WD_TH_HIGH the load actuation is managed in hysteresis mode:

If drivers are ON it will be stopped only when WD_CNT becomes lower than WD_TH_LOW, while if actuation was OFF it will be performed only when WD_CNT becomes equal to WD_TH_HIGH and only when WD_CNT exceeds this threshold drivers are activated.

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In this way, activation of the drivers can be performed only if the watchdog has been started and a certain number of good Request/Answer has been exchanged.

Figure 18. WD1_RESET & DRIVERS ENABLE versus WD_CNT value



All the status information is stored into the WD_Status_reg, readable through SPI. This register will be cleaned as a consequence of each read operation. In case a WD1_RESET is sent to the microcontroller, the device restarts the WD state machine in IDLE mode waiting for the seed request from microcontroller through SPI. This is valid also in case PRUN WD sends a reset to µC. WD configuration registers are preserved, but can be modified by the microcontroller before the WD mechanism has started. In the same way, also the status register, WD_Status_reg, is preserved and can be read through SPI.

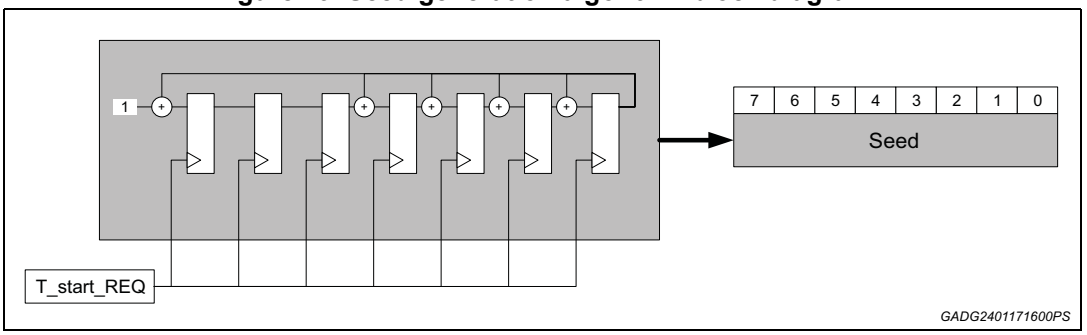
Two cases of unexpected errors have been identified:

- If a request of a new seed arrives to the device before the previous answer is received, the device will serve the new request, sending the old seed decreasing the value of WD_CNT by the amount WD_cnt_bad_step.
- If an answer arrives to the device before a new request and after another answer, the device will ignore this answer but it will decrease the value of WD_CNT by the amount WD_cnt_bad_step.

Seeds are 8-bit long words generated by a 7-bit LSFR pseudo-random algorithm. A new seed is sent into SPI word (WD_Seed) each time a new seed request (T_start_REQ) is sent to the device (if the last answer was correct).

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Figure 19. Seed generation algorithm block diagram



Seed is generated by the LSFR algorithm in Figure above. In particular the algorithm generates a 7-bit length word, while the seed has 8 bits including a zero as MSB. In this way the seeds are always positive. A new seed will be stored onto the WD_Seed only in case of a correct answer received. In case of an error, the same seed will be available into the WD_Seed until a correct answer will be received.

Figure 20. Seed selection and elaboration flow

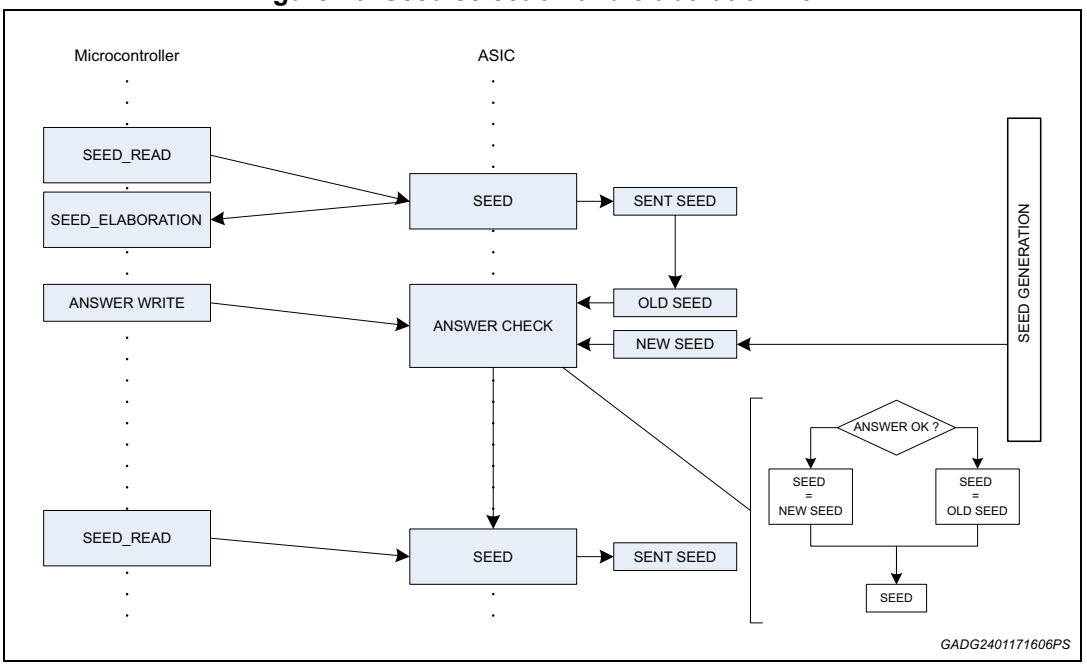
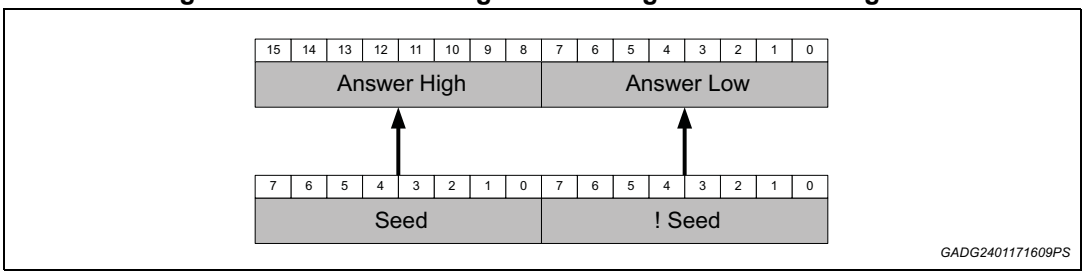


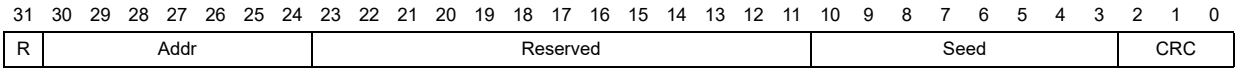
Figure 21. Answer check generation algorithm block diagram



The answer is a 16-bit long word checked against a 16-bit word composed by two bytes, Answer_Low and Answer_High, generated from the sent seed. Answer_Low is the logical 2's complement of the seed, while Answer_High is a replica of the seed being sent.

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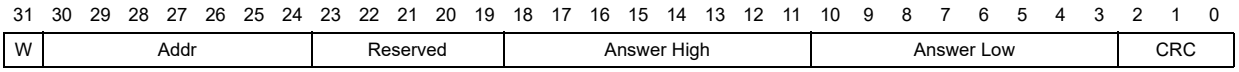
WD Seed



SPI parameter	Size (bits)	default	Description
Seed	8	-	Current value of the Seed sent to the Micro to be used for the Answer elaboration

Note: WD Seed and WD Answer will be into the same SPI register. When a Read operation will be performed a new seed will be sent and the read will be treated as a new Seed request. When an Answer write will not be treated as a new Seed request and the seed related to that answer will be sent back.

WD Answer



SPI parameter	Size (bits)	default	Description
Answer Low	8	-	Lower part of the answer
Answer High	8	-	Higher part of the answer

Note: WD Seed and WD Answer will be onto the same SPI register. When a Read operation will be performed a new seed will be sent and the read will be treated as a new Seed request. When an Answer write will not be treated as a new Seed request and the seed related to that answer will be sent back.

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WD Answer Timing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	Addr							-	T_Answ_TimeOut_Delta						T_Valid_Answ_End_Delta						T_Valid_Answ_Start									CRC		

SPI parameter	Size (bits)	default	Description
T_Valid_Answ_Start	8	0xFF	Start of the timing window inside which answers must be received. Absolute value. Time = T_Valid_Answ_Start * WD_clk
T_Valid_Answ_End_Delta	6	0x30	End of the timing window inside which answers must be received. The value specified is an incremental time starting from T_Valid_Answ_Start. Time = (T_Valid_Answ_Start + T_Valid_Answ_End_Delta) * WD_clk
T_Answ_TimeOut_Delta	6	0x00	End of the period for answers acceptance. Once reached, the WD1_RESET signal will be sent independently of the Error status (WD_CNT). The value specified is an incremental time starting from T_Valid_Answ_Start and T_Valid_Answ_End_Delta. Time = (T_Valid_Answ_Start + T_Valid_Answ_End_Delta + T_Answ_TimeOut_Delta) * WD_clk

SPI parameters are programmable only before the WD mechanism starts. After the first seed request, these parameters can be only read.

A WD1_RESET event does not clear programmed parameters; default values are applied only as a consequence of a WSM RESET.

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WD Request Timing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	Addr							-	T_Req_TimeOut_Delta						T_Valid_Req_End_Delta						T_Valid_Req_Start									CRC		

SPI parameter	Size (bits)	default	Description
T_Valid_Req_Start	8	0xFF	Start of the timing window inside which requests must be received. Absolute value. Time = T_Valid_Req_Start * WD_clk
T_Valid_Req_End_Delta	6	0x30	End of the timing window inside which requests must be received. The value specified is an incremental time starting from T_Valid_Req_Start. Time = (T_Valid_Req_Start + T_Valid_Req_End_Delta) * WD_clk
T_Req_TimeOut_Delta	6	0x00	End of the period for requests acceptance. Once reached, the WD1_RESET signal will be sent independently of the Error status (WD_CNT). The value specified is an incremental time starting from T_Valid_Req_Start and T_Valid_Req_End_Delta. Time = (T_Valid_Req_Start + T_Valid_Req_End_Delta + T_Req_TimeOut_Delta) * WD_clk

SPI parameters are programmable only before the WD mechanism starts. After the first seed request, these parameters can be only read.

A WD1_RESET event does not clear programmed parameters; default values are applied only as a consequence of a WSM_RESET.

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WD Counter Setup

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	Addr							-			WD_RST_EN	WD_REQ_CHECK_EN	WD_TO_RST_EN	WD_CLK_DIV	-	WD_Th_Low			WD_Th_High				WD_cnt_good_step			WD_cnt_bad_step			CRC		

SPI parameter	Size (bits)	default	Description
WD_RST_ EN	1	1	Enable for the WD_RST signal. 0: WD_RST signal not sent 1: WD_RST signal sent in case of failure
WD_REQ_CHECK_EN	1	0	Enable for the Request timing checking. 0: Request timing check not performed 1: Request timing check performed
WD_TO_RST_EN	1	0	Enable for the RST after Timeout generation. 0: RST not generated after a TO event 1: RST generated after a TO event
WD_CLK_DIV	1	0	Frequency Clock division setup. 0: clock not divided (64 µs) 1: clock divided by (256 µs)
WD_Th_Low	4	7	Threshold level to inhibit the drivers. If WD_CNT is lower than the threshold no drivers are activated. WD_Th_Low must be lower than WD_Th_High and minimum 1.
WD_Th_High	4	15	Threshold level to start the actuation. If WD_CNT is lower than the threshold actuation will be performed depending on the previous state as shown in *Figure 18*. WD_Th_High must be higher than WD_Th_Low.
WD_cnt_good_step	3	1	Number of incremental steps for WD_CNT as consequence of a good event
WD_cnt_bad_step	3	3	Number of incremental steps for WD_CNT as consequence of an error

SPI parameters are programmable only before the WD mechanism starts. After the first seed request, these parameters can be only read.

A WD1_RESET event does not clear programmed parameters; default values are applied only as a consequence of a WSM_RESET.

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WD Status register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	Addr							Reserved				-	WD_RST_Event_Value			-	WD_RST_Cnt	WD_RST_TO_Req	WD_RST_TO_Answ	WD_Late_Req	WD_Early_Req	WD_Bad_Answ	WD_Late_Answ	WD_Early_Answ	WD_Cnt_Value				CRC		

SPI parameter	Size (bits)	default	Description
WD_Cnt_Value	4	7	Current value of the WD counter
WD_Early_Answ	1	0	Flag set if the last answer has been sent too early related to the programmed timing parameters. 0: Ok 1: Answer sent before T_Valid_Answ_Start time
WD_Late_Answ	1	0	Flag set if the last answer has been sent too late related to the programmed timing parameters. 0: Ok 1: Answer sent after T_Valid_Answ_End time
WD_Bad_Answ	1	0	Flag set if the last answer has been sent inside the right timing window (between T_Valid_Answ_Start and T_Valid_Answ_End time) but it isn't the expected answer. 0: Ok 1: Wrong answer
WD_Early_Req	1	0	Flag set if the last request has been sent too early related to the programmed timing parameters. 0: Ok 1: Request sent before T_Valid_Req_Start time
WD_Late_Req	1	0	Flag set if the last request has been sent too late related to the programmed timing parameters. 0: Ok 1: Request sent after T_Valid_Req_End time
WD_RST_ TO_Answ	1	0	Flag set if the WD1_RESET signal has been sent because Answer time out elapsed. 0: Ok 1: WD1_RESET because T_Answ_Timeout elapsed
WD_RST_ TO_Req	1	0	Flag set if the WD1_RESET signal has been sent because Request time out elapsed. 0: Ok 1: WD1_RESET because T_Req_Timeout elapsed

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SPI parameter	Size (bits)	default	Description
WD_RST_ Cnt	1	0	Flag set if the WD1_RESET signal has been sent because error counter reached zero. 0: Ok 1: WD1_RESET because WD_CNT reached the value of zero
WD_RST_Event_Value	4	0	Current value of the WD_RST event already sent

Except the WD_Cnt_Value and WD_RST_Event_Value fields, this register is automatically cleared once read.

A WD1_RESET event does not clear programmed parameters; default values are applied only as a consequence of a WSM_RESET.

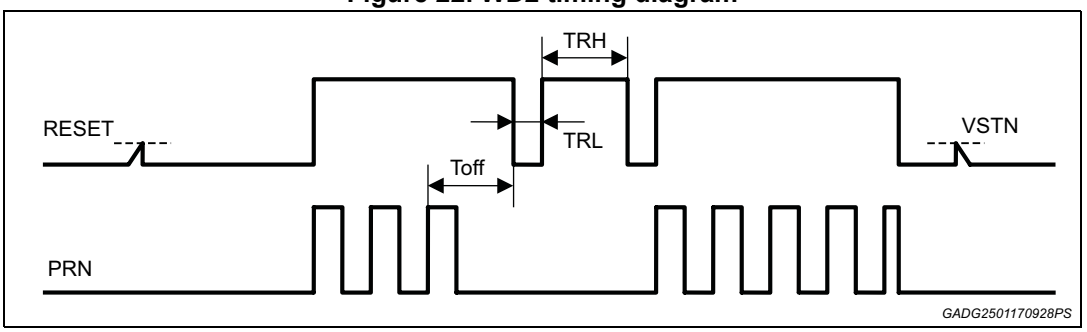
7.4.2 Second Watchdog (WD2)

When PRN signal input via PRN pin is not in the range of certain frequency, RESET is asserted. The watchdog logic detects the only rising edge of PRN signal on PRN pin.

When RESET is deasserted (or at WDTDIS deasserting) the WD2 is in IDLE state for at least TWAIT in order to wait the Microcontroller's logic bist end; after TWAIT the WD2 works normally.

When PRN signal stops for at least Toff, RESET pin generates low signal for a time equal to TRL (equal to Ton_RESET). This signal returns to high after TRL and for a time defined as TRH. If PRN signal is still not a proper one, the RESET signal returns low for TRL and then back high, repeating the above sequence.

Figure 22. WD2 timing diagram



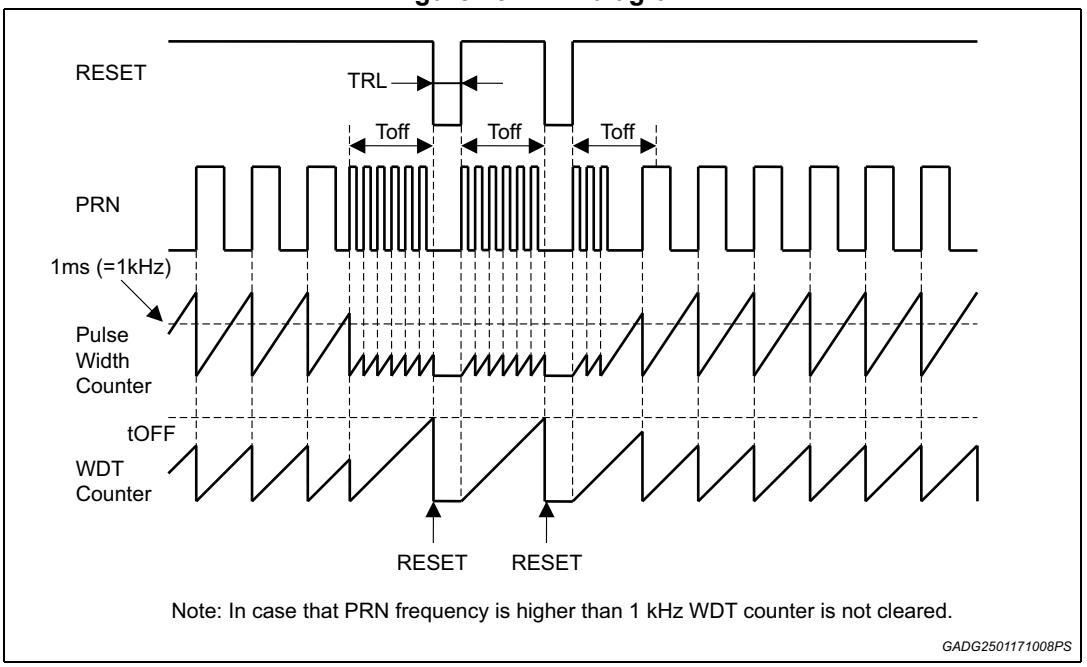
PRN frequency error is detected if the frequency is higher than 1 kHz and is not detected if the frequency is lower than 750 Hz. In other words, when the interval between PRN rising edges is less than 1 ms, watchdog detects PRN over frequency and does not clear WDT counter. If this condition continues during t_{off}, RESET pin drives low.

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Table 54. WD2 characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
FWD_{valid}	WD2 Frequency valid range	ADV_CONFIG[14,13] = '00'	91	-	750	Hz
		ADV_CONFIG[14,13] = '01'		-	1500	
		ADV_CONFIG[14,13] = '10'	46	-	750	
		ADV_CONFIG[14,13] = '11'		-	1500	
T_{off}	WD2 timeout reset time	ADV_CONFIG[14] = '0'	11	-	16.5	ms
		ADV_CONFIG[14] = '1'	22	-	33	
TRH	RESET re-engagement time between two consecutive assertion events		200	-	-	ms
TWAIT	WD2 quiescent time at power-up		200	-	-	ms

Figure 23. WD2 diagram



7.4.3 Watchdog Timer Disable Input (WDTDIS)

When controlled to a voltage higher than VIH_WDTDIS, this pin is used to disable the WD2 timer. It implements a passive pulldown to ensure the voltage level would not interrupt the WD control in case of open connection. The state of this pin can be read by SPI because it is acquired by an internal A2D converter. When WDTDIS pin is asserted, the watchdog timer is disabled, the timer is reset to its starting value and no faults are generated. When the watchdog timer is disabled, WD_2_RESET_FLAG bit is set to '0'.

-40°C ≤ T_j ≤ 175°C; 3 V ≤ VCC ≤ 5.5 V, unless otherwise specified.

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Table 55. WDTDIS characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL_WDTDIS}	WDTDIS Logic Input Low Voltage	-	-	-	0.75	V
V_{IH_WDTDIS}	WDTDIS Logic Input High Voltage	-	1.75	-	-	V
$V_{hysteresis}$	WDTDIS Input hysteresis Voltage	-	0.1	-	1	V
WDTDIS PD	WDTDIS pull-down	WDTDIS = 3.3V	10	-	100	µA

7.5 Fail safe output

L9396 provides the active low FSN output to let the system know the device enters the fail safe state. It means that the device has left its functional operating range due to:

- weak supply conditions or supply over/under voltage detections (see the table below for the signals monitored),
- thermal shutdown (see the table below),
- wrong SPI communications or wrong watchdog operation.

During fail-safe conditions, corresponding failure bits are set until the faults disappear and the flags are read. When the device enters a fail-safe condition, it remains in this state until both the following criteria are met:

- the failure condition disappears,
- the microcontroller performs a SPI reading on the failure bit(s).

The FSN output is intended to control functional safety logic through a redundant path (since the µC is not operational anymore) for up to ASIL-D applications.

The functional safety path is intended to control the applications loads in order to either maintain the functionality in a degraded mode or deactivate the loads. It is fault tolerant (programmed from 1 to 8 failures before activation) and has a programmable delay; all this can be programmed via SPI interface. To exit the fail-safe mode a specific SPI access on the original failure(s) has to be performed when the application recovers in order to clear the flags and fail safe fault tolerant counter.

FSN output is enabled (can be driven low) only at the end of power up cycle. This happens only when undervoltage of regulators (VPREREG, VCC, VCC5, VCORE) is no more present after power up.

After that FSN stays enabled until power down by wake-up is triggered or undervoltage of VPREREG is generated.

Here the table of masking bits and fault sources.

Table 56. Masking bits and fault sources

-	FAILSAFE / FAULT OUTPUT WD1 and WD2 FAULT MASK	FAILSAFE / FAULT OUTPUT THERMAL WARNING MASK	FAILSAFE / FAULT OUTPUT µC VOLTAGE FAULT MASK	FAILSAFE / FAULT OUTPUT BOOST FAULT MASK
WD Q/A ERR	MASKED	FAILSAFE FAULT	FAILSAFE FAULT	FAILSAFE FAULT
WD PRUN ERR	MASKED	FAILSAFE FAULT	FAILSAFE FAULT	FAILSAFE FAULT

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Table 56. Masking bits and fault sources (continued)

-	FAILSAFE / FAULT OUTPUT WD1 and WD2 FAULT MASK	FAILSAFE / FAULT OUTPUT THERMAL WARNING MASK	FAILSAFE / FAULT OUTPUT µC VOLTAGE FAULT MASK	FAILSAFE / FAULT OUTPUT BOOST FAULT MASK
BOOST OT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT	FAILSAFE FAULT
BUCK OT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT	FAILSAFE FAULT
VCC OT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT	FAILSAFE FAULT
CP OT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT	FAILSAFE FAULT
VCC UV/OV	FAILSAFE FAULT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT
VCORE UV/OV	FAILSAFE FAULT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT
VCC5 UV/OV	FAILSAFE FAULT	FAILSAFE FAULT	MASKED	FAILSAFE FAULT
SPI ERROR	FAILSAFE FAULT	FAILSAFE FAULT	FAILSAFE FAULT	FAILSAFE FAULT

Table 57. Fail safe output

Symbol	Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
V_{OL}	FSN Logic Output Low Voltage	5 kΩ tied to VCC	-	-	0.4	V
V_{OH}	FSN Logic Output High Voltage	5 kΩ tied to VCC	VCC-0.05	-	-	V
t_r	Rise time	Load = 50 pF; 20%-80%	-	-	1	µs
t_f	Fall time	Load = 50 pF; 20%-80%	-	-	1	µs
$Ileak_{_FSN}$	FSN leakage current	FSN output off 0 < FSN < VCC	-2	-	2	µA
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=000		0		mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=001	0	-	2	mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=010	2	-	4	mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=011	6	-	8	mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=100	8	-	10	mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=101	28	-	30	mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=110	48	-	50	mS
TFSN_DELAY	FSN digital assertion delay	Guaranteed by scan, ADV_CONFIG[7:9]=111	98	-	100	mS

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7.6 Temperature sensor

The device provides an internal analog temperature sensor. The sensor is aimed at having a reference for the average junction temperature on silicon surface. The sensor is placed far away from power dissipating stages and drivers. The output of the temperature sensor is available via SPI through ADC conversion. The formula to calculate temperature from ADC reading is the following one:

T(°C) = (0.154 - 2.5 * ADCdec / (2^10*4.5)) * 220 / 0.369 + 180

where ADCdec is ADC reading in decimal.

Table 58. Temperature sensor

Symbol	Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
T_{MON}	Monitoring temperature range	-	-40	-	175	°C
T_{ACC}	Temperature accuracy	-	-15	-	15	°C

7.7 Over temperature protection

Device is equipped with 9 independent thermal protection circuits placed close to circuits that can experience over temperature in fault condition.

These circuits are: 4 remote sensor interfaces (WSS), GPO driver, one shared between VCC and VCC5, VPREREG, Charge Pump, Boost.

The effect of thermal protections and how to manage this kind of fault is described in the paragraphs related to those blocks.

7.8 Bist

7.8.1 Logic Bist

In order to test the correct operation of the main safety relevant digital blocks, a logic bist is implemented.

The logic bist check can be controlled via SPI using the register BIST_CTRL.

The digital blocks checked are:

1. Wheel Speed Sensor Logic
2. Driver Controllers Logic
   a) BATTERY SWITCH
   b) PUMP MOTOR PRE DRIVER
   c) GPO
   d) FAIL SAFE PRE DRIVER
3. ADC Controller Logic

If Logic BIST runs the logic under test and the SPI registers related to these digital blocks are not available and reset to its default values at Logic Bist Exit.

Microcontroller can activate Logic bist setting the bit LOGIC BIST RUN = 1 in the register BIST_CTRL. After that, the Logic Under Test is in BIST mode: the sequential cells are

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reconfigured as scan chains in order to be tested by an internal bist controller. Once µC sets LOGIC BIST RUN =1 it can perform a polling on BIST_CTRL register (bit 1:0) in order to read the status of Logic Bist Test.

"01" means BIST RUNNING

"10" BIST PASSED

"11" BIST FAILED

"00" BIST STOPPED

If BIST STATUS is "10" (or "11") the Logic Bist test is finished and passed (or failed).

Microcontroller can write LOGIC BIST RUN = 0 to exit from BIST mode at Logic Bist end (PASSED or FAILED) but also during the test (BIST RUNNING).

Once LOGIC BIST RUN is set from 1 to 0 the logic under test and SPI registers are reset to the default condition.

The IC does not take actions if the Logic Bist Test fails. The decision to enable/disable the drivers and WSS is however given to the µC.

Table 59. Logic Bist

Symbol	Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
T_{BIST}	Duration of digital BIST	Design Information	4.8	5.15	5.5	ms

7.8.2 Analog Bist

Analog BIST is performed periodically during normal operation on the overvoltage and undervoltage monitors of VDD, VINTA, VBST, VPREREG, VCORE, VCOREFDBK, VCC, VCC5 and Tracking regulators and open of GNDD. In case of ABIST fail, the failing comparator reports overvoltage or undervoltage or POR is asserted in case of GNDD open.

7.8.3 OTP check

In each power up cycle (POR transition from low to high) the content of internal OTP is checked. Parity bits have been implemented to monitor the change of state of the trimming bits. In case check is not completed or not passed a dedicated fault bit is set (OTP_STABLE bit of ADV_CONFIG register).

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8 Serial Peripheral Communication

The SPI interface is used to configure the device, control the output and read the diagnostic and output status registers.

The SPI protocol is defined by frames of 32 bits with 3 bits of CRC (Cyclic Redundancy Check) both in input and output directions.

Every time the device sets a Clear on Read bit in one of the SPI registers (for example when an error is detected), such a bit will not be cleared until the corresponding register is read via SPI. The bit will not be reset if an SPI error occurs during the access to the register by the microcontroller or while L9396 sends the content of the register as an answer.

8.1 CRC Field Details

SPI frame (upstream/downstream) includes a 3-bit CRC field. CRC field is evaluated /checked in MISO by using a three-degree poly G3(x) = x3+x+1 and covers the bits 0:28 in the SPI frame. In MOSI, instead, the CRC is calculated in a different way. The expected SDO CRC value (E2, E1, E0), calculated over bits 0 to 28 according to the third-degree polynomial G3(x) = x3+x+1, must be modified using the formula (E1 xor E2, E0, E1).

CRC flops are initialized to 0 at the beginning of the SPI frame.

8.2 SPI frame

Bit 0 to 15	Bit 16 to 31
SDI	
Frame 0	Frame 1
SDO	
Frame 0	Frame 1

SDI

FRAME 0															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
W/R	ADD							0	DATA[19..13]						

FRAME 1															
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DATA[12..0]													CRC[2..0]		

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0 : Write/Read
1...7 : Address
8 : '0'
9...28 : Data
29...31: CRC

SDO

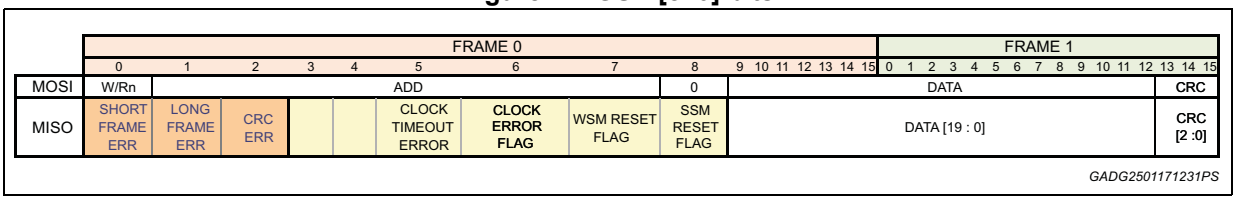
FRAME 0															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GSW[8..0]									DATA[19..13]						

FRAME 1															
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DATA[12..0]													CRC[2..0]		

0…8 : SPI error
9...28 : Data
29...31: CRC

The GSW[8..0] bits are mapped as in the following figure:

Figure 24. GSW[8..0] bits



0: Short Frame Error (less than 32 bits received in the last frame)
1: Long Frame Error (more than 32 bits received in the last frame)
2: CRC Error (wrong CRC received in the last frame)
3:4: '00'
5: Clock Timeout Error (Oscillator stuck, RO)
6: Clock Error Flag / CLOCKFRERR (1st or 2nd oscillator with a wrong frequency, R/C)
7: WSM Reset Flag (R/C)
8: SSM Reset Flag (R/C)

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8.3 SPI registers

The register table is on 10 pages containing 16 registers each. Address 3 MSBs indicate page selection, the remaining address 4 LSBs indicates the register.

Maximum word length of registers is 20 bits.

The bits ***colored in gray*** are called safe registers.

After the safe registers set has been written, the MCU sends a lock frame writing the lock word h-AAAAA into the write-protection register (address b-1000010).

From now on, it's mandatory to write consecutively the unlock words h-55555 (first access) and h-33333 (second access) into the write-protection register in order to write again the safe registers set.

The write-protection register echo (SDO) reports the lock-state: h-AAAAA in case of lock or h-55555 in case of unlock.

The write-protection register initial status is unlock.

The summary of the registers is defined in *Table 60*.

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Table 60. Registers summary

ADDRESS			Name	Description	Type	DATA																																	
BIN	Page [6:4]	REG [3:0]				19		18		17		16		15		14		13		12		11		10		9		8		7		6		5		4		3		2		1		0	
						W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R
0000000	0	0	RESERVED	NO OPERATION	N/A																																						
0000001	0	1	SYS_CONFIG_1	CONFIGURATION 1 TYPE = R/W	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	**BUCK OC LIMITATTION**: 0=LOW, 1=HIGH DEFAULT=0, RST = POR		**TEMPERATURE SENSOR** DISABLE DEFAULT = 0, RST = SSM RESET		**THERMAL PROT**. DISABLE DEFAULT = 0, RST = SSM RESET		-	-	-	-	**TRACK REGULATOR 1** SEL 1=VCC5 - **0=VCC** DEFAULT = 0, RST = SSM RESET		**TRACK REGULATOR 0** VOLTAGE SEL(1=VCC5 , **0=VCC)** DEFAULT = 0, RST = SSM RESET		**TRACK REGULATOR 1** ENABLE DEFAULT = 0, RST = SSM RESET		**TRACK REGULATOR 0** ENABLE DEFAULT = 0, RST = SSM RESET		**BOOST** ENABLE DEFAULT = 1, RST = SSM RESET		**BUCK** VOLTAGE SELECTION: 1 = 7V2V - **0 = 6V5** DEFAULT = 0, RST = SSM RESET	
0000010	0	2	SYS_CONFIG_2	CONFIGURATION 2 TYPE = R/W	R/W	**PUMP MOTOR SWITCHING TMR** 6µs=0, 12µs=1, 24µs=2, 48µs=3, 96µs=4, 192µs=5/6/7 DEFAULT = '0', RESET = SSM RESET						**PROTECTED BATTERY SWITCH** ENABLE DEFAULT = 1, RST = SSM RESET		**GPO DRIVER** RSU SEL [1:0] Range of values 0-3, WS ch 0-3 **DEFAULT = 00, RST = SSM RESET**		**GPO DRIVER** CONFIG [1:0] '00' WSO; '01' PWM MODE; '10' ON-OFF; '11' NOTHING **DEFAULT = 0, RST = SSM RESET**		**GPO DRIVER** ENABLE **DEFAULT = 0, RST = SSM RESET**		**PUMP MOTOR PRE DRIVER OVERLAP** TMR [4:0] (Range of values 0-23, 0.25-6µs; 24-31, 80µs) DEFAULT = 0000, RST = SSM RESET								**PUMP MOTOR PRE DRIVER** VDS SEL [1:0] DEFAULT = 00, RST = SSM RESET		**PUMP MOTOR PRE DRIVER** ENABLE DEFAULT = 0 , RST = SSM RESET		**FAIL SAFE DRIVER** VDS SEL [1:0] DEFAULT = 00, RST = SSM RESET		**FAIL SAFE DRIVER** ENABLE DEFAULT = 0, RST = SSM RESET	

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Table 60. Registers summary (continued)

ADDRESS			Name	Description	Type	DATA																																					
BIN	Page [6:4]	REG [3:0]				19		18		17		16		15		14		13		12		11		10		9		8		7		6		5		4		3		2		1		0	
						W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R
0000011	0	3	SYS_CONFIG_3	CONFIGURATION 3 TYPE = R/W	R/W	-	-	-	-	-	-	**GPO DRIVER** PWM DUTY CYCLE [7:0] DUTY % = GPO DRIVER PWM DUTY CYCLE [7:0] * 100 / 255 DEFAULT=127 , RST = SSM RESET																-	-	**GPO DRIVER** PWM PERIOD [7:0] PERIOD = 64µs * GPO DRIVER PWM PERIOD [7:0] + 1920 µs Range 0 – 214 , 521 Hz – 64Hz DEFAULT=92 , RST = SSM RESET																			
0000100	0	4	SUPPLY_CONTROL_1	SUPPLY CONTROL 1 DEFAULT = 0 , RESET POR (masked during power up) TYPE = C/R	R	-	**VCC** OVER TEMPERATURE	-	**VCC** OVER CURRENT	-	**VCC** OVER VOLTAGE	-	**VCC** UNDER VOLTAGE	-	**VCC5** OVER CURRENT	-	**VCC5** OVER VOLTAGE	-	**VCC5** UNDER VOLTAGE	-	1 - **VCORE** AS BUCK / 0 - VCORE AS LINEAR	-	**VCORE** OVER CURRENT	-	-	-	-	-	**VCORE** OVER VOLTAGE	-	-	**VCORE** UNDER VOLTAGE	-	-	-	**BUCK** OVER CURRENT	-	**BUCK** OVER TEMPERATURE	-	**BUCK** OVER VOLTAGE	-	**BUCK** UNDER VOLTAGE	-	**CP** OVER TEMPERATURE	-	**CP** LOW
0000101	0	5	SUPPLY_CONTROL_2	SUPPLY CONTROL 2 DEFAULT = 0 , RESET POR (masked during power up) TYPE = C/R (bits 19, 14:9, 3:0) TYPE = R/O (bits 7:6, 4)	R	-	-	**PREREG BUCK OFF LATCHED** (Read Only): 1=buck OFF; 0=buck ON		**VCORE OFF LATCHED** (Read Only): 1=VCORE OFF;0=VCORE ON		**VCORE MON ITOR TYPE** (Read Only): 1=VCORE; 0=VCOREFDB		**CP LOW 2**		-		**TRACK 1** OVER CURRENT		**TRACK 0** OVER CURRENT		**TRACK 1** OVER VOLTAGE		**TRACK 1** UNDER VOLTAGE		**TRACK 0** OVER VOLTAGE		**TRACK 0** UNDER VOLTAGE		**VCORE INTERNAL MON ITOR VOLTAGE** (Read Only) 0=3V; 1=5V		-	**BOOST** READY (Read Only)	-	**BOOST** KEPT OFF (Read Only)	-	-	-	-	-	**BOOST ON FLAG**	-	**BOOST** UNDER VOLTAGE	-	-	-	**BUCK** UNDER VOLTAGE	-	**BOOST** LOSS OF GROUND	-	**BOOST** OVER TEMPERATURE

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Table 60. Registers summary (continued)

ADDRESS			Name	Description	Type	DATA																																					
BIN	Page [6:4]	REG [3:0]				19		18		17		16		15		14		13		12		11		10		9		8		7		6		5		4		3		2		1		0	
						W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R
0000110	0	6	DRV_CONTROL 1	DRIVER CONTROL 1 DEFAULT = 0, RST = SSM RESET (bits 19:17) RST = POR (bits 15:0), (masked during power up) TYPE = R/W (bits 19:17) TYPE = R/C (bits 15:11, 6:0) TYPE = R/O (bits 10:7)	R/W	**PROTECTED BATTERY SWITCH** COMMAND DEFAULT = 0 , RESET = SSM RESET		**GPO DRIVER** COMMAND **DEFAULT = 0 , RESET = SSM RESET**		**FAIL SAFE DRIVE COMMAND** **DEFAULT = 0 , RESET = SSM RESET**		-	-	-	**FAILSAFE PRE DRIVER** VDS COMPARATOR	-	**PROTECTED BACTERY SWITCH** OVER CURRENT	-	**GPO DRIVER** OVER CURRENT	-	**GPO DRIVER** OPEN LOAD	-	**GPO DRIVER OVER** TEMPERATURE	-	**PUMP MOTOR PRE DRIVER** PDG	-	**PUMP MOTOR PRE DRIVER** PDI	-	**PUMP MOTOR PRE DRIVER** PRG	-	**PUMP MOTOR PRE DRIVER** PRI	-	**PUMP MOTOR PRE DRIVER** FLYBACK OPEN	-	**PUMP MOTOR PRE DRIVER** PDG OFF FAULT	-	**PUMP MOTOR PRE DRIVER** PDG ON FAULT	-	**PUMP MOTOR PRE DRIVER** PRG OFF FAULT	-	**PUMP MOTOR PRE DRIVER** PRG ON FAULT	-	**PUMP MOTOR PRE DRIVER** QPD OFF FAULT	-	**PUMP MOTOR PRE DRIVER** QPD ON FAULT	
0000111	0	7	POWER_ON	POWER ON TYPE = R/W	R/W	-	-	-	-	**SW RESET REQUEST** (SSM and WSM reset are generated)		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	**SPREAD SPECTRUM DISABLE MODE** DEFAULT = 0, RESET = SSM RESET		**POWER HOLD** BIT DEFAULT = 0, RESET = SSM RESET		**KEEP ALIVE** BIT (W/C)		

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Table 60. Registers summary (continued)

| ADDRESS | | | Name | Description | Type | DATA | | |

Table 60. Registers summary (continued)

| ADDRESS | | | Name | Description | Type | DATA | | |

Table 60. Registers summary (continued)

| ADDRESS | | | Name | Description | Type | DATA | | |

Table 60. Registers summary (continued)

| ADDRESS | | | Name | Description | Type | DATA | | |

Table 60. Registers summary (continued)

| ADDRESS | | | Name | Description | Type | DATA | | |

Table 60. Registers summary (continued)

ADDRESS			Name	Description	Type	DATA																																					
BIN	Page [6:4]	REG [3:0]				19		18		17		16		15		14		13		12		11		10		9		8		7		6		5		4		3		2		1		0	
						W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R
0110010	3	2	ADC CONV RES 2	ADC CONV RES 2 RESET SSM_RESET	R	VBST																																				AI 0			
0110011	3	3	ADC CONV RES 3	ADC CONV RES 3 RESET SSM_RESET	R	VCP																																				GPOD0			
0110100	3	4	ADC CONV RES 4	ADC CONV RES 4 RESET SSM_RESET	R	VB																																				VB_SW			
0110101	3	5	ADC CONV RES 5	ADC CONV RES 5 RESET SSM_RESET	R	VBM																																				VDBATT			
0110110	3	6	ADC CONV RES 6	ADC CONV RES 6 RESET SSM_RESET	R	VDS																																				PDS			
0110111	3	7	ADC CONV RES 7	ADC CONV RES 7 RESET SSM_RESET	R	IGN																																				WDTDIS			
0111000	3	8	ADC CONV RES 8	ADC CONV RES 8 RESET SSM_RESET	R	TEMPERATURE SENSOR																																				VPREREG			
0111001	3	9	ADC CONV RES 9	ADC CONV RES 9 RESET SSM_RESET	R	RSUH 3																																				RSUH 2			
0111010	3	10	ADC CONV RES 10	ADC CONV RES 10 RESET SSM_RESET	R	RSUH 1																																				RSUH 0			
0111011	3	11	ADC CONV RES 11	ADC CONV RES 11 RESET SSM_RESET	R	RSUL 3																																				RSUL 2			
0111100	3	12	ADC CONV RES 12	ADC CONV RES 12 RESET SSM_RESET	R	RSUL 1																																				RSUL 0			
0111101	3	13	ADC CONV RES 13	ADC CONV RES 13 RESET SSM_RESET	R	VCC5																																				VCC			
0111110	3	14	ADC CONV RES 14	ADC CONV RES 14 RESET SSM_RESET	R	VCORE																																				SCORE			
0111111	3	15	ADC CONV RES 15	ADC CONV RES 15 RESET SSM_RESET	R	VINTD																																				VINTA			
1000000	4	0	ADC CONV RES 16	ADC CONV RES 16 RESET SSM_RESET	R	BGR																																				BGM			

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Table 60. Registers summary (continued)

| ADDRESS | | | Name | Description | Type | DATA | | |

8.4 SPI parameters

8.4.1 DC Electrical Parameters

The SPI interface is composed of:

- Supply: VCC
- Inputs: SCLK, SDI, CS
- Output: SDO

-40 °C ≤ T_j ≤ 175 °C unless otherwise specified.

Table 61. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VCC	SPI Dedicated Power Supply	Application note	3.0	-	5.5	V
V_{IL}	PRN Logic Input Low Voltage	-	-	-	0.75	V
V_{IH}	PRN Logic Input High Voltage	-	1.75	-	-	V
$V_{hysteresis}$	PRN Input hysteresis Voltage	-	0.1	-	1	V
PRNPD	PRN pull-down	PRN= 3.3V	10	-	100	µA
V_{IL}	SCLK Logic Input Low Voltage	-	-	-	0.75	V
V_{IH}	SCLK Logic Input High Voltage	-	1.75	-	-	V
$V_{hysteresis}$	SCLK Input hysteresis Voltage	-	0.1	-	1	V
SCLKPD	SCLK pull-down	SCLK = 3.3V	10	-	100	µA
V_{IL}	SDI Logic Input Low Voltage	-	-	-	0.75	V
V_{IH}	SDI Logic Input High Voltage	-	1.75	-	-	V
$V_{hysteresis}$	SDI Input hysteresis Voltage	-	0.1	-	1	V
SDIPU	SDI pull-up	SDI = 0V	-100	-	-10	µA
V_{IL}	CS Logic Input Low Voltage	-	-	-	0.75	V
V_{IH}	CS Logic Input High Voltage	-	1.75	-	-	V
$V_{hysteresis}$	CS Input hysteresis Voltage	-	0.1	-	1	V
CSPU	CS pull-up to internal logic supply	CS = 0V	-100	-	-10	µA
V_{OL}	SDO Logic Output Low Voltage	Isource = 1mA	-	-	0.4	V
V_{OH}	SDO Logic Output High Voltage	Isink = 1mA	VCC-0.4	-	-	V
Ileak	SDO Tristate leakage current	CS high 0<SDO<VCC-0.1V	-3	-	3	µA

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8.4.2 AC electrical parameters

Figure 25. SPI timing diagram

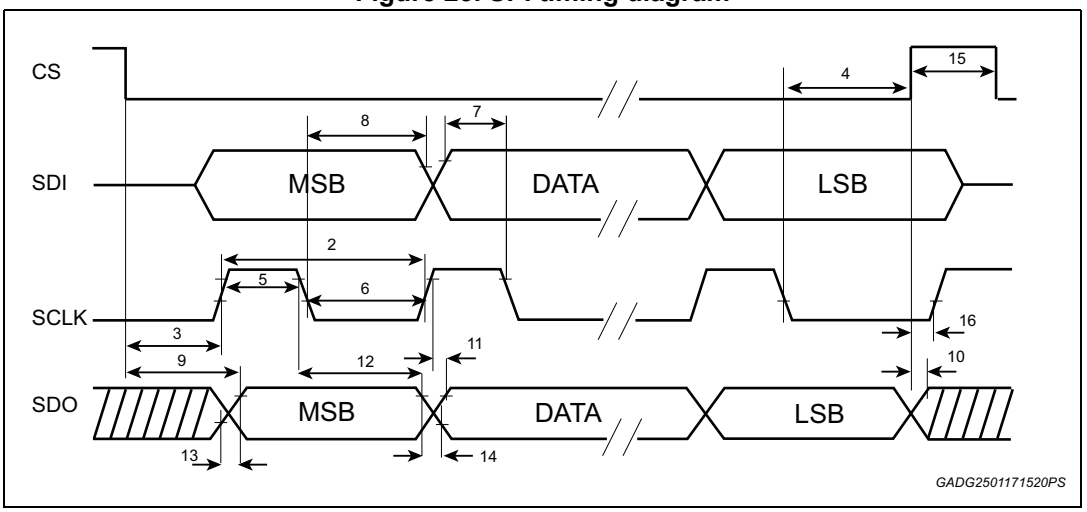


Table 62. SPI timing characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	note
fop	Transfer Frequency	Design Information	-	-	6	MHz	SCLK
tsclk	SCLK Period (2)	Design Information	167	-	-	ns	SCLK
tlead	Enable Lead Time (3)	Design Information	750	-	-	ns	SCLK
tlag	Enable Lag Time (4)	Design Information	100	-	-	ns	SCLK, CS
tsclkhs	SCLK High Time (5)	Design Information	75	-	-	ns	SCLK
tsclkls	SCLK Low Time (6)	Design Information	75	-	-	ns	SCLK
tsus	SDI Input Setup Time (7)	Design Information	30	-	-	ns	SDI
ths	SDI Input Hold Time (8)	Design Information	30	-	-	ns	SDI
ta	SDO Access Time (9)	50pF load	-	-	100	ns	SDO
tdis	SDO Disable Time (10)	50pF load	-	-	100	ns	SDO
tvs	SDO Output Valid Time (11)	50pF load	-	-	70	ns	SDO
tho	SDO Output Hold Time (12)	50pF load	10	-	-	ns	SDO
tr	SDO Rise Time (13)	50pF load	-	-	50	ns	SDO
tf	SDO Fall Time (14)	50pF load	-	-	50	ns	SDO
tcsn	CS Negated Time (15)	Design Information	750	-	-	ns	CS
tsh	SCLK Hold Time (16)	Design Information	100	-	-	ns	SCLK

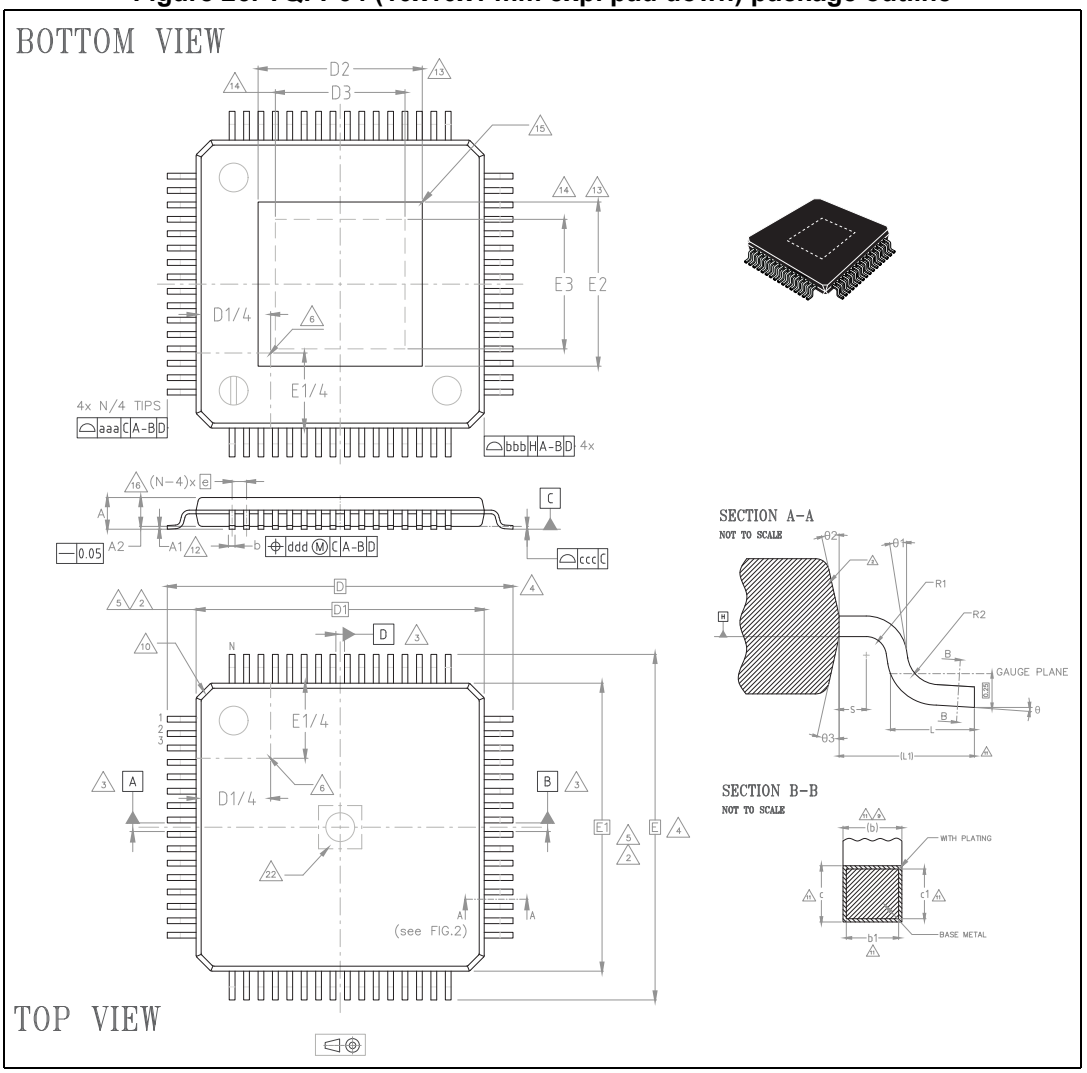
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9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

9.1 TQFP64 (10x10x1 mm exp. pad down) package information

Figure 26. TQFP64 (10x10x1 mm exp. pad down) package outline



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Table 63. TQFP64 (10x10x1 mm exp. pad down) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	3.5°	6°	0°	3.5°	6°
Θ1	0°	-	-	0°	-	-
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
A	-	-	1.20	-	-	0.0472
A1	0.05	-	0.15	0.002	-	0.0059
A2	0.95	1.0	1.05	0.0374	0.0394	0.0413
b	0.17	0.22	0.27	0.0067	0.0079	0.0091
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.09	-	0.20	0.0354	-	0.0079
c1	0.09	-	0.16	0.0354	-	0.0063
D	-	12.00 BSC	-	-	0.4724 BSC	-
D1[2]	-	10.00 BSC	-	-	0.3937 BSC	-
D2	VARIATION					
e	-	0.50 BSC	-	-	0.0197 BSC	-
E	-	12.00 BSC	-	-	0.4724 BSC	-
E1 [2]	-	10.00 BSC	-	-	0.3937 BSC	-
E2	VARIATION					
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00 REF	-	-	0.0394 REF	-
N	-	64.00	-	-	2.5197	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
TOLERANCE OF FORM AND POSITION						
aaa	-	0.20	-	-	0.0079	-
bbb	-	0.20	-	-	0.0079	-
ccc	-	0.08	-	-	0.0031	-
ddd	-	0.07	-	-	0.0028	-

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Table 63. TQFP64 (10x10x1 mm exp. pad down) package mechanical data (continued)

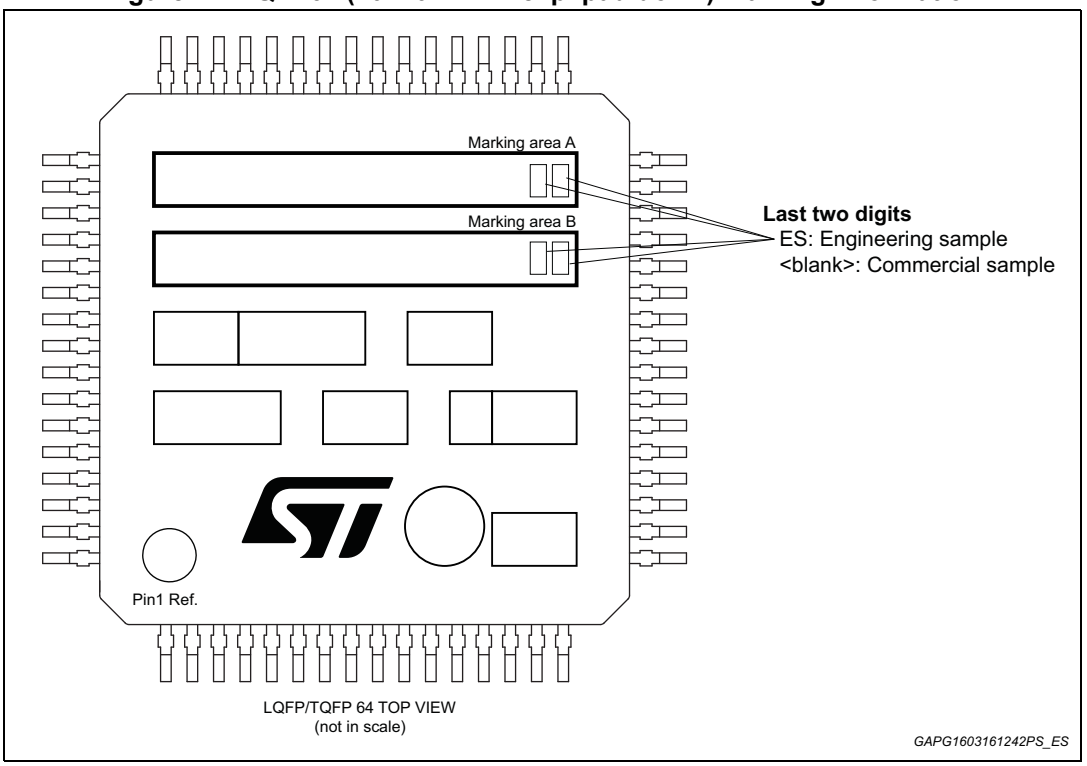
Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
VARIATIONS[3]						
Option A						
D2	-	4.50	-	-	0.1772	-
E2	-	4.50	-	-	0.1772	-
Option B						
D2	-	6.0	-	-	0.2362	-
E2	-	6.0	-	-	0.2362	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D1 and E1 do not include mold flash or protrusions.
   Allowable mold flash or protrusion is “0.25 mm” per side.
3. L9396 mounts option A: 4.5x4.5 die pad.

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9.2 TQFP64 (10x10x1 mm exp. pad down) marking information

Figure 27. TQFP64 (10x10x1 mm exp. pad down) marking information



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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10 Revision history

Table 64. Document revision history

Date	Revision	Changes
06-Apr-2018	1	Initial release.
27-Sep-2019	2	Updated: – Table 5: Configuration and control DC specifications; – Table 6: Boost regulator electrical characteristics; – Table 10: VPREREG buck regulator; – Table 45: Analog to digital converter; – Table 54: WD2 characteristics; – Table 57: Fail safe output. Minor text changes.
12-Nov-2020	3	Updated: – Table 54: WD2 characteristics; – Section : Features; – Section 7.4.1: Watchdog (WD1); – Section 8.2: SPI frame (SDI and SDO FRAME1); – Section 9.1: TQFP64 (10x10x1 mm exp. pad down) package information.
19-Jul-2021	4	Minor text changes in Section 3.7: VCORE regulator (GCORE resistor value).
01-Dec-2021	5	Typo corrections.
25-Jan-2022	6	Added Note in Section 3.6: VPREREG buck regulator.
08-Nov-2022	7	Updated Section 3.7: VCORE regulator.
08-May-2023	8	Minor text changes in Table 41: WSS configuration.
27-Jun-2024	9	Updated Table 41: WSS configuration. Minor text changes in: – Section 3.7: VCORE regulator; – Section 4.3: Pump motor diagnostics; – Section 5.1.1: Wheel speed data register formats.
29-Jul-2025	10	Added new L9396-TR order code in cover page.
10-Apr-2026	11	Added IGN rise time parameter in *Table 8* and note in *Section 3.6*. Updated *Section 3.11*, *Figure 6* and *Section 8.1*. Minor text change.

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