

ADuM130D/ADuM130E/ADuM131D/ADuM131E

3.0 kV RMS/3.75 kV RMS Triple-Channel Digital Isolators

FEATURES

- ▶ High common-mode transient immunity: 100 kV/μs
- ▶ High robustness to radiated and conducted noise
- ▶ Low propagation delay: 13 ns maximum for 5 V operation, 15 ns maximum for 1.8 V operation
- ▶ 150 Mbps maximum guaranteed data rate
- ▶ [Safety and regulatory approvals](#) (pending)
 - ▶ R-16 [SOIC_N] Package
 - ▶ UL 1577
 - ▶ $V_{ISO} = 3000$ V rms for 1 minute
 - ▶ IEC/EN/CSA 60950-1
 - ▶ IEC/CSA 60601-1
 - ▶ IEC/CSA 61010-1
 - ▶ CQC GB 4943.1 (pending)
 - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
 - ▶ $V_{IORM} = 849$ V_{PEAK}
 - ▶ RW-16 [SOIC_W] Package
 - ▶ UL 1577
 - ▶ $V_{ISO} = 3750$ V rms for 1 minute
 - ▶ IEC/EN/CSA 62368-1
 - ▶ IEC/CSA 60601-1
 - ▶ IEC/CSA 61010-1
 - ▶ CQC GB 4943.1 (pending)
 - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
 - ▶ $V_{IORM} = 849$ V_{PEAK}
- ▶ Backward compatibility
 - ▶ ADuM130E1/ADuM131E1 pin-compatible with [ADuM1300/ADuM1301](#)
- ▶ Low dynamic power consumption
- ▶ 1.8 V to 5 V level translation
- ▶ High temperature operation: 125°C
- ▶ Fail-safe high or low options
- ▶ 16-lead, RoHS compliant, SOIC package

APPLICATIONS

- ▶ General-purpose multichannel isolation
- ▶ Serial peripheral interface (SPI)/data converter isolation
- ▶ Industrial field bus isolation

FUNCTIONAL BLOCK DIAGRAMS

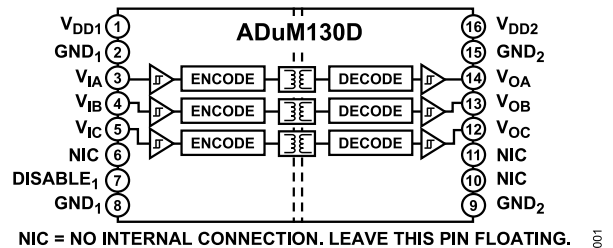


Figure 1. ADuM130D Functional Block Diagram

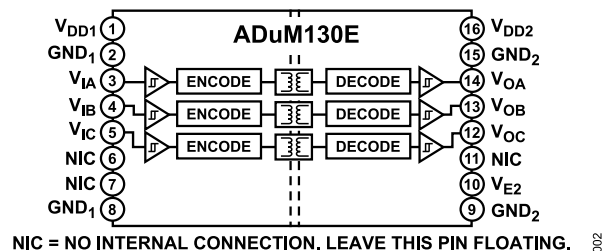


Figure 2. ADuM130E Functional Block Diagram

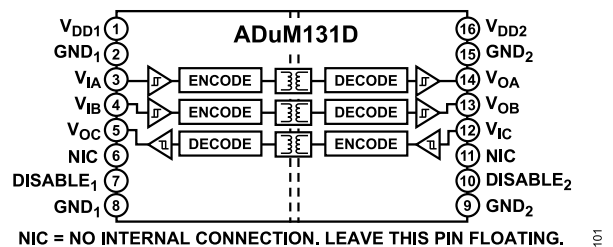


Figure 3. ADuM131D Functional Block Diagram

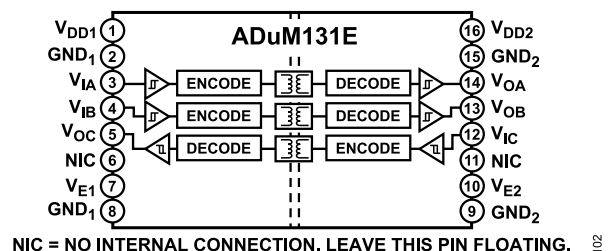


Figure 4. ADuM131E Functional Block Diagram

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REVISION HISTORY**11/2024—Rev. A to Rev. B**

Changes to Features Section.....	1
Changes to Table 9 and Table 10.....	10
Changes to Regulatory Information Section, Table 12, and Table 13.....	11
Changes to Table 14 and Table 15.....	12
Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE V 0884-17) Insulation Characteristics Section.....	12
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Changes to Figure 5 Caption and Figure 6 Caption.....	13
Deleted Table 18 and Table 19; Renumbered Sequentially	14
Deleted Insulation Lifetime Section, Surface Tracking Section, Insulation Wear Out Section, Calculation and Use of Parameters Example Section, and Figure 22; Renumbered Sequentially	20

GENERAL DESCRIPTION

The ADuM130D/ADuM130E/ADuM131D/ADuM131E¹ are triple-channel digital isolators based on Analog Devices, Inc., iCoupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 3 ns at 5 V operation. Channel matching is tight at 3.0 ns maximum.

The ADuM130D/ADuM130E/ADuM131D/ADuM131E data channels are independent and are available in a variety of configurations

with a withstand voltage rating of 3.0 kV rms or 3.75 kV rms (see the [Ordering Guide](#)). The devices operate with the supply voltage on either side ranging from 1.8 V to 5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available, in which the outputs transition to a pre-determined state when the input power supply is not applied or the inputs are disabled. The ADuM130E1/ADuM131E1 are pin-compatible with the [ADuM1300/ADuM1301](#).

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range of $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate ¹		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL} , t_{PLH}	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter			630		ps p-p	See the Jitter Measurement section
			80		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DDX}$			V	
Logic Low	V_{IL}			$0.3 \times V_{DDX}$	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OX}^2 = -20\text{ }\mu\text{A}$, $V_{IX} = V_{IXH}^3$
		$V_{DDX} - 0.4$	$V_{DDX} - 0.2$		V	$I_{OX}^2 = -4\text{ mA}$, $V_{IX} = V_{IXH}^3$
Logic Low	V_{OL}		0.0	0.1	V	$I_{OX}^2 = 20\text{ }\mu\text{A}$, $V_{IX} = V_{IXL}^4$
			0.2	0.4	V	$I_{OX}^2 = 4\text{ mA}$, $V_{IX} = V_{IXL}^4$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IX} \leq V_{DDX}$
V_{E2} Enable Input Pull-Up Current	I_{PU}	-10	-3		μA	$V_{E2} = 0\text{ V}$
DISABLE ₁ Input Pull-Down Current	I_{PD}		9	15	μA	DISABLE ₁ = V_{DDX}
Tristate Output Current per Channel	I_{OZ}	-10	+0.01	+10	μA	$0\text{ V} \leq V_{OX} \leq V_{DDX}$
Quiescent Supply Current						
ADuM130D/ADuM130E						
	$I_{DD1(Q)}$		1.35	2.6	mA	$V_I^5 = 0\text{ (E0, D0), 1 (E1, D1)}^6$
	$I_{DD2(Q)}$		1.73	2.9	mA	$V_I^5 = 0\text{ (E0, D0), 1 (E1, D1)}^6$
	$I_{DD1(Q)}$		9.7	15.2	mA	$V_I^5 = 1\text{ (E0, D0), 0 (E1, D1)}^6$
	$I_{DD2(Q)}$		1.87	3.0	mA	$V_I^5 = 1\text{ (E0, D0), 0 (E1, D1)}^6$
ADuM131D/ADuM131E						
	$I_{DD1(Q)}$		1.62	2.7	mA	$V_I^5 = 0\text{ (E0, D0), 1 (E1, D1)}^6$
	$I_{DD2(Q)}$		1.61	2.8	mA	$V_I^5 = 0\text{ (E0, D0), 1 (E1, D1)}^6$
	$I_{DD1(Q)}$		7.4	11.4	mA	$V_I^5 = 1\text{ (E0, D0), 0 (E1, D1)}^6$
	$I_{DD2(Q)}$		5.34	7.2	mA	$V_I^5 = 1\text{ (E0, D0), 0 (E1, D1)}^6$
Dynamic Supply Current						
Dynamic Input	$I_{DDI(D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO(D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDX} Threshold	V_{DDXUV+}		1.6		V	
Negative V_{DDX} Threshold	V_{DDXUV-}		1.5		V	

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
V_{DDX} Hysteresis	V_{DDXUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity ⁷	$ CM_H $	75	100		kV/ μ s	$V_{IX} = V_{DDX}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ μ s	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{OX} is the Channel x output current, where x = A, B, or C.

³ V_{IXH} is the input side logic high.

⁴ V_{IXL} is the input side logic low.

⁵ V_I is the voltage input.

⁶ E0 refers to the ADuM130E0/ADuM131E0 models, D0 refers to the ADuM130D0/ADuM131D0 models, E1 refers to the ADuM130E1/ADuM131E1 models, and D1 refers to the ADuM130D1/ADuM131D1 models. See the [Ordering Guide](#) section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDX} . $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OX} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM130D/ADuM130E											
Supply Current Side 1	I _{DD1}		5.6	9.0		6.3	9.8		9.4	14.3	mA
Supply Current Side 2	I _{DD2}		1.9	3.7		3.1	4.9		6.8	10	mA
ADuM131D/ADuM131E											
Supply Current Side 1	I _{DD1}		4.6	7.2		5.5	8.3		8.8	11.9	mA
Supply Current Side 2	I _{DD2}		3.6	5.8		4.6	6.8		8.0	11.3	mA

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3$ V. Minimum/maximum specifications apply over the entire recommended operation range: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate ¹		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL} , t_{PLH}	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			640		ps p-p	See the Jitter Measurement section

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
			75		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DDx}$			V	
Logic Low	V_{IL}			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox}^2 = -20 \mu A$, $V_{Ix} = V_{IxH}^3$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox}^2 = -2 \text{ mA}$, $V_{Ix} = V_{IxH}^3$
Logic Low	V_{OL}		0.0	0.1	V	$I_{Ox}^2 = 20 \mu A$, $V_{Ix} = V_{IxL}^4$
			0.2	0.4	V	$I_{Ox}^2 = 2 \text{ mA}$, $V_{Ix} = V_{IxL}^4$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0 \text{ V} \leq V_{Ix} \leq V_{DDx}$
V_{E2} Enable Input Pull-Up Current	I_{PU}	-10	-3		μA	$V_{E2} = 0 \text{ V}$
DISABLE ₁ Input Pull-Down Current	I_{PD}		9	15	μA	DISABLE ₁ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	-10	+0.01	+10	μA	$0 \text{ V} \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM130D/ADuM130E						
	$I_{DD1} (Q)$		1.25	2.5	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD2} (Q)$		1.65	2.8	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD1} (Q)$		9.57	15.0	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
	$I_{DD2} (Q)$		1.79	2.9	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
ADuM131D/ADuM131E						
	$I_{DD1} (Q)$		1.52	2.6	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD2} (Q)$		1.52	2.6	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD1} (Q)$		7.28	11.3	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
	$I_{DD2} (Q)$		5.24	7.1	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
Dynamic Supply Current						
Dynamic Input	$I_{DDI} (D)$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO} (D)$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity ⁷	$ CM_H $	75	100		kV/ μs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ μs	$V_{Ix} = 0 \text{ V}$, $V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{Ox} is the Channel x output current, where x = A, B, or C.

³ V_{IxH} is the input side logic high.

⁴ V_{IxL} is the input side logic low.

⁵ V_I is the voltage input.

⁶ E0 refers to the ADuM130E0/ADuM131E0 models, D0 refers to the ADuM130D0/ADuM131D0 models, E1 refers to the ADuM130E1/ADuM131E1 models, and D1 refers to the ADuM130D1/ADuM131D1 models. See the [Ordering Guide](#) section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx} . $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

Table 4. Total Supply Current vs. Data Throughput

Table 10. Total Supply Current for Data Rate Output											
Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM130D/ADuM130E											
Supply Current Side 1	I _{DD1}		5.4	8.8		6.0	9.4		8.5	12.7	mA
Supply Current Side 2	I _{DD2}		1.8	3.6		2.9	4.7		6.2	8.4	mA
ADuM131D/ADuM131E											
Supply Current Side 1	I _{DD1}		4.4	7.1		5.2	8.0		8.1	10.7	mA
Supply Current Side 2	I _{DD2}		3.4	5.6		4.3	6.5		7.4	9.5	mA

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$, $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate ¹		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL} , t_{PLH}	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/ $^\circ\text{C}$	
Propagation Delay Skew	t_{PSK}			6.8	ns	Between any two devices at the same temperature, voltage, load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			770		ps p-p	See the Jitter Measurement section
			160		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DDx}$			V	
Logic Low	V_{IL}			$0.3 \times V_{DDx}$	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox}^2 = -20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxH}^3$
		$V_{DDx} - 0.4$	$V_{DDx} - 0.2$		V	$I_{Ox}^2 = -2\text{ mA}$, $V_{Ix} = V_{IxH}^3$
Logic Low	V_{OL}		0.0	0.1	V	$I_{Ox}^2 = 20\text{ }\mu\text{A}$, $V_{Ix} = V_{IxL}^4$
			0.2	0.4	V	$I_{Ox}^2 = 2\text{ mA}$, $V_{Ix} = V_{IxL}^4$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
V_{E2} Enable Input Pull-Up Current	I_{PU}	-10	-3		μA	$V_{E2} = 0\text{ V}$
DISABLE ₁ Input Pull-Down Current	I_{PD}		9	15	μA	DISABLE ₁ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	-10	+0.01	+10	μA	$0\text{ V} \leq V_{Ox} \leq V_{DDx}$
Quiescent Supply Current						
ADuM130D/ADuM130E						
	$I_{DD1(Q)}$		1.2	2.4	mA	$V_I^5 = 0\text{ (E0, D0), 1 (E1, D1)}^6$
	$I_{DD2(Q)}$		1.61	2.7	mA	$V_I^5 = 0\text{ (E0, D0), 1 (E1, D1)}^6$
	$I_{DD1(Q)}$		9.52	14.9	mA	$V_I^5 = 1\text{ (E0, D0), 0 (E1, D1)}^6$
	$I_{DD2(Q)}$		1.76	2.8	mA	$V_I^5 = 1\text{ (E0, D0), 0 (E1, D1)}^6$

SPECIFICATIONS

Table 5. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM131D/ADuM131E	I_{DD1} (Q)		1.47	2.5	mA	$V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶
	I_{DD2} (Q)		1.48	2.5	mA	$V_I^5 = 0$ (E0, D0), 1 (E1, D1) ⁶
	I_{DD1} (Q)		7.23	11.2	mA	$V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶
	I_{DD2} (Q)		5.19	7.0	mA	$V_I^5 = 1$ (E0, D0), 0 (E1, D1) ⁶
Dynamic Supply Current						
Dynamic Input	I_{DDI} (D)		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	I_{DDO} (D)		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive V_{DDX} Threshold	V_{DDXUV+}		1.6		V	
Negative V_{DDX} Threshold	V_{DDXUV-}		1.5		V	
V_{DDX} Hysteresis	V_{DDXUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity ⁷	$ CM_H $	75	100		kV/ μ s	$V_{IX} = V_{DDX}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ μ s	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V

¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

² I_{OX} is the Channel x output current, where x = A, B, or C.

³ V_{IXH} is the input side logic high.

⁴ V_{IXL} is the input side logic low.

⁵ V_I is the voltage input.

⁶ E0 refers to the ADuM130E0/ADuM131E0 models, D0 refers to the ADuM130D0/ADuM131D0 models, E1 refers to the ADuM130E1/ADuM131E1 models, and D1 refers to the ADuM130D1/ADuM131D1 models. See the [Ordering Guide](#) section.

⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDX} . $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OX} > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM130E/ADuM130D											
Supply Current Side 1	I _{DD1}		5.3	8.7		5.9	9.3		8.2	12.3	mA
Supply Current Side 2	I _{DD2}		1.8	3.6		2.6	4.4		5.2	7.4	mA
ADuM131E/ADuM131D											
Supply Current Side 1	I _{DD1}		4.4	7.1		5.0	7.8		7.5	10.1	mA
Supply Current Side 2	I _{DD2}		3.4	5.6		4.1	6.3		6.6	8.7	mA

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 1.8$ V. Minimum/maximum specifications apply over the entire recommended operation range: $1.7\text{ V} \leq V_{DD1} \leq 1.9\text{ V}$, $1.7\text{ V} \leq V_{DD2} \leq 1.9\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						

SPECIFICATIONS

Table 7. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate ¹		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL} , t_{PLH}	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two devices at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			600		ps p-p	See the Jitter Measurement section
			90		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DDX}$			V	
Logic Low	V_{IL}			$0.3 \times V_{DDX}$	V	
Output Voltage						
Logic High	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OX}^2 = -20 \mu A$, $V_{IX} = V_{IXH}^3$
		$V_{DDX} - 0.4$	$V_{DDX} - 0.2$		V	$I_{OX}^2 = -2 \text{ mA}$, $V_{IX} = V_{IXH}^3$
Logic Low	V_{OL}		0.0	0.1	V	$I_{OX}^2 = 20 \mu A$, $V_{IX} = V_{IXL}^4$
			0.2	0.4	V	$I_{OX}^2 = 2 \text{ mA}$, $V_{IX} = V_{IXL}^4$
Input Current per Channel	I_I	-10	+0.01	+10	μA	$0 \text{ V} \leq V_{IX} \leq V_{DDX}$
V_{E2} Enable Input Pull-Up Current	I_{PU}	-10	-3		μA	$V_{E2} = 0 \text{ V}$
DISABLE ₁ Input Pull-Down Current	I_{PD}		9	15	μA	DISABLE ₁ = V_{DDX}
Tristate Output Current per Channel	I_{OZ}	-10	+0.01	+10	μA	$0 \text{ V} \leq V_{OX} \leq V_{DDX}$
Quiescent Supply Current						
ADuM130D/ADuM130E						
	$I_{DD1} (Q)$		1.15	2.3	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD2} (Q)$		1.58	2.6	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD1} (Q)$		9.41	14.8	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
	$I_{DD2} (Q)$		1.72	2.7	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
ADuM131D/ADuM131E						
	$I_{DD1} (Q)$		1.42	2.4	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD2} (Q)$		1.44	2.4	mA	$V_I^5 = 0 (E0, D0), 1 (E1, D1)^6$
	$I_{DD1} (Q)$		7.15	11.1	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
	$I_{DD2} (Q)$		5.13	6.9	mA	$V_I^5 = 1 (E0, D0), 0 (E1, D1)^6$
Dynamic Supply Current						
Dynamic Input	$I_{DDI} (D)$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO} (D)$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDX} Threshold	V_{DDXUV+}		1.6		V	
Negative V_{DDX} Threshold	V_{DDXUV-}		1.5		V	
V_{DDX} Hysteresis	V_{DDXUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity ⁷	$ CM_H $	75	100		kV/ μs	$V_{IX} = V_{DDX}$, $V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V
	$ CM_L $	75	100		kV/ μs	$V_{IX} = 0 \text{ V}$, $V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V

SPECIFICATIONS

- ¹ 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.
- ² I_{Ox} is the Channel x output current, where x = A, B, or C.
- ³ $V_{I\text{H}}$ is the input side logic high.
- ⁴ $V_{I\text{L}}$ is the input side logic low.
- ⁵ V_I is the voltage input.
- ⁶ E0 refers to the ADuM130E0/ADuM131E0 models, D0 refers to the ADuM130D0/ADuM131D0 models, E1 refers to the ADuM130E1/ADuM131E1 models, and D1 refers to the ADuM130D1/ADuM131D1 models. See the [Ordering Guide](#) section.
- ⁷ $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) $> 0.8 V_{DDx}$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{Ox} > 0.8 V$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

Table 1. Total Supply Current for Data Throughput											
Parameter	Symbol	1 Mbps			25 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SUPPLY CURRENT											
ADuM130D/ADuM130E											
Supply Current Side 1	I _{DD1}		5.2	8.6		5.8	9.3		8.1	12.2	mA
Supply Current Side 2	I _{DD2}		1.7	3.5		2.5	4.3		5.2	7.3	mA
ADuM131D/ADuM131E											
Supply Current Side 1	I _{DD1}		4.3	7.0		4.9	7.7		7.26	10.0	mA
Supply Current Side 2	I _{DD2}		3.3	5.5		4.0	6.2		6.5	8.6	mA

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 9. R-16 Narrow Body [SOIC_N] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

Table 10. RW-16 Wide Body [SOIC_W] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

SPECIFICATIONS

PACKAGE CHARACTERISTICS

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) ¹	R _{I-O}		10 ¹³		Ω	f = 1 MHz
Capacitance (Input to Output) ¹	C _{I-O}		2.2		pF	
Input Capacitance ²	C _I		4.0		pF	
IC Junction to Ambient Thermal Resistance						
R-16 Narrow Body [SOIC_N] Package	θ _{JA}		76		°C/W	Thermocouple located at center of package underside
RW-16 Wide Body [SOIC_W] Package	θ _{JA}		45		°C/W	Thermocouple located at center of package underside

¹ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM130D/ADuM130E/ADuM131D/ADuM131E is approved or pending approval by the organizations in [and Table 13](#).

Table 12. R-16 Narrow Body [SOIC_N] Package

UL	CSA	VDE	CQC
UL 1577 ¹ Single Protection, 3000 V rms	IEC/EN/CSA 60950-1 Basic insulation, 400 V rms Reinforced insulation, 200 V rms IEC/CSA 60601-1 Reinforced Insulation (2 MOPP), 250 V rms IEC/CSA 61010-1 Basic insulation, 300 V rms, overvoltage category IV Reinforced insulation, 300 V rms	DIN EN IEC 60747-17 (VDE 0884-17) ² Reinforced insulation, 565 V peak	CQC GB4943.1 Basic insulation, 400 V rms
File E214100	File No. 205078	Certificate No. 40051926	Certificate No. CQC16001160842

¹ In accordance with UL 1577, each ADuM130D/ADuM130E/ADuM131D/ADuM131E in the R-16 narrow body [SOIC_N] package is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

² In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM130D/ADuM130E/ADuM131D/ADuM131E in the R-16 narrow body [SOIC_N] package is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 13. RW-16 Wide Body [SOIC_W] Package

UL	CSA	VDE	CQC
UL 1577 ¹ Single Protection, 3750 V rms	IEC/EN/CSA 62368-1 Basic insulation, 780 V rms Reinforced insulation, 390 V rms IEC/CSA 60601-1 Reinforced insulation (2 MOPP), 237.5 V rms IEC/CSA 61010-1 Basic insulation, 600 V rms, overvoltage category III Reinforced insulation, 300 V rms	DIN EN IEC 60747-17 (VDE 0884-17) ² Reinforced insulation, 565 V peak	CQC GB4943.1 Basic Insulation, 760 V rms Reinforced Insulation, 380 V rms
File E214100	File No. 205078	Certificate No. 40051926	Certificate No. CQC16001160842

SPECIFICATIONS

- ¹ In accordance with UL 1577, each ADuM130D/ADuM130E/ADuM131D/ADuM131E in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.
- ² In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM130D/ADuM130E/ADuM131D/ADuM131E in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

DIN EN IEC 60747-17 (VDE V 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 14. R-16 Narrow Body [SOIC_N] Package

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1			I to IV	
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 600 V rms			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Repetitive Isolation Voltage		V_{IORM}	565	V peak
Maximum Working Insulation Voltage		V_{IOWM}	400	V rms
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1059	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	904	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	V peak
Maximum Transient Isolation Voltage		V_{IOTM}	4200	V peak
Maximum Impulse Voltage	Tested in air, 1.2 μ s/50 μ s waveform per IEC 61000-4-5	V_{IMP}	4200	V _{PEAK}
Maximum Surge Isolation Voltage	Tested in oil, 1.2 μ s/50 μ s waveform per IEC 61000-4-5, $V_{TEST} = V_{IMP} \times 1.3$ or ≥ 10 kV	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.64	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

Table 15. RW-16 Wide Body [SOIC_W] Package

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1			I to IV	
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 600 V rms			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Repetitive Isolation Voltage		V_{IORM}	565	V peak
Maximum Working Insulation Voltage		V_{IOWM}	400	V rms
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1059	V peak
Input to Output Test Voltage, Method A		$V_{pd(m)}$		

SPECIFICATIONS

Table 15. RW-16 Wide Body [SOIC_W] Package (Continued)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		904	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		678	V peak
Maximum Transient Isolation Voltage		V_{IOTM}	5300	V peak
Maximum Impulse Voltage	Tested in air, 1.2 μ s/50 μ s waveform per IEC 61000-4-5	V_{IMP}	5300	V _{PEAK}
Maximum Surge Isolation Voltage	Tested in oil, 1.2 μ s/50 μ s waveform per IEC 61000-4-5, $V_{TEST} = V_{IMP} \times 1.3$ or ≥ 10 kV	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

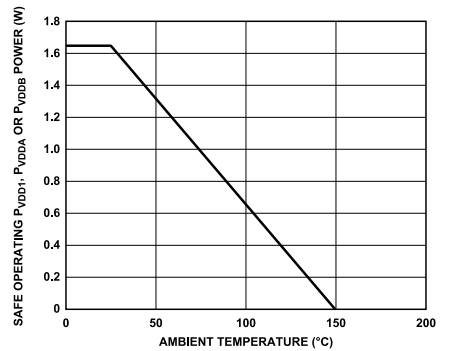


Figure 5. Thermal Derating Curve for R-16 Narrow Body [SOIC_N] Package, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

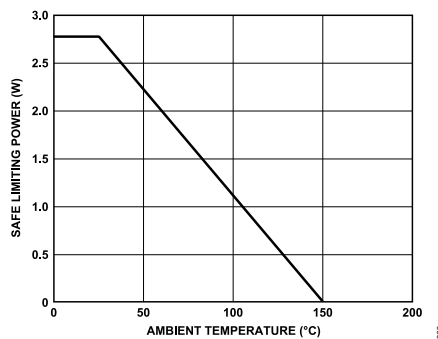


Figure 6. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 16.

Parameter	Symbol	Rating
Operating Temperature	T_A	-40°C to +125°C
Supply Voltages	V_{DD1} , V_{DD2}	1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 17.

Parameter	Rating
Storage Temperature (T_{ST}) Range	-65°C to $+150^\circ\text{C}$
Ambient Operating Temperature (T_A) Range	-40°C to $+125^\circ\text{C}$
Supply Voltages (V_{DD1} , V_{DD2})	-0.5 V to $+7.0\text{ V}$
Input Voltages (V_{IA} , V_{IB} , V_{IC} , V_{E1} , V_{E2} , DISABLE_1 , DISABLE_2)	-0.5 V to $V_{DD1}^1 + 0.5\text{ V}$
Output Voltages (V_{OA} , V_{OB} , V_{OC})	-0.5 V to $V_{DDO}^2 + 0.5\text{ V}$
Average Output Current per Pin ³	
Side 1 Output Current (I_{O1})	-10 mA to $+10\text{ mA}$
Side 2 Output Current (I_{O2})	-10 mA to $+10\text{ mA}$
Common-Mode Transients ⁴	$-150\text{ kV}/\mu\text{s}$ to $+150\text{ kV}/\mu\text{s}$

¹ V_{DD1} is the input side supply voltage.

² V_{DDO} is the output side supply voltage.

³ See Figure 5 for the R-16 narrow body [SOIC_N] package or Figure 6 for the RW-16 wide body [SOIC_W] package for the maximum rated current values for various ambient temperatures.

⁴ Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TRUTH TABLES

Table 18. ADuM130D/ADuM131D Truth Table (Positive Logic)

V_{IX} Input ^{1,2}	V_{DISABLE_X} Input ^{1,2}	V_{DD1} State ²	V_{DDO} State ²	Default Low (D0), V_{OX} Output ^{1,2,3}	Default High (D1), V_{OX} Output ^{1,2,3}	Test Conditions/Comments
L	L or NC	Powered	Powered	L	L	Normal operation
H	L or NC	Powered	Powered	H	H	Normal operation
X	H	Powered	Powered	L	H	Inputs disabled, fail-safe output
X^4	X^4	Unpowered	Powered	L	H	Fail-safe output
X^4	X^4	Powered	Unpowered	Indeterminate	Indeterminate	

¹ L means low, H means high, X means don't care, and NC means not connected.

² V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, or C). V_{DISABLE_X} refers to the input disable signal on the same side as the V_{IX} inputs. V_{DD1} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

³ E0 refers to the ADuM130E0/ADuM131E0 models, D0 refers to the ADuM130D0/ADuM131D0 models, E1 refers to the ADuM130E1/ADuM131E1 models, and D1 refers to the ADuM130D1/ADuM131D1 models. See the Ordering Guide section.

⁴ Input pins (V_{IX} , DISABLE_1 , and DISABLE_2) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

Table 19. ADuM130E/ADuM131E Truth Table (Positive Logic)

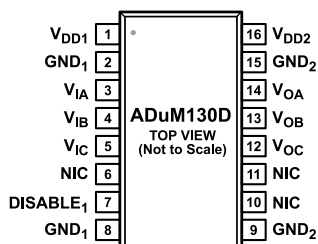
V_{IX} Input ^{1,2}	V_{EX} Input ^{1,2}	V_{DD1} State ²	V_{DDO} State ²	Default Low (E0), V_{OX} Output ^{1,2,3}	Default High (E1), V_{OX} Output ^{1,2,3}	Test Conditions/Comments
L	H or NC	Powered	Powered	L	L	Normal operation
H	H or NC	Powered	Powered	H	H	Normal operation
X	L	Powered	Powered	Z	Z	Outputs disabled
L	H or NC	Unpowered	Powered	L	H	Fail-safe output
X^4	L^4	Unpowered	Powered	Z	Z	Outputs disabled
X^4	X^4	Powered	Unpowered	Indeterminate	Indeterminate	

¹ L means low, H means high, X means don't care, and NC means not connected, and Z means high impedance.

ABSOLUTE MAXIMUM RATINGS

- ² V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, or D). V_{EX} refers to the output enable signal on the same side as the V_{OX} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.
- ³ E0 refers to the ADuM130E0/ADuM131E0 models, D0 refers to the ADuM130D0/ADuM131D0 models, E1 refers to the ADuM130E1/ADuM131E1 models, and D1 refers to the ADuM130D1/ADuM131D1 models. See the [Ordering Guide](#) section.
- ⁴ Input pins (V_{IX} , V_{E1} , and V_{E2}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

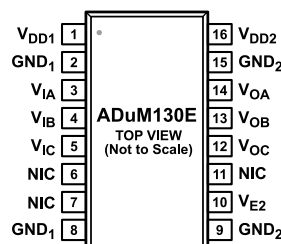
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NIC = NO INTERNAL CONNECTION.
LEAVE THIS PIN FLOATING.

004

Figure 7. ADuM130D Pin Configuration



NIC = NO INTERNAL CONNECTION.
LEAVE THIS PIN FLOATING.

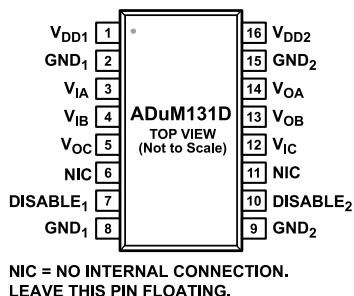
005

Figure 8. ADuM130E Pin Configuration

Table 20. Pin Function Descriptions

Pin No. ¹			
ADuM130D	ADuM130E	Mnemonic	Description
1	1	V _{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND ₁	Ground 1. Ground reference for Isolator Side 1.
3	3	V _{IA}	Logic Input A.
4	4	V _{IB}	Logic Input B.
5	5	V _{IC}	Logic Input C.
6, 10, 11	6, 7, 11	NIC	No Internal Connection. Leave these pins floating.
7	Not applicable	DISABLE ₁	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide .
9, 15	9, 15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
Not applicable	10	V _{E2}	Output Enable 2. Active high logic input. When V _{E2} is high or disconnected, the V _{OA} , V _{OB} , and V _{OC} outputs are enabled. When V _{E2} is low, the V _{OA} , V _{OB} , and V _{OC} outputs are disabled to the high-Z state.
12	12	V _{OC}	Logic Output C.
13	13	V _{OB}	Logic Output B.
14	14	V _{OA}	Logic Output A.
16	16	V _{DD2}	Supply Voltage for Isolator Side 2.

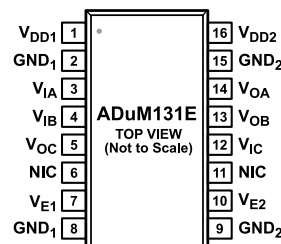
¹ Reference the [AN-1109 Application Note](#) for specific layout guidelines.



NIC = NO INTERNAL CONNECTION.
LEAVE THIS PIN FLOATING.

104

Figure 9. ADuM131D Pin Configuration



NIC = NO INTERNAL CONNECTION.
LEAVE THIS PIN FLOATING.

105

Figure 10. ADuM131E Pin Configuration

Table 21. Pin Function Descriptions

Pin No. ¹			
ADuM131D	ADuM131E	Mnemonic	Description
1	1	V _{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND ₁	Ground 1. Ground reference for Isolator Side 1.
3	3	V _{IA}	Logic Input A.
4	4	V _{IB}	Logic Input B.
5	5	V _{OC}	Logic Output C.
6, 11	6, 11	NIC	No Internal Connection. Leave this pin floating.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 21. Pin Function Descriptions (Continued)

Pin No. ¹			
ADuM131D	ADuM131E	Mnemonic	Description
7	Not applicable	DISABLE ₁	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide .
Not applicable	7	V _{E1}	Output Enable 1. Active high logic input. When V _{E1} is high or disconnected, the V _{OC} output is enabled. When V _{E1} is low, the V _{OC} output is disabled to the high-Z state.
9, 15	9, 15	GND ₂	Ground 2. Ground reference for Isolator Side 2.
10	Not applicable	DISABLE ₂	Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide .
Not applicable	10	V _{E2}	Output Enable 2. Active high logic input. When V _{E2} is high or disconnected, the V _{OA} and V _{OB} outputs are enabled. When V _{E2} is low, the V _{OA} and V _{OB} outputs are disabled to the high-Z state.
12	12	V _{IC}	Logic Input C.
13	13	V _{OB}	Logic Output B.
14	14	V _{OA}	Logic Output A.
16	16	V _{DD2}	Supply Voltage for Isolator Side 2.

¹ Reference the AN-1109 Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

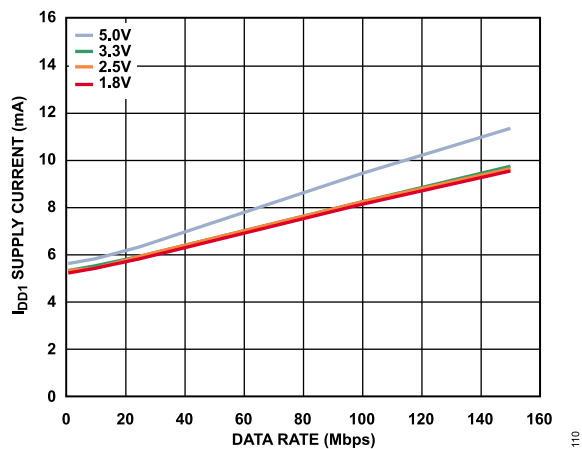


Figure 11. ADuM130D/ADuM130E I_{DD1} Supply Current vs. Data Rate at Various Voltages

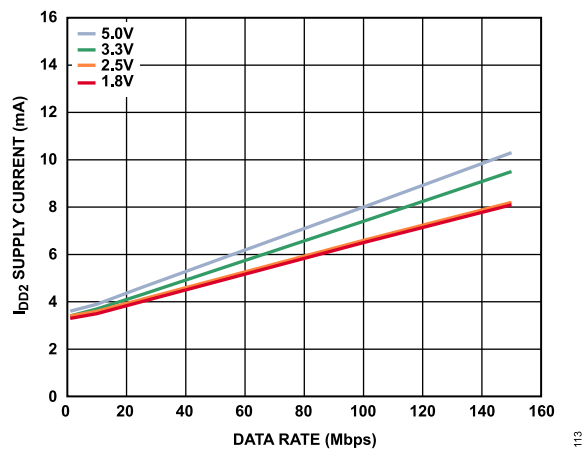


Figure 14. ADuM131D/ADuM131E I_{DD2} Supply Current vs. Data Rate at Various Voltages

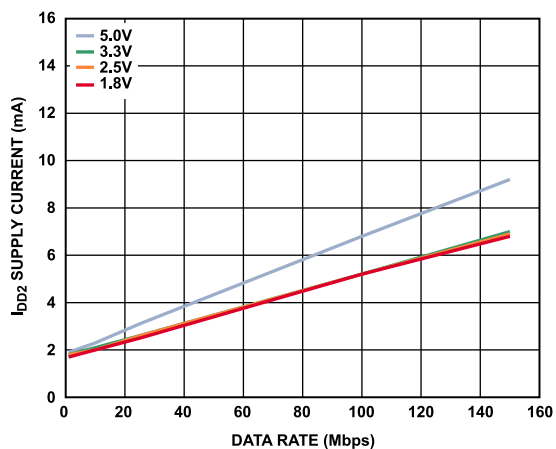


Figure 12. ADuM130D/ADuM130E I_{DD2} Supply Current vs. Data Rate at Various Voltages

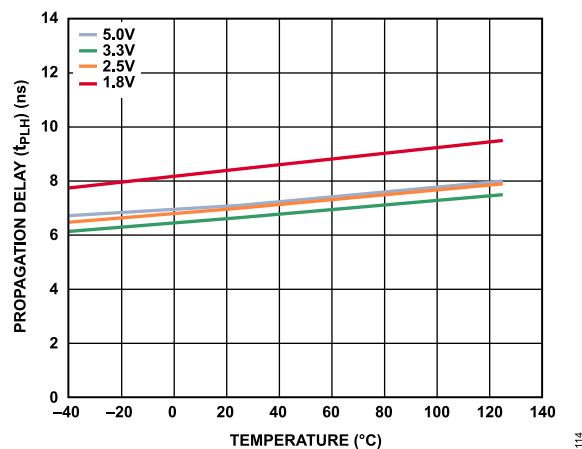


Figure 15. Propagation Delay (t_{PLH}) vs. Temperature at Various Voltages

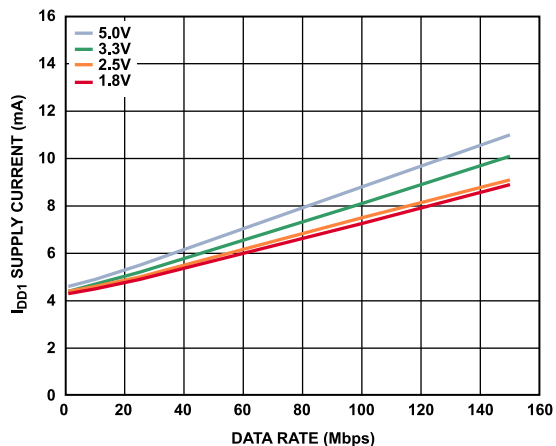


Figure 13. ADuM131D/ADuM131E I_{DD1} Supply Current vs. Data Rate at Various Voltages

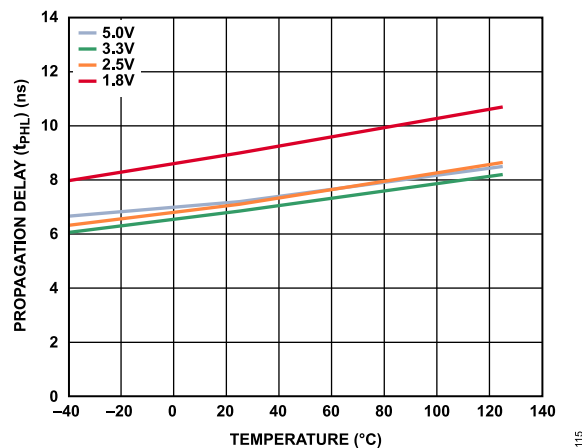


Figure 16. Propagation Delay (t_{PHL}) vs. Temperature at Various Voltages

APPLICATIONS INFORMATION

OVERVIEW

The ADuM130D/ADuM130E/ADuM131D/ADuM131E use a high frequency carrier to transmit data across the isolation barrier using iCoupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 18 and Figure 19, the ADuM130D/ADuM130E/ADuM131D/ADuM131E have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 18 illustrates the waveforms for models of the ADuM130D/ADuM130E/ADuM131D/ADuM131E that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the fail-safe output state of low (the ADuM130D0, ADuM131D0, ADuM130E0, and ADuM131E0 models) sets the output to low. For the ADuM130D/ADuM130E/ADuM131D/ADuM131E that have a fail-safe output state of high, Figure 19 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high (the ADuM130D1, ADuM131D1, ADuM130E1, and ADuM131E1 models) sets the output to high. See the [Ordering Guide](#) for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM130D/ADuM130E/ADuM131D/ADuM131E digital isolators require no external interface circuitry for the logic interfaces.

Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2} . The recommended bypass capacitor value is between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

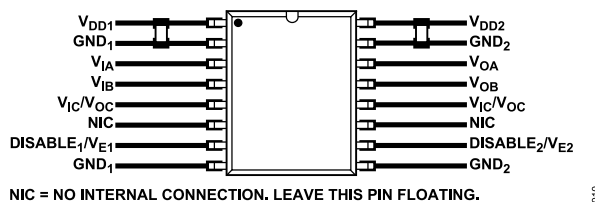


Figure 17. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the [Absolute Maximum Ratings](#) of the device, thereby leading to latch-up or permanent damage.

See the [AN-1109 Application Note](#) for board layout guidelines.

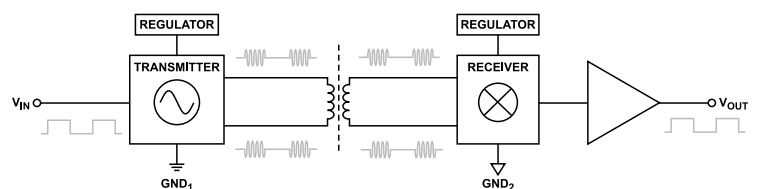


Figure 18. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

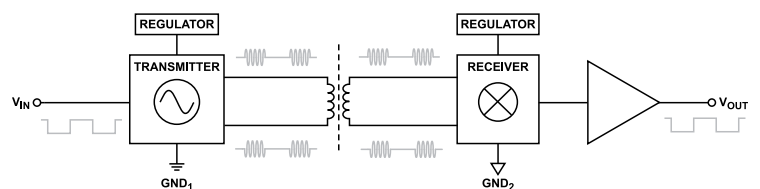


Figure 19. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

APPLICATIONS INFORMATION

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

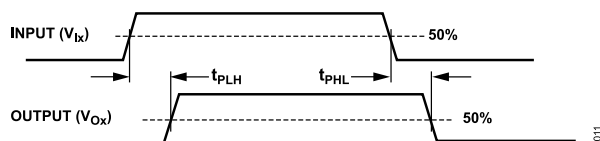


Figure 20. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM130D/ADuM130E/ADuM131D/ADuM131E component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM130D/ADuM130E/ADuM131D/ADuM131E components operating under the same conditions.

JITTER MEASUREMENT

Figure 21 shows the eye diagram for the ADuM130D/ADuM130E/ADuM131D/ADuM131E. The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudo-random bit sequences (PRBS), $2(n-1)$, $n = 14$, for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, at 1 GHz, 10 GSPS with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the ADuM130D/ADuM130E/ADuM131D/ADuM131E with 630 ps p-p jitter.

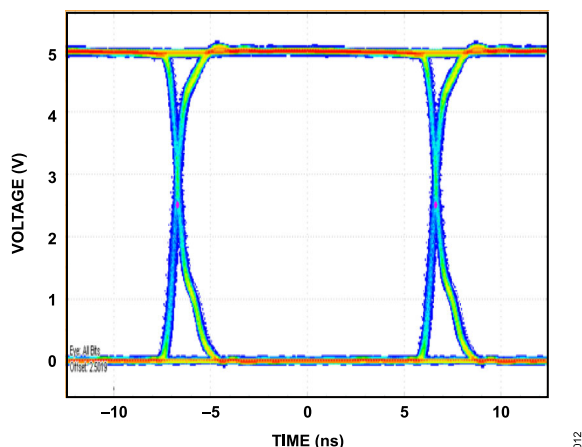


Figure 21. Eye Diagram

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
R-16	SOIC_N	16-Lead Standard Small Outline Package
RW-16	SOIC_W	16-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADuM130D1BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130D1BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130D0BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130D0BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130E1BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130E1BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130E0BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130E0BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM130D1BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130D1BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130D0BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130D0BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130E1BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130E1BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130E0BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM130E0BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131D1BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131D1BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131D0BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131D0BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131E1BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131E1BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131E0BRZ	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131E0BRZ-RL7	-40°C to +125°C	16-Lead SOIC_N	R-16
ADuM131D1BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131D1BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131D0BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131D0BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131E1BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131E1BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131E0BRWZ	-40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM131E0BRWZ-RL	-40°C to +125°C	16-Lead SOIC_W	RW-16

¹ Z = RoHS Compliant Part.

NO. OF INPUTS, WITHSTAND VOLTAGE RATING, FAIL-SAFE OUTPUT STATE, INPUT DISABLE, AND OUTPUT ENABLE OPTIONS

Model ¹	No. of Inputs, V _{DD1} Side	No. of Inputs, V _{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Input Disable	Output Enable
ADuM130D1BRZ	3	0	3.0	High	Yes	No
ADuM130D1BRZ-RL7	3	0	3.0	High	Yes	No

OUTLINE DIMENSIONS

Model ¹	No. of Inputs, V _{DD1} Side	No. of Inputs, V _{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Input Disable	Output Enable
ADuM130D0BRZ	3	0	3.0	Low	Yes	No
ADuM130D0BRZ-RL7	3	0	3.0	Low	Yes	No
ADuM130E1BRZ	3	0	3.0	High	No	Yes
ADuM130E1BRZ-RL7	3	0	3.0	High	No	Yes
ADuM130E0BRZ	3	0	3.0	Low	No	Yes
ADuM130E0BRZ-RL7	3	0	3.0	Low	No	Yes
ADuM130D1BRWZ	3	0	3.75	High	Yes	No
ADuM130D1BRWZ-RL	3	0	3.75	High	Yes	No
ADuM130D0BRWZ	3	0	3.75	Low	Yes	No
ADuM130D0BRWZ-RL	3	0	3.75	Low	Yes	No
ADuM130E1BRWZ	3	0	3.75	High	No	Yes
ADuM130E1BRWZ-RL	3	0	3.75	High	No	Yes
ADuM130E0BRWZ	3	0	3.75	Low	No	Yes
ADuM130E0BRWZ-RL	3	0	3.75	Low	No	Yes
ADuM131D1BRZ	2	1	3.0	High	Yes	No
ADuM131D1BRZ-RL7	2	1	3.0	High	Yes	No
ADuM131D0BRZ	2	1	3.0	Low	Yes	No
ADuM131D0BRZ-RL7	2	1	3.0	Low	Yes	No
ADuM131E1BRZ	2	1	3.0	High	No	Yes
ADuM131E1BRZ-RL7	2	1	3.0	High	No	Yes
ADuM131E0BRZ	2	1	3.0	Low	No	Yes
ADuM131E0BRZ-RL7	2	1	3.0	Low	No	Yes
ADuM131D1BRWZ	2	1	3.75	High	Yes	No
ADuM131D1BRWZ-RL	2	1	3.75	High	Yes	No
ADuM131D0BRWZ	2	1	3.75	Low	Yes	No
ADuM131D0BRWZ-RL	2	1	3.75	Low	Yes	No
ADuM131E1BRWZ	2	1	3.75	High	No	Yes
ADuM131E1BRWZ-RL	2	1	3.75	High	No	Yes
ADuM131E0BRWZ	2	1	3.75	Low	No	Yes
ADuM131E0BRWZ-RL	2	1	3.75	Low	No	Yes

¹ Z = RoHS Compliant Part.