A19520

Vibration-Tolerant Hall-Effect Transmission Speed and Direction Sensor IC

FEATURES AND BENEFITS

- **Differential Hall-effect sensor** measures ring magnets and ferrous targets with inherent stray field immunity
- **SolidSpeed Digital Architecture** provides robust, adaptive performance with advanced algorithms that provide vibration immunity over the full target pitch
- **Integrated solution** includes a capacitor in a single overmolded miniature package
- **ASIL-Compliant:** ASIL B safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
  - Integrated diagnostics and certified safety design process
- **Two-wire current source output** pulse-width protocol supporting speed, direction, and ASIL error reporting
- **EEPROM** enables factory traceability

ISO 26262 ASIL Compliant

SOLIDSPEED DIGITAL ARCHITECTURE

PACKAGE

2-Pin SIP
(suffix UB)

Not to scale

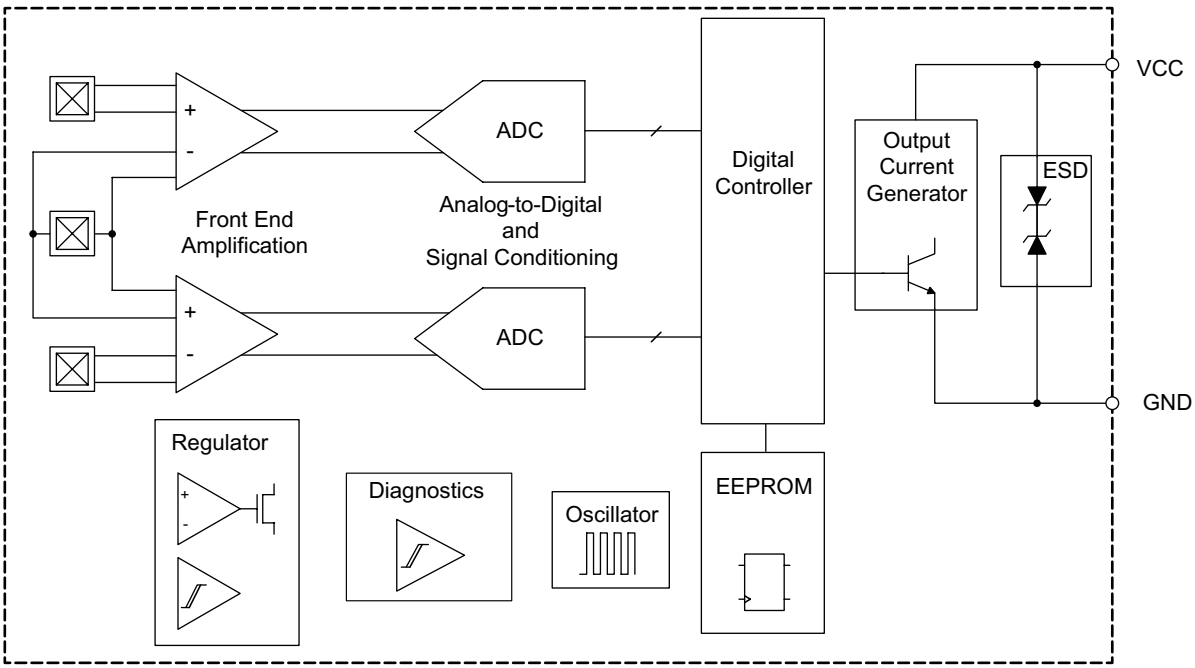
DESCRIPTION

The A19520 is an advanced vibration-tolerant Hall-effect integrated circuit (IC) that measures the speed and direction of rotating targets. This sensor IC can directly measure ring magnets or be back-biased with a magnet to measure ferrous targets. The package features an integrated capacitor for electromagnetic compatibility (EMC).

The A19520 employs intelligent algorithms that allow stable operation during vibration and highly dynamic air gap environments common to transmission applications. In addition, the A19520 differential sensing offers inherent rejection of interfering common-mode magnetic fields.

The IC has been designed to a certified ISO 26262 design process to allow easy integration into high safety level systems. Integrated diagnostics are used to detect an IC failure that impacts the output protocol's accuracy, providing coverage compatible with ASIL B compliance.

The A19520 is provided in a 2-pin miniature SIP package (suffix UB) that is lead (Pb) free, with tin leadframe plating. The UB package includes an IC and capacitor integrated into a single overmolded package, with an additional molded lead-stabilizing bar for robust shipping and ease of assembly.



Functional Block Diagram

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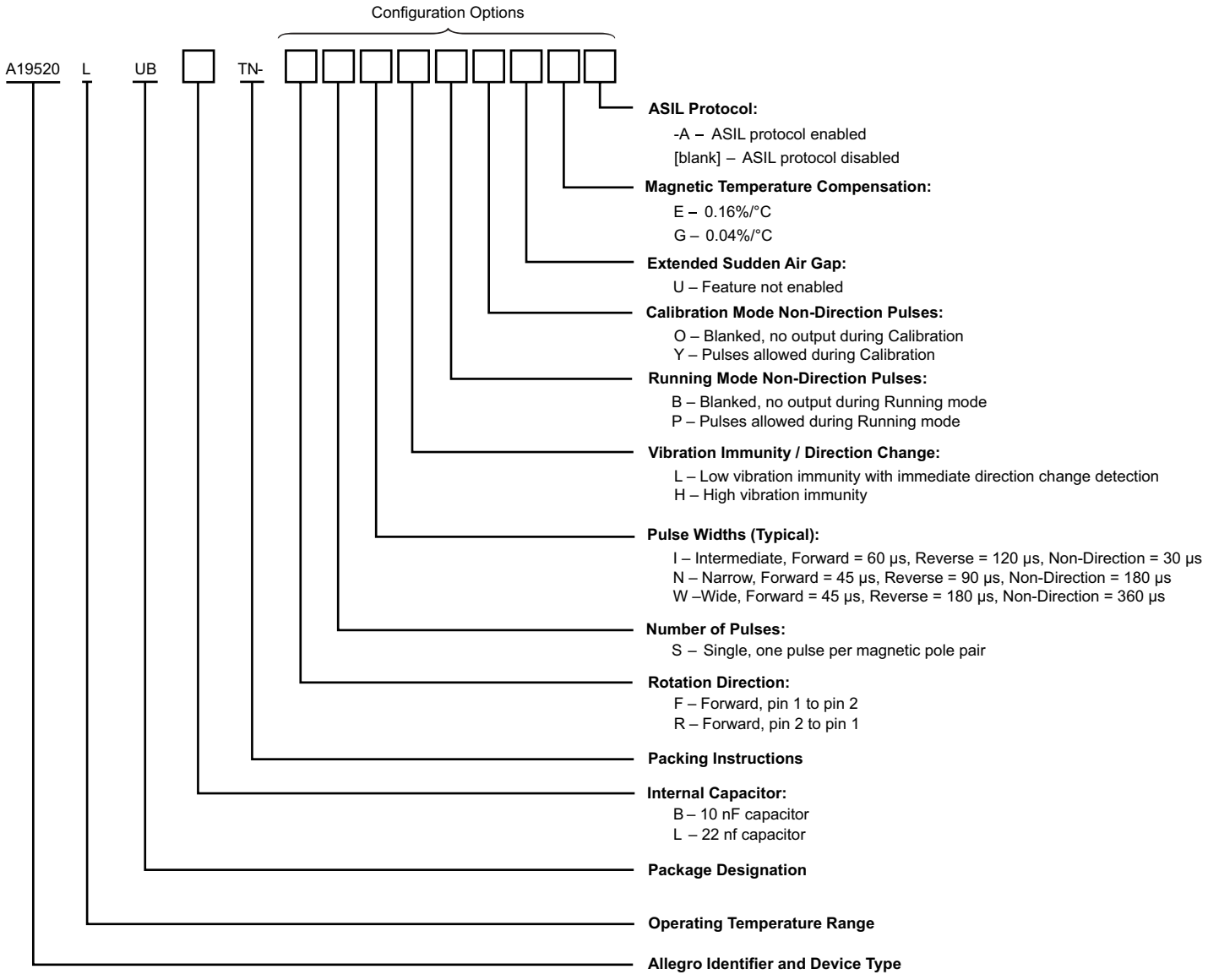
SELECTION GUIDE*

Part Number	Packing
A19520LUBBTN-FSNHPYUE-A	Tape and reel, 4000 pieces per reel
A19520LUBBTN-RSNHPYUE-A	Tape and reel, 4000 pieces per reel
A19520LUBBTN-FSNHPYUE	Tape and reel, 4000 pieces per reel
A19520LUBBTN-RSNHPYUE	Tape and reel, 4000 pieces per reel

* Not all combinations are available. Contact Allegro sales for availability and pricing of custom programming options.



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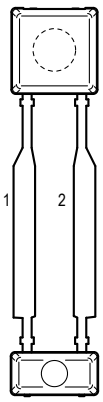
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating section	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A		–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Test Conditions		Value (Typ.)	Unit
Nominal Capacitance	C_{SUPPLY}	Connected between pin 1 and pin 2 (refer to Figure 1)	UBB variant	10	nF
			UBL variant	22	nF

PINOUT DIAGRAM AND TERMINAL LIST



UB Package, 2-Pin SIP Pinout Diagram

Terminal List Table

Name	Number	Function
VCC	1	Supply Voltage
GND	2	Ground

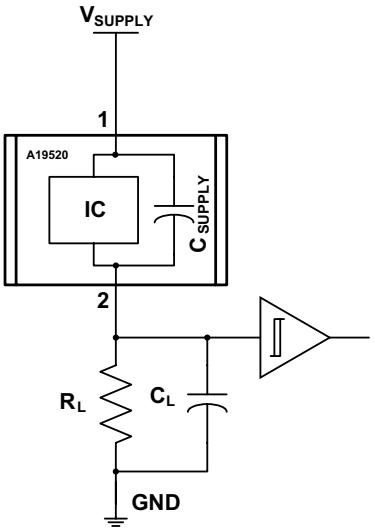


Figure 1: Typical Application Circuit

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OPERATING CHARACTERISTICS: Valid throughout full operating and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit
GENERAL							
Supply Voltage [2]	V_{CC}	Operating, $T_J < T_{J(max)}$, voltage across pin 1 and pin 2; does not include voltage across R_L		4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 V → 5 V or 5 V → 0 V		–	3.6	3.95	V
Reverse Supply Current [3]	I_{RCC}	$V_{CC} = V_{RCC(max)}$		–10	–	–	mA
Supply Current	$I_{CC(LOW)}$	Low-current state		5.9	7	8	mA
	$I_{CC(HIGH)}$	High-current state		12	14	16	mA
	$I_{CC(HIGH)}$ / $I_{CC(LOW)}$	Ratio of high current to low current (isothermal)		1.9	–	–	–
ASIL Safety Current	I_{RESET}	Refer to Figure 15		1.5	–	3.9	mA
PROTECTION CIRCUITS							
Supply Zener Clamp Voltage	$V_{Zsupply}$	I_{CC} = 19 mA, T_A = 25°C		28	–	–	V
POWER-ON CHARACTERISTICS							
Power-On State	POS	$V_{CC} > V_{CC(min)}$, as connected in Figure 1		$I_{CC(LOW)}$			mA
Power-On Time [4]	t_{PO}	Time from $V_{CC} > V_{CC(min)}$, until device has entered calibration		–	–	1	ms
OUTPUT PULSE CHARACTERISTICS, PULSE PROTOCOL [5]							
Output Rise Time	t_r	Voltage measured at pin 2 in Figure 1, R_L = 100 Ω, C_L = 10 pF, measured between 10% and 90% of signal	UBB variant	0	2	4	µs
			UBL variant	0	4.5	8	µs
Output Fall Time	t_f	Voltage measured at pin 2 in Figure 1, R_L = 100 Ω, C_L = 10 pF, measured between 10% and 90% of signal	UBB variant	0	2	4	µs
			UBL variant	0	4.5	8	µs
Pulse Width, ASIL Warning	$t_{w(ASILwarn)}$	Refer to Figure 15		63	–	121	µs
Pulse Width, ASIL Critical	$t_{w(ASILcrit)}$	Refer to Figure 15		4	–	8	ms

Continued on next page...

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Output transients prior to t_{PO} should be ignored.
[5] Timing from start of rising output transition. Measured pulse width will vary on load circuit configurations and thresholds. Pulse width measured at threshold of ($I_{CC(HIGH)}$ + $I_{CC(LOW)}$) / 2 for non-ASIL pulses and (I_{RESET} + $I_{CC(LOW)}$) / 2 for ASIL pulses.

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
INTERMEDIATE PULSE WIDTH OPTION (PART NUMBER -xxIxxxxx)						
Threshold to Enter High-Speed Mode	f_{HIGH}	T_{CYCLE} frequency increasing	0.935	1.1	1.265	kHz
Threshold to Exit High-Speed Mode	f_{LOW}	T_{CYCLE} frequency decreasing	0.850	1	1.150	kHz
Pulse Width, Forward Rotation	$t_{w(FWD)}$	T_{CYCLE} frequency < f_{LOW}	51	60	69	µs
Pulse Width, Reverse Rotation	$t_{w(REV)}$	T_{CYCLE} frequency < f_{LOW}	102	120	138	µs
Pulse Width, High-Speed	$t_{w(HS)}$	T_{CYCLE} frequency > f_{HIGH}	25	30	35	µs
Pulse Width, Non-Direction	$t_{w(ND)}$		25	30	35	µs
Operating Frequency, Forward Rotation [6][7]	f_{FWD}		0	–	12	kHz
Operating Frequency, Reverse Rotation [6][7]	f_{REV}		0	–	12	kHz
Operating Frequency, Non-Direction Pulses [6]	f_{ND}		0	–	12	kHz
NARROW PULSE WIDTH OPTION (PART NUMBER -xxNxxxxx)						
Pulse Width, Forward Rotation	$t_{w(FWD)}$		38	45	52	µs
Pulse Width, Reverse Rotation	$t_{w(REV)}$		76	90	104	µs
Pulse Width, Non-Direction	$t_{w(ND)}$		153	180	207	µs
Operating Frequency, Forward Rotation [6]	f_{FWD}		0	–	12	kHz
Operating Frequency, Reverse Rotation [6]	f_{REV}		0	–	7	kHz
Operating Frequency, Non-Direction Pulses [6]	f_{ND}		0	–	4	kHz
WIDE PULSE WIDTH OPTION (PART NUMBER -xxWxxxxx)						
Pulse Width, Forward Rotation	$t_{w(FWD)}$		38	45	52	µs
Pulse Width, Reverse Rotation	$t_{w(REV)}$		153	180	207	µs
Pulse Width, Non-Direction	$t_{w(ND)}$		306	360	414	µs
Operating Frequency, Forward Rotation [6]	f_{FWD}		0	–	12	kHz
Operating Frequency, Reverse Rotation [6]	f_{REV}		0	–	4	kHz
Operating Frequency, Non-Direction Pulses [6]	f_{ND}		0	–	2.2	kHz

[6] Maximum Operating Frequency is determined by satisfactory separation of output pulses. If shorter low-state durations can be resolved, the maximum f_{REV} and f_{ND} may be higher, excluding the -xxIxxxx variant or $f_{(FWD)}$ as filter bandwidth limitation applies.
[7] Direction information is not available when frequency > f_{HIGH} for the Intermediate Pulse Width option.

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
INPUT CHARACTERISTICS AND PERFORMANCE						
Operating Differential Magnetic Input [8]	$B_{DIFF(pk-pk)}$	Peak-to-peak of differential magnetic input	30	–	–	G
Operating Differential Magnetic Range [8]	B_{DIFF}	Differential input signal; refer to Figure 5	–750	–	750	G
Allowable Differential Sequential Signal Variation	$B_{SEQ(n+1)}$ / $B_{SEQ(n)}$	Signal cycle-to-cycle variation (refer to Figure 2)	0.7	–	1.3	–
	$B_{SEQ(n+i)}$ / $B_{SEQ(n)}$	Overall signal variation (refer to Figure 2)	0.1	–	–	–
Operate Point	B_{OP}	% of peak-to-peak IC-processed signal	–	75	–	%
Release Point	B_{RP}	% of peak-to-peak IC-processed signal	–	25	–	%
Switch Point Separation	$B_{DIFF(SP-SEP)}$	Required amount of amplitude separation between channels at each B_{OP} and B_{RP} occurrence; refer to Figure 4	20	–	–	$\%B_{DIFF(pk-pk)}$
Initial Calibration	T_{CAL}	Periods after t_{PO} completed and first valid speed and direction output. Constant direction of rotation. Refer to Figure 3 for definition of t_{CYCLE}.	–	–	4 × T_{CYCLE}	–
Vibration Immunity (Startup)		High Vibration (-xxxHxxxx variant)	1 × T_{CYCLE}	–	–	–
		Low Vibration (-xxxLxxxx variant)	1 × T_{CYCLE}	–	–	–
Vibration Immunity (Running Mode)		High Vibration (-xxxHxxxx variant)	1 × T_{CYCLE}	–	–	–
		Low Vibration (-xxxLxxxx variant)	0.12 × T_{CYCLE}	–	–	–
THERMAL CHARACTERISTICS						
Magnetic Temperature Coefficient [9]	T_C	Based on magnetic material makeup (-xxxxxxxE variant)	–	0.16	–	%/°C
		Based on magnetic material makeup (-xxxxxxxG variant)	–	0.04	–	%/°C
Package Thermal Resistance [10]	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	–	213	–	°C/W

[8] Differential magnetic field is measured for Channel A (E1-E2) and Channel B (E2-E3) independently. Refer to Figure 5. Each channel's differential magnetic field is measured between two Hall elements with spacing determined by Figure 16. Magnetic field is measured orthogonally to the front of the package.
[9] Magnets and magnetic encoders decrease in magnetic strength with rising temperature. The device temperature coefficient compensates, to help maintain a consistent air gap over temperature.
[10] Additional thermal information is available on the Allegro website.

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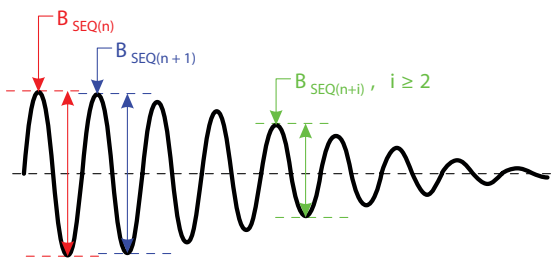
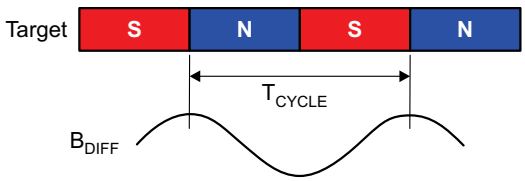


Figure 2: Differential Signal Variation



B_{DIFF} = Differential Input Signal; the differential magnetic flux sensed by the sensor

T_{CYCLE} = Target Cycle; the amount of rotation that moves one north pole and one south pole across the sensor

Figure 3: Definition of T_{CYCLE}

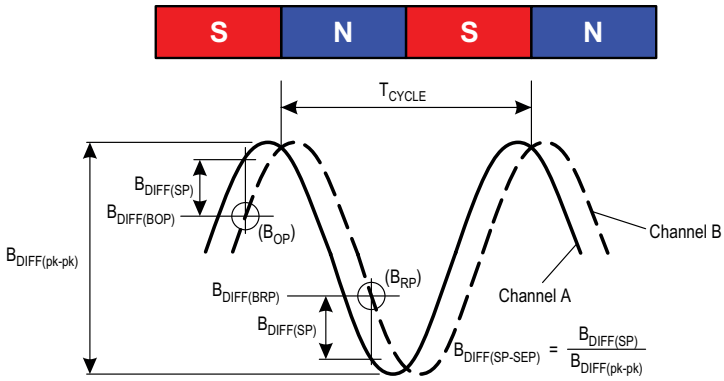


Figure 4: Definition of Switch Point Separation

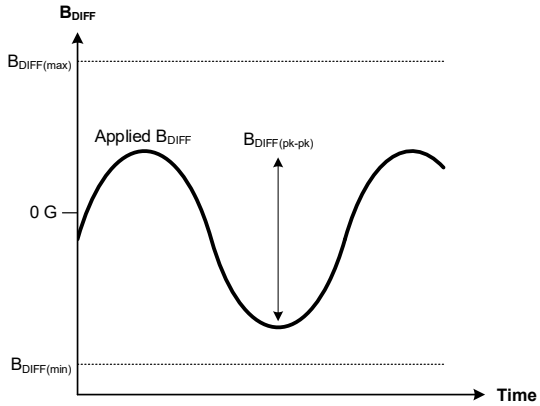


Figure 5: Differential Magnetic Input

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FUNCTIONAL DESCRIPTION

The A19520 sensor IC contains a single-chip Hall-effect circuit that supports three Hall elements. These elements are used in differential pairs to provide electrical signals containing information regarding speed, direction of target rotation, and edge position. The A19520 is intended for use with ring magnet targets, or, when back-biased with an appropriate magnet, with ferrous targets. The IC detects the peaks of the magnetic signals and sets dynamic thresholds based on these detected signals. Output edges are triggered by B_{DIFF} transitions through the switch points.

ROTATION DIRECTION

When the target is rotating such that a target feature passes from pin 1 to pin 2, this is referred to as forward rotation. This direction of rotation is indicated on the IC output by a $t_{w(FWD)}$ pulse width. For the "-Rxxxxxxx" variant, forward direction is indicated for target rotation from pin 2 to 1.

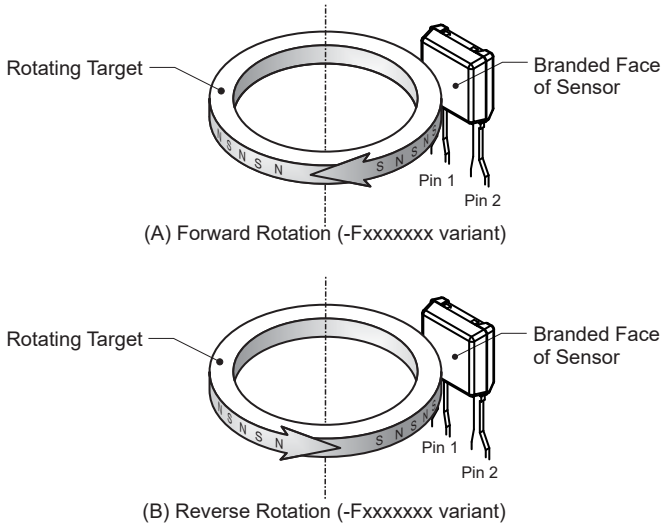

Figure 6: Target Orientation Relative to Device (ring magnet shown).

General Protocol Description

When a target passes in front of the device (opposite the branded face of the package case), the sensor IC generates an output pulse for each magnetic pole-pair of the target or for each tooth-valley pair. Speed information is provided by the output pulse rate, while direction of target rotation is provided by the duration of the output pulses. The sensor IC can sense target movement in both the forward and reverse directions.

For the "-xxIxxxxx" variant, when in High Speed Mode, output pulses will be of $t_{w(HS)}$ duration for either target direction of rotation.

Refer to Figure 6 for target orientation to the device and Figure 7 through Figure 9 for a general output protocol understanding.

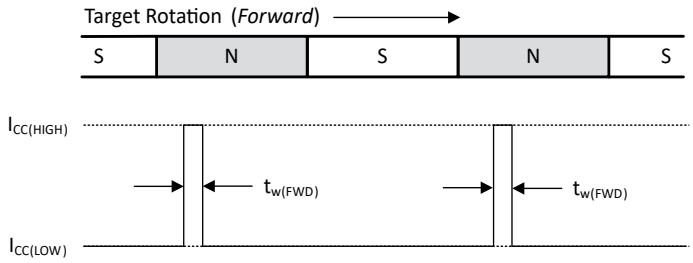

Figure 7: Output Protocol (-Fxxxxxxx), No High Speed Mode, Forward Rotation

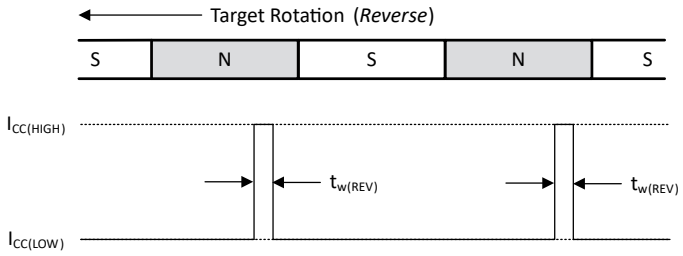

Figure 8: Output Protocol (-Fxxxxxxx), No High Speed Mode, Reverse Rotation

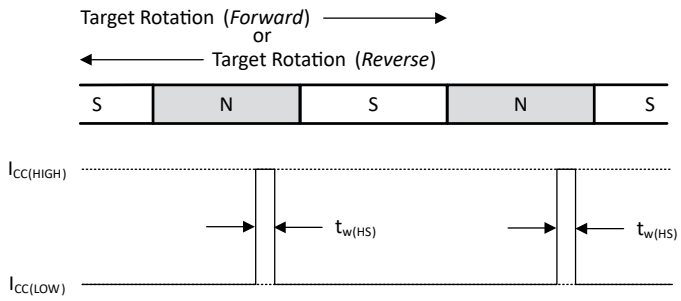

Figure 9: Output Protocol (-xxIxxxxx), High Speed Mode

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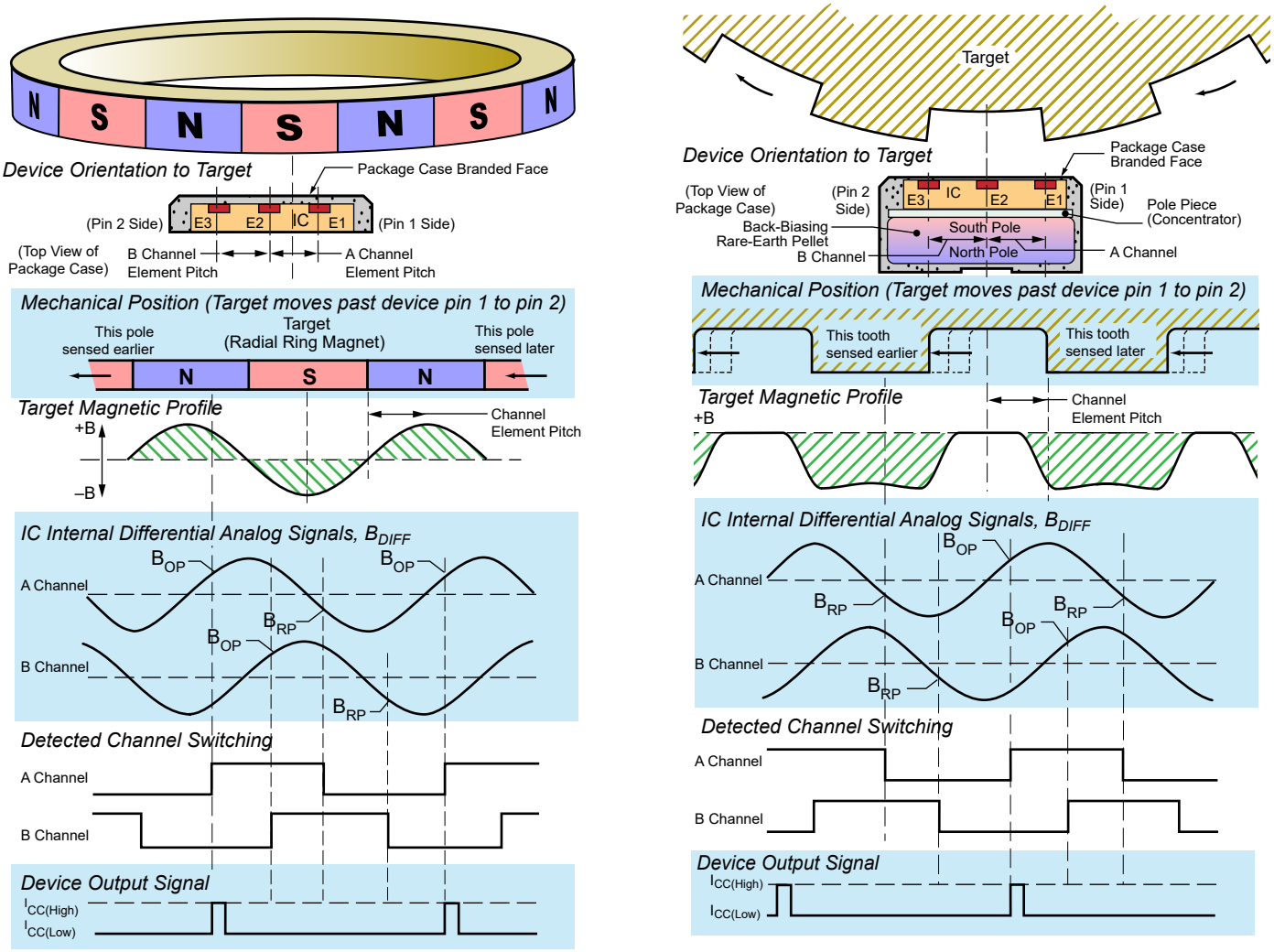

Figure 10: Basic Operation

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Startup Detection/Calibration

After proper supply voltage is applied to the IC, the IC detects the magnetic profile of the rotating target.

The calibration period occurs on the first few features of the target that pass in front of the IC.

Direction information is available after calibration is complete.

Figure 11 and Figure 12 show where the first output edges may occur for various starting target phases.

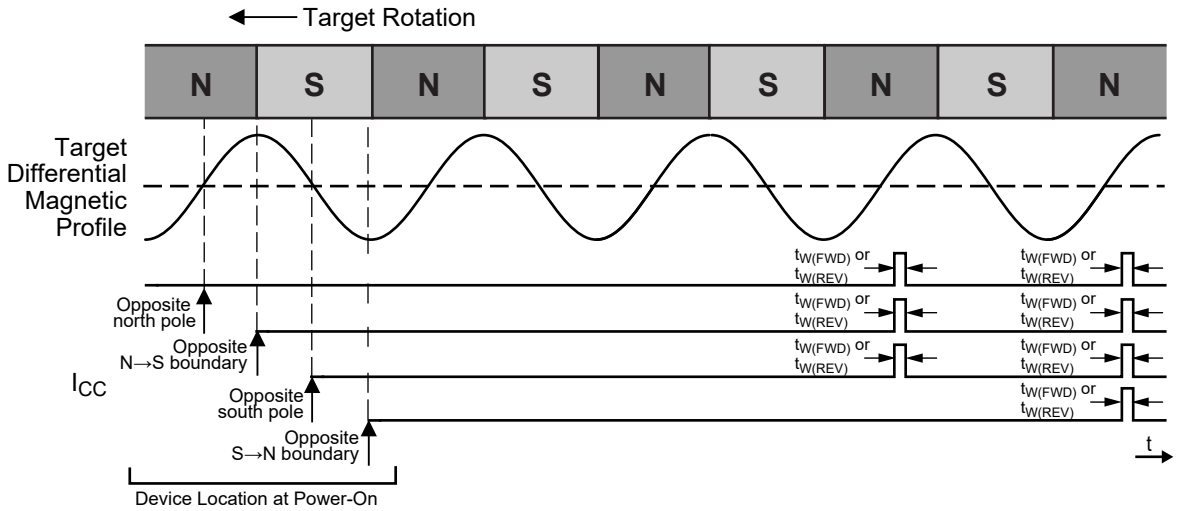

Figure 11: Startup Position Effect on First Device Output Switching (-xxxxxOxx variant)

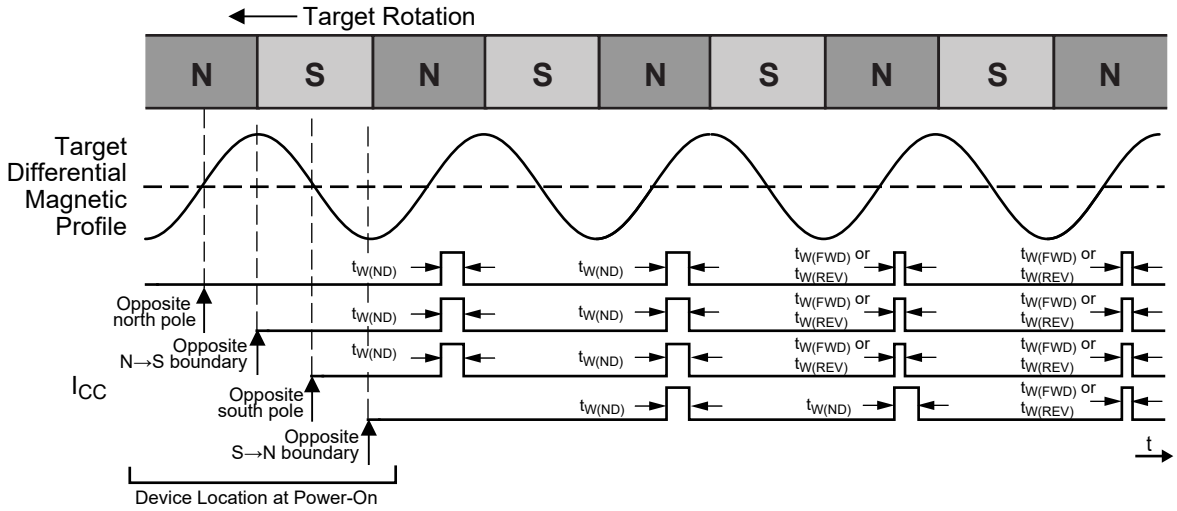

Figure 12: Startup Position Effect on First Device Output Switching (-xxxxxYxx variant)

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Vibration Immunity and Direction Detection

Algorithms embedded in the IC's digital controller detect the presence of target vibration (oscillation) and direction changes through analysis of magnetic input signals.

The advanced detection algorithm provides robust vibration immunity. With the High vibration immunity variant, the vibration algorithm is activated on the first detected direction change and/or vibration event that is less than the specified vibration immunity. The IC will suppress direction output and does not resume normal operation until constant direction information is verified.

With the Low vibration immunity variant, additionally, the IC will report the first direction change immediately to output.

As shown in Figure 13, the -P option may produce non-direction pulses during vibration event, depending on the signal amplitude.

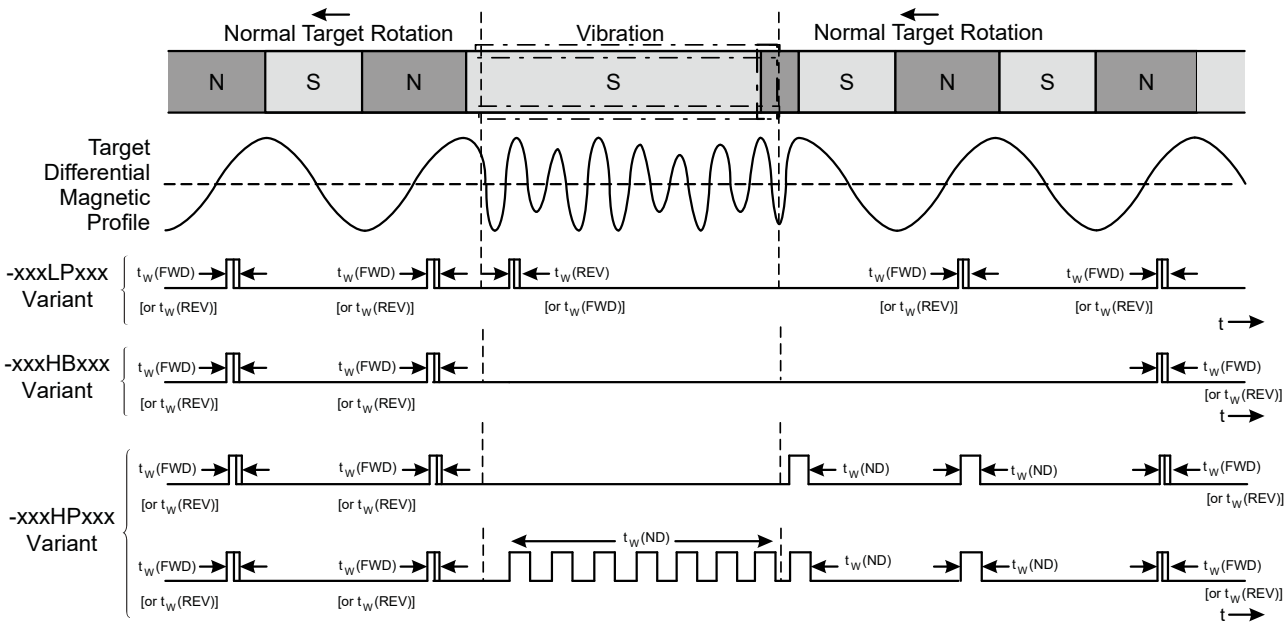

Figure 13: Output Functionality in the Presence of Running Mode Target Vibration

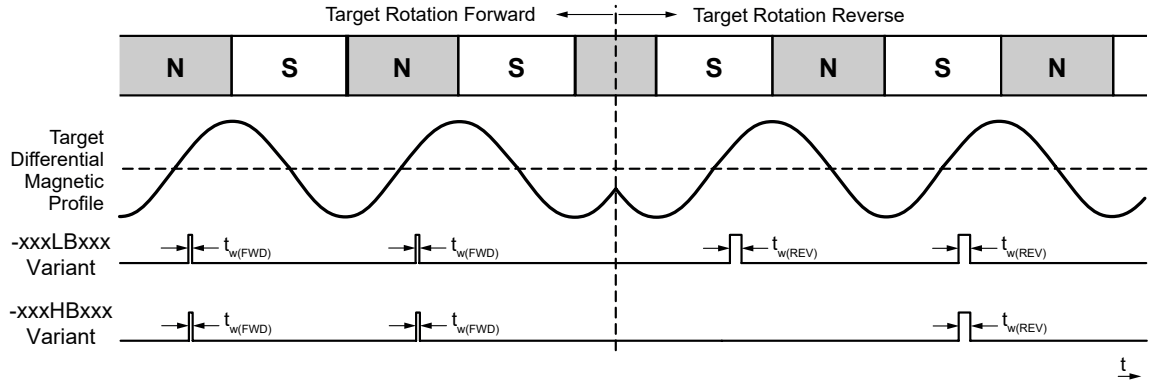

Figure 14: Direction Change Behavior

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ASIL Protocol

The A19520 sensor IC contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 15 for the output protocol of the ASIL Safe State after an internal defect has been detected. Error Protocol will result from faults which cause incorrect signal transmission (i.e., too few or too many output pulses).

Note: If a fault exists continuously, the device will attempt recovery indefinitely. Refer to the A19520 Safety Manual for additional details on the ASIL Safe State Output Protocol.

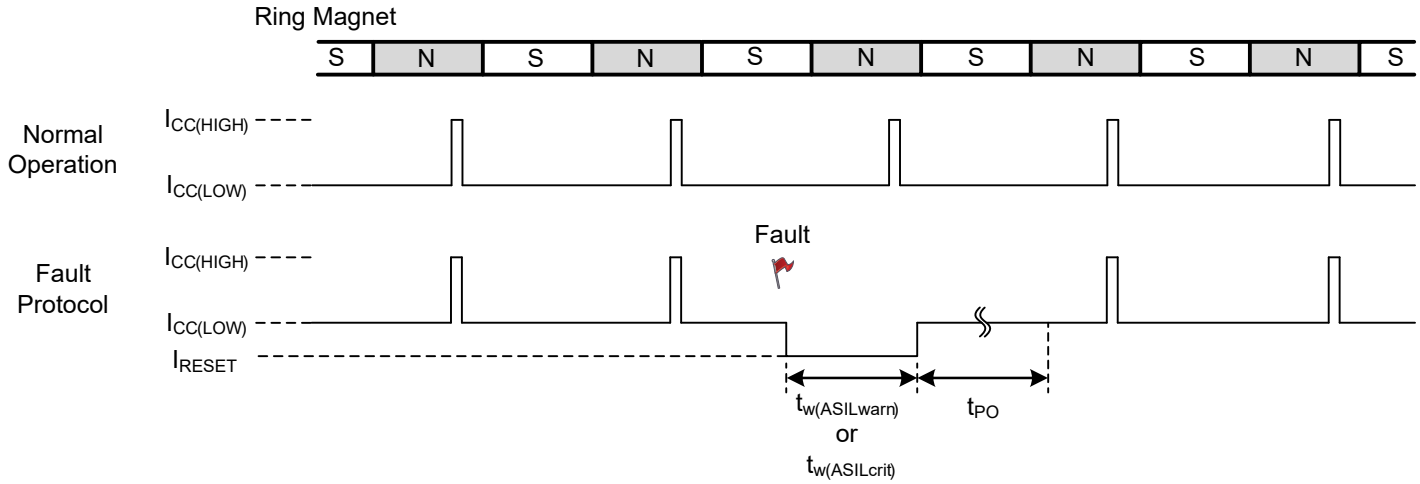

Figure 15: Output Protocol (ASIL Safe State)

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POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is a relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 14 mA, and $R_{\theta JA}$ = 213°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 14\ mA = 168\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 168\ mW \times 213°C/W = 35.8°C$$

$$T_J = T_A + \Delta T = 25°C + 35.8°C = 60.8°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UB, using 1-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=213°C/W, $T_{J(max)}$ =165°C, $V_{CC(max)}$= 24 V, and $I_{CC(AVG)}$ = 14.6 mA. $I_{CC(AVG)}$ is computed using $I_{CC(HIGH)(max)}$ and $I_{CC(LOW)(max)}$, with a duty cycle of 83% computed from $t_{w(REV)(max)}$ on-time at 4 kHz maximum operating frequency.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

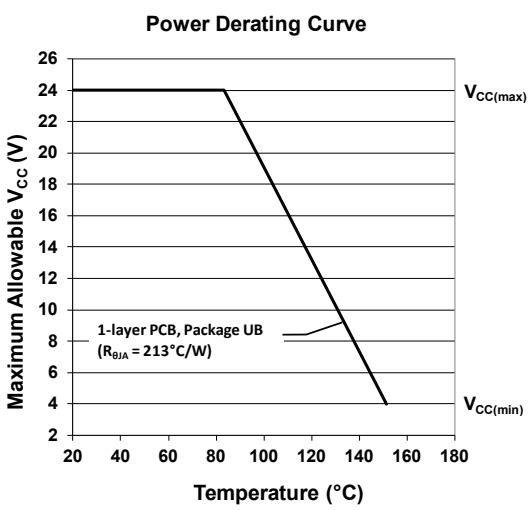
$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 213°C/W = 70.4\,mW$$

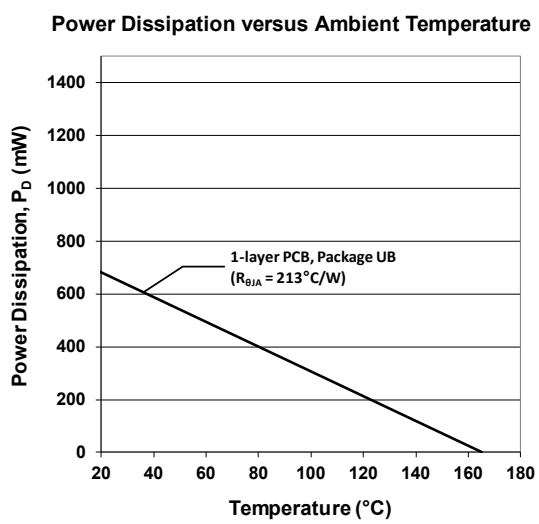
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(AVG)} = 70.4\,mW \div 14.6\,mA = 4.8\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat ≤4.8 V at 150°C.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \le V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \ge V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.





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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000408, Rev. 4)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

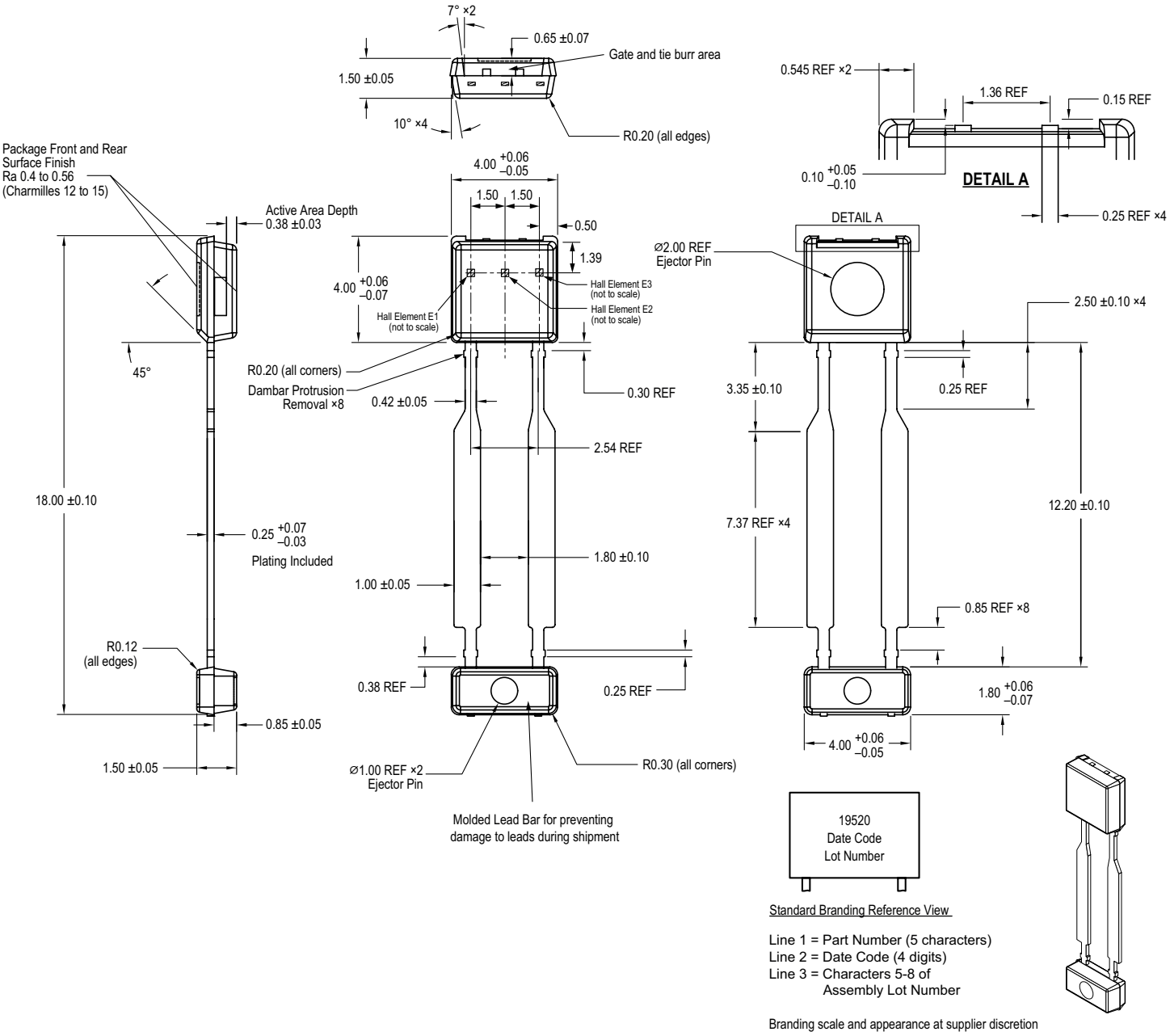

Figure 16: Package UB, 2-Pin SIP

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Revision History

Number	Date	Description
–	December 17, 2018	Initial release
1	October 31, 2019	Corrected Output Fall Time symbol (page 4), footnotes (page 6), B_{DIFF} symbols and magnet polarity (page 9), and package branding (page 14).
2	October 15, 2020	Updated Operate and Release Point values (page 6).
3	April 21, 2021	Added UBL variant (pages 2-4).
4	March 14, 2023	Updated Power Derating (page 13) to read “The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat ≤4.8 V at 150°C“, and other minor editorial updates
5	October 31, 2023	Updated Vibration Immunity and Direction Detection section (page 11)
6	April 25, 2024	Updated package drawing (page 14)
7	April 11, 2025	Updated A^2-SIL logo and descriptions (page 1), modified selection guide illustration (page 2) and operating characteristic footnotes (pages 5 and 6), and reformatted document for interactive PDF capability (all pages)

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