60V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_C = +25°C
60V	50mΩ @ V_{GS} = 10V	25A
	65mΩ @ V_{GS} = 4.5V	22A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

- Power Management Functions
- DC-DC Converters
- Backlighting

Features

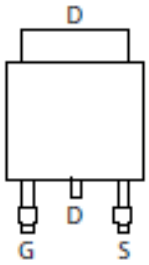
- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable and Robust End Application
- Low On-Resistance
- Low Input Capacitance
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **An Automotive-Compliant Part is Available Under Separate Datasheet (DMNH6042SK3Q)**

Mechanical Data

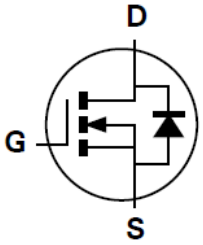
- Case: TO252 (DPAK)
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.315 grams (Approximate)



Top View



Pin Out Top View



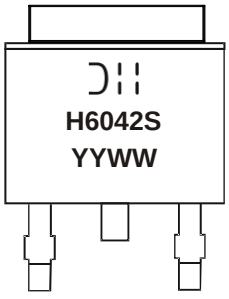
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMNH6042SK3-13	TO252 (DPAK)	2,500/Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



= Manufacturer's Marking
H6042S = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 16 = 2016)
WW = Week Code (01 to 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 7) V_{GS} = 10V	Steady State	T_C = +25°C T_C = +70°C	I_D	25 17	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I_{DM}	40	A
Maximum Continuous Body Diode Forward Current (Note 7)			I_S	25	A
Avalanche Current (Note 8) L = 10mH			I_{AS}	3.5	A
Avalanche Energy (Note 8) L = 10mH			E_{AS}	65	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		P_D	2	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	73	°C/W
	t<10s		36	
Total Power Dissipation (Note 6)		P_D	3.5	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	43	°C/W
	t<10s		21	
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	3.2	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	30	50	mΩ	V_{GS} = 10V, I_D = 6A
		—	45	65		V_{GS} = 4.5V, I_D = 6A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 2.6A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	492	—	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	54	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	27	—	pF	
Gate Resistance	R_g	—	3.8	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	4.2	—	nC	V_{DS} = 44V, I_D = 5.2A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	8.8	—	nC	
Gate-Source Charge	Q_{gs}	—	1.8	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.8	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.4	—	ns	V_{GS} = 10V, V_{DS} = 30V, R_G = 6Ω, I_D = 1A
Turn-On Rise Time	t_R	—	1.9	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	10.1	—	ns	
Turn-Off Fall Time	t_F	—	4.5	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	12.9	—	ns	I_F = 2.6A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	5.4	—	nC	

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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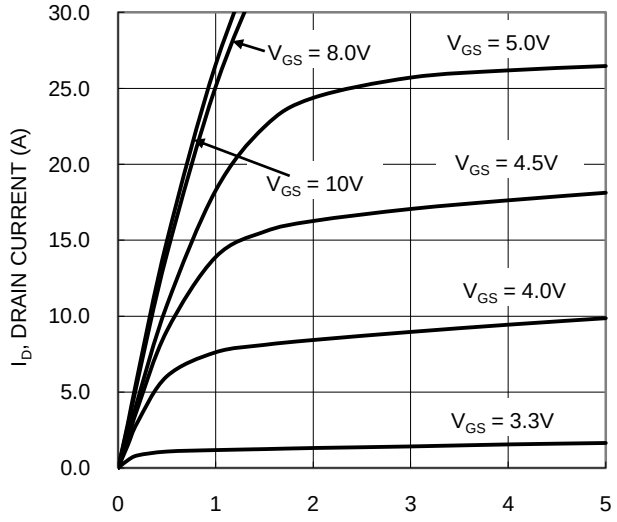


Figure 1. Typical Output Characteristic

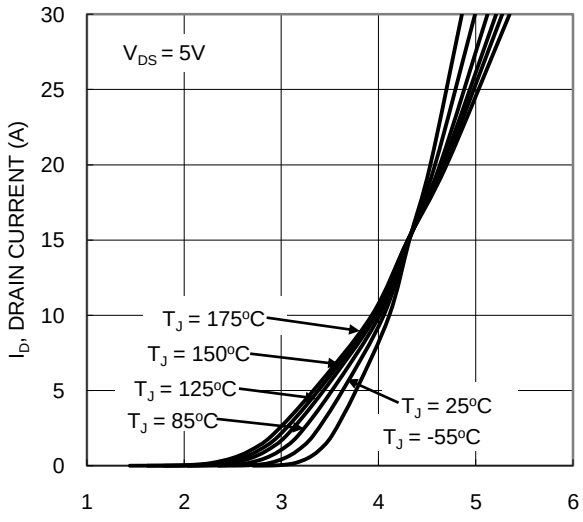


Figure 2. Typical Transfer Characteristic

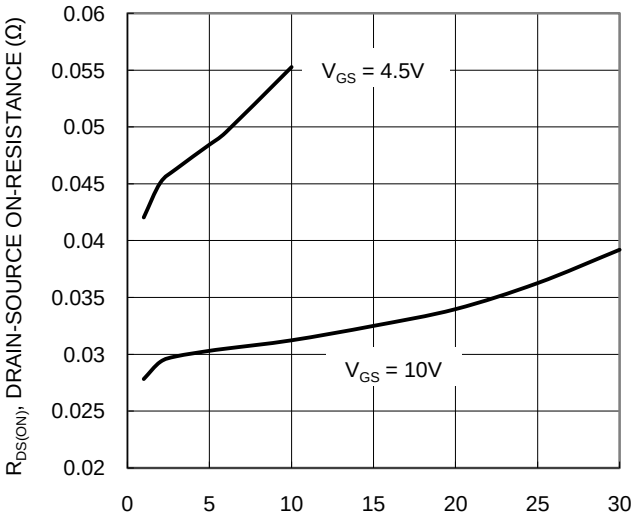


Figure 3. Typical On-Resistance vs Drain Current and Gate Voltage

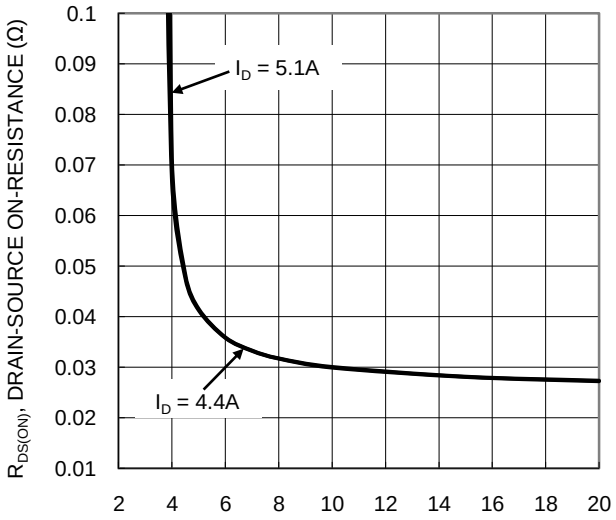


Figure 4. Typical Transfer Characteristic

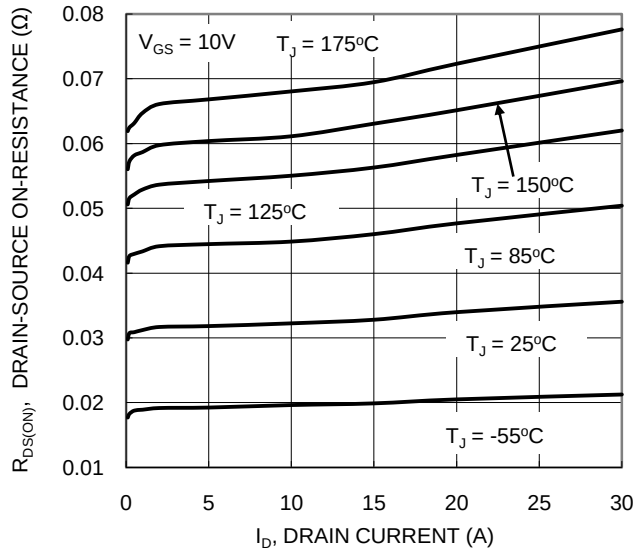


Figure 5. Typical On-Resistance vs Drain Current and Temperature

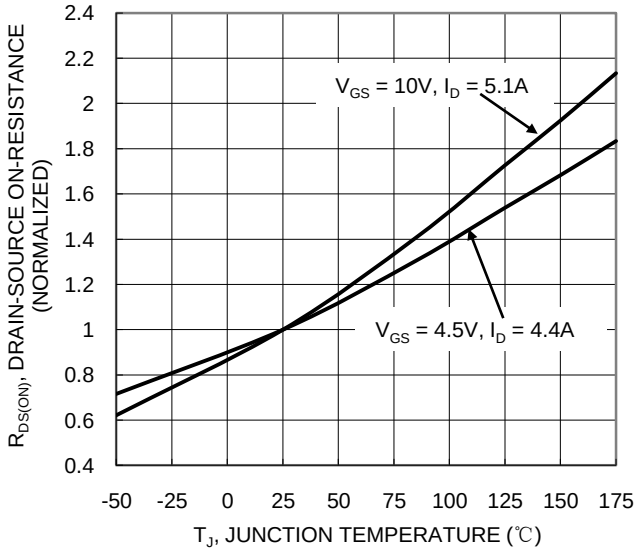


Figure 6. On-Resistance Variation with Temperature

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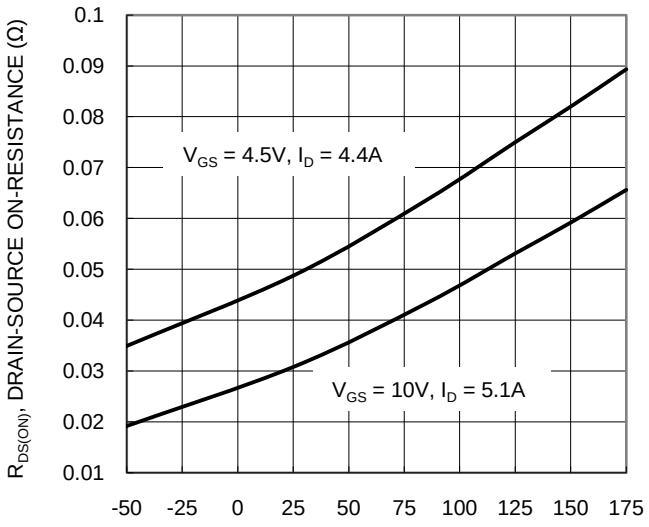


Figure 7. On-Resistance Variation with Temperature

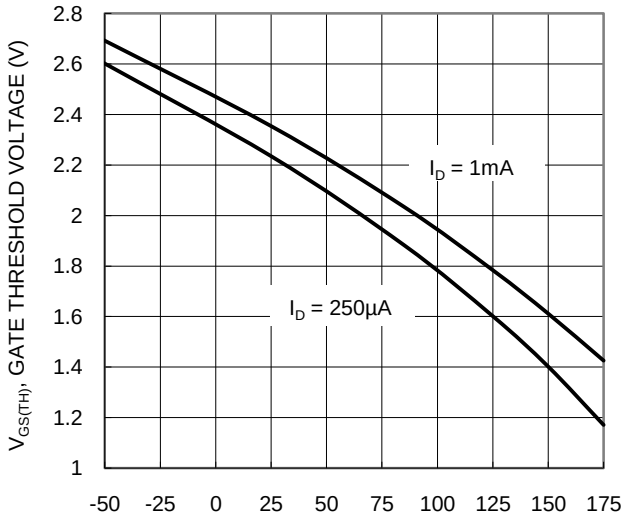


Figure 8. Gate Threshold Variation vs Junction Temperature

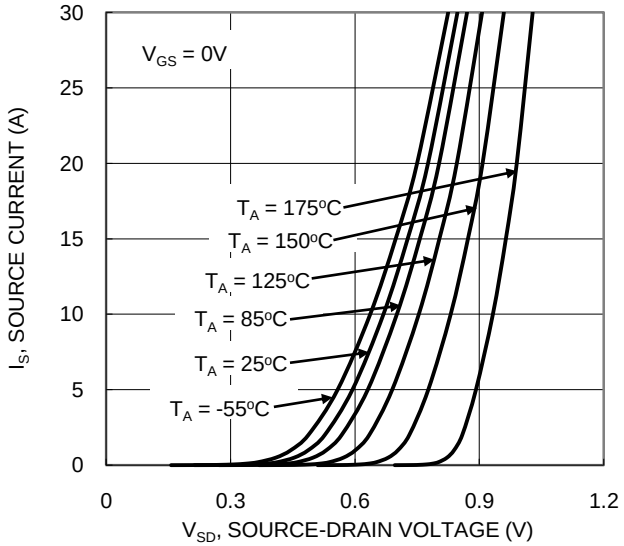


Figure 9. Diode Forward Voltage vs. Current

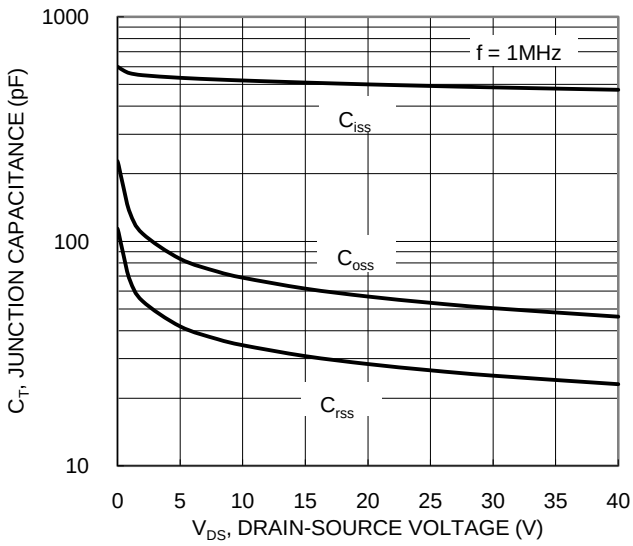


Figure 10. Typical Junction Capacitance

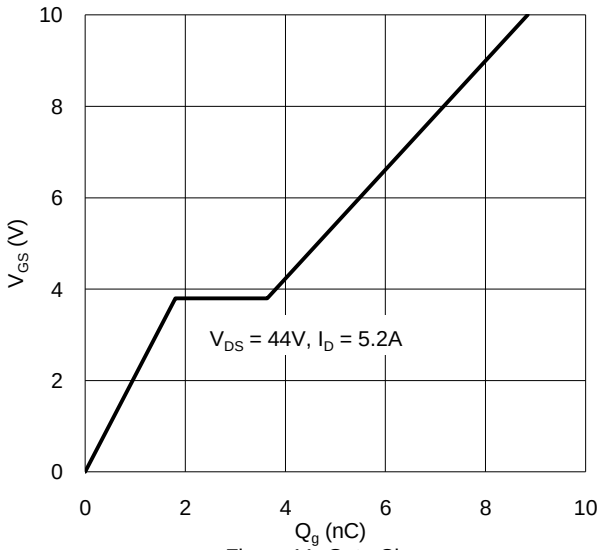


Figure 11. Gate Charge

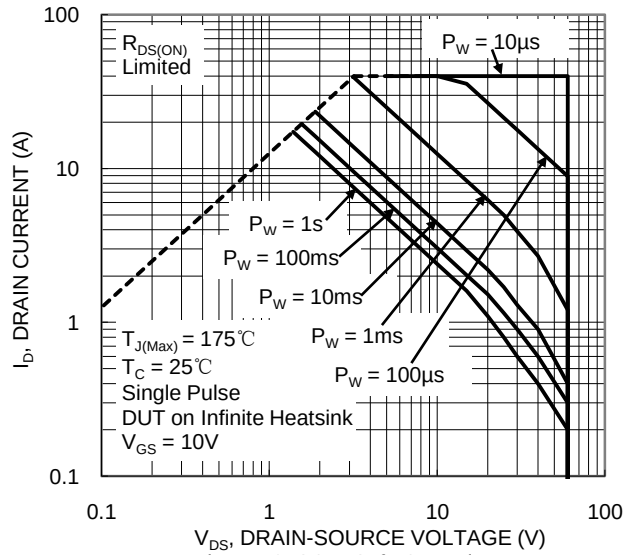


Figure 12. SOA, Safe Operation Area

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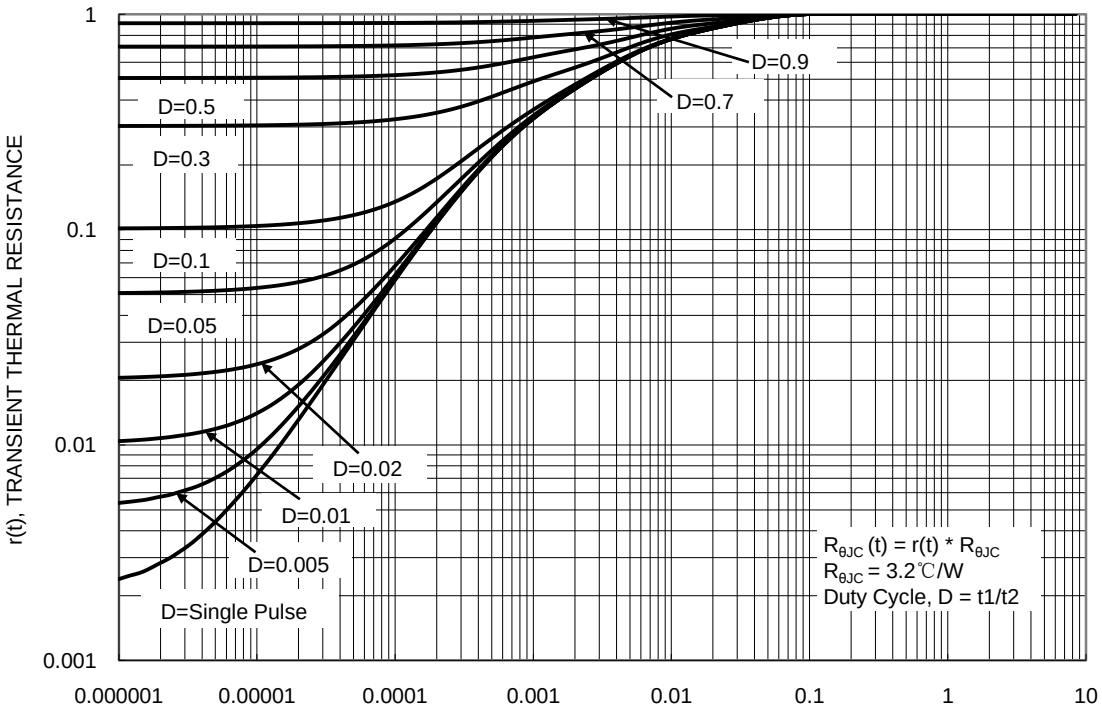


Figure 13. Transient Thermal Resistance

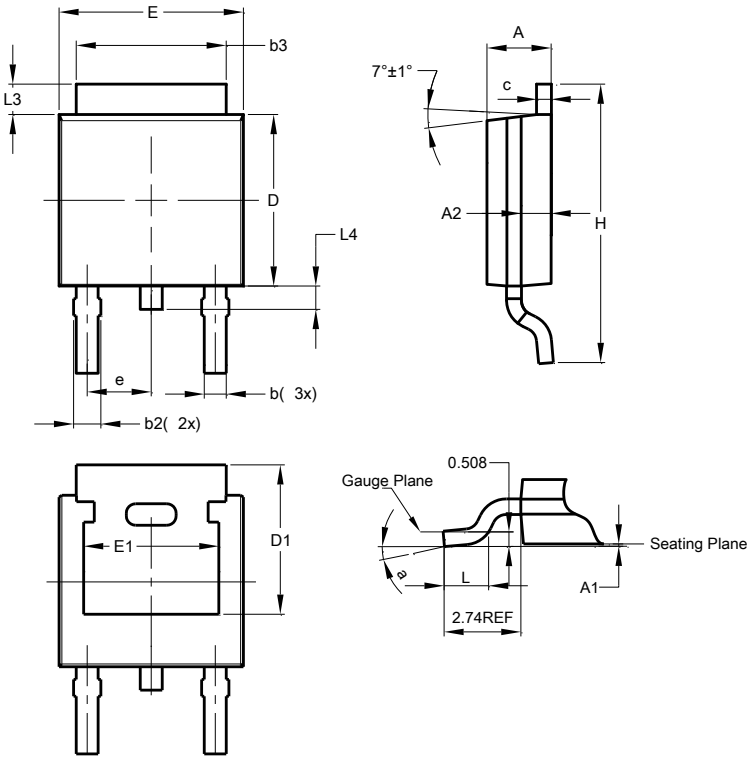
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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TO252 (DPAK)

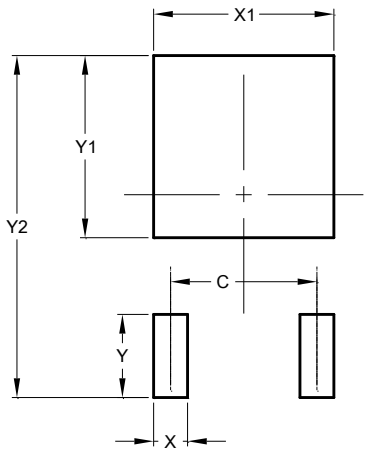


TO252 (DPAK)			
Dim	**Min**	**Max**	**Typ**
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TO252 (DPAK)



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

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