LDO Regulator - Ultra-Low Iq, Dual Power Mode

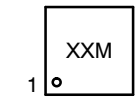
50 nA, 80 mA

NCP171



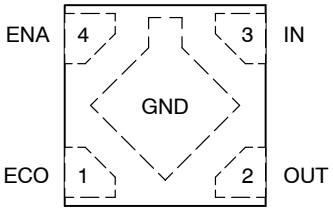
XDFN4 1.2x1.2
AM SUFFIX
CASE 711BC

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 20 of this data sheet.

The NCP171 is a Dual mode LDO offering up to 80 mA in Active Mode and as low as 50 nA of Iq in Low Power Mode. The Dual Mode function is selectable with the ECO pin allowing for dynamic switching between Active and Low Power Modes, ideal in long life battery powered applications.

The output Voltage in Low Power mode can be lowered by an internally factory programmed value ranging 50 mV, 100 mV, 150 mV or 200 mV with respect to the nominal output voltage in Active Mode. This feature further lowers the application consumption in sleep mode. The NCP171 is in the SLIQ (Super Low Iq) LDO family and is available in small XDFN4 1.2 x 1.2 package.

Features

- Operating Input Voltage Range: 1.7 V to 5.5 V
- Output Voltage Range: 0.6 V to 3.3 V (50 mV steps)
- Low Power Mode / Active Mode Externally Controlled by ECO pin
- Internally Factory Programmable Output Voltage Offset for Low Power/Active Mode to 50 mV, 100 mV, 150 mV, 200 mV
- Quiescent Current of 50 nA at No Load, (Low Power mode)
- Maximum Current 80 mA in Active Mode and 5 mA in Low Power Mode
- Low Dropout: 41 mV Typ. at 80 mA (Vout = 3.3 V)
- ±2% Output Voltage Accuracy in Active Mode
- High PSRR: 65 dB at 1 kHz in Active Mode
- Active Output Discharge for Fast Output Turn−Off
- Current Limitation, Thermal Shutdown
- Available in Small XDFN4 1.2x1.2 Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- IoT
- RFID
- Portable Communication Equipment
- Consumer Electronics

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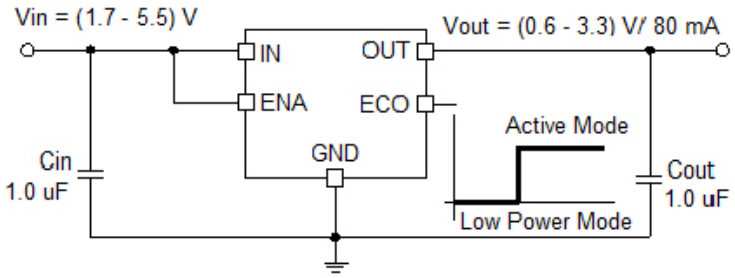

Figure 1. Typical Application Schematic

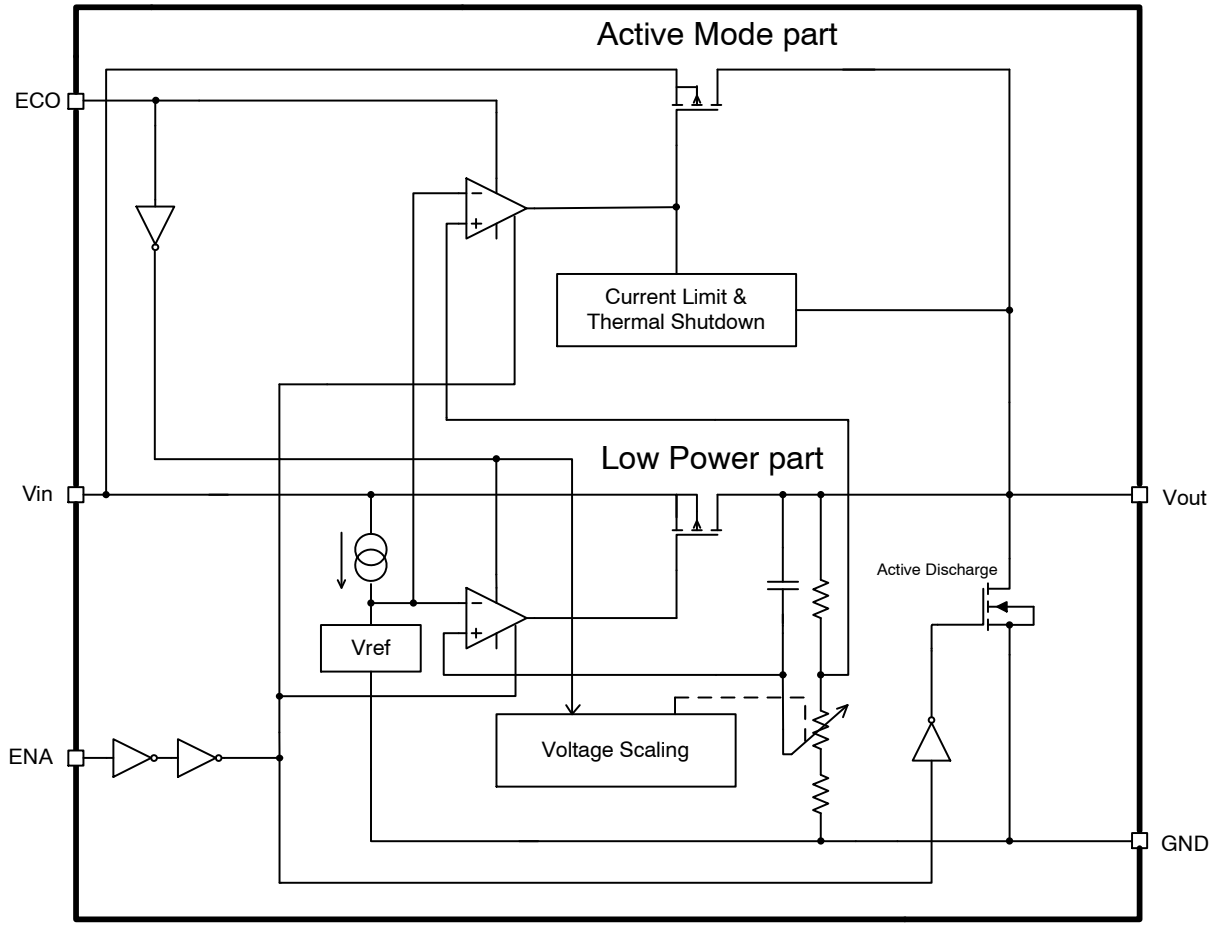

Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. XDFN4	Pin Name	Description
1	ECO	Low Power and Active mode control pin. Pulling this pin to ground switches the device into Low Power mode and pushing this pin to output voltage switches the device into Active mode.
2	OUT	Output pin
3	IN	Input pin
4	ENA	Enable pin. Driving ENA above 1.2 V turns on the regulator. Driving ENA below 0.4 V puts the regulator into shutdown mode.
5(EP)	GND	Ground

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Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	6.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN}	V
Enable pin	V_{ENA}	−0.3 to V_{IN}	V
ECO pin	V_{ECO}	−0.3 to V_{IN}	V
Output Current	I_{OUT}	120	mA
Power Dissipation XDFN4	P_D	400	mW
Maximum Junction Temperature	$T_{J(MAX)}$	85	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	170	°C/W

3. This data was derived by thermal simulations for a single device mounted on the 40 mm x 40 mm x 1.6 mm FR4 PCB with 2−ounce 800 sq mm copper area on top and bottom.

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Table 4. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; $V_{IN} = V_{OUTNOM}$ + 0.5 V or 1.7 V, whichever is greater; I_{OUT} = 100 μA at Low Power Mode / 1 mA at Active Mode, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.7		5.5	V
Output Voltage	$-40°C \le T_J \le 85°C$, I_{OUT} < 5 mA	Low Power Mode (LP) ECO = 0 NCP171A3MXxxxyyy	$V_{OUTAC} = V_{OUTLP} + V_{OFFSET}$	x0.97		x1.03	V
	$-40°C \le T_J \le 85°C$, I_{OUT} < 5 mA	Low Power Mode (LP) ECO = 0 NCP171AMXxxxyyy		x0.95		x1.05	V
	T_J = +25°C, $0 \le I_{OUT}$ <80 mA	Active Mode (AC) ECO = Voutnom		x0.98		x1.02	V
	$-40°C \le T_J \le 85°C$, $0 \le I_{OUT}$ <80 mA	Active Mode ECO = Voutnom		x0.97		x1.03	V
Offset (Note 5)		T_J = +25°C	V_{OFFSET}		50, 100, 150, 200		mV
Line Regulation	$V_{IN} = V_{OUT}$ + 0.5 V to 5.5 V, $V_{IN} \ge$ 1.7 V	I_{OUT} = 100 μA, LP Mode	$Line_{Reg}$			10	mV
		I_{OUT} = 1 mA, AC Mode				10	
Load Regulation	1 mA $\le I_{OUT} \le$ 80 mA, $V_{IN} = V_{OUT}$ + 0.5 V or $V_{IN} \ge$ 1.7 V Active Mode, ECO = Voutnom		$Load_{Reg}$			10	mV
	0 mA < I_{OUT} < 5 mA, $V_{IN} = V_{OUT}$ + 0.5 V or $V_{IN} \ge$ 1.7 V Low Power Mode, ECO = 0					30	mV
Dropout Voltage (Note 6)	I_{OUT} = 80 mA, Active Mode, ECO = V_{OUTNOM}	V_{OUT} = 1.8 V			81	110	mV
		V_{OUT} = 2.5 V			51	80	
		V_{OUT} = 2.8 V			47	75	
		V_{OUT} = 3.0 V			43	65	
		V_{OUT} = 3.3 V			41	55	
Output Current	Active Mode, ECO = V_{OUTNOM}		I_{OUTAM}	80			mA
Output Current	Low Power Mode, ECO = 0		I_{OUTLP}	5			mA
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$, Active mode, ECO = V_{OUTNOM}		I_{SC}		140	170	mA
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$, Low Power mode, ECO = 0		I_{SC}		9	15	mA
Quiescent Current	I_{OUT} = 0 Low Power Mode	T_J = +25°C	I_Q		50		nA
	I_{OUT} = 0 mA, Low Power Mode	$-40°C \le T_J \le 85°C$				150	nA
	I_{OUT} = 0 mA, Active Mode	$-40°C \le T_J \le 85°C$			55	95	μA
Shutdown Current (Note 7)	$V_{ENA} \le$ 0.4 V, V_{IN} = 5.5 V		I_{DIS}		30		nA

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible
5. The Offset voltage is internally programed to 50 mV, 100 mV, 150 mV or 200 mV. See the table ORDERING INFORMATION for more details.
6. The Dropout at Nominal Output Voltage below 1.8 V and output current 80 mA was not defined and tested. The dropout at Nominal Output Voltage above 1.8 V was characterized when V_{OUT} falls 3% below the nominal regulated voltage.
7. Shutdown Current is the current flowing into the IN pin when the device is in the disable state (V_{ENA} < 0.4 V).
8. Guaranteed by design and characterization.

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Table 4. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; $V_{IN} = V_{OUTNOM}$ + 0.5 V or 1.7 V, whichever is greater; I_{OUT} = 100 μA at Low Power Mode / 1 mA at Active Mode, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Ground Current	Low Power Mode, Iout = 10 μA	I_{GND}		230		nA
	Low Power Mode, Iout = 100 μA			620		
	Low Power Mode, Iout = 1 mA			1500		
	Low Power Mode, Iout = 5 mA			2500		
	Active Mode, I_{OUT} = 1 mA			120		μA
	Active Mode, I_{OUT} = 10 mA			190		
	Active Mode, I_{OUT} = 80 mA			420		
ENA Pin Threshold Voltage	ENA Input Voltage “H”	V_{ENAH}	1.2			V
	ENA Input Voltage “L”	V_{ENAL}			0.4	V
ECO Pin Threshold Voltage	ECO Input Voltage “H”	V_{ECOH}	0.5			V
	ECO Input Voltage “L”	V_{ECOL}			0.2	
Power Supply Rejection Ratio	$V_{IN} = V_{OUT}$ + 1 V or 2.0 V whichever is higher, ΔV_{IN} = 0.1 V_{pk-pk}, IOUT = 10 mA, f = 1 kHz, Active Mode	PSRR		65		dB
Output Noise Voltage	V_{OUT} = 0.8 V, I_{OUT} = 80 mA, f = 10 Hz to 100 kHz, Active Mode	V_N		54		μV_{rms}
Thermal Shutdown Temperature (Note 8)	Temperature increasing from T_J = +25°C, Active Mode	T_{SD}		165		°C
Thermal Shutdown Hysteresis (Note 8)	Temperature falling from T_{SD}, Active Mode	T_{SDH}		20		°C

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible
5. The Offset voltage is internally programed to 50 mV, 100 mV, 150 mV or 200 mV. See the table ORDERING INFORMATION for more details.
6. The Dropout at Nominal Output Voltage below 1.8 V and output current 80 mA was not defined and tested. The dropout at Nominal Output Voltage above 1.8 V was characterized when V_{OUT} falls 3% below the nominal regulated voltage.
7. Shutdown Current is the current flowing into the IN pin when the device is in the disable state (V_{ENA} < 0.4 V).
8. Guaranteed by design and characterization.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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APPLICATION INFORMATION

A typical application circuit for NCP171 series is shown in Figure 3.

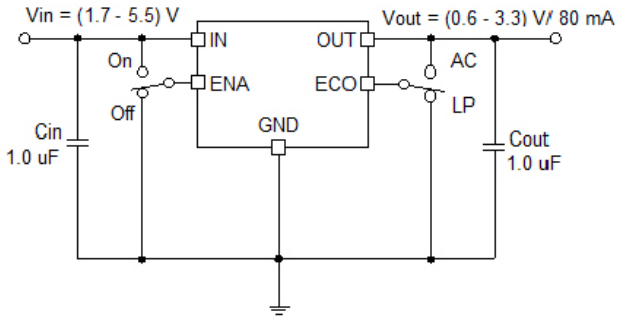

Figure 3. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 1.0 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP171. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1.0 μF ceramic output decoupling capacitor is sufficient to achieve stable operation of the IC. If tantalum capacitor is used, and its ESR is high, the loop oscillation may result. If output capacitor is composed from few ceramic capacitors in parallel, the operation can be unstable. The capacitor should be connected as close as possible to the output and ground pin. Larger values and lower ESR improves dynamic parameters. The maximum capacitor 4.7 μF could be connected to the output in order to keep stable operation.

ECO Mode, Voltage Scaling

The NCP171 has two distinct modes of operation, Active mode and Low Power mode, selectable with the ECO pin. When asserted low the ECO pin switches the device to Low Power mode with reduced load of 5 mA and while significantly reducing the quiescent current down to 50 nA. Further system level power reduction is made possible by reducing the output Voltage by the internally programmed offsets of 50 mV, 100 mV, 150 mV and 200 mV in Low Power mode. When asserted high the ECO pin switches the device to Active mode. Active mode features higher loads, up to 80 mA, Faster transient, High PSRR and lower noise.

Upon startup by Enable or Input Voltage the NCP171 defaults into Active mode, regardless of the state of the ECO pin, to enable fast and stable startup to the target output voltage. The duration of this enforced Active mode is typically 35 ms. This function helps to absorb high current spikes for the proper charging of output capacitor and startup current of the customer's application. The transitions from Low power mode to Active mode and reversely are depicted in Typical Characteristics chapter.

Enable Operation

The NCP171 device uses the ENA pin to enable/disable its device. If the ENA pin voltage is higher than 1.2 V the device is guaranteed to be enabled. The voltage below 0.4 V at the ENA pin assures turned−off output voltage. The active discharge transistor is active so that the output voltage VOUT is pulled to GND through the internal NMOS with $R_{DS(on)}$ about 50 ohms. In the disable state the device consumes as low as 30 nA from the VIN. In the case where the ENABLE function isn't required the ENA pin should be tied directly to VIN.

Thermal

As power across the NCP171 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature rise for the part. This is stating that when the NCP171 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation.

The power dissipation across the device can be roughly represented by the equation:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \ [W] \qquad \text{(eq. 1)}$$

The maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature differential between the junction and ambient, PCB orientation and the rate of air flow.

The maximum allowable power dissipation can be calculated using the following equation:

$$P_{MAX} = (T_{JUNCTION} - T_{AMBIENT})/\theta_{JA} \ [W] \qquad \text{(eq. 2)}$$

Where $(T_{JUNCTION} - T_{AMBIENT})$ is the temperature differential between the junction and the surrounding environment and θ_{JA} is the thermal resistance from the junction to the ambient.

Connecting the exposed pad or non connected pins to a large ground pad or plane helps to conduct away heat and improves thermal relief.

PCB layout

Make VIN and GND line sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

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TYPICAL CHARACTERISTICS

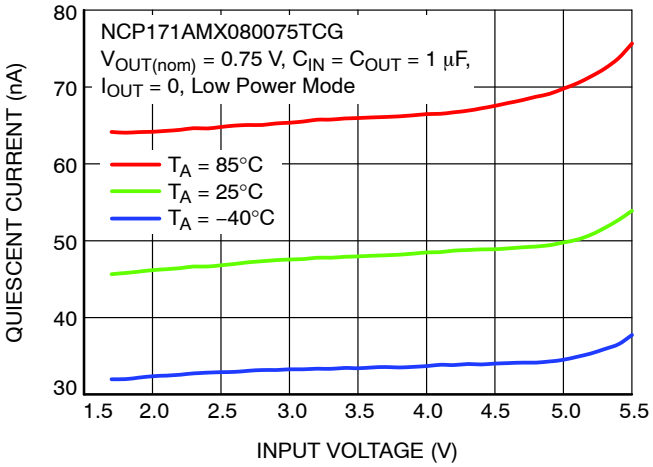

Figure 4. Quiescent Current vs. Input Voltage in Low Power Mode

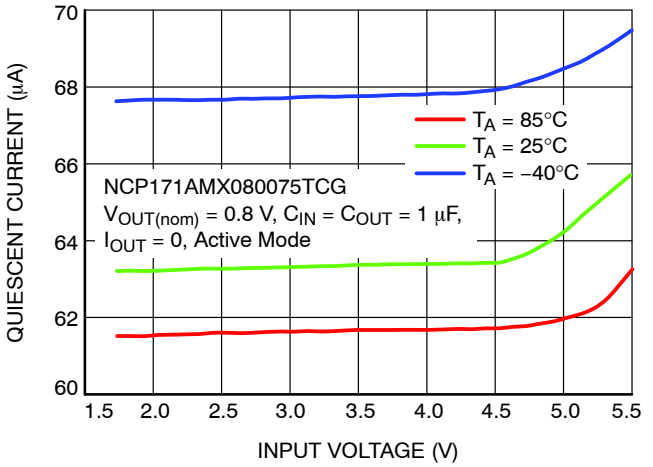

Figure 5. Quiescent Current vs. Input Voltage in Active Mode

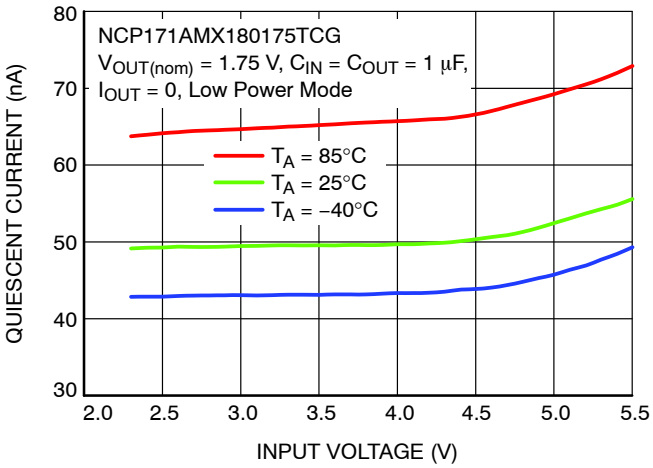

Figure 6. Quiescent Current vs. Input Voltage in Low Power Mode

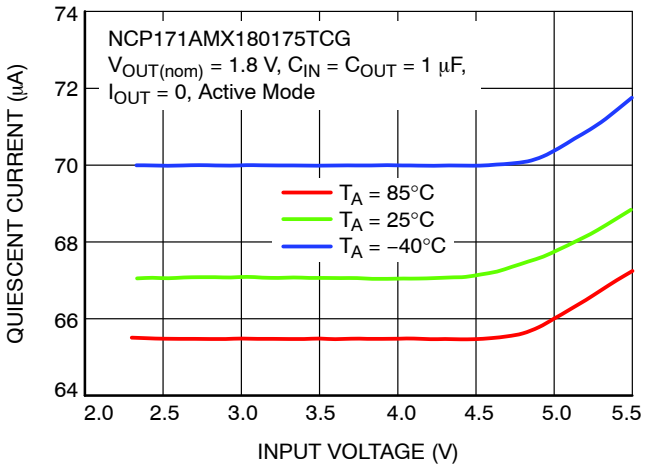

Figure 7. Quiescent Current vs. Input Voltage in Active Mode

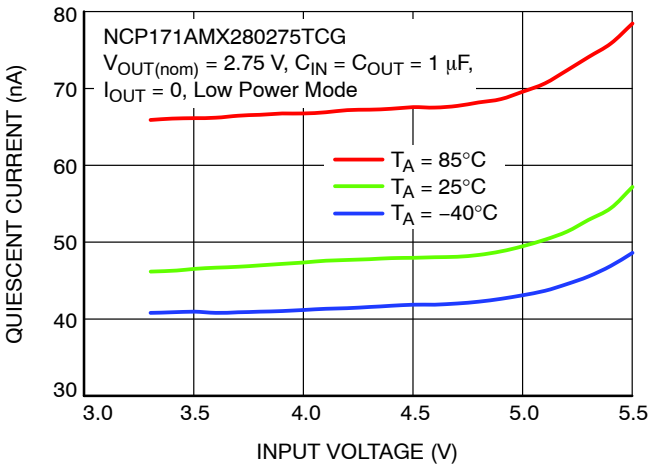

Figure 8. Quiescent Current vs. Input Voltage in Low Power Mode

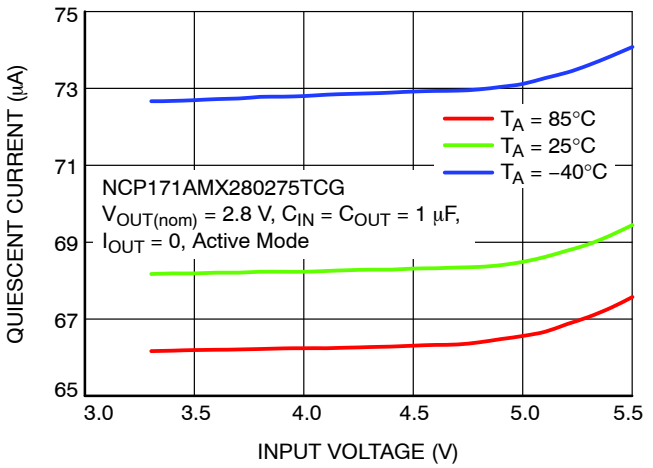

Figure 9. Quiescent Current vs. Input Voltage in Active Mode

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TYPICAL CHARACTERISTICS

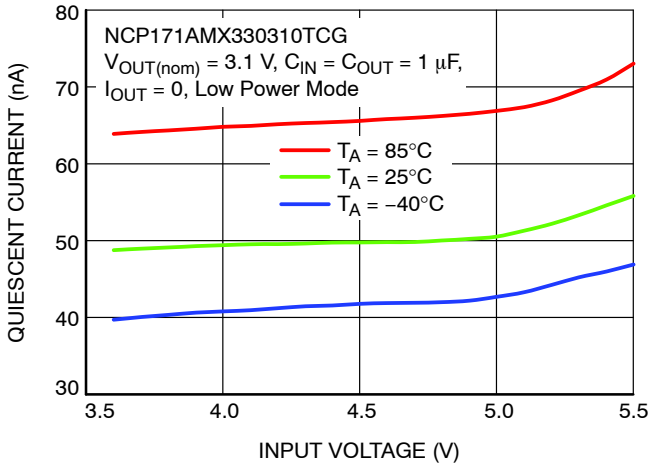

Figure 10. Quiescent Current vs. Input Voltage in Low Power Mode

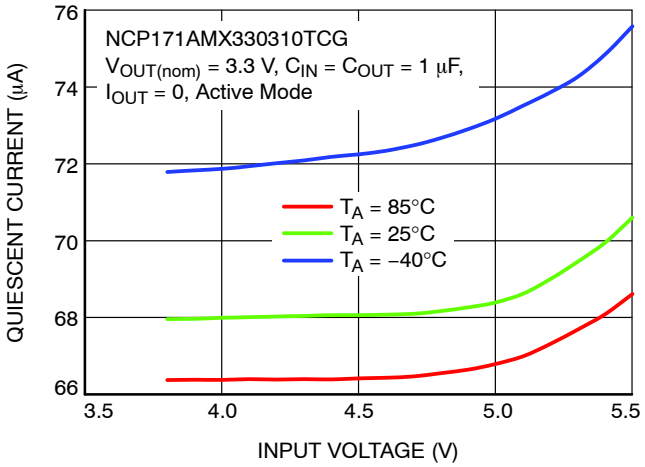

Figure 11. Quiescent Current vs. Input Voltage in Active Mode

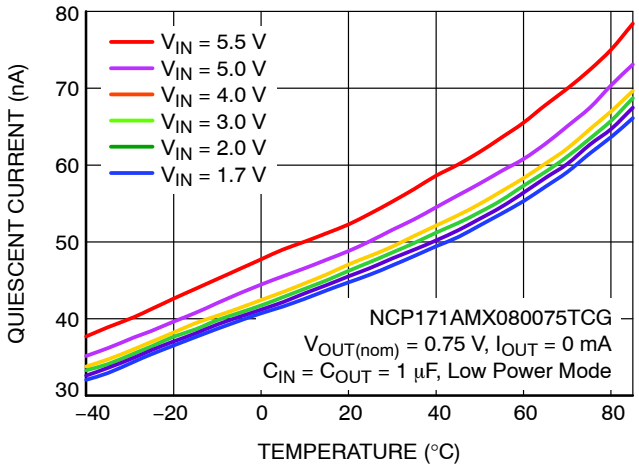

Figure 12. Quiescent Current vs. Temperature in Low Power Mode

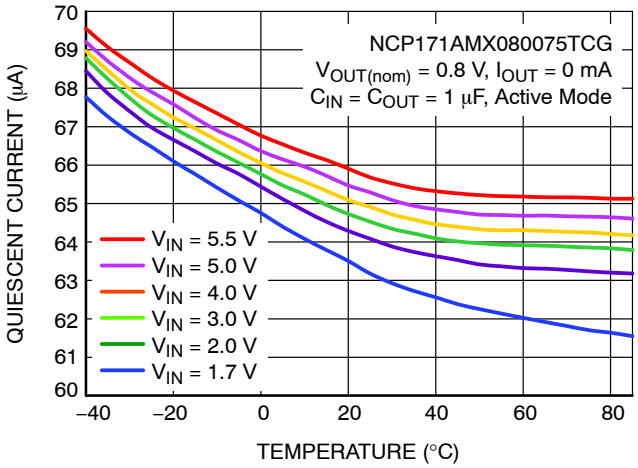

Figure 13. Quiescent Current vs. Temperature in Active Mode

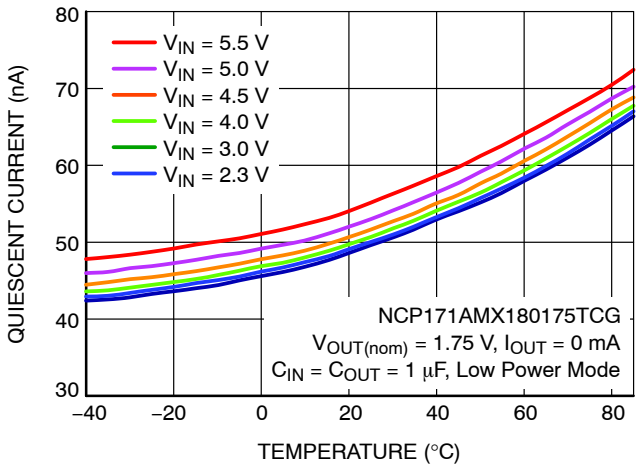

Figure 14. Quiescent Current vs. Temperature in Low Power Mode

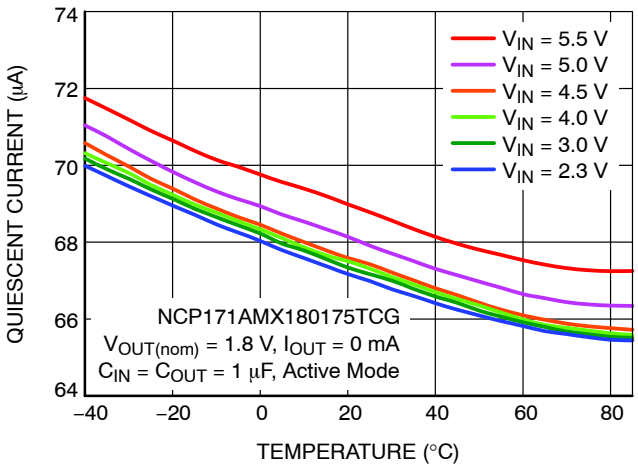

Figure 15. Quiescent Current vs. Temperature in Active Mode

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TYPICAL CHARACTERISTICS

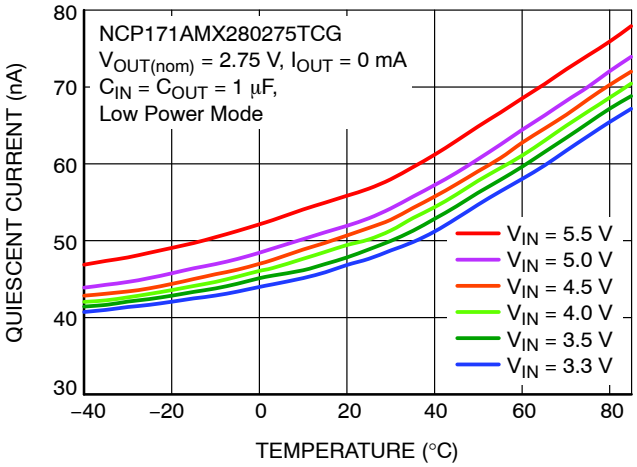

Figure 16. Quiescent Current vs. Temperature in Low Power Mode

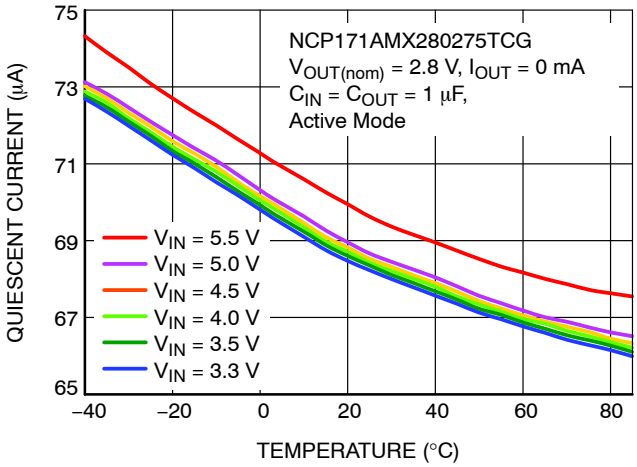

Figure 17. Quiescent Current vs. Temperature in Active Mode

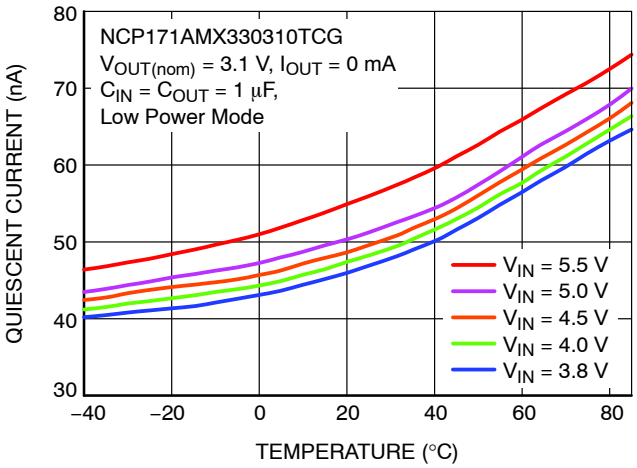

Figure 18. Quiescent Current vs. Temperature in Low Power Mode

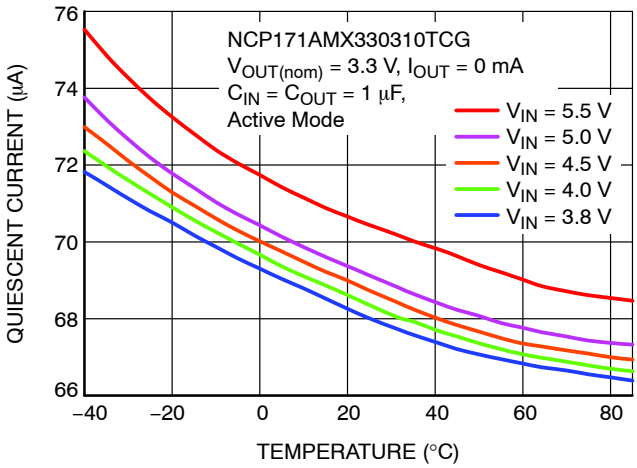

Figure 19. Quiescent Current vs. Temperature in Active Mode

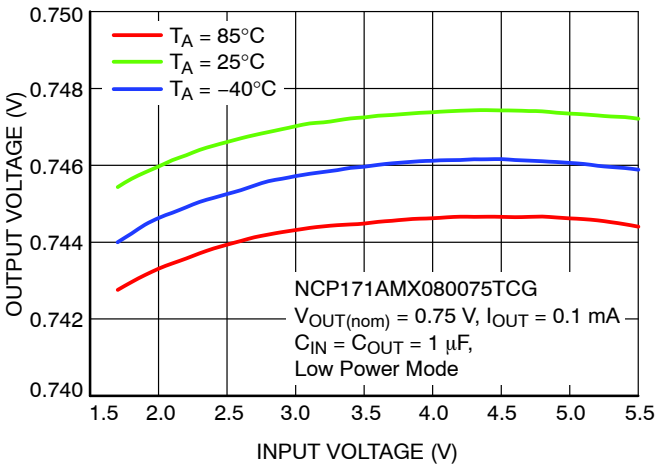

Figure 20. Output Voltage vs. Input Voltage in Low Power Mode

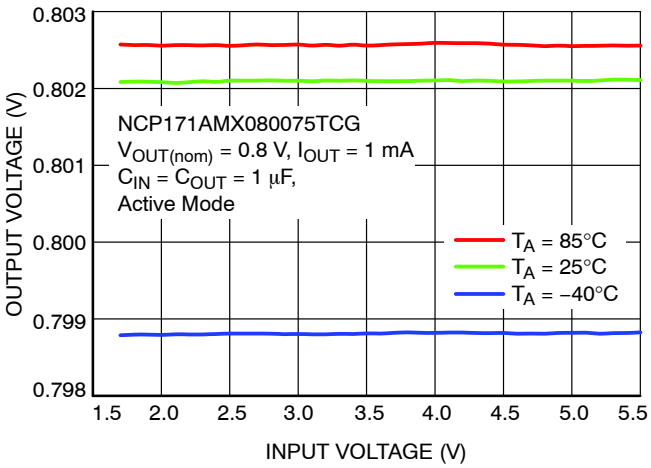

Figure 21. Output Voltage vs. Input Voltage in Active Mode

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TYPICAL CHARACTERISTICS

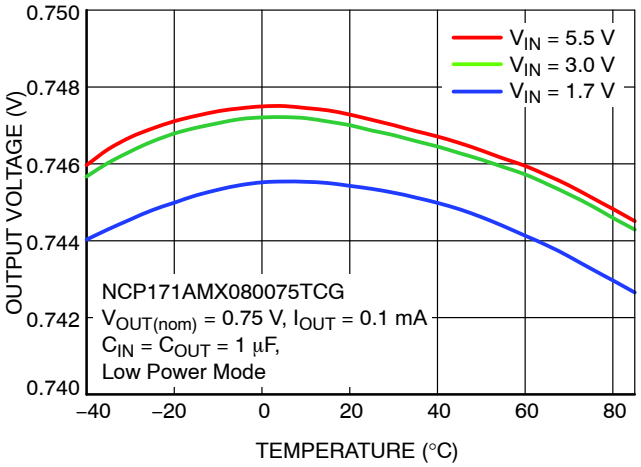

Figure 22. Output Voltage vs. Temperature in Low Power Mode

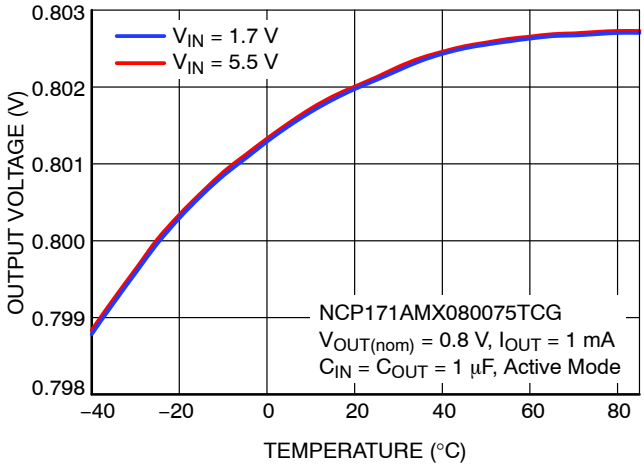

Figure 23. Output Voltage vs. Temperature in Active Mode

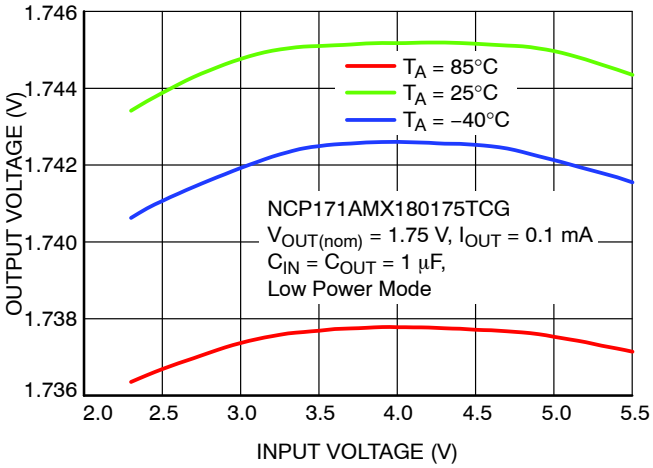

Figure 24. Output Voltage vs. Input Voltage in Low Power Mode

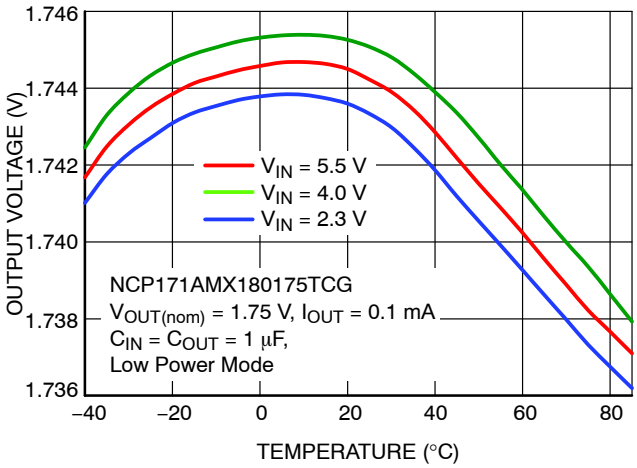

Figure 25. Output Voltage vs Temperature in Low Power Mode

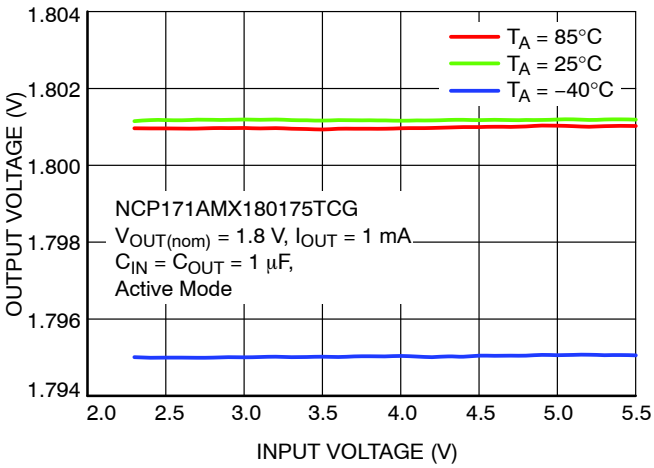

Figure 26. Output Voltage vs. Input Voltage in Active Mode

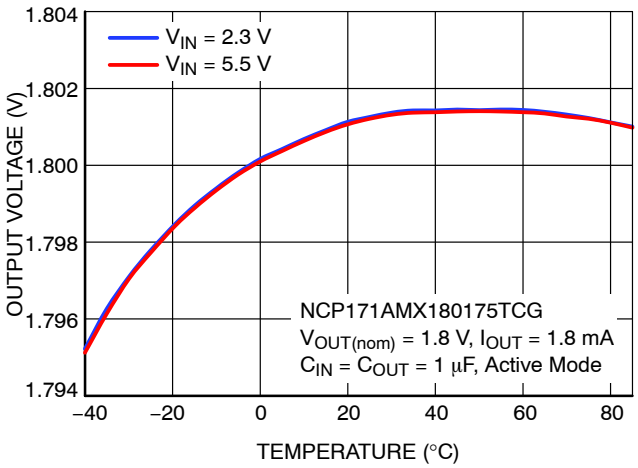

Figure 27. Output Voltage vs. Temperature in Active Mode

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TYPICAL CHARACTERISTICS

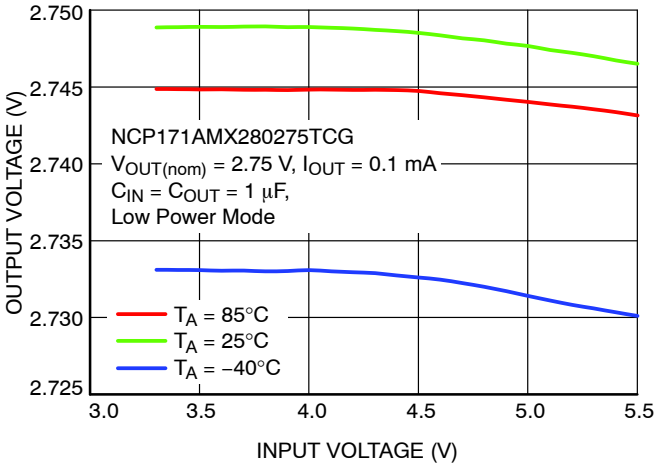

Figure 28. Output Voltage vs. Input Voltage in Low Power Mode

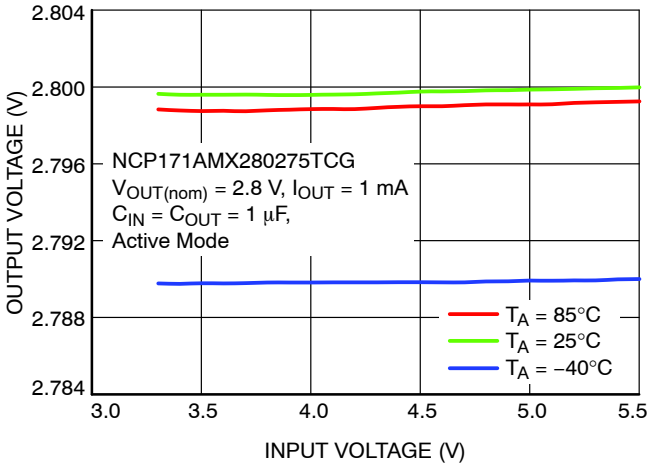

Figure 29. Output Voltage vs. Input Voltage in Active Mode

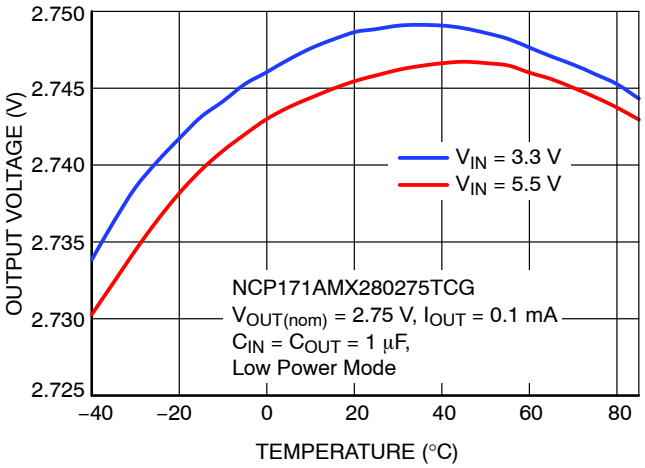

Figure 30. Output Voltage vs. Temperature in Low Power Mode

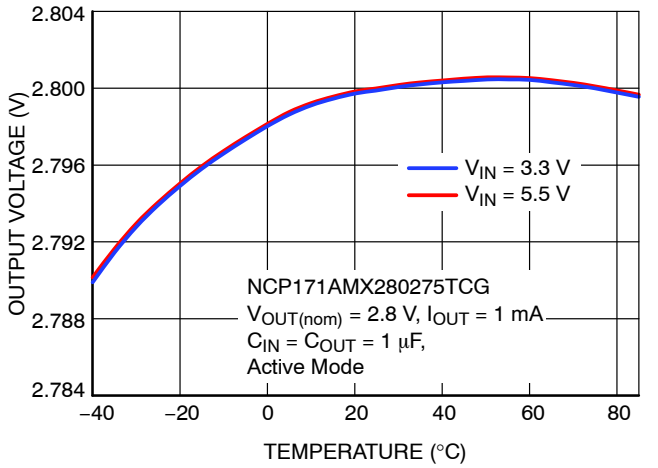

Figure 31. Output Voltage vs Temperature in Active Mode

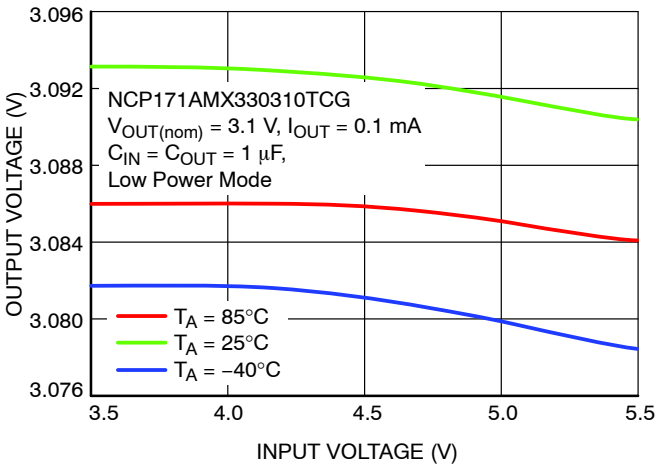

Figure 32. Output Voltage vs. Input Voltage in Low Power Mode

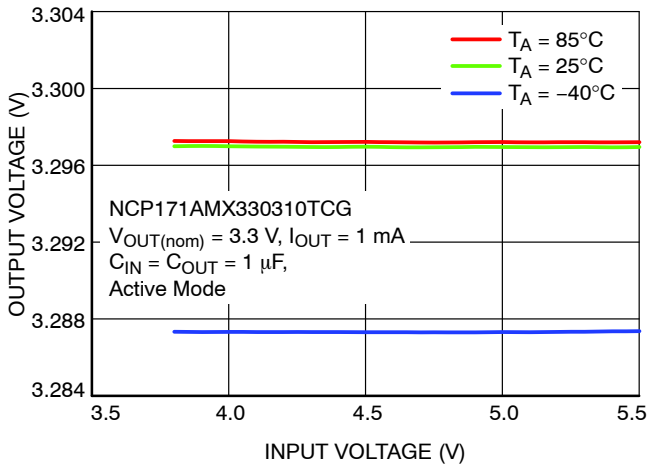

Figure 33. Output Voltage vs. Input Voltage in Active Mode

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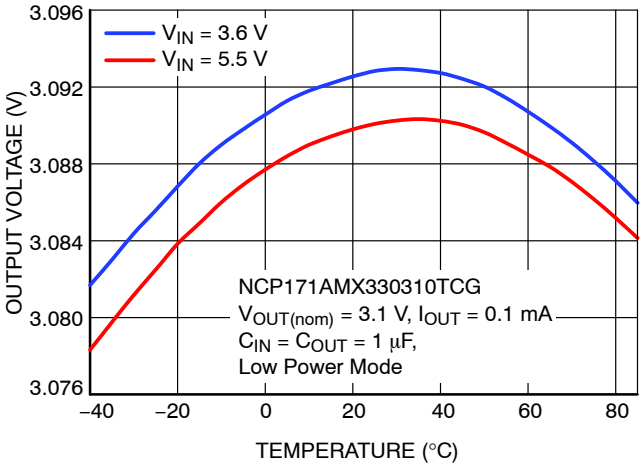

Figure 34. Output Voltage vs. Temperature in Low Power Mode

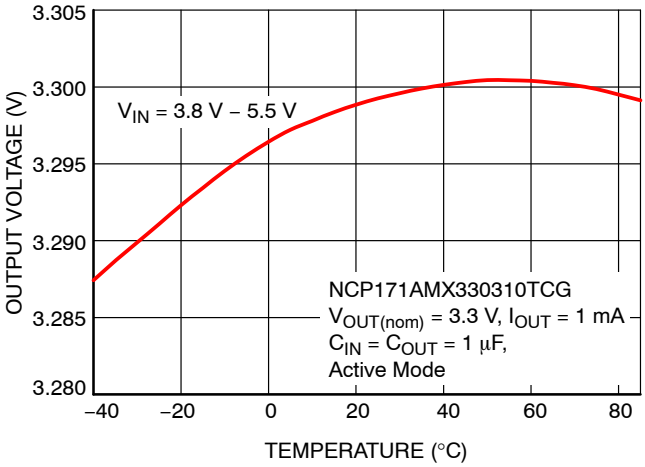

Figure 35. Output Voltage vs. Temperature in Active Mode

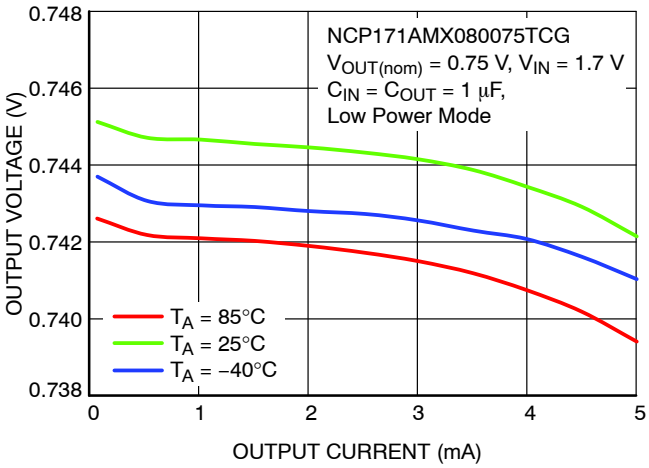

Figure 36. Output Voltage vs. Output Current in Low Power Mode

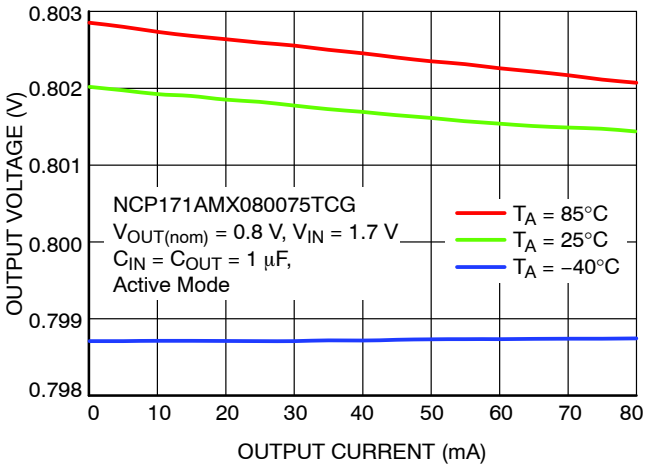

Figure 37. Output Voltage vs. Output Current in Active Mode

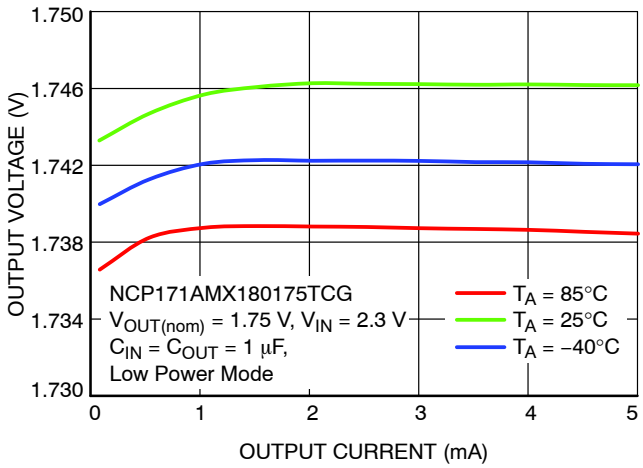

Figure 38. Output Voltage vs. Output Current in Low Power Mode

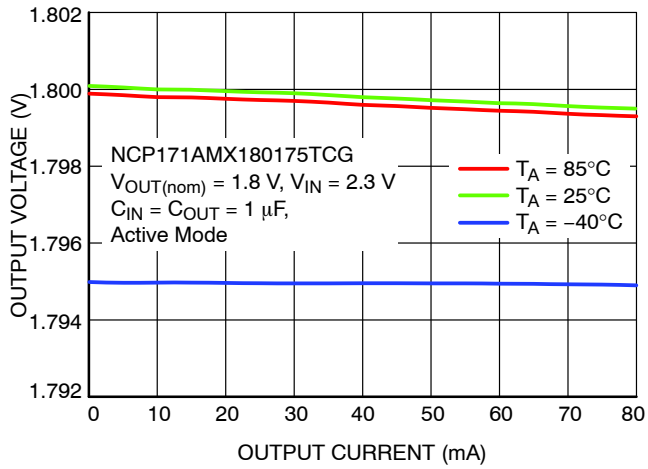

Figure 39. Output Voltage vs. Output Current in Active Mode

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TYPICAL CHARACTERISTICS

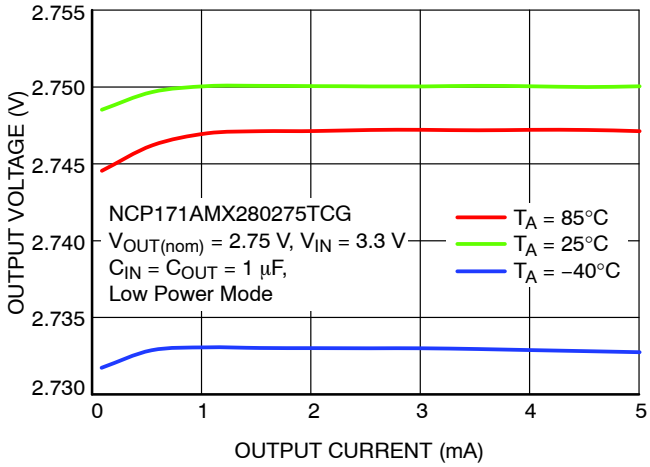

Figure 40. Output Voltage vs. Output Current in Low Power Mode

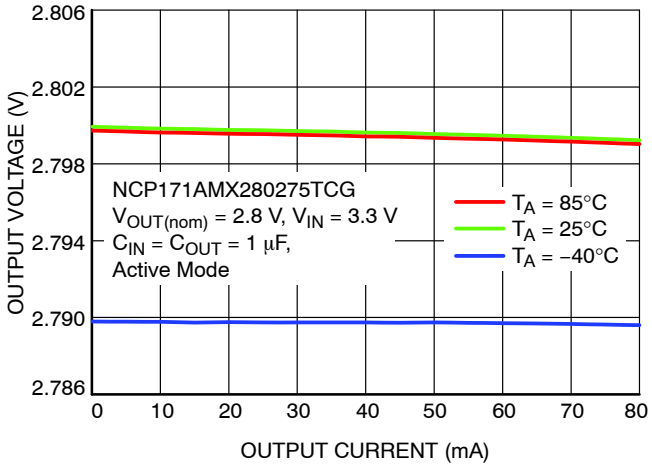

Figure 41. Output Voltage vs. Output Current in Active Mode

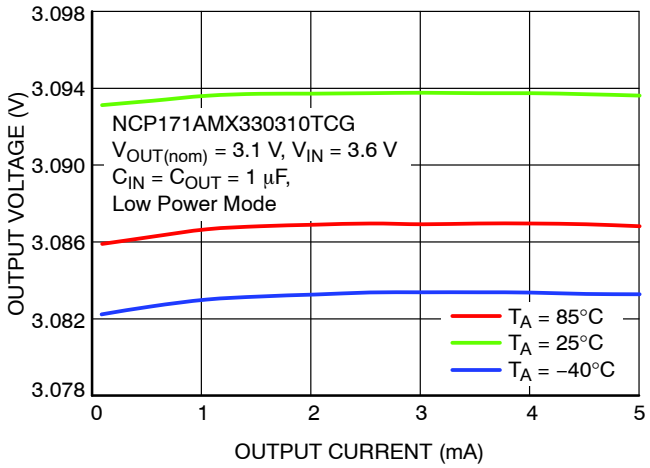

Figure 42. Output Voltage vs. Output Current in Low Power Mode

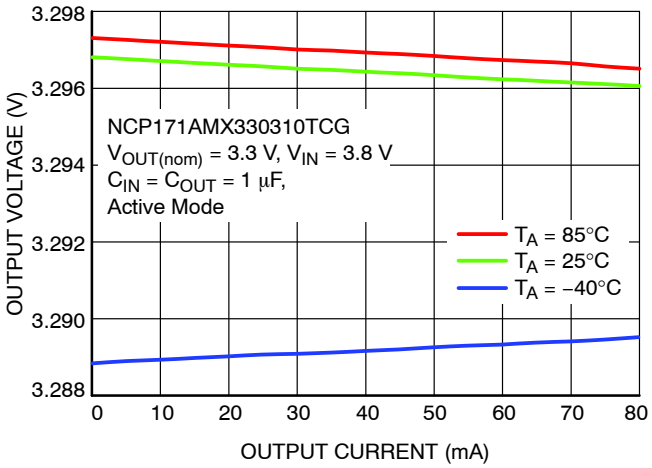

Figure 43. Output Voltage vs. Output Current in Active Mode

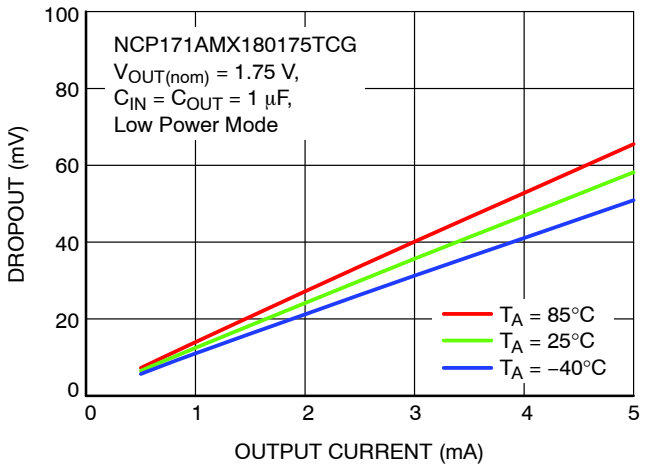

Figure 44. Dropout vs. Output Current in Low Power Mode

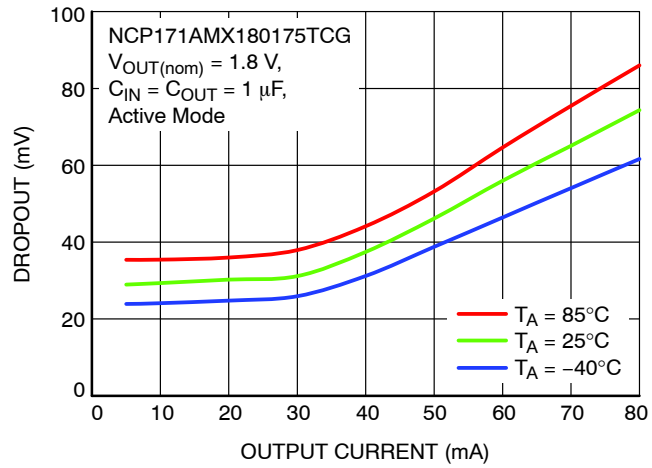

Figure 45. Dropout vs. Output Current in Active Mode

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TYPICAL CHARACTERISTICS

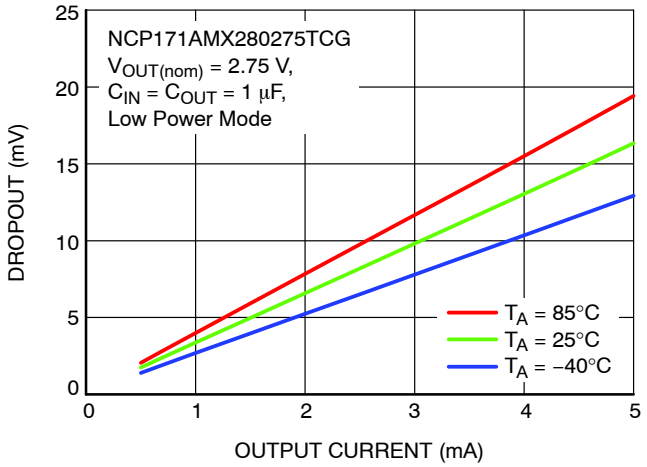

Figure 46. Dropout vs. Output Current in Low Power Mode

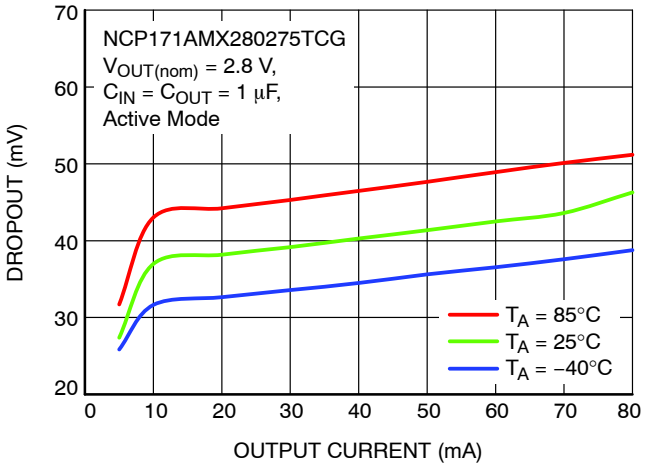

Figure 47. Dropout vs. Output Current in Active Mode

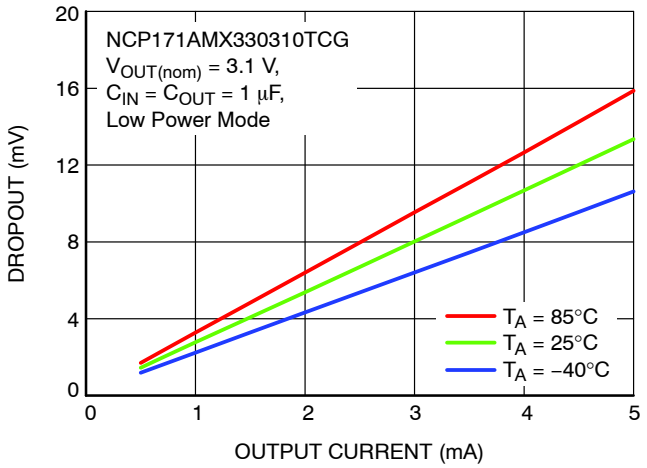

Figure 48. Dropout vs. Output Current in Low Power Mode

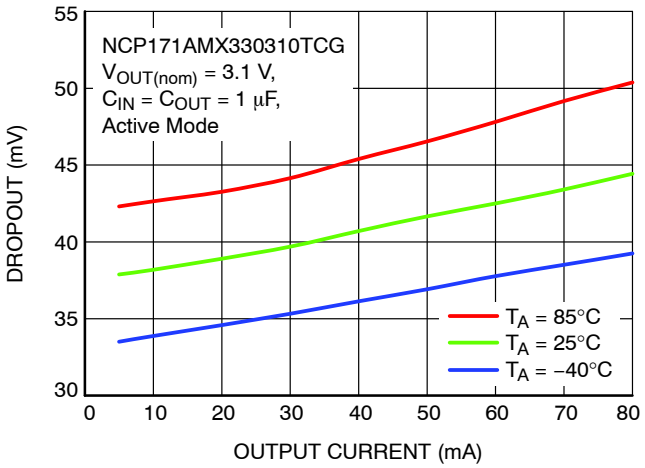

Figure 49. Dropout vs. Output Current in Active Mode

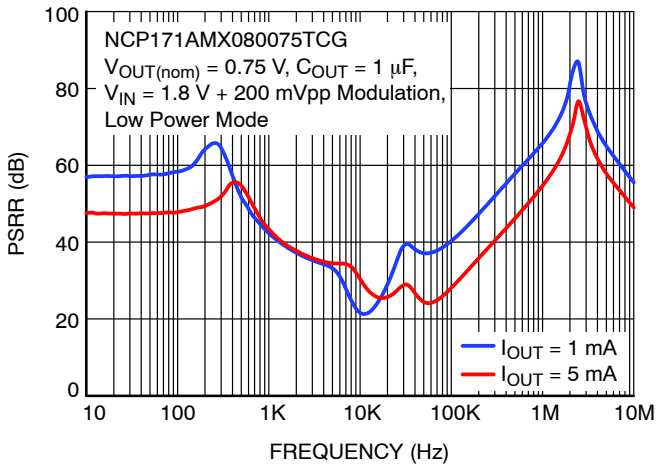

Figure 50. PSRR vs. Frequency in Low Power Mode

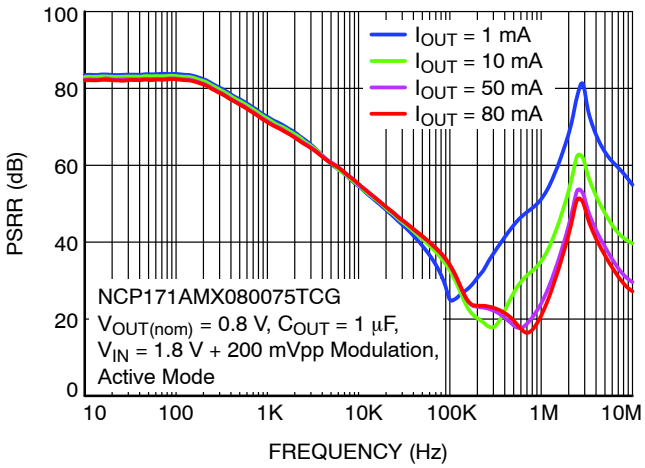

Figure 51. PSRR vs. Frequency in Active Mode

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TYPICAL CHARACTERISTICS

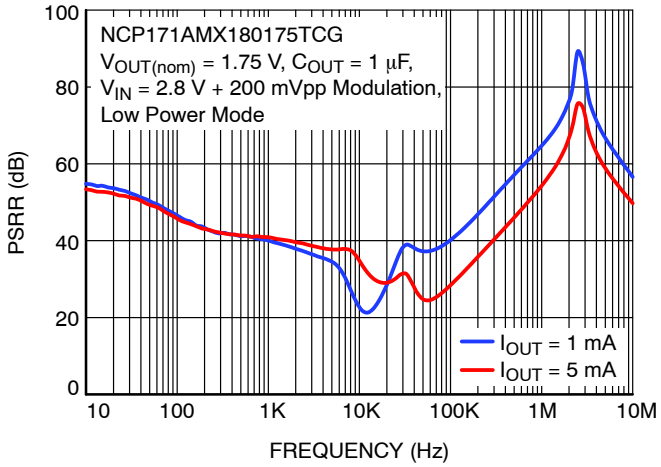

Figure 52. PSRR vs. Frequency in Low Power Mode

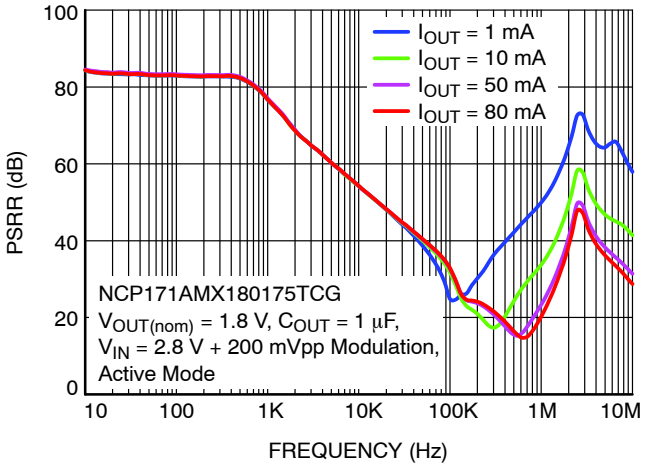

Figure 53. PSRR vs. Frequency in Active Mode

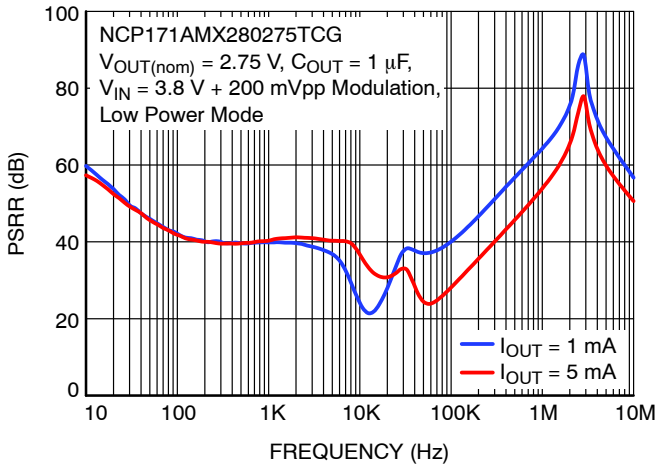

Figure 54. PSRR vs. Frequency in Low Power Mode

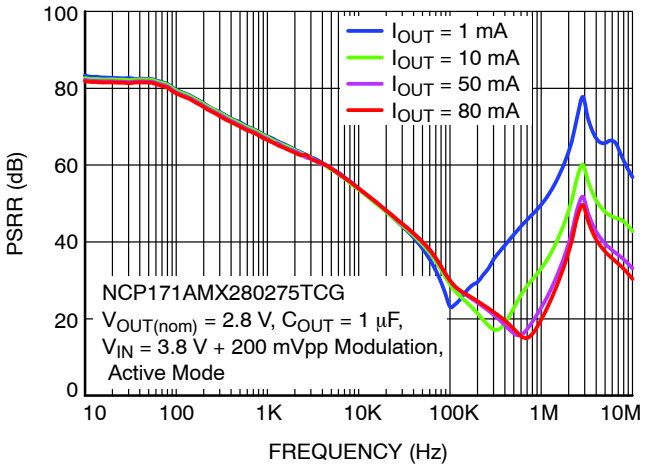

Figure 55. PSRR vs. Frequency in Active Mode

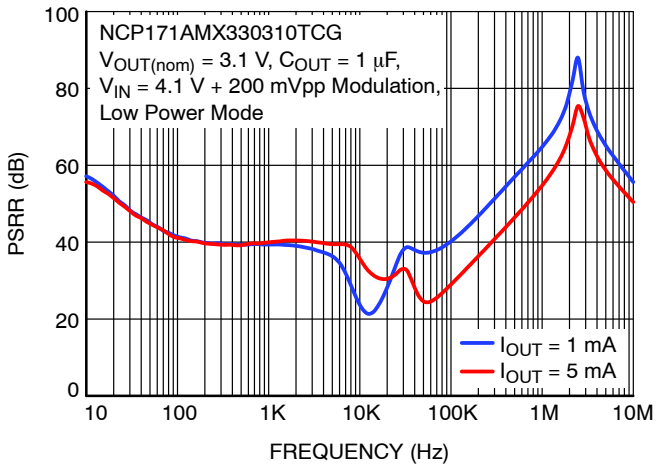

Figure 56. PSRR vs. Frequency in Low Power Mode

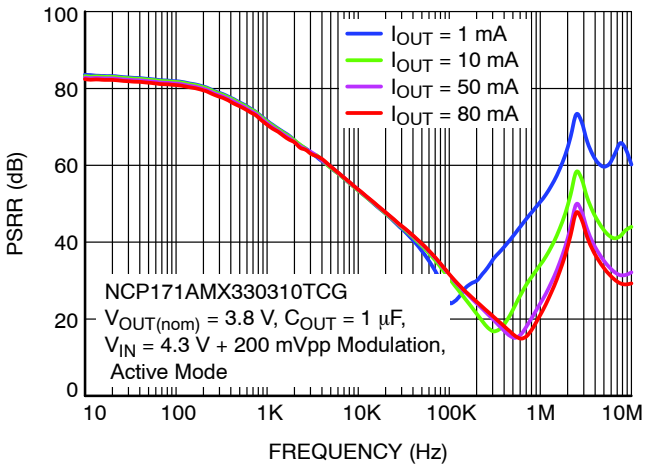

Figure 57. PSRR vs. Frequency in Active Mode

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TYPICAL CHARACTERISTICS

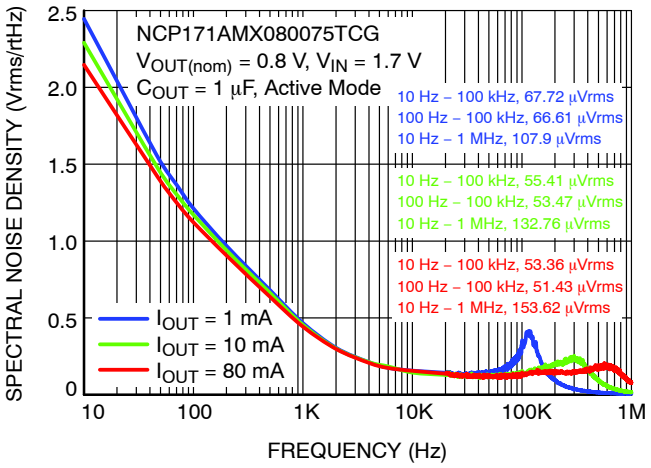

Figure 58. Noise vs. Frequency

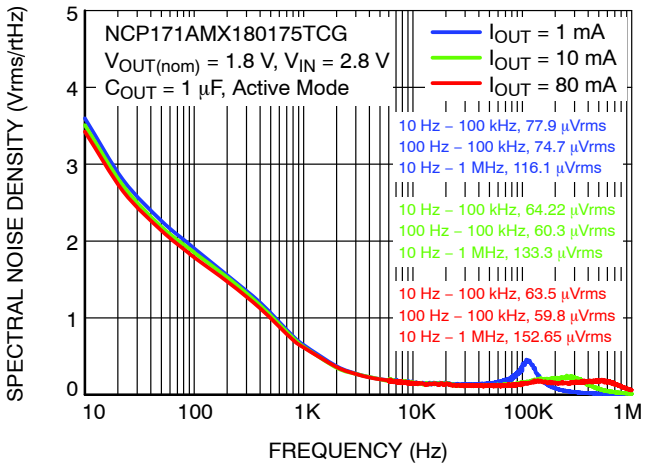

Figure 59. Noise vs. Frequency

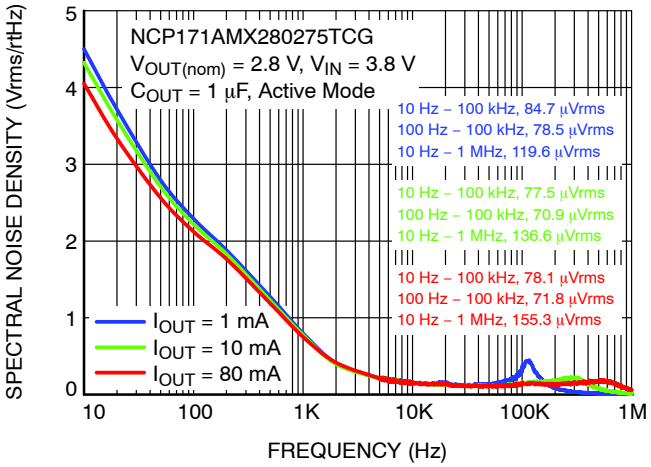

Figure 60. Noise vs. Frequency

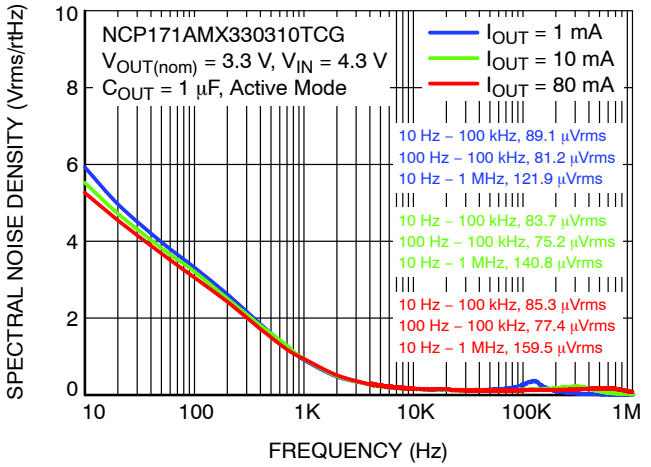

Figure 61. Noise vs. Frequency

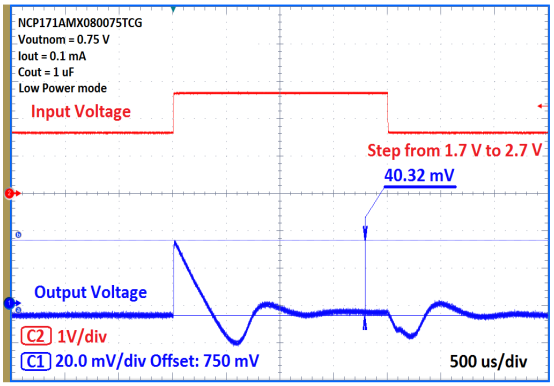

Figure 62. Line Transient Response in Low Power Mode

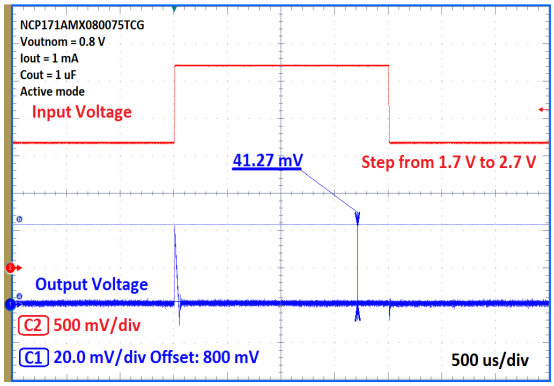

Figure 63. Line Transient Response in Active Mode

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TYPICAL CHARACTERISTICS

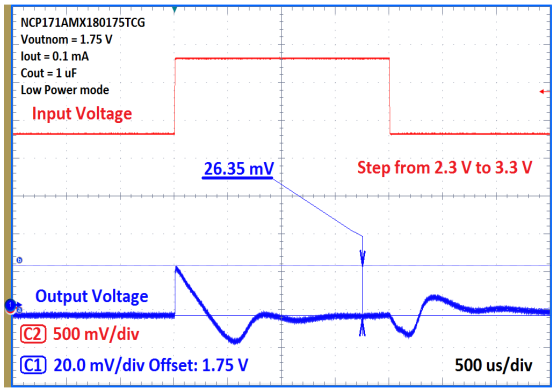

Figure 64. Line Transient Response in Low Power Mode

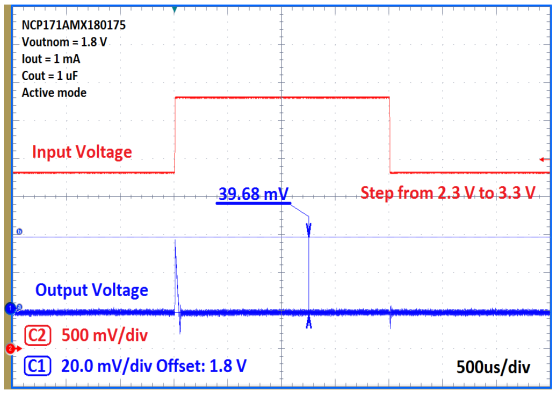

Figure 65. Line Transient Response in Active Mode

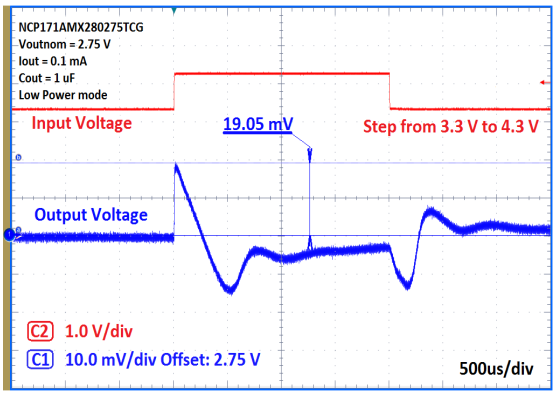

Figure 66. Line Transient Response in Low Power Mode

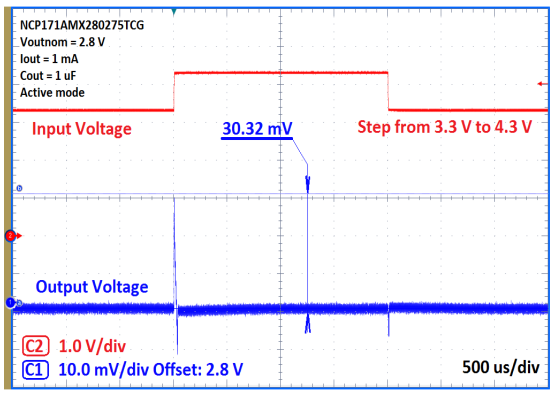

Figure 67. Line Transient Response in Active Mode

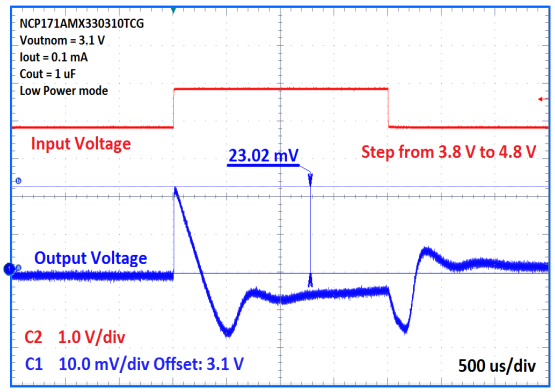

Figure 68. Line Transient Response in Low Power Mode

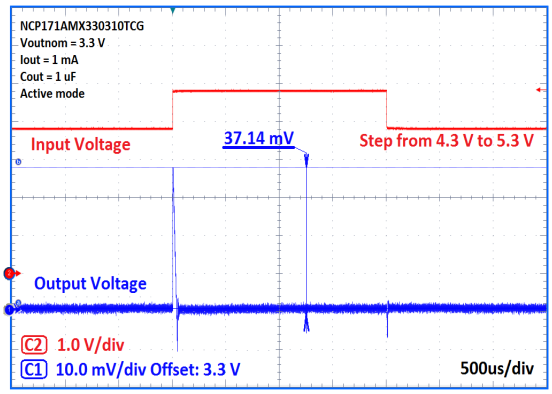

Figure 69. Line Transient Response in Active Mode

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TYPICAL CHARACTERISTICS

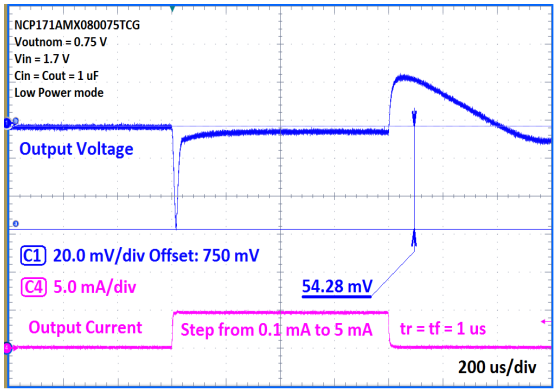

Figure 70. Load Transient Response in Low Power Mode

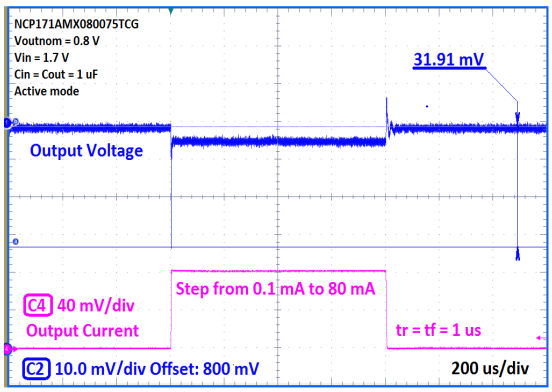

Figure 71. Load Transient Response in Active Mode

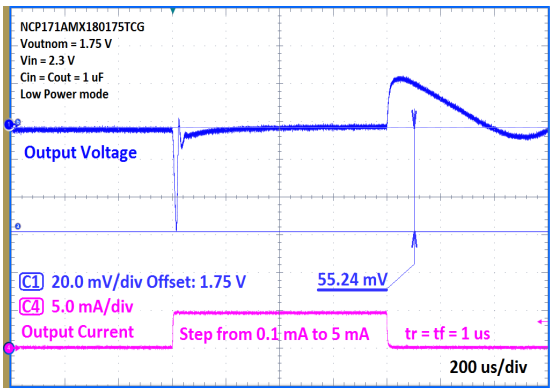

Figure 72. Load Transient Response in Low Power Mode

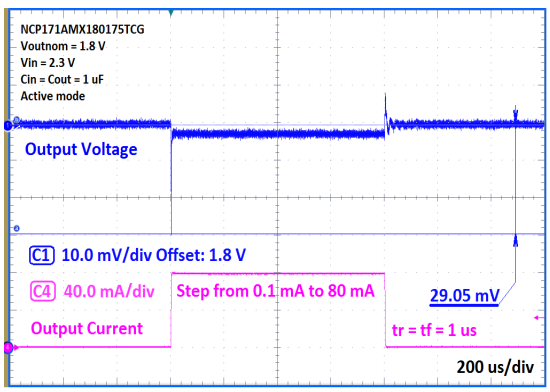

Figure 73. Load Transient Response in Active Mode

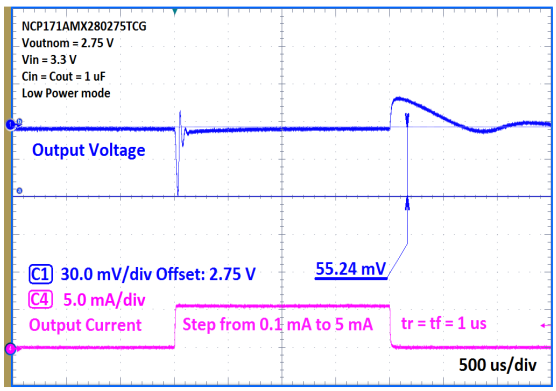

Figure 74. Load Transient Response in Low Power Mode

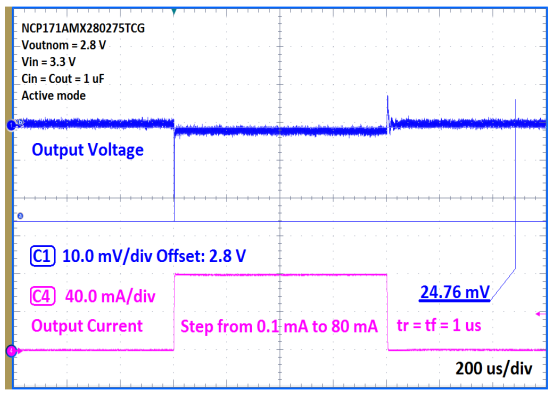

Figure 75. Load Transient Response in Active Mode

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TYPICAL CHARACTERISTICS

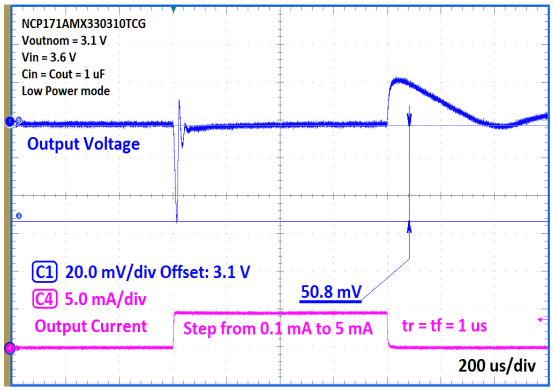

Figure 76. Load Transient Response in Low Power Mode

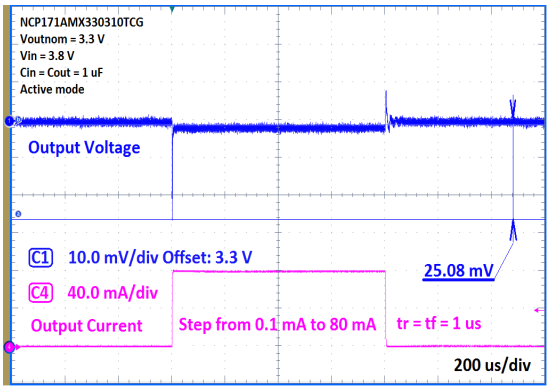

Figure 77. Load Transient Response in Active Mode

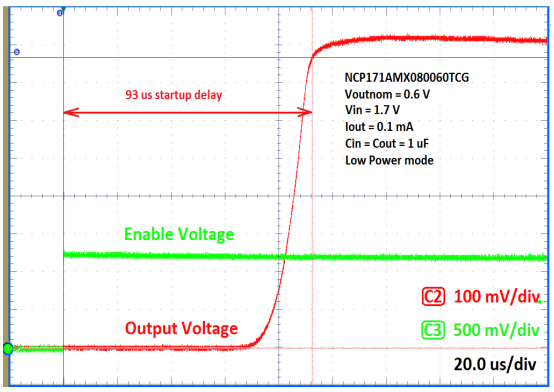

Figure 78. Startup by Enable in Low Power Mode

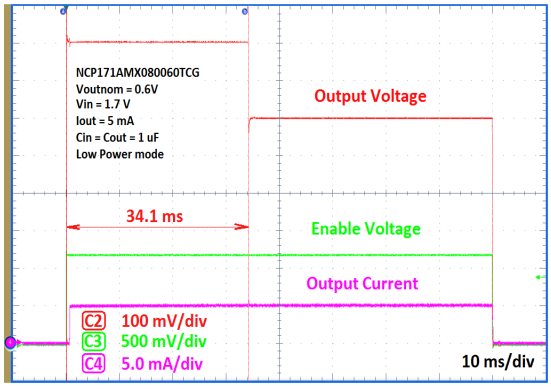

Figure 79. Startup by Enable in Low Power Mode

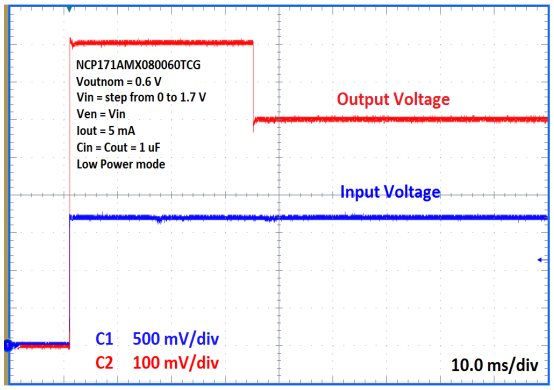

Figure 80. Startup by Input Voltage in Low Power Mode

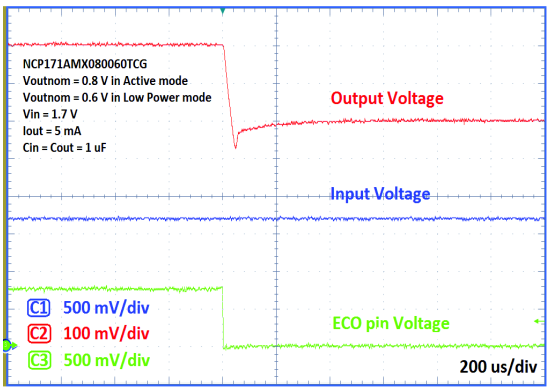

Figure 81. Output Voltage vs. ECO Voltage

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TYPICAL CHARACTERISTICS

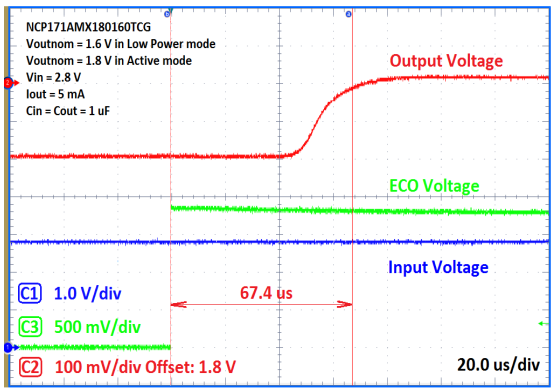

Figure 82. Transition from Low Power Mode to Active Mode

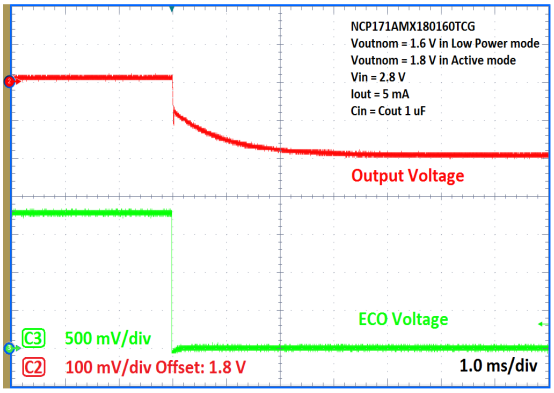

Figure 83. Transition from Active Mode to Low Power Mode

ORDERING INFORMATION

Device	Nominal Output Voltage	Output Voltage Offset	Marking	Active Discharge	Package	Shipping†
NCP171AMX080075TCG (Note 9)	0.8 V	50 mV	JA	Yes	XDFN4 CASE 711BC (Pb−Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP171AMX080060TCG (Note 9)	0.8 V	200 mV	JT	Yes		
NCP171AMX100080TCG (Note 9)	1.0 V	200 mV	JP	Yes		
NCP171AMX120100TCG (Note 9)	1.2 V	200 mV	JM	Yes		
NCP171AMX165160TCG (Note 9)	1.65 V	50 mV	JL	Yes		
NCP171AMX170165TCG (Note 9)	1.7 V	50 mV	JN	Yes		
NCP171A3MX170165TCG (Note 9)	1.7 V	50 mV	JQ	Yes		
NCP171AMX180175TCG (Note 9)	1.8 V	50 mV	JU	Yes		
NCP171AMX250245TCG	2.5 V	50 mV	JD	Yes		
NCP171AMX280275TCG (Note 9)	2.8 V	50 mV	JH	Yes		
NCP171AMX330325TCG (Note 9)	3.3 V	50 mV	JE	Yes		
NCP171AMX330310TCG (Note 9)	3.3 V	200 mV	JF	Yes		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. Product processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel

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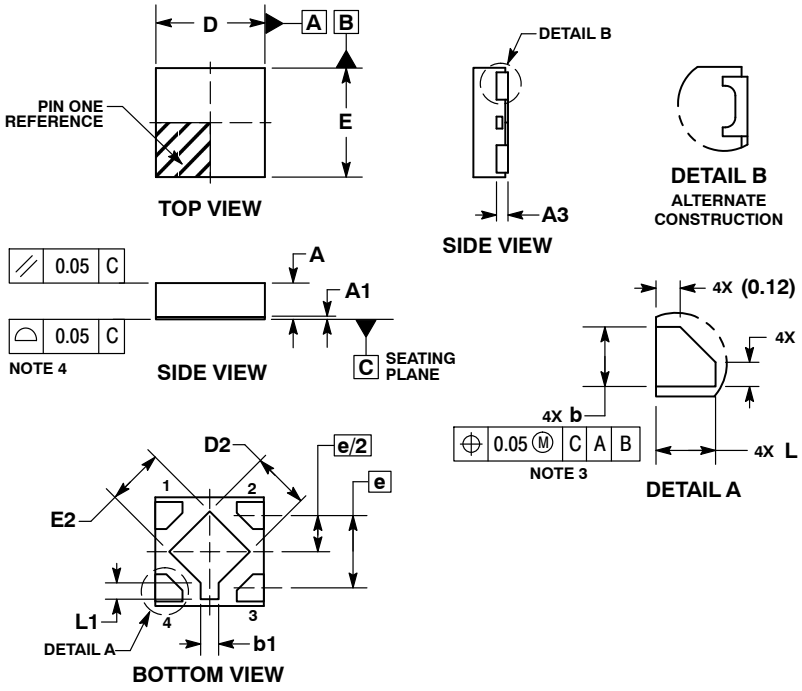
XDFN4 1.2x1.2, 0.8P
CASE 711BC
ISSUE O

DATE 15 SEP 2015

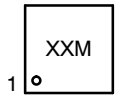
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.35	0.45
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
b1	0.15	0.25
D	1.15	1.25
D2	0.58	0.68
E	1.15	1.25
E2	0.58	0.68
e	0.80 BSC	
L	0.25	0.35
L1	0.13	0.23

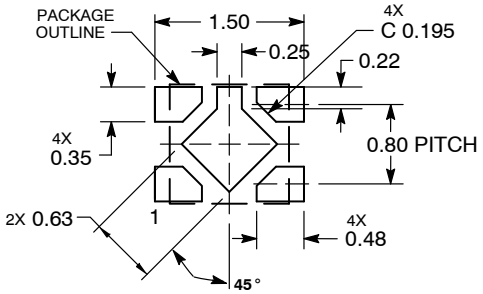
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**XDFN4, 1.2X1.2, 0.8P**		**PAGE 1 OF 1**

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