Automotive MOSFET

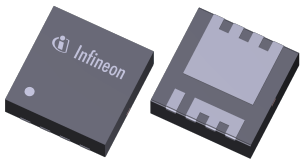
OptiMOS™ 7 Power-Transistor

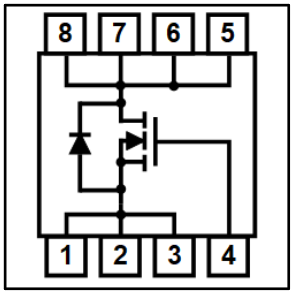
RoHS Infineon Automotive Quality AEC Qualified

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

PG-TSDSON-8-44





Potential Applications

General automotive applications.

Product Validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	100	V
$R_{DS(on)}$	28.9	mΩ
I_D (chip limited)	27	A

Type	Package	Marking
IAUZN10S7L289	PG-TSDSON-8-44	1B

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Maximum Ratings

at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS} = 10 V, Chip limitation[1,2)]	27	A
		V_{GS} = 10 V, DC current	27	
		T_a = 100°C, V_{GS} = 10 V, R_{thJA} on 2s2p[2,3)]	5	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C = 25°C, t_p = 100 µs	54	
Avalanche energy, single pulse[2)]	E_{AS}	I_D = 9 A	11.8	mJ
Avalanche current, single pulse	I_{AS}	–	18	A
Gate source voltage	V_{GS}	–	±16	V
		Limited to duty factor of 1%	+20	
Power dissipation	P_{tot}	T_C = 25°C	45	W
Operating temperature	T_j	–	-55 ... +175	°C

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Thermal Characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	3.3	K/W
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	–	41.0	–	

Electrical Characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static Characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = 1 mA	100	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 9 µA	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V, T_j = 25°C	–	–	1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_j = 100°C[2)]	–	–	3	
Gate-source leakage current	I_{GSS}	V_{GS} = 16 V, V_{DS} = 0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 14 A	–	28.9	38.5	mΩ
		V_{GS} = 10 V, I_D = 14 A	–	25.8	28.9	
Gate resistance[2)]	R_G	–	–	1.2	–	Ω

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics[2]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	–	428	557	pF
Output capacitance	C_{oss}		–	180	234	
Reverse transfer capacitance	C_{rss}		–	5	8	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 50 V, V_{GS} = 10 V, I_D = 14 A, R_G = 3.5 Ω	–	1.6	–	ns
Rise time	t_r		–	1.2	–	
Turn-off delay time	$t_{d(off)}$		–	9.1	–	
Fall time	t_f		–	2.6	–	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD} = 50 V, I_D = 14 A, V_{GS} = 0 to 10 V	–	1.4	1.8	nC
Gate to drain charge	Q_{gd}		–	1.5	2.3	
Gate charge total	Q_g		–	10.9	14.2	
Gate plateau voltage	$V_{plateau}$		–	3.2	–	V
Reverse Diode						
Diode continuous forward current[2]	I_S	T_C = 25°C	–	–	27	A
Diode pulse current[2]	$I_{S,pulse}$	T_C = 25°C, t_p = 100 µs	–	–	54	
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 14 A, T_j = 25°C	–	0.9	1.0	V
Reverse recovery time[2]	t_{rr}	V_R = 50 V, I_F = 27 A, di_F/dt = 100 A/µs	–	21	32	ns
Reverse recovery charge[2]	Q_{rr}		–	8	16	nC

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

[2] The parameter is not subject to production testing – specified by design.

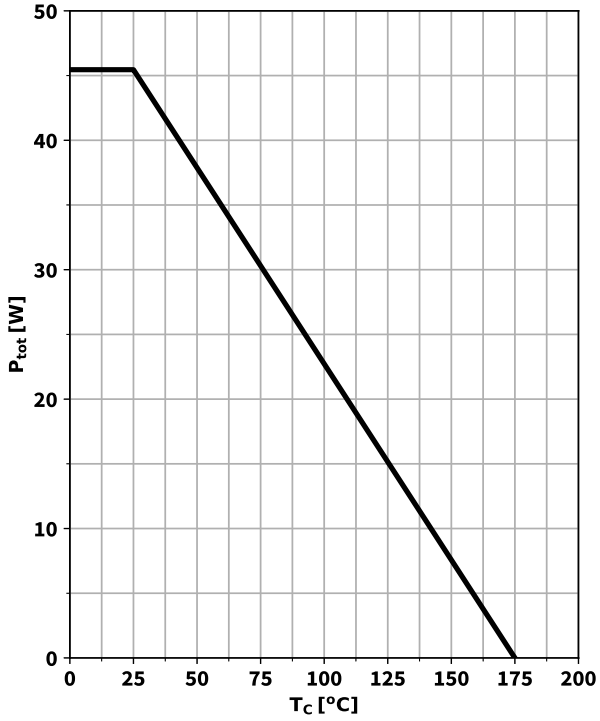
[3] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

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Electrical characteristics diagrams

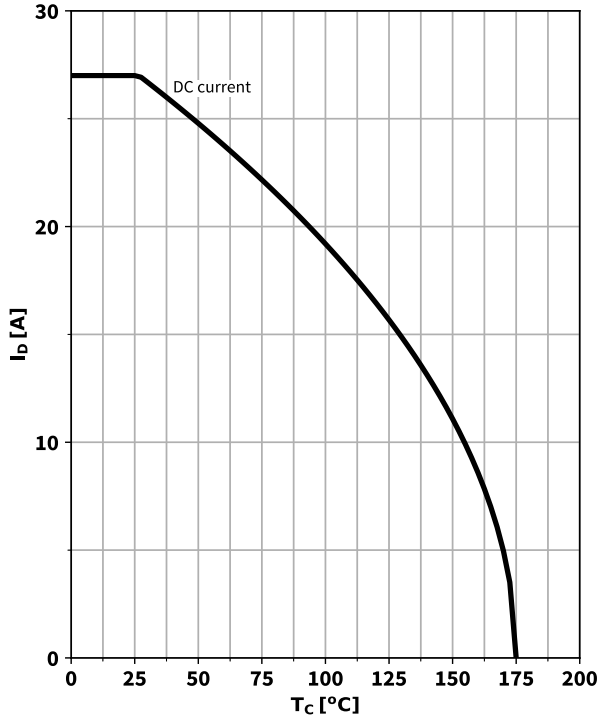
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



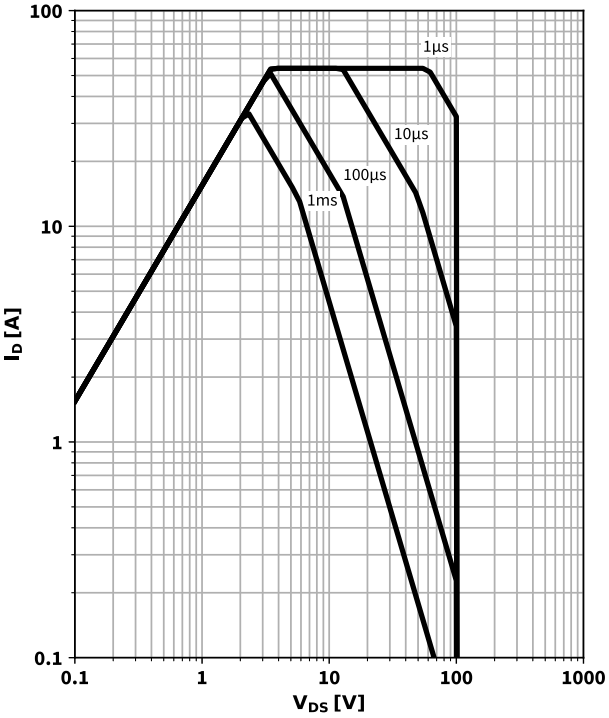
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



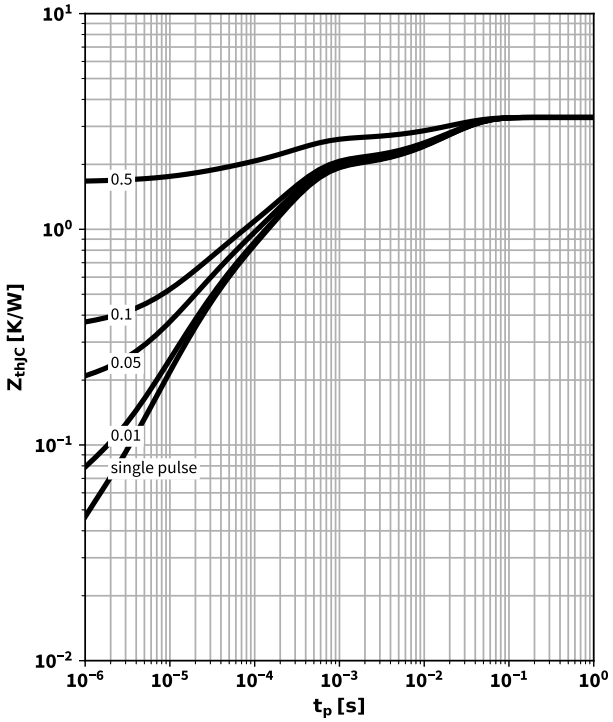
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



4 Max. transient thermal impedance

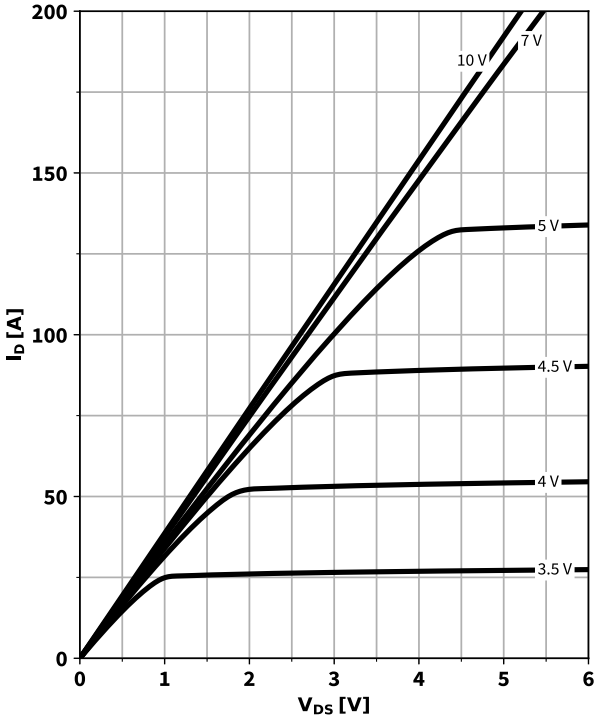
$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$



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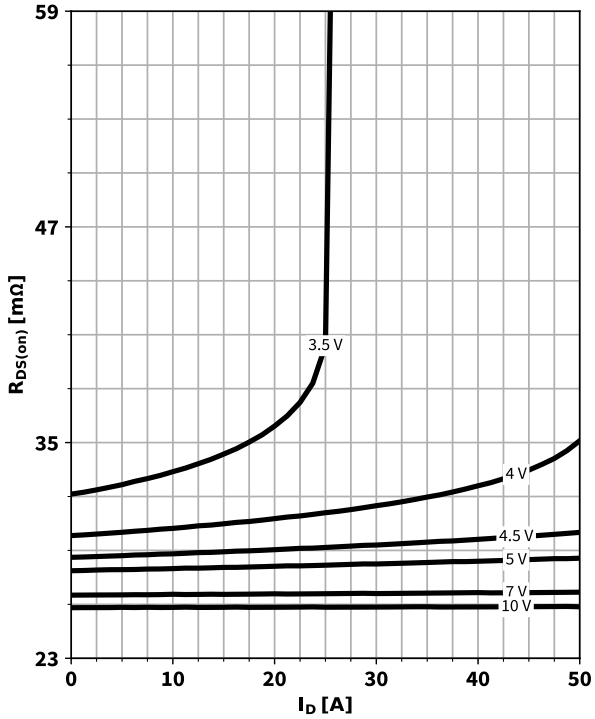
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



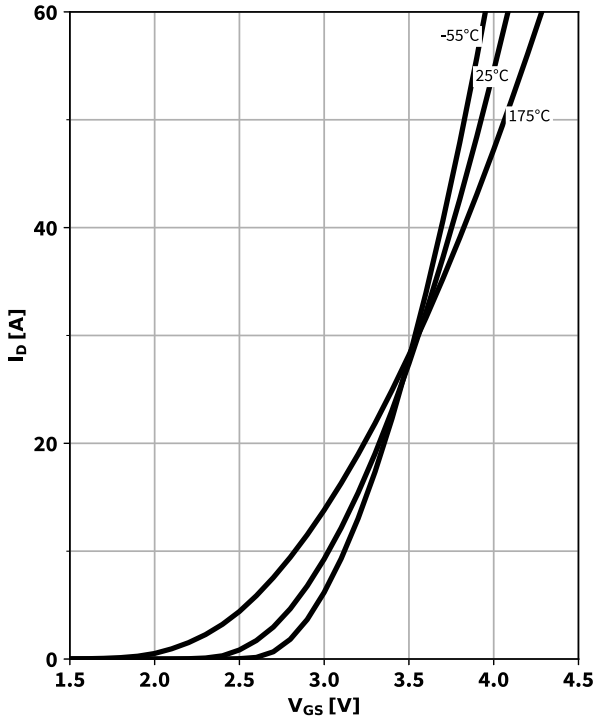
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



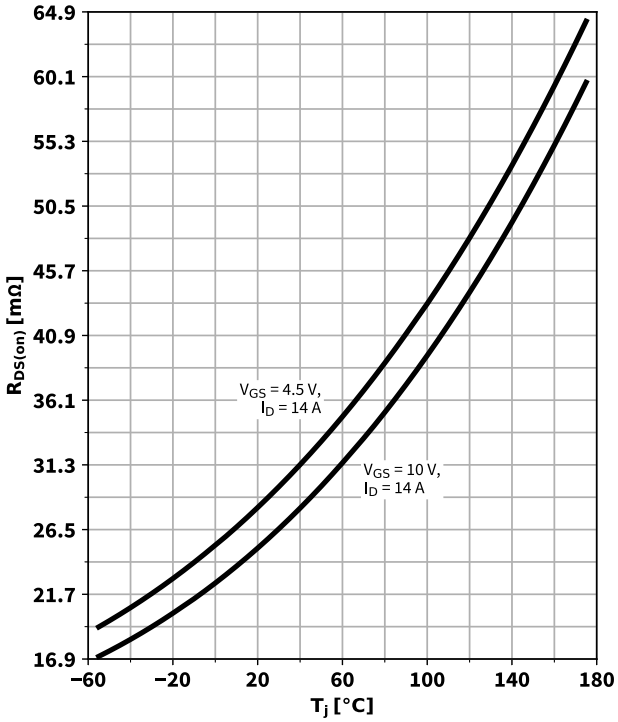
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$ V; parameter: T_j



8 Typ. drain-source on-state resistance

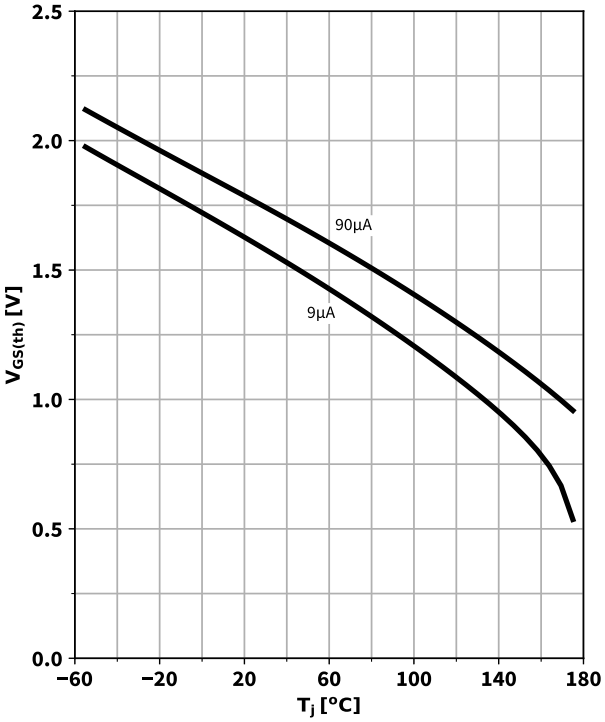
$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



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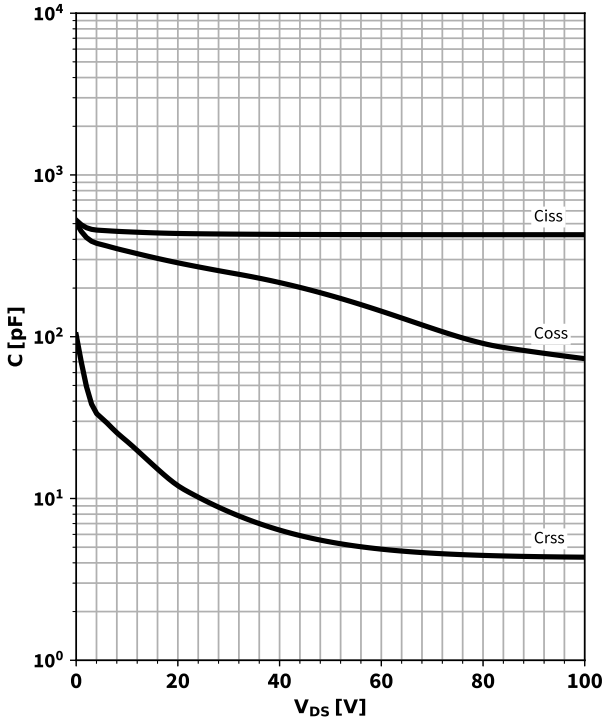
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



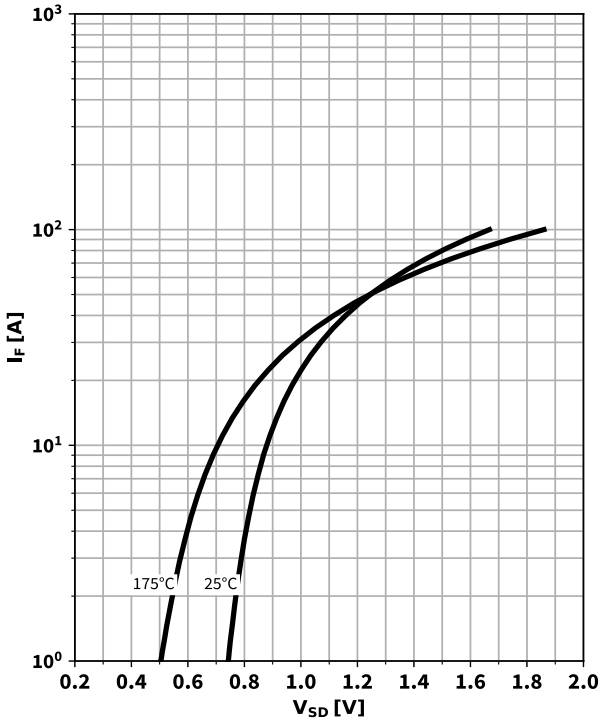
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



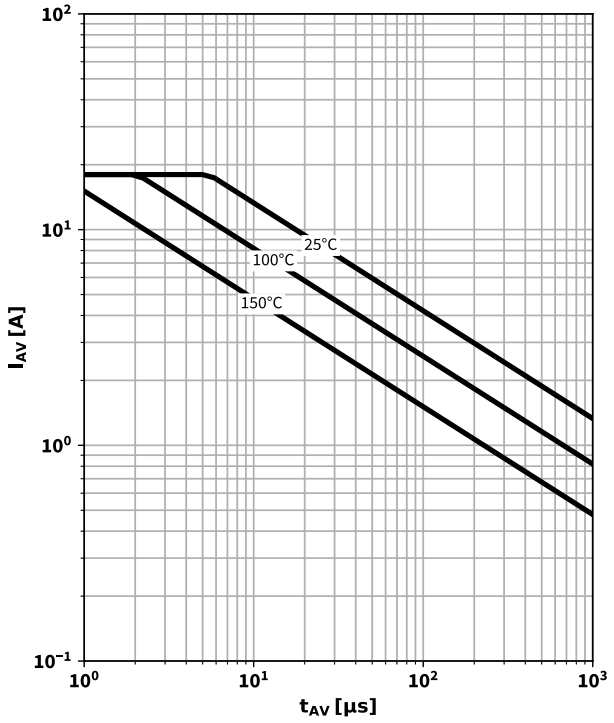
11 Typ. forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



12 Typ. avalanche characteristics

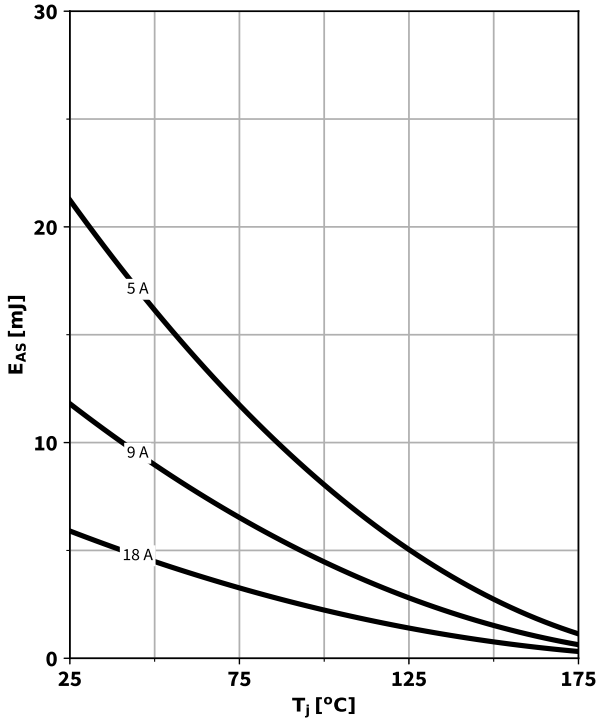
$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



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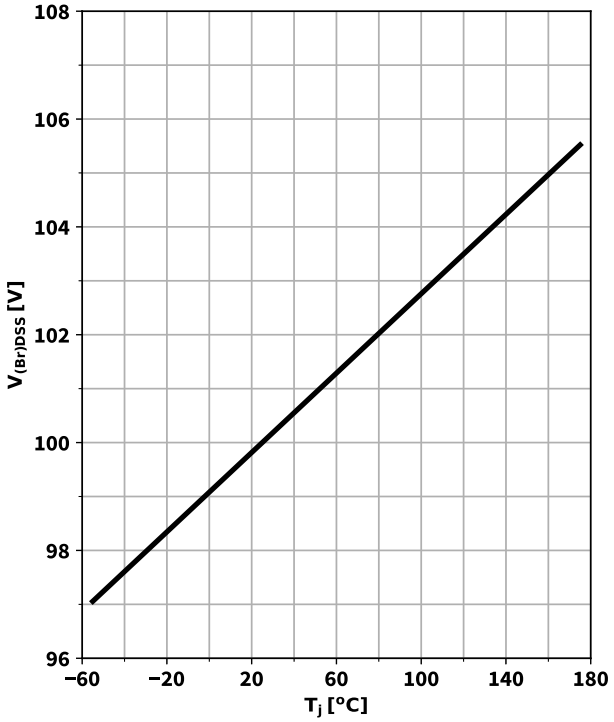
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



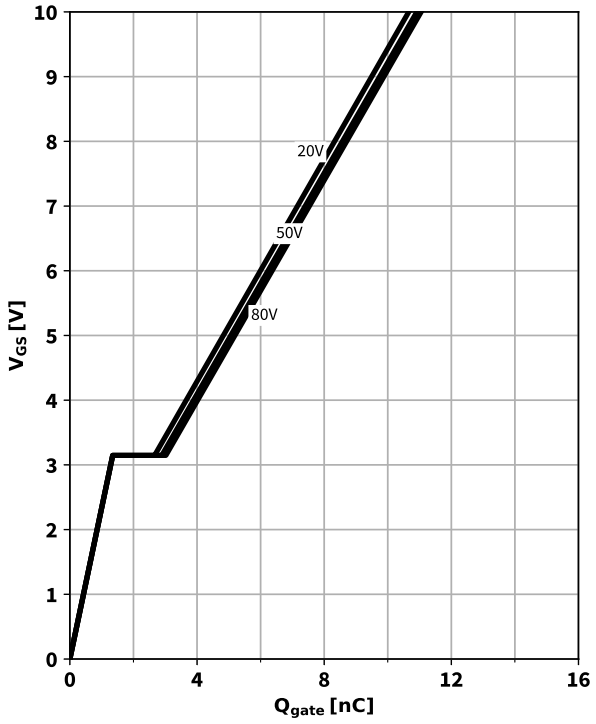
14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; I_D = 1 mA

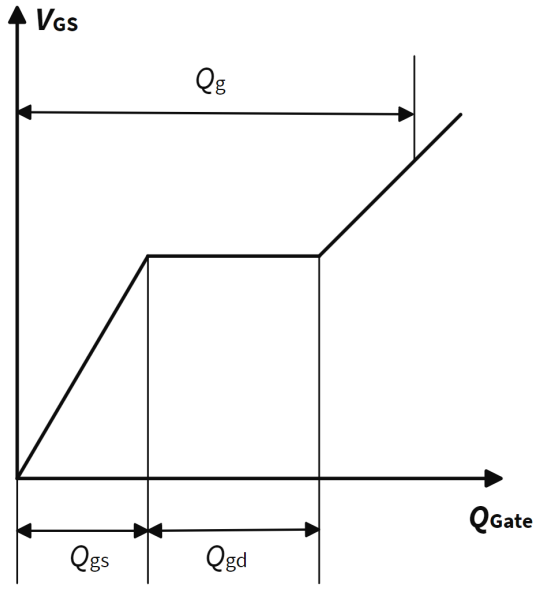


15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; I_D = 14 A pulsed; parameter: V_{DD}

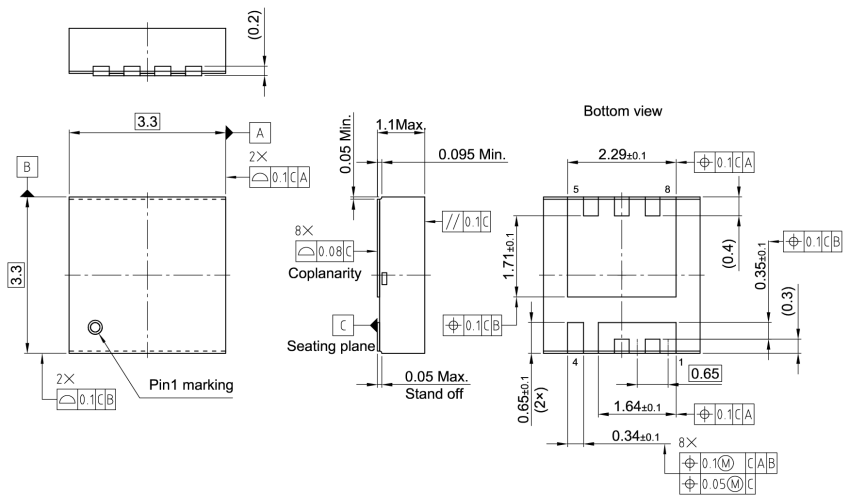


16 Gate charge waveforms

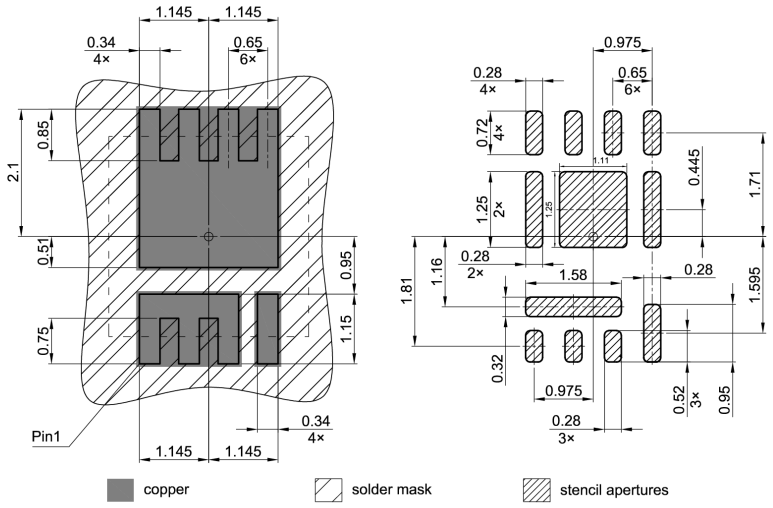


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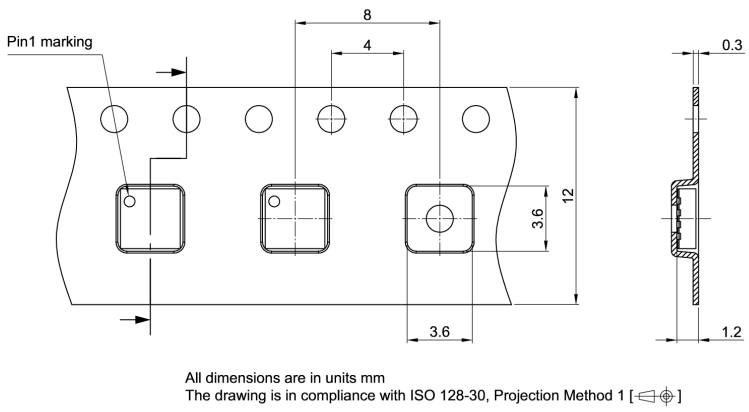
Package Outline



Footprint



Packaging



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Revision History

Revision	Date	Changes
Revision 1.0	2025-04-24	Final data sheet

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