

Features

- Pin- and function-compatible with CY7C107B/CY7C1007B
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 80 \text{ mA @ } 10 \text{ ns}$
- Low complementary metal oxide semiconductor (CMOS) standby power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Transistor transistor logic (TTL) compatible inputs and outputs
- CY7C107D available in Pb-free 28-pin 400-Mil wide Molded SOJ package. CY7C1007D available in Pb-free 28-pin 300-Mil wide Molded SOJ package

Functional Description

The CY7C107D ^[1] and CY7C1007D ^[1] are high-performance CMOS static RAMs organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and tri-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when deselected. The output pin (D_{OUT}) is placed in a high-impedance state when:

- Deselected ($\overline{CE}$ HIGH)
- When the write operation is active ($\overline{CE}$ and $\overline{WE}$ LOW)

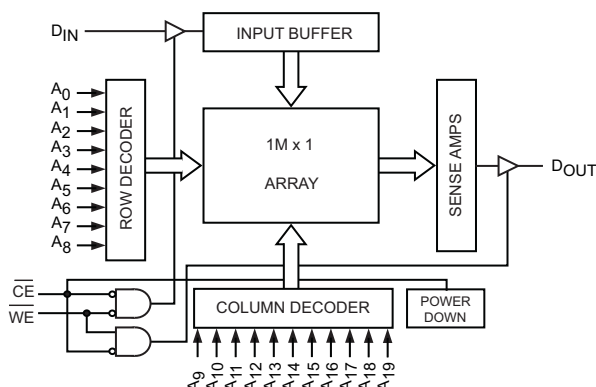
Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Read from the device by taking Chip Enable ($\overline{CE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the data output (D_{OUT}) pin.

The CY7C107D and CY7C1007D devices are suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see [Electrical Characteristics on page 4](#) for more details and suggested alternatives.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Note

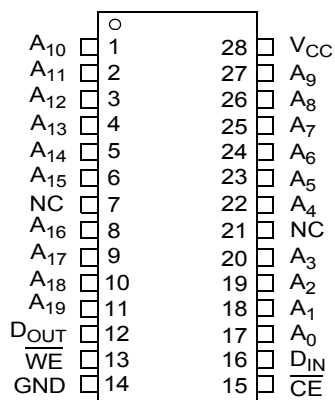
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

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Pin Configuration

Figure 1. 28-pin SOJ pinout (Top View) ^[2]



Selection Guide

Description	CY7C107D-10 CY7C1007D-10	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current, I _{SB2}	3	mA

Note

- NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} relative to GND ^[3] -0.5 V to +6.0 V

DC voltage applied to outputs in High-Z state ^[3] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage ^[3] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40 °C to +85 °C	5 V $\pm$ 0.5 V	10 ns

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		7C107D-10 7C1007D-10		Unit
				Min	Max	
V _{OH}	Output HIGH voltage	I _{OH} = −4.0 mA		2.4	–	V
		I _{OH} = −0.1 mA		–	3.4 ^[4]	
V _{OL}	Output LOW voltage	I _{OL} = 8.0 mA		–	0.4	V
V _{IH}	Input HIGH voltage			2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW voltage ^[3]			−0.5	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}		−1	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _I ≤ V _{CC} , output disabled		−1	+1	μA
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{max} = 1/t _{RC}	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I _{SB1}	Automatic $\overline{\text{CE}}$ Power-down current – TTL Inputs	Max V _{CC} , $\overline{\text{CE}} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max}		–	10	mA
I _{SB2}	Automatic $\overline{\text{CE}}$ Power-down current – CMOS Inputs	Max V _{CC} , $\overline{\text{CE}} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = 0		–	3	mA

Note

3. V_{IL} (min) = -2.0 V and V_{IH} (max) = $V_{CC} + 1$ V for pulse durations of less than 5 ns.

4. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

Capacitance

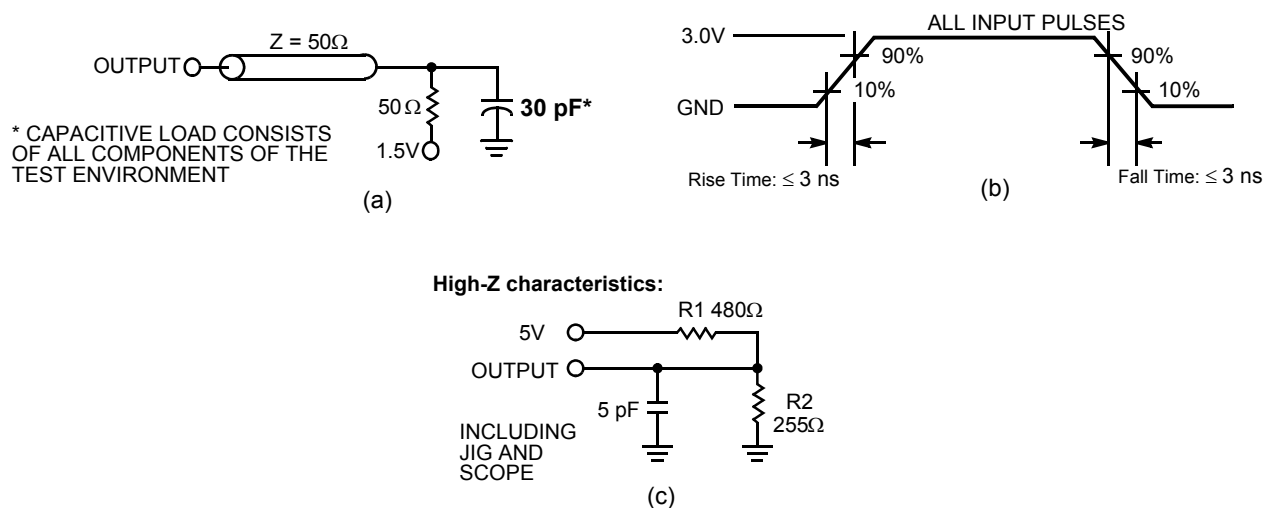
Parameter ^[5]	Description	Test Conditions	Max	Unit
C _{IN} : Addresses	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	7	pF
C _{IN} : Controls			10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[5]	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	58.76	°C/W
Θ _{JC}	Thermal resistance (junction to case)		40.84	40.54	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[6]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

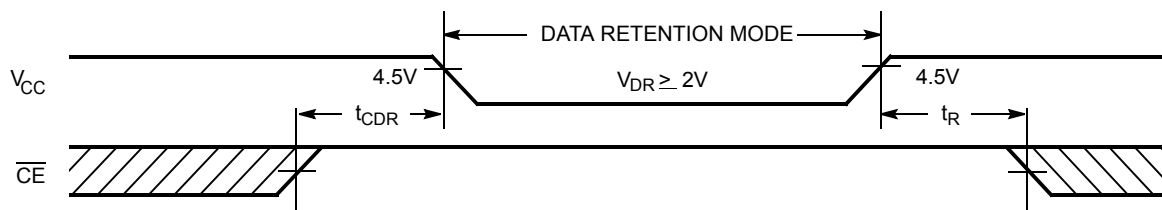
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[7]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[8]}$	Operation recovery time		t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- AC characteristics (except High-Z) are tested using the load conditions shown in Figure 2 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 50\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[9]	Description	7C107D-10 7C1007D-10		Unit
		Min	Max	
Read Cycle				
t _{power} ^[10]	V _{CC} (typical) to the first access	100	–	μs
t _{RC}	Read cycle time	10	–	ns
t _{AA}	Address to data valid	–	10	ns
t _{OHA}	Data hold from address change	3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	10	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[11]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[11, 12]	–	5	ns
t _{PU} ^[13]	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t _{PD} ^[13]	$\overline{\text{CE}}$ HIGH to power-down	–	10	ns
Write Cycle ^[14]				
t _{WC}	Write cycle time	10	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	7	–	ns
t _{AW}	Address set-up to write end	7	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address set-up to write start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	7	–	ns
t _{SD}	Data set-up to write end	6	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[11]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[11, 12]	–	6	ns

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 30-pF load capacitance.
10. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of [Figure 2 on page 5](#). Transition is measured when the outputs enter a high impedance state.
13. This parameter is guaranteed by design and is not tested.
14. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) ^[15, 16]

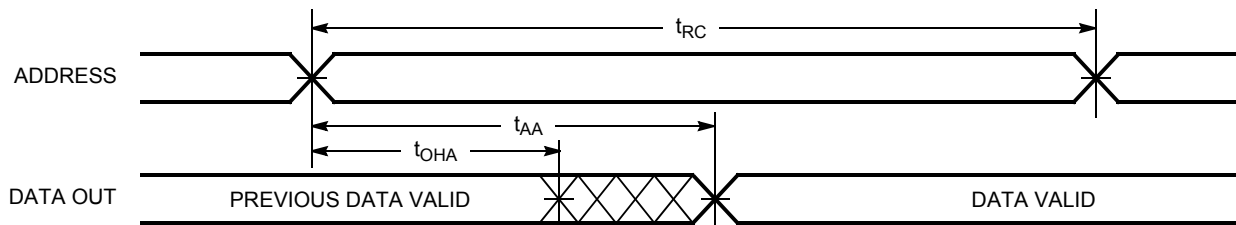
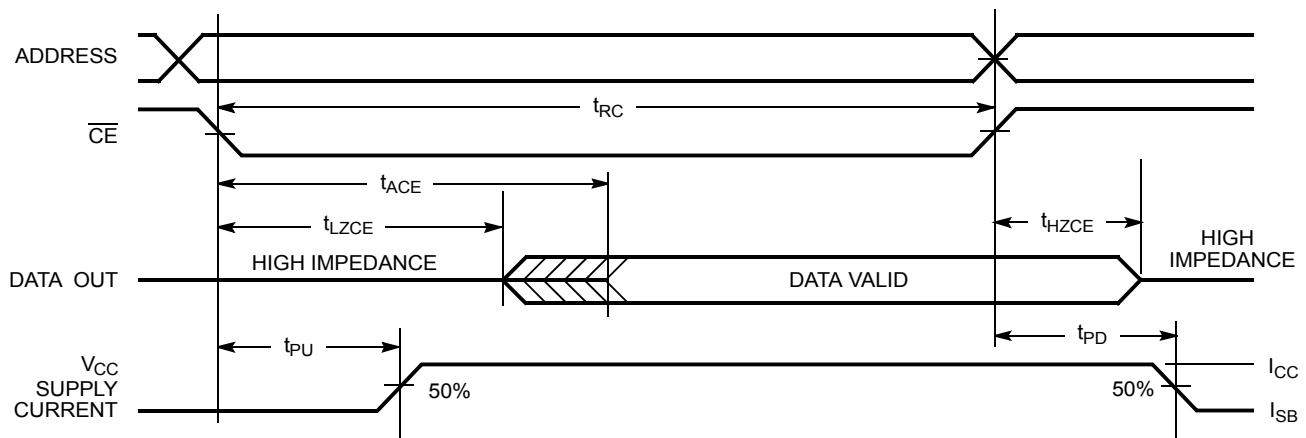


Figure 5. Read Cycle No. 2 ^[16, 17]



Notes

15. Device is continuously selected, $\overline{CE} = V_{IL}$.

16. $\overline{WE}$ is HIGH for read cycle.

17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms(continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [18]

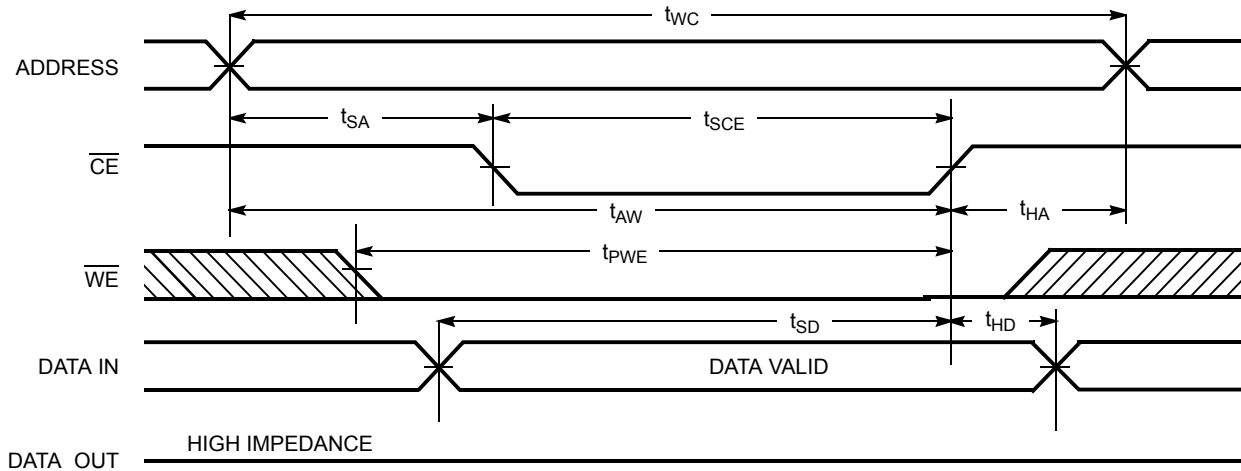
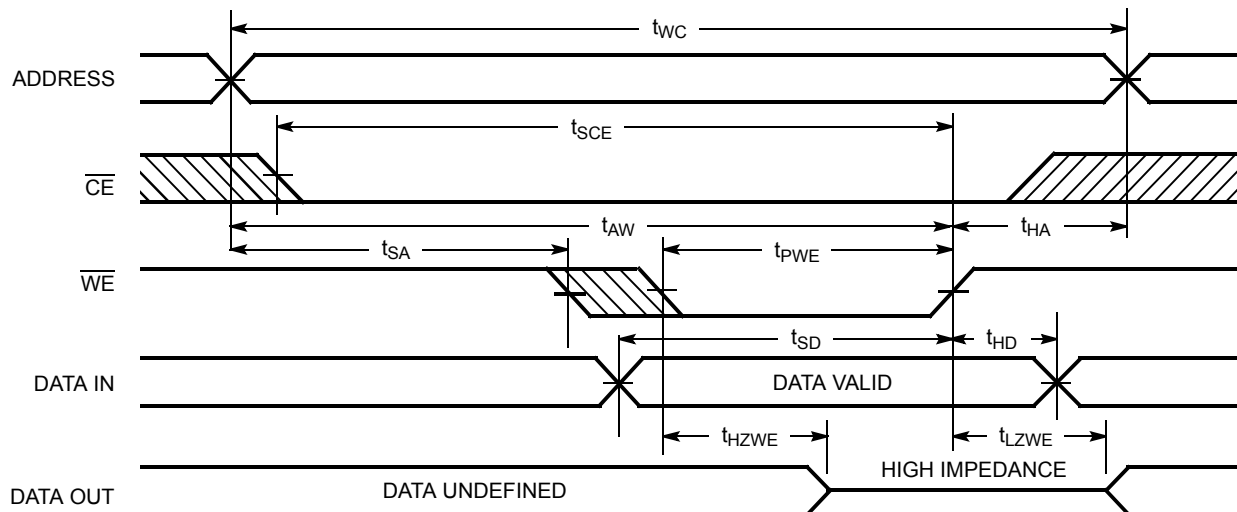


Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled) [18]



Note

18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Truth Table

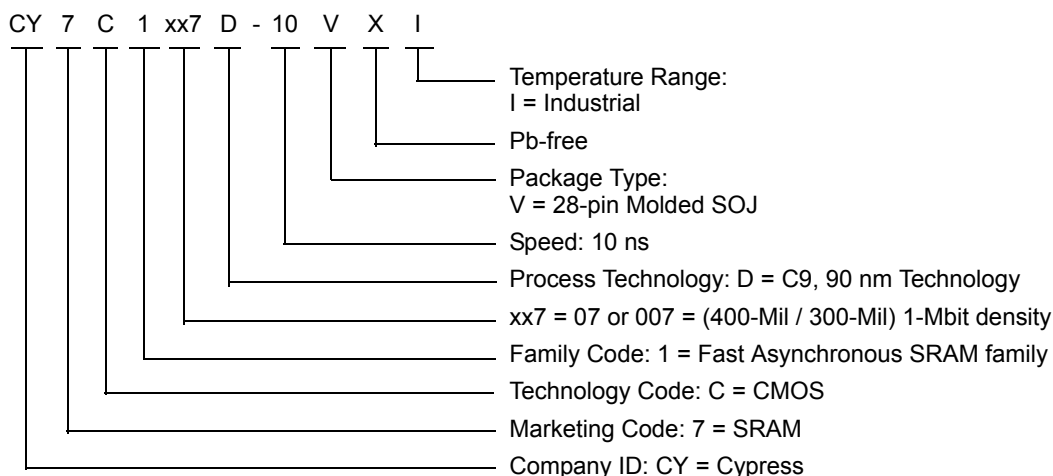
$\overline{CE}$	$\overline{WE}$	D _{OUT}	Mode	Power
H	X	High Z	Power-down	Standby (I _{SB})
L	H	Data out	Read	Active (I _{CC})
L	L	High Z	Write	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C107D-10VXI	51-85032	28-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1007D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	

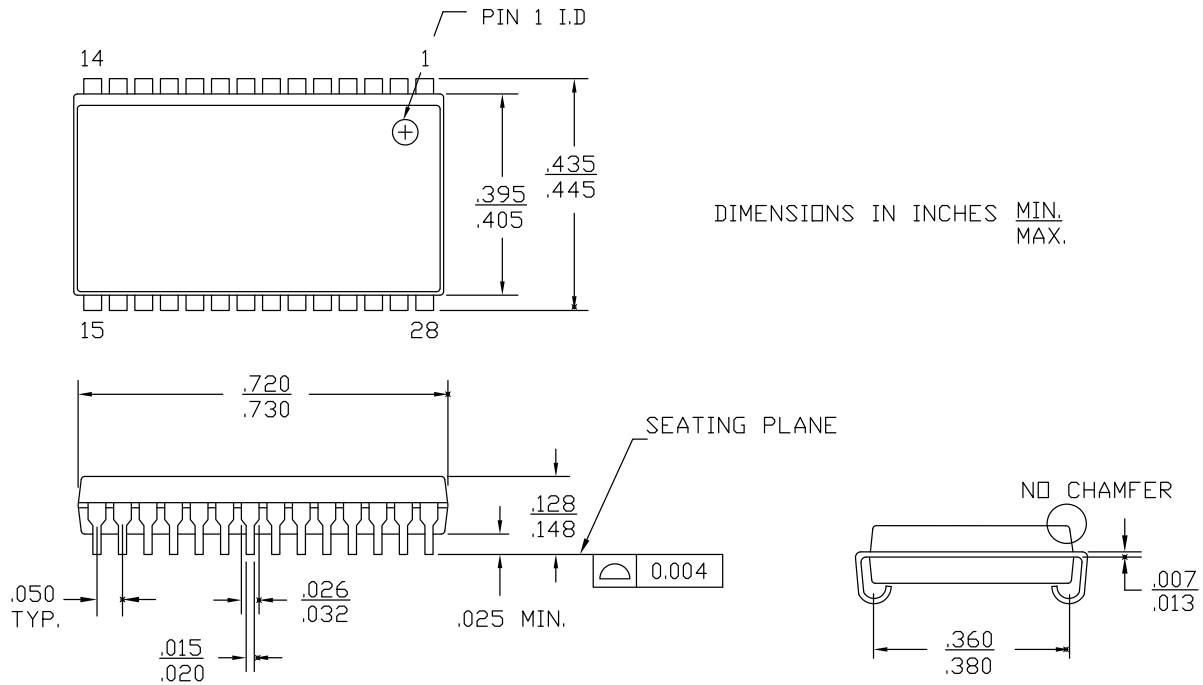
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 8. 28-pin SOJ (400 Mils) V28.4 (Molded SOJ V28) Package Outline, 51-85032



NOTES :

1. PACKAGE WEIGHT : 1.24g
2. JEDEC REFERENCE : MS-027

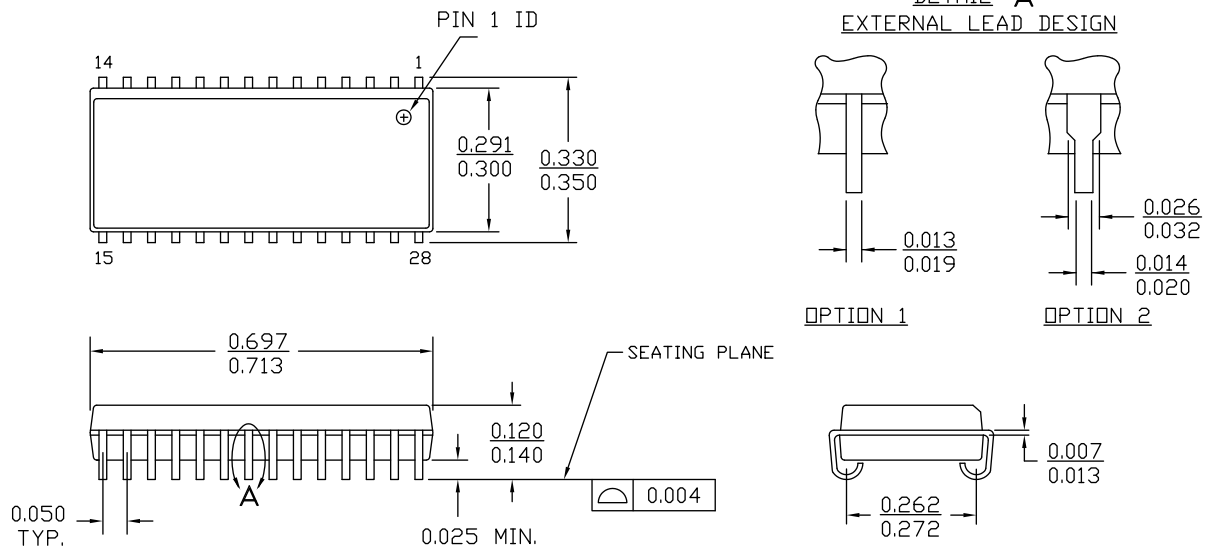
51-85032 *F

Package Diagrams(continued)

Figure 9. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.
MAX.



51-85031 *E

Acronyms

Acronym	Description
BGA	Ball Grid Array
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Very Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C107D/CY7C1007D, 1-Mbit (1 M × 1) Static RAM Document Number: 38-05469				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free offering in Ordering Information
*B	263769	See ECN	RKF	Added Data Retention Characteristics table Added T _{power} Spec in Switching Characteristics Table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to –10 and –12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #3
*E	802877	See ECN	VKN	Changed I _{CC} specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	2898399	03/24/2010	AJU	Updated Package Diagrams
*G	3104943	12/08/2010	AJU	Added Ordering Code Definitions .
*H	3218989	04/07/2011	PRAS	Added TOC Added Acronyms and Units of Measure table. Updated Package diagrams from *C to *D (51-85032)
*I	4040950	06/26/2013	MEMJ	Updated Functional Description . Updated Electrical Characteristics Added one more Test Condition “I _{OH} = –0.1mA” for V _{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 4 and referred the same note in maximum value for V _{OH} parameter corresponding to Test Condition “I _{OH} = –0.1mA”. Updated Package Diagrams : spec 51-85031 – Changed revision from *D to *E. Updated in new template.
*J	4385003	05/23/2014	MEMJ	Updated Package Diagrams : spec 51-85032 – Changed revision from *E to *F. Completing Sunset Review.
*K	4578500	11/24/2014	MEMJ	Added related documentation hyperlink in page 1.

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