Multiband RF Power Controllers for EDGE/TDMA

FEATURES

- **Supports AM Modulation in EDGE/TDMA (ANSI-136) Applications**
- **Single Output RF Power Amplifier Control (LTC4403-1)**
- **Dual Output RF Power Amplifier Control (LTC4403-2)**
- **Internal Schottky Diode Detector with >40dB Range**
- **Wide Input Frequency Range: 300MHz to 2.4GHz**
- **Autozero Loop Cancels Offset Errors and Temperature Dependent Offsets**
- **Wide V_{IN} Range: 2.7V to 6V**
- Allows Direct Connection to Battery
- RF Output Power Set by External DAC
- Internal Frequency Compensation
- Rail-to-Rail Power Control Outputs
- Low Operating Current: 1mA
- Low Shutdown Current: <10µA
- PCTL Input Filter
- Available in a 8-Pin MSOP Package (LTC4403-1) and 10-Pin MSOP (LTC4403-2)

APPLICATIONS

- Multiband GSM/GPRS/EDGE Cellular Telephones
- PCS Devices
- Wireless Data Modems
- U.S. TDMA Cellular Phones

DESCRIPTION

The LTC®4403-2 is a multiband RF power controller for RF power amplifiers operating in the 300MHz to 2.4GHz range. The LTC4403-2 has two outputs to control dual T_X PA modules with two control inputs. An internal sample and hold circuit enables the LTC4403-2 to be used with AM modulation via the carrier or PA supply. The input voltage range is optimized for operation from a single lithium-ion cell or 3× NiMH.

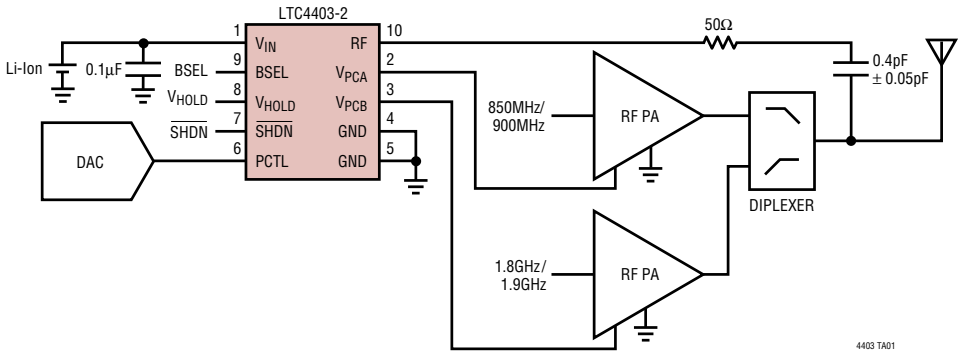
RF power is controlled by driving the RF amplifier power control pins and sensing the resultant RF output power. The RF sense voltage is peak detected using an on-chip Schottky diode. This detected voltage is compared to the DAC voltage at the PCTL pin to control the output power.

The LTC4403-1 is a single output RF power controller with identical performance to the LTC4403-2. The LTC4403-1 has one output to control a single T_X PA or dual T_X PA module with a single control input and is available in an 8-pin MSOP package.

Internal and external offsets are cancelled over temperature by an autozero control loop. The shutdown feature disables the part and reduces the supply current to <10µA.

TYPICAL APPLICATION

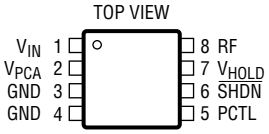
LTC4403-2 Multiband EDGE Cellular Telephone Transmitter



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} to GND ..... –0.3V to 6.5V
V_{PCA}, V_{PCB} Voltage ..... –0.3V to 4.6V
PCTL Voltage ..... –0.3V to (V_{IN} + 0.3V)
$\overline{RF}$ Voltage ..... (V_{IN} ± 2.6V) to 7V
$\overline{SHDN}$, V_{HOLD}, BSEL Voltage to GND ..... –0.3V to (V_{IN} + 0.3V)
$I_{VPCA/B}$ 10mA
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

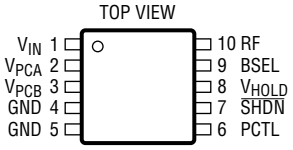
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LTC4403-1EMS8
MS8 PART MARKING
LTXG



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LTC4403-2EMS
MS PART MARKING
LTXJ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $\overline{SHDN}$ = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage		●	2.7		6	V
I_{VIN} Shutdown Current	$\overline{SHDN}$ = 0V	●		10	20	µA
I_{VIN} Operating Current	I_{VPCA} = I_{VPCB} = 0mA	●		1.5	2	mA
$V_{PCA/B}$ V_{OL}	R_{LOAD} = 400Ω, Enabled	●	0		0.1	V
$V_{PCA/B}$ Dropout Voltage	I_{LOAD} = 6mA, V_{IN} = 2.7V	●			V_{IN} – 0.25	V
$V_{PCA/B}$ Output Current	$V_{PCA/B}$ = 2.4V, V_{IN} = 2.7V, ΔV_{OUT} = 10mV	●	6			mA
$V_{PCA/B}$ Enable Time	$\overline{SHDN}$ = High (Note 5)	●		9	11	µs
$V_{PCA/B}$ Bandwidth	C_{LOAD} = 33pF, R_{LOAD} = 400 (Note 7) PCTL < 80mV PCTL > 160mV			250 130		kHz kHz
$V_{PCA/B}$ Load Capacitance	(Note 6)	●			100	pF
$V_{PCA/B}$ Slew Rate	V_{PCTL} = 2V Step, C_{LOAD} = 100pF, R_{LOAD} = 400 (Note 3)			1.4		V/µs
$V_{PCA/B}$ V_{HOLD} Droop	Unity Gain, V_{PCTL} = 2V, V_{HOLD} = High			1		µV/ms
V_{HOLD} Time	Time from V_{HOLD} High to Hold Switch Opening			100		ns
$V_{PCA/B}$ Start Voltage	Open Loop	●	250	450	550	mV
$V_{PCA/B}$ Voltage Clamp	PCTL = 1V, V_{IN} = 5V	●	3.6	4	4.4	V
$\overline{SHDN}$, V_{HOLD}, BSEL Input Threshold Low	V_{IN} = 2.7V to 6V	●			0.35	V
$\overline{SHDN}$, V_{HOLD}, BSEL Input Threshold High	V_{IN} = 2.7V to 6V	●	1.4			V
$\overline{SHDN}$, BSEL, V_{HOLD} Input Current	$\overline{SHDN}$, BSEL, V_{HOLD} = V_{IN} = 3.6V	●	16	24	36	µA
PCTL Input Voltage Range	(Note 4)	●	0		2.4	V
PCTL Input Resistance		●	60	90	120	kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $\overline{SHDN}$ = V_{IN}, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PCTL Input Filter				270		kHz
Autozero Range	Maximum DAC Zero-Scale Offset Voltage that can be applied to PCTL	●			400	mV
RF Input Frequency Range	(Note 6)	●	300		2400	MHz
RF Input Power Range	F = 900MHz (Note 6) F = 1800MHz (Note 6) F = 2400MHz (Note 6)			–27 to 18 –25 to 18 –23 to 16		dBm dBm dBm
RF Input Resistance	Referenced to V_{IN}	●	150	250	350	Ω

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Specifications are assured over the –40°C to 85°C temperature range by design characterization and correlation with statistical process controls.

Note 3: Slew rate is measured open loop. The rise time at V_{PCA} or V_{PCB} is measured between 1V and 2V.

Note 4: Includes maximum DAC offset voltage and maximum control voltage.

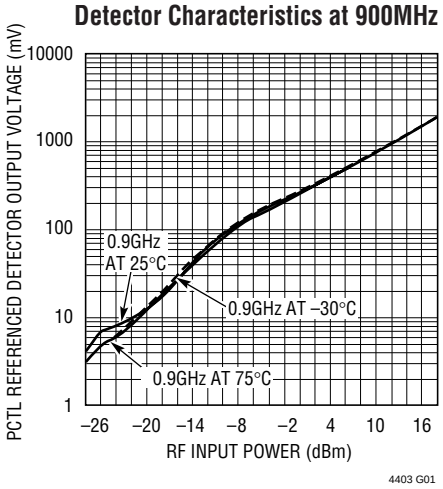
Note 5: This is the time from $\overline{SHDN}$ rising edge 50% switch point to $V_{PCA/B}$ = 250mV.

Note 6: Guaranteed by design. This parameter is not production tested.

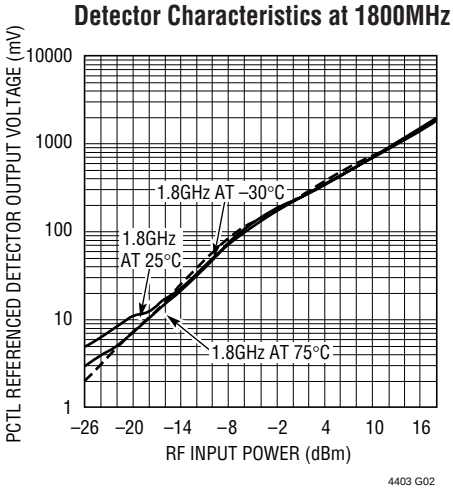
Note 7: Bandwidth is calculated using the 10% to 90% rise time: BW = 0.35/rise time

TYPICAL PERFORMANCE CHARACTERISTICS

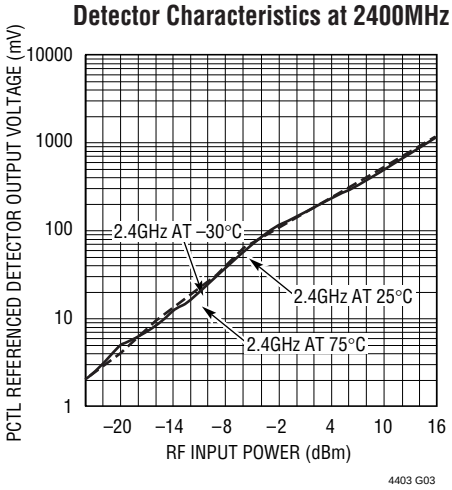
Detector Characteristics at 900MHz



Detector Characteristics at 1800MHz



Detector Characteristics at 2400MHz



PIN FUNCTIONS (LTC4403-1/LTC4403-2)

V_{IN} (Pin 1): Input Supply Voltage, 2.7V to 6V. V_{IN} should be bypassed with 0.1µF and 100pF ceramic capacitors.

V_{PCA} (Pin 2): Power Control Voltage Output. This pin drives an external RF power amplifier power control pin. The maximum load capacitance is 100pF. The output is capable of rail-to-rail swings at low load currents. Selected when BSEL is low.

V_{PCB} (Pin 3): (LTC4403-2 Only) Power Control Voltage Output. This pin drives an external RF power amplifier power control pin. The maximum load capacitance is 100pF. The output is capable of rail-to-rail swings at low load currents. Selected when BSEL is high.

GND (Pin 3/4): System Ground.

PIN FUNCTIONS (LTC4403-1/LTC4403-2)

GND (Pin 4/5): System Ground.

PCTL (Pin 5/6): Analog Input. The external power control DAC drives this input. The amplifier servos the RF power until the RF detected signal equals the DAC signal applied at this pin.

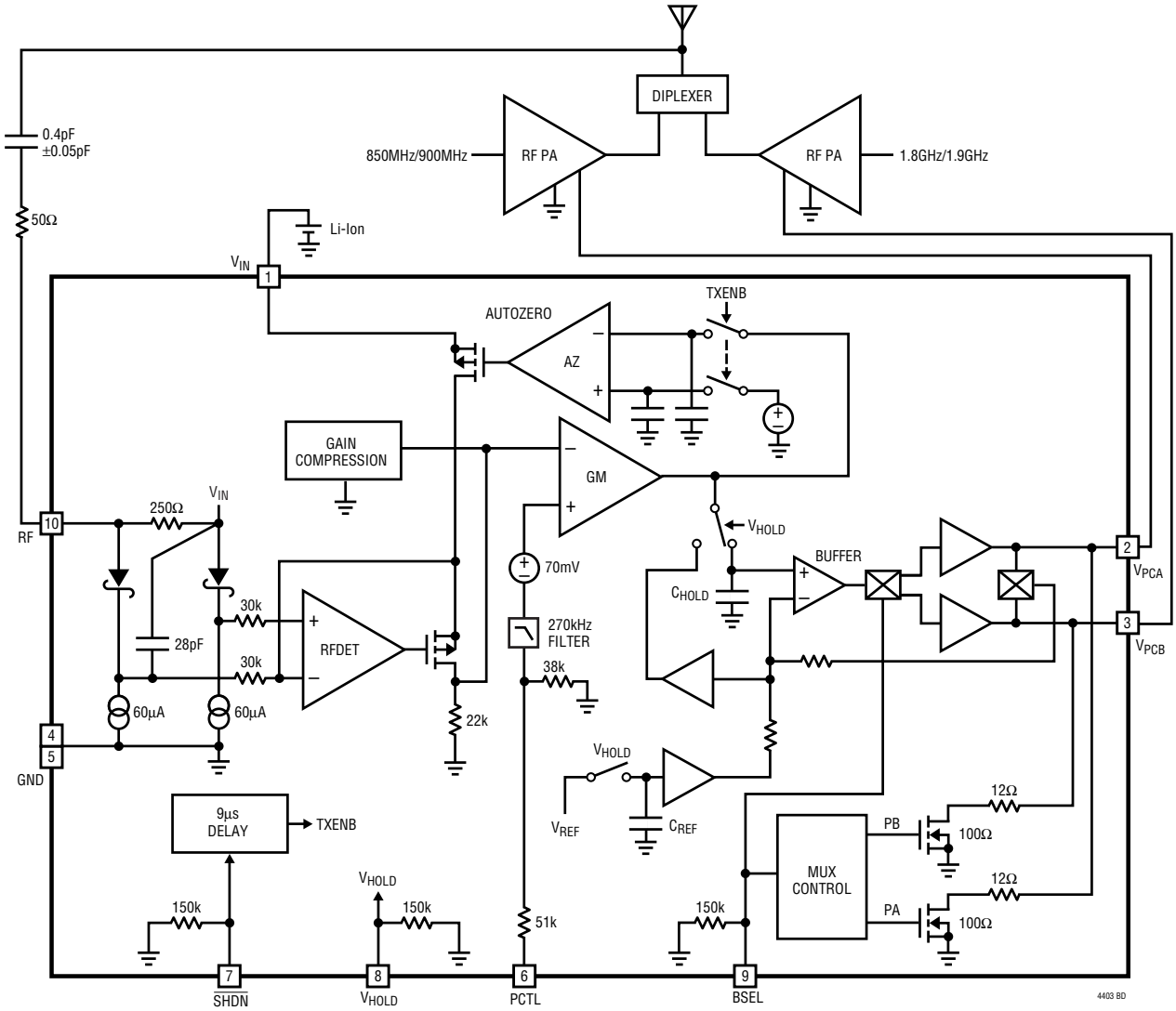
$\overline{\text{SHDN}}$ (Pin 6/7): Shutdown Input. A logic low on the $\overline{\text{SHDN}}$ pin places the part in shutdown mode. A logic high enables the part after 10µs. $\overline{\text{SHDN}}$ has an internal 150k pull-down resistor to ensure that the part is in shutdown when no input is applied. In shutdown, V_{PCA} and V_{PCB} are pulled to ground via a 112Ω resistor.

V_{HOLD} (Pin 7/8): Asserted high prior to AM modulation, opens control loop and holds voltage at V_{PCA} or V_{PCB} during EDGE modulation.

BSEL (Pin 9): (LTC4403-2 Only) Selects V_{PCA} when low and V_{PCB} when high. This input has an internal 150k resistor to ground.

RF (Pin 8/10): Coupled RF Feedback Voltage . This input is referenced to V_{IN}. The frequency range is 300MHz to 2400MHz. This pin has an internal 250Ω termination, an internal Schottky diode detector and peak detector capacitor.

BLOCK DIAGRAM (LTC4403-2)



APPLICATIONS INFORMATION

Operation

The LTC4403-1/-2 single/dual band RF power controller integrates several functions to provide RF power control over frequencies ranging from 300MHz to 2.4GHz. These functions include an internally compensated amplifier to control the RF output power, an autozero section to cancel internal and external voltage offsets, an RF Schottky diode peak detector and amplifier to convert the RF feedback signal to DC, a multiplexer to switch the controller output to either V_{PCA} or V_{PCB}, a $V_{PCA/B}$ overvoltage clamp, compression and a bandgap reference.

Band Selection

The LTC4403-2 is designed for multiband operation. The BSEL pin will select output V_{PCA} when low and output V_{PCB} when high. For example, V_{PCA} could be used to drive an 850MHz/900MHz channel and V_{PCB} a 1.8GHz/1.9GHz channel. BSEL must be established before the part is enabled. The LTC4403-1 can be used to drive a single RF channel or dual channel with integral multiplexer.

Control Amplifier

The control amplifier supplies the power control voltage to the RF power amplifier. A portion (typically –19dB for low frequencies and –14dB for high frequencies) of the RF output voltage is coupled into the RF pin, to close the gain control loop. When a DAC voltage is applied to PCTL, the amplifier quickly servos V_{PCA} or V_{PCB} positive until the detected feedback voltage applied to the RF pin matches the voltage at PCTL. This feedback loop provides accurate RF power control. V_{PCA} or V_{PCB} are capable of driving a 6mA load current and 100pF load capacitor.

RF Detector

The internal RF Schottky diode peak detector and amplifier convert the coupled RF feedback voltage to a low frequency voltage. This voltage is compared to the DAC voltage at the PCTL pin by the control amplifier to close the RF power control loop. The RF pin input resistance is typically 250Ω and the frequency range of this pin is 300MHz to 2400MHz. The detector demonstrates excellent efficiency and linearity over a wide range of input power. The Schottky detector is biased at about 60µA and drives an on-chip peak detector capacitor of 28pF.

Autozero

An autozero system is included to improve power programming accuracy over temperature. This section cancels internal offsets associated with the Schottky diode detector and control amplifier. External offsets associated with the DAC driving the PCTL pin are also cancelled. Offset drift due to temperature is cancelled between each burst. The maximum offset allowed at the DAC output is limited to 400mV. Autozeroing is performed after $\overline{SHDN}$ is asserted high. An internal delay of typically 9µs enables the $V_{PCA/B}$ output after the autozero has settled. When the part is enabled, the autozero capacitors are held and the V_{PCA} or V_{PCB} pin is connected to the buffer amplifier output. The hold droop voltage of typically <1µV/ms provides for accurate offset cancellation.

Filter

There is a 270kHz filter included in the PCTL path. This filter is trimmed at test.

Modes of Operation

Shutdown: The part is in shutdown mode when $\overline{SHDN}$ is low. V_{PCA} and V_{PCB} are held at ground and the power supply current is typically 10µA.

Enable: When $\overline{SHDN}$ is asserted high the part will automatically calibrate out all offsets. This takes about 9µs and is controlled by an internal delay circuit. After 9µs V_{PCA} or V_{PCB} will step up to the starting voltage of 450mV. The user can then apply the ramp signal. The user should wait at least 11µs after $\overline{SHDN}$ has been asserted high before applying the ramp. The DAC should be settled 2µs after asserting $\overline{SHDN}$ high.

Hold: When the V_{HOLD} pin is low, the RF power control feedback loop is closed and the LTC4403-X servos the V_{PCA}/V_{PCB} pins according to the voltages at the PCTL and RF inputs. When the V_{HOLD} pin is asserted high, the RF power control feedback loop is opened and the power control voltage at V_{PCA} or V_{CPB} is held at its present level. Generally, the V_{HOLD} pin is asserted high after the power up ramp has been completed and the desired RF output power has been achieved. The power control voltage is then held at a constant voltage during the EDGE modulation time. After the EDGE modulation is completed and prior to power ramping down, the V_{HOLD} pin is set low.

APPLICATIONS INFORMATION

This closes the RF power control loop and the RF power is then controlled during ramp down.

LTC4403-1 Description

The LTC4403-1 is identical in performance to the LTC4403-2 except that only one control output (V_{PCA}) is available. The LTC4403-1 can drive a single band (300MHz to 2400MHz) or a dual RF channel module with an internal multiplexer. Several manufacturers offer dual RF channel modules with an internal multiplexer.

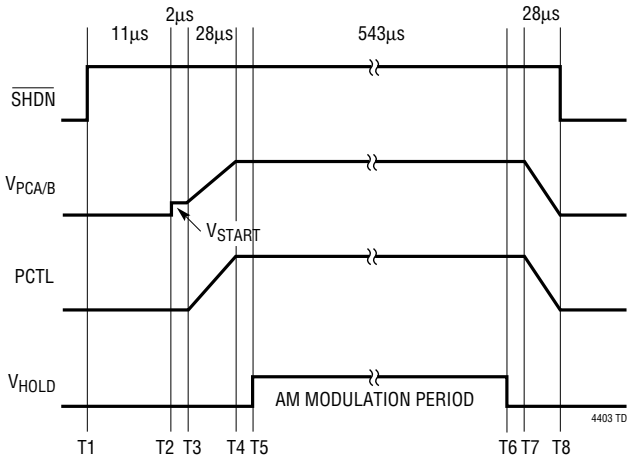
General Layout Considerations

The LTC4403-X should be placed near the coupling components. The feedback signal line to the RF pin should be a 50Ω transmission line.

Capacitive Coupling

An alternative to a directional coupler is illustrated on the first page of this data sheet. This method couples RF from the power amplifier to the power controller through a 0.4pF ±0.05pF capacitor and 50Ω series resistor, completely eliminating the directional coupler.

LTC4403-X Timing Diagram



T1: PART COMES OUT OF SHUTDOWN 11µs PRIOR TO BURST.
T2: INTERNAL TIMER COMPLETES AUTOZERO CORRECTION, TYPICALLY 9µs.
T3: BASEBAND CONTROLLER STARTS RF POWER RAMP UP AT LEAST 11µs AFTER $\overline{SHDN}$ IS ASSERTED HIGH.
T4: BASEBAND CONTROLLER COMPLETES RAMP UP.
T5: CONTROL LOOP OPENS, $V_{PCA/B}$ VOLTAGE HELD, AM MODULATION STARTS.
T6: AM MODULATION STOPS, CONTROL LOOP CLOSES, $V_{PCA/B}$ WILL FOLLOW DAC.
T7: BASEBAND CONTROLLER STARTS RF POWER RAMP DOWN AT END OF BURST.
T8: RETURNS TO SHUTDOWN MODE BETWEEN BURSTS.

Application Note AN91 describes the capacitive coupling scheme in full detail. Demo boards featuring this coupling method are available upon request.

Power Ramp Profiles

The external voltage gain associated with the RF channel can vary significantly between RF power amplifier types. Frequency compensation generally defines the loop dynamics that impact the power/time response and possibly (slow loops) the power ramp sidebands. The LTC4403-X operates open loop until an RF voltage appears at the RF pin, at which time the loop closes and the output power follows the DAC profile. The RF power amplifier will require a certain control voltage level (threshold) before an RF output signal is produced. The LTC4403-X $V_{PCA/B}$ outputs must quickly rise to this threshold voltage in order to meet the power/time profile. To reduce this time, the LTC4403-X starts at 450mV. However, at very low power levels the PCTL input signal is small, and the $V_{PCA/B}$ outputs may take several microseconds to reach the RF power amplifier threshold voltage. To reduce this time, it may be necessary to apply a positive pulse at the start of the ramp to quickly bring the $V_{PCA/B}$ outputs to the threshold voltage. This can generally be achieved with DAC programming. The magnitude of the pulse is dependent on the RF amplifier characteristics.

Power ramp sidebands and power/time are also a factor when ramping to zero power. For RF amplifiers requiring high control voltages, it may be necessary to further adjust the DAC ramp profile. When the power is ramped down, the loop will eventually open at power levels below the LTC4403-X detector threshold. The LTC4403-X will then go open loop and the output voltage at V_{PCA} or V_{PCB} will stop falling. If this voltage is high enough to produce RF output power, the power/time or power ramp sidebands may not meet specification. This problem can be avoided by starting the DAC ramp from 200mV (Figure 1). At the end of the cycle, the DAC can be ramped down to 0mV. This applies a negative signal to the LTC4403-X thereby ensuring that the $V_{PCA/B}$ outputs will ramp to 0V. The 200mV ramp step must be applied at least 2µs after $\overline{SHDN}$ is asserted high to allow the autozero to cancel the step.

APPLICATIONS INFORMATION

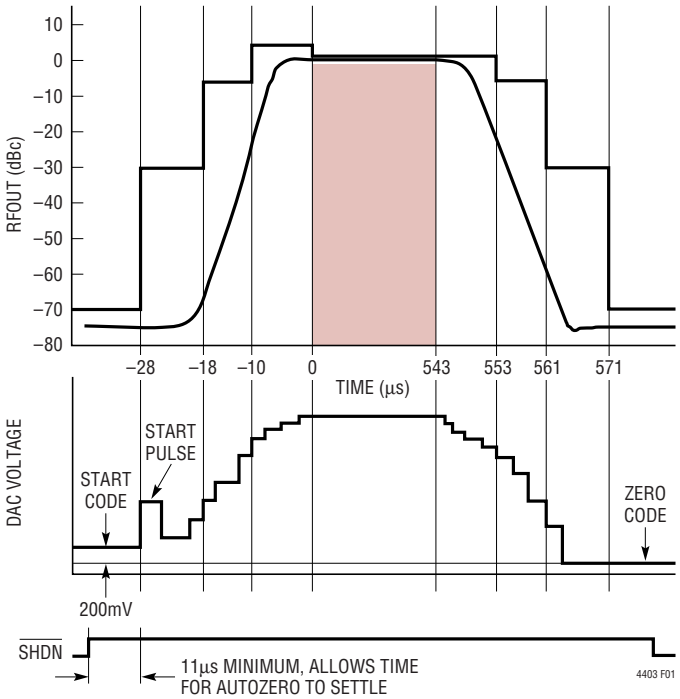


Figure 1. LTC4403 Ramp Timing

Demo Board

The LTC4403-X demo board is available upon request. The demo board has a 900MHz and an 1800MHz RF channel and V_{HOLD} controlled by the LTC4403-X. Timing signals for $\overline{SHDN}$ are generated on the board using a 13MHz crystal oscillator reference. The PCTL power control pin is driven by a 10-bit DAC and the DAC profile can be loaded via a serial port. The serial port data is stored in a flash memory which is capable of storing eight ramp profiles. The board is supplied preloaded with four GSM power profiles and four DCS power profiles covering the entire power range. External timing signals can be used in place of the internal crystal controlled timing. A power ramp software package is available which allows the user to create power control ramps.

LTC4403 Control Loop Stability

There are several factors that can improve or degrade loop frequency stability.

1) The additional voltage gain supplied by the RF power amplifier increases the loop gain, raising poles normally below the 0dB axis. The extra voltage gain can vary significantly over input/output power ranges, frequency, power supply, temperature and manufacturer. RF power amplifier gain control transfer functions are often not available and must be generated by the user. Loop oscillations are most likely to occur in the midpower range where the external voltage gain associated with the RF power amplifier typically peaks. It is useful to measure the oscillation or ringing frequency to determine whether it corresponds to the expected loop bandwidth and thus is due to high gain bandwidth.

2) Loop voltage losses supplied by the coupler network will improve phase margin. The larger the coupler loss the more stable the loop will become. However, larger losses reduce the RF signal to the LTC4403-X and detector performance may be degraded at low power levels. (See RF Detector Characteristics.)

3) Additional poles within the loop due to filtering or the turn-on response of the RF power amplifier can degrade the phase margin if these pole frequencies are near the effective loop bandwidth frequency. Generally loops using RF power amplifiers with fast turn-on times have more phase margin. Extra filtering below 16MHz should never be placed within the control loop, as this will only degrade phase margin.

4) Control loop instability can also be due to open loop issues. RF power amplifiers should first be characterized in an open loop configuration to ensure self oscillation is not present. Self-oscillation is often related to poor power supply decoupling, ground loops, coupling due to poor layout and extreme V_{SWR} conditions. The oscillation frequency is generally in the 100kHz to 10MHz range. Power supply related oscillation suppression requires large value ceramic decoupling capacitors placed close to the RF power amp supply pins. The range of decoupling capacitor values is typically 1nF to 3.3µF.

5) Poor layout techniques associated with the coupler network may result in high frequency signals bypassing the coupler. This could result in stability problems due to the reduction in the coupler loss.

APPLICATIONS INFORMATION

Determining External Loop Gain and Bandwidth

The external loop voltage gain contributed by the RF channel and coupler network should be measured in a closed loop configuration. A voltage step is applied to PCTL and the change in V_{PCA} (or V_{PCB}) is measured. The detected RF voltage is 0.6 • PCTL and the external voltage gain contributed by the RF power amplifier and coupler network is $0.6 \bullet \Delta V_{PCTL}/\Delta V_{VPCA}$. Measuring voltage gain in the closed loop configuration accounts for the nonlinear detector gain that is dependent on RF input voltage and frequency.

The LTC4403-X unity gain bandwidth specified in the data sheet assumes that the net voltage gain contributed by the RF power amplifier and coupler network is unity. The bandwidth is calculated by measuring the rise time between 10% and 90% of the voltage change at V_{PCA} or V_{PCB} for a small step in voltage applied to PCTL.

BW1 = 0.35/rise time

The LTC4403-X control amplifier unity gain bandwidth (BW1) is typically 250kHz. For PCTL <100mV the phase margin of the control amplifier is typically 90°.

For PCTL voltages <100mV, the RF detected voltage is 0.6PCTL. For PCTL voltages >200mV, RF detected voltage is 1.22PCTL – 0.1. This change in gain is due to an internal compression circuit designed to extend the detector range.

For example, to determine the external RF channel loop voltage gain with the loop closed, apply a 100mV step to PCTL from 0mV to 100mV. V_{PCA} (or V_{PCB}) will increase to supply enough feedback voltage to the RF pin to cancel this 100mV step which would be the required detected voltage of 60mV. Suppose that V_{PCA} changed from 1.498V to 1.528V to create the RF output power change required. The net external voltage gain contributed by the RF power amplifier and directional coupler network can be calculated by dividing the 60mV change at the RF pin by the 30mV change at the V_{PCA} pin. The net external voltage gain would then be approximately 2. The loop bandwidth extends to 2 • BW1. If BW1 is 250kHz, the loop bandwidth increases to approximately 0.5MHz. The phase margin can be determined from Figures 2 and 3. Repeat the above voltage gain measurement over the full power and frequency range.

External pole frequencies within the loop will further reduce phase margin. The phase margin degradation, due to external and internal pole combinations, is difficult to determine since complex poles are present. Gain peaking may occur, resulting in higher bandwidth and lower phase margin than predicted from the open loop Bode plot. A low frequency AC SPICE model of the LTC4403-X power controller is included (Figures 6 and 7) to better determine pole and zero interactions. The user can apply external gains and poles to determine bandwidth and phase margin. DC, transient and RF information cannot be extracted from this model. The model is suitable for external gain evaluations up to 6×. The 270kHz PCTL input filter limits the bandwidth; therefore, use the RF input as demonstrated in the model.

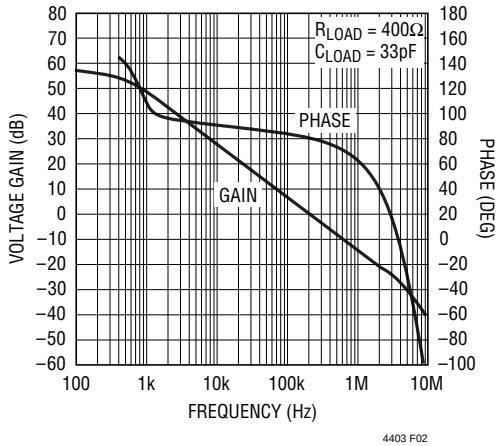


Figure 2. Measured Open Loop Gain and Phase, PCTL <100mV

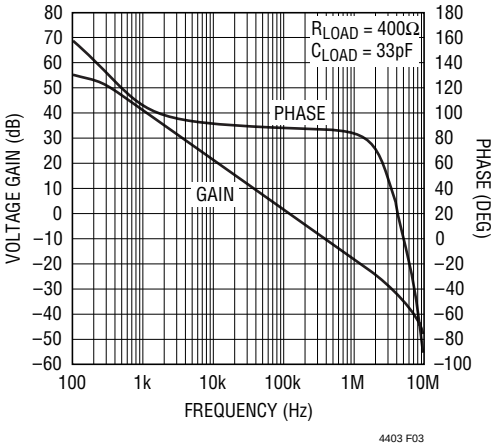


Figure 3. Measured Open Loop Gain and Phase, PCTL >200mV

APPLICATIONS INFORMATION

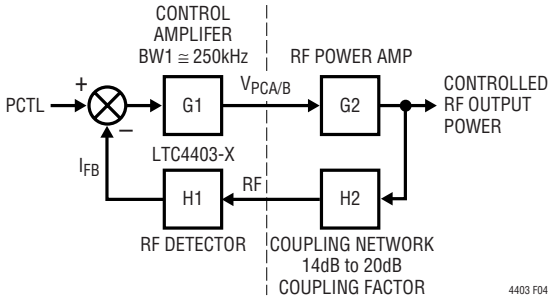


Figure 4. Closed Loop Block Diagram

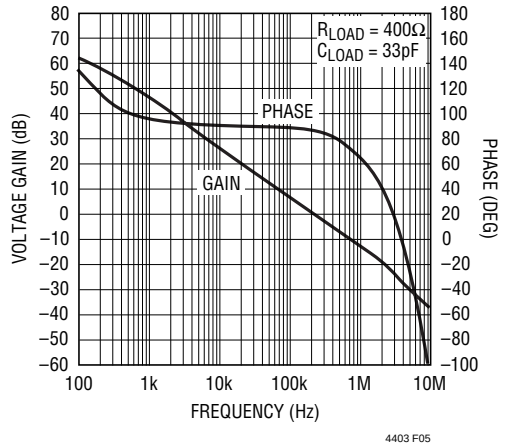


Figure 5. SPICE Model Open Loop Gain and Phase Characteristics from RF to V_{PCA}, PCTL <100mV

This model (Figure 6) is being supplied to LTC users as an aid to low frequency AC circuit design, but its use is not suggested as a replacement for breadboarding. Simulation should be used as a supplement to traditional lab testing.

Users should note very carefully the following factors regarding this model: Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully. While reasonable care has been taken in the preparation, LTC is not responsible for their correct application. These models are supplied “as is”, with no direct or implied responsibility on the part of LTC for their operation within a customer circuit or system. Further, Linear Technology Corporation reserves the right to change these models without prior notice.

In all cases, the current data sheet information is your final design guideline, and is the only performance guarantee. For further technical information, refer to individual device data sheets.

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APPLICATIONS INFORMATION

```
*LTC4403-X Low Frequency AC Spice Model*
*Main Network Description
GGIN1 ND3 0  ND2 IFB 86E-6
GGXFB IFB 0 0 ND12 33E-6
GGX5 ND11 0 0 ND10 1E-6
GGX6 ND12 0 0 ND11 1E-6
GGX1 ND4 0 0 ND3 1E-6
GGX2 ND6 0 0 ND4 1E-6
GGX3 ND7 0 0 ND6 1E-6
GGX4 ND8 0 0 ND7 1E-6
EEX1 ND9 0 0 ND8 2
CCC1 ND3 0 75E-12
CCPCTL2 ND2 0 7E-12
CCPCTL1 ND1 0 13E-12
CCLINT VPCA 0 5E-12
CCLOAD VPCA 0 33E-12
CCFB1 IFB 0 2.4E-12
CCX5 ND11 0 16E-15
CCX6 ND12 0 2E-15
CCP ND10 0 28E-12
CCX2 ND6 0 16E-15
CCX3 ND7 0 32E-15
LLX1 ND5 0 65E-3
RR01 ND3 0 20E6
RRFILT ND2 ND1 44E3
RRPCTL1 PCTL ND1 51E3
RRPCTL2 ND1 0 38E3
RR9 VPCA ND9 50
RRLOAD VPCA 0 400
RRFB1 IFB 0 22E3
RRT RF 0 250
RRX5 ND11 0 1E6
RRX6 ND12 0 1E6
RRSD RF ND10 500
RRX1 ND4 ND5 1E6
RRX2 ND6 0 1E6
RRX3 ND7 0 1E6
RRX4 ND8 0 1E6
**Closed loop feedback, comment-out VPCTL, VRF, Adjust EFB gain
to reflect external gain, currently set at 3X**
*EFB RF 0 VPCA VIN 3
*VIN VIN 0 DC 0 AC 1
*VPCTL PCTL 0 DC 0
**Open loop connections, comment-out EFB, VIN and VPCTL******
VPCTL PCTL 0 DC 0
VRF RF 0 DC 0 AC 1
******Add AC statement and print statement as required***
.AC DEC 50 10 1E7
*****for PSPICE only*****
.OP
.PROBE
**************************
.END
```

Figure 6. LTC4403-X Low Frequency AC SPICE Model

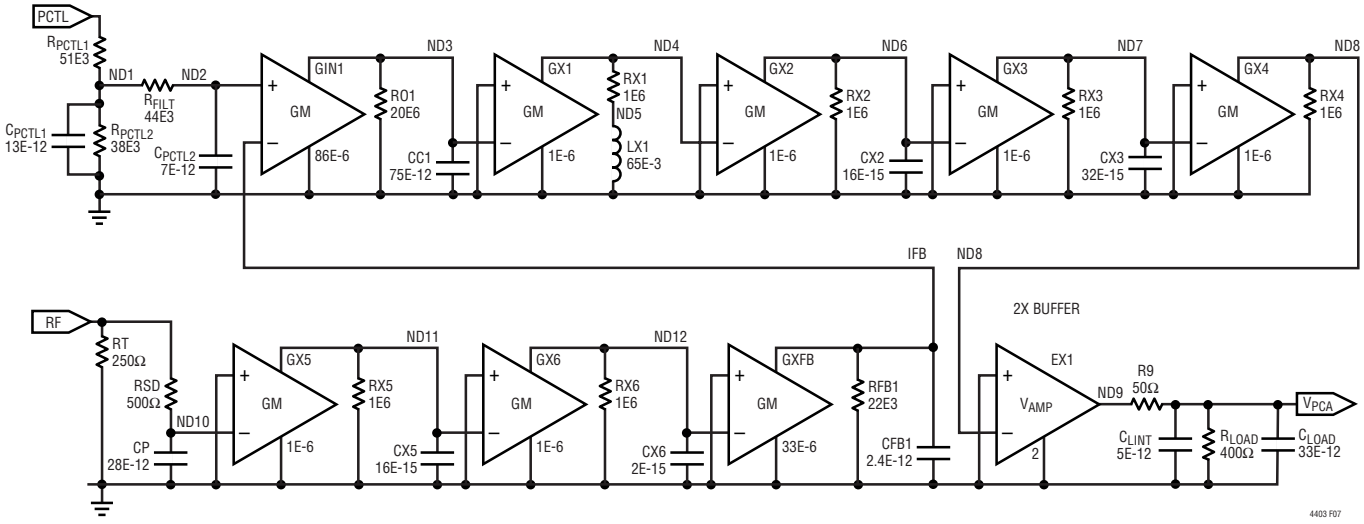
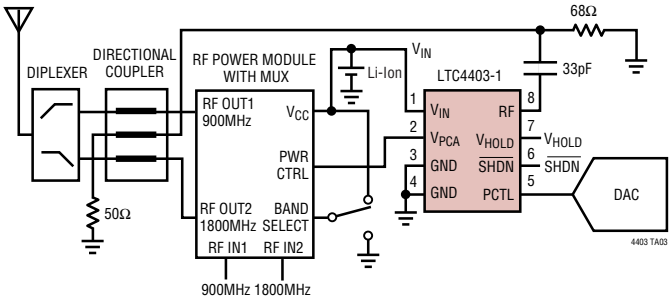


Figure 7. LTC4403 Low Frequency AC Model

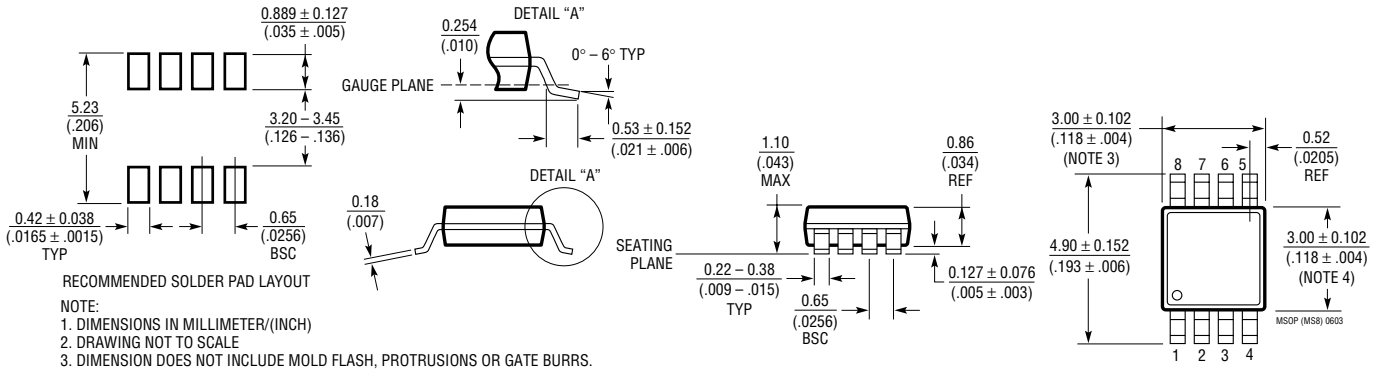
TYPICAL APPLICATION

Dual Band Cellular Telephone Transmitter



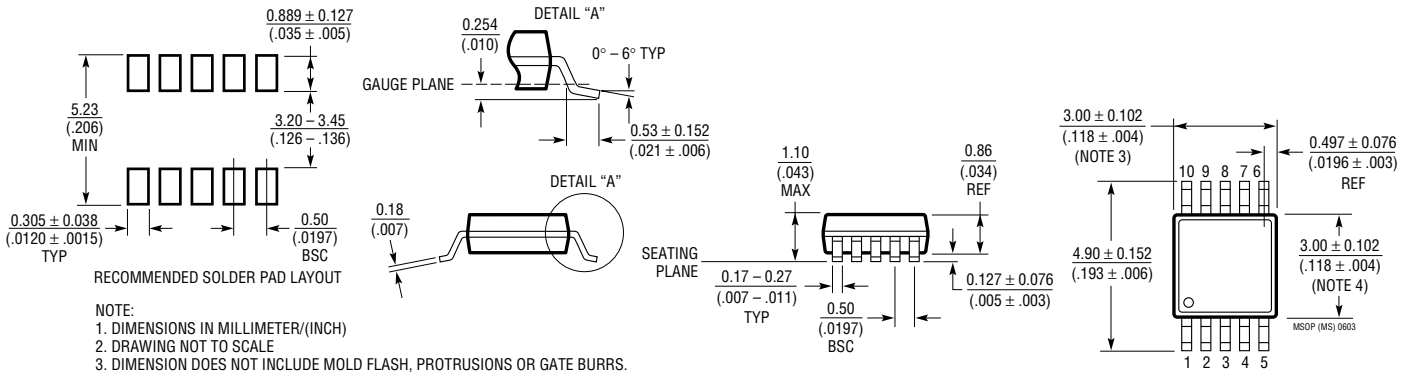
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

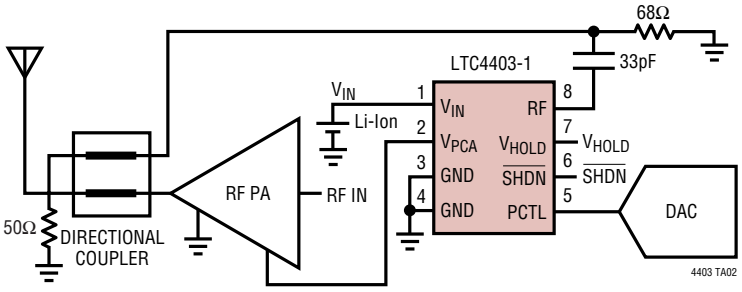
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Single Band Cellular Telephone Transmitter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1757A	RF Power Controller	Single/Dual Band GSM/DCS/GPRS Mobile Phones
LTC1758	RF Power Controller	Single/Dual Band GSM/DCS/GPRS Mobile Phones
LTC1957	RF Power Controller	Single/Dual Band GSM/DCS/GPRS Mobile Phones
LTC4400	SOT-23 RF PA Controller	Multiband GSM/DCS/GPRS Phones, 45dB Dynamic Range, 450kHz Loop BW
LTC4401	SOT-23 RF PA Controller	Multiband GSM/DCS/GPRS Phones, 45dB Dynamic Range, 250kHz Loop BW
LT®5500	1.8GHz to 2.7GHz Receiver Front End	Dual LNA Gain Setting +13.5dB/–14dB at 2.5GHz, Double-Balanced Mixer, $1.8V \le V_{SUPPLY} \le 5.25V$
LT5502	400MHz Quadrature IF Demodulator with RSSI	70MHz to 400MHz IF, $1.8V \le V_{SUPPLY} \le 5.25V$, 84dBm Limiting Gain, 90dB RSSI Range
LT5503	1.2GHz to 2.7GHz Direct IQ Modulator with Mixer	Direct IQ Modulator with Integrated 90° Phase Shifter, 4-Step RF Power Control, $1.8V \le V_{SUPPLY} \le 5.25V$
LT5504	800MHz to 2.7GHz RF Measuring Receiver	80dB Dynamic Range, Temperature Compensated, 2.7V to 5.5V Supply
LTC5505	300MHz to 3.5GHz RF Power Detector	>40dB Dynamic Range, Temperature Compensated, 2.7V to 6V Supply
LTC5507	100kHz to 1GHz RF Power Detector	40dB Dynamic Range, Temperature Compensated, 2.7V to 6V Supply
LTC5508	300MHz to 7GHz RF Power Detector	40dB Dynamic Range, 2.7V to 6V Supply, SC-70 Package
LTC5509	300MHz to 3GHz RF Power Detector	36dB Dynamic Range, Low Power, SC-70 Package
LT5511	High Signal Level Up Converting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5512	High Signal Level Down Converting Mixer	DC-3GHz RF Input, 20dBm IIP3, Integrated LO Buffer
LT5515	Direct Conversion Quadrature Demodulator	1.5GHz to 2.5GHz, 20dBm IIP3, Integrated Precision I/Q Demodulator
LT5516	Direct Conversion Quadrature Demodulator	800MHz to 1.5GHz, 21.5dBm IIP3, 12.8dB NF, 4.3dB Conversion Gain
LT5522	High Linearity Downconvert Mixer	600MHz to 2.7GHz, 25dBm IIP3, 50Ω Matched RF and LO Inputs
LTC5532	Precision 7GHz RF Power Detector	300MHz to 7GHz, 40dB Dynamic Range, Built-In Gain and Offset Adjustment

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