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MAX II CPLD: Lowest Power, Lowest Cost CPLD Family Ever

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Altera's MAX® II family of CPLD family are the lowest power, lowest cost CPLDs ever. MAX II CPLD family is based on a groundbreaking architecture that delivers the lowest power and the lowest cost per I/O pin of any CPLD family. With the introduction of the MAX IIZ CPLD, there are now three variants that all use the same innovative CPLD architecture:

- MAX II CPLD
- MAX IIG CPLD
- MAX IIZ CPLD

This instant-on, non-volatile CPLD family targets general-purpose, low-density logic and portable applications, such as cellular handset design. In addition to delivering the lowest cost for traditional CPLD designs, the MAX II CPLD drives power and cost improvements to higher densities, enabling you to use a MAX II CPLD in place of a higher power or higher cost ASSP or and standard-logic CPLD.

Advanced CPLD features

The MAX II CPLD enables a high level of functional integration to reduce system design costs. This section describes the advanced features found in every MAX II CPLD.

Low power CPLD

- One-tenth the power consumption (compared to a previous-generation 3.3-V MAX CPLD)
- 1.8-V core voltage for reduced power consumption and increased reliability
- CPLD industry's lowest standby specification, allowing longer use in battery powered applications
- Auto start/stop capability for turning off the CPLD when not in use

Cost-optimized architecture

- Four times the density at half the price (compared to previous MAX CPLD generations)
- Designed for minimum die size, giving the lowest cost per I/O pin in the industry

High performance

- Support for internal clock frequency rates of up to 300 MHz
- Twice the performance (compared to a 3.3-V MAX CPLD)

Unique features

- On-board oscillator and user flash memory
- Reduces chip count by eliminating discrete oscillators or non-volatile storage devices

Real-time in-system programmability (ISP)

- Capable of downloading a second design while the device is operational
- Reduces the cost of remote field updates

MultiVolt core flexibility

- On-chip voltage regulator accepts 3.3-V, 2.5-V, or 1.8-V supply
- Simplifies board design with fewer power rails

Parallel flash loader megafunction

- Improves configuration efficiency of non-JTAG-compliant flash devices on the board
- Simplifies board management by allowing JTAG command implementation via the MAX II CPLD

I/O capabilities

- MultiVolt I/O capability allows interface with devices at 1.5-V, 1.8-V, 2.5-V, or 3.3-V logic levels
- Schmitt triggers, programmable slew rate, and programmable drive strength improve signal integrity

Easiest-to-use software

- Altera's no-cost Quartus® II Web Edition software supports all devices in the MAX II CPLD family and optimizes pin-locked fitting and performance
- New MAX+PLUS® II look-and-feel option in the Quartus II software enhances ease of use

CPLD Applications

The MAX II CPLD family targets common control path applications, including:

- Power-up sequencing
- System configuration
- I/O expansion
- Interface bridging

Related CPLD links

- *MAX II CPLD Backgrounder* (PDF)
- MAX II CPLD Questions and Answers
- *MAX II CPLD Device Handbook*

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