Low Power Consumption Class D Speaker Amplifier series

9 W + 9 W Analog Input Class D Stereo Speaker Amplifier

BD28412MUV

General Description

BD28412MUV is 9 W + 9 W stereo (or 18 W monaural under parallel connection) class D amplifier which can output power without an external heat sink.
This LSI has built-in precise oscillator which generate selectable switching frequencies, so AM radio interference can be avoided. In addition, 2.1 Ch audio system can be achieved by master and slave operation without caring about beat noise.
This LSI achieves lower power consumption under low output power, and suitable for speaker systems in which battery is equipped such as wireless speakers.

Features

- Analog Differential Input
- Low Standby Current
- Output Feedback Circuitry Prevents Sound Quality Degradation Caused by Power Supply Voltage Fluctuation, Achieves Low Noise and Low Distortion, Eliminates the Need of Large Electrolytic-Capacitors for Decoupling
- Power Limit Function (Linearly-programmable for voltage of PLIMIT)
- Selectable Switching Frequency (AM Avoidance Function)
- Synchronization Control is Supported (Selectable Master and Slave Operation)
- Parallel BTL (PBTL) is Supported
- Wide Voltage Range (V_{CC} = 4.5 V to 13 V)
- Operate with Single Power Supply
- High Efficiency and Low-heat-generation Make the System Smaller, Thinner, and More Power-saving
- Pop Noise Prevention During Power Supply ON/OFF
- High Reliability Design by Built-in Protection Circuits
  - Overheat Protection
  - Under Voltage Protection
  - Output Short Protection
  - Output DC Voltage Protection
- Small Package (VQFN032V5050) Achieves Mount Area Reduction

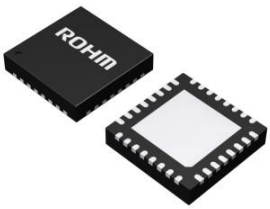
Applications

- Wireless Speakers, Small Active Speakers, Portable Audio Equipments, etc.

Key Specifications

- Supply Voltage Range: 4.5 V to 13 V
- Speaker Output Power: 9 W + 9 W (Typ)
  (V_{CC} = 12 V, R_L = 8 Ω, PLIMIT = 0 V)
- Speaker Output Power(PBTL): 18 W (Typ)
  (V_{CC} = 12 V, R_L = 4 Ω, PLIMIT = 0 V)
- Total Harmonic Distortion Ratio:
  0.03 % (Typ) @P_O = 1 W
  (V_{CC} = 11 V, R_L = 8 Ω, PLIMIT = 0 V)
- Crosstalk: 100 dB (Typ)
- PSRR: 55 dB (Typ)
- Output Noise Voltage: -80 dBV (Typ)
- Standby Current: 0.1 µA (Typ)
- Operating Current: 16 mA (Typ)
  (No Load nor Filter, No Signal)
- Operating Temperature Range: -25 °C to +85 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN032V5050	5.00 mm x 5.00 mm x 1.00 mm



Typical Application Circuit

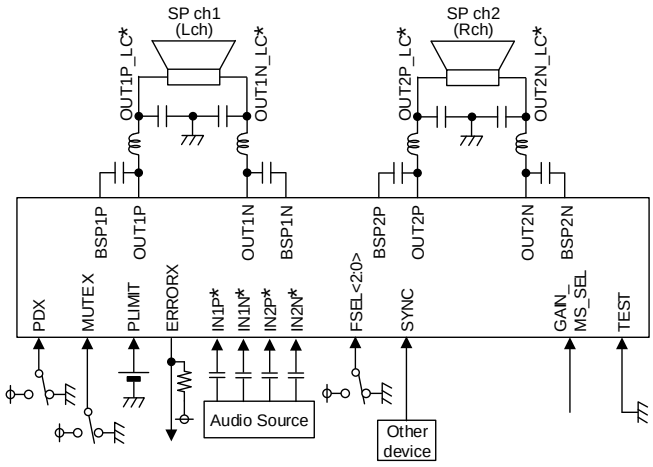


Figure 1. Typical Application Circuit

*The phase of OUTxx_LC is inverted from the phase of INxx.
ex. The phase of OUT1P_LC is inverted from the phase of IN1P.

Pin Configuration

(TOP VIEW)

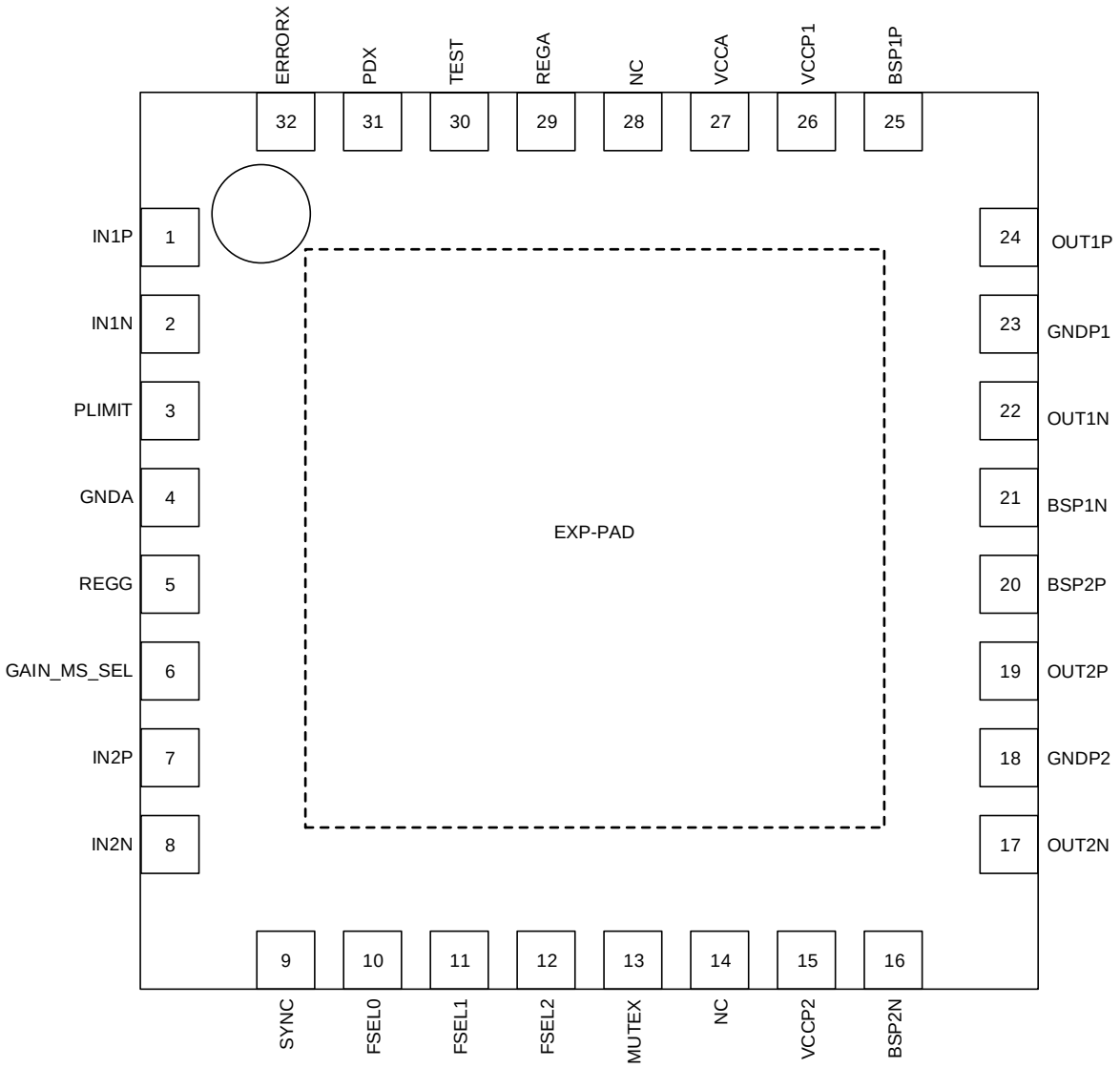
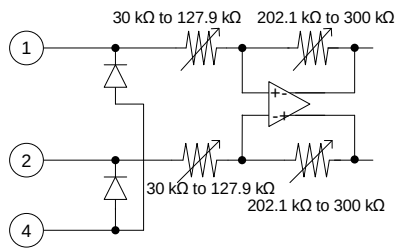
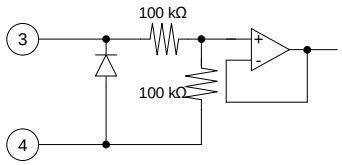
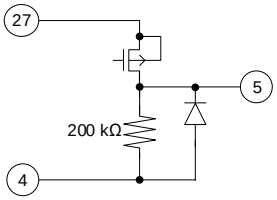
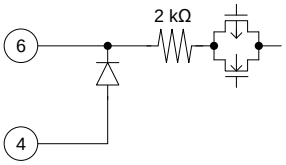
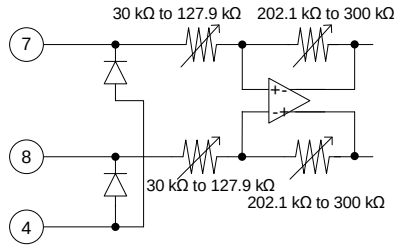
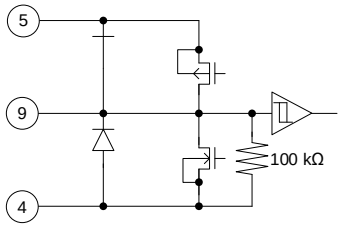
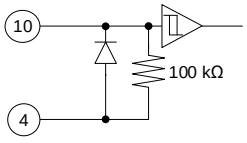
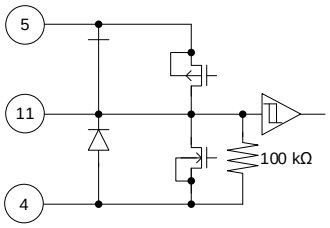
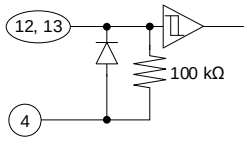
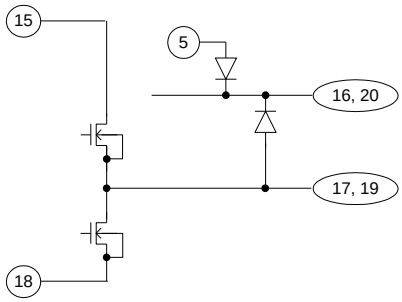
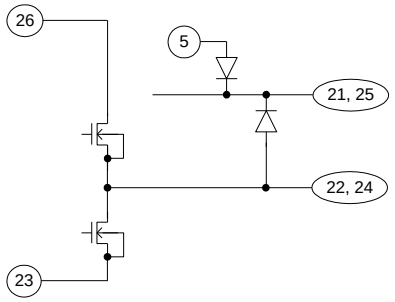
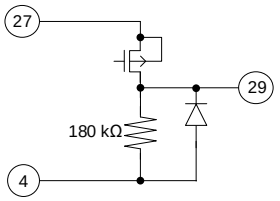


Figure 2. Pin Configuration

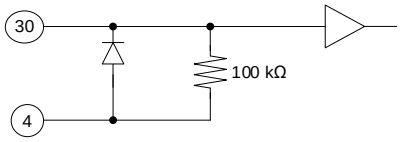
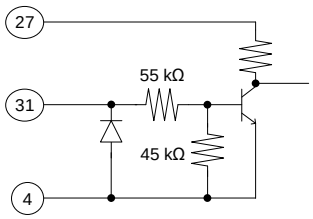
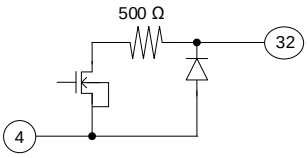
Pin Description

Pin No.	Pin Name(Note 2)	IO	Function	Internal Equivalent Circuit(Note 1)
1	IN1P	I	Positive audio signal input pin for Ch1	
2	IN1N	I	Negative audio signal input pin for Ch1	
3	PLIMIT	I	Power limit level setting pin	
4	GNDA	-	Ground pin for Analog	-
5	REGG	O	Internal power supply pin for gate driver Please connect a capacitor. ***Caution:*** *REGG of BD28412MUV should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization and the resistors for setting of GAIN_MS_SEL and PLIMIT.*	
6	GAIN_MS_SEL	I	Gain and Master/Slave mode setting pin	
7	IN2P	I	Positive audio signal input pin for Ch2	
8	IN2N	I	Negative audio signal input pin for Ch2	
9	SYNC	I/O	PWM clock input/output pin to synchronize multiple class D amplifiers	
10	FSEL0	I	PWM frequency setting pin 0	

Pin Description – continued

Pin No.	Pin Name(Note 2)	IO	Function	Internal Equivalent Circuit(Note 1)
11	FSEL1	I	PWM frequency setting pin 1	
12	FSEL2	I	PWM frequency setting pin 2	
13	MUTEX	I	Speaker output mute control pin High: Mute OFF Low: Mute ON	
14	NC	-	Non- connection This pin should be opened. Connecting to ground is also available.	-
15	VCCP2	-	Power supply pin for Ch2 Please connect a capacitor.	
16	BSP2N	O	Boot-strap pin of Ch2 negative Please connect a capacitor.	
17	OUT2N(Note 3)	O	Output pin of Ch2 negative PWM signal Please connect to output LPF.	
18	GNDP2	-	Ground pin for Ch2 for power.	
19	OUT2P(Note 3)	O	Output pin of Ch2 positive PWM signal Please connect to output LPF.	
20	BSP2P	O	Boot-strap pin of Ch2 positive Please connect a capacitor.	
21	BSP1N	O	Boot-strap pin of Ch1 negative Please connect a capacitor.	
22	OUT1N(Note 3)	O	Output pin of Ch1 negative PWM signal Please connect to output LPF.	
23	GNDP1	-	Ground pin for Ch1 for power	
24	OUT1P(Note 3)	O	Output pin of Ch1 positive PWM signal Please connect to output LPF.	
25	BSP1P	O	Boot-strap pin of Ch1 positive Please connect a capacitor.	
26	VCCP1	-	Power supply pin for Ch1 Please connect a capacitor.	
27	VCCA	-	Power supply pin for Analog Please connect a capacitor.	-
28	NC	-	Non- connection This pin should be opened. Connecting to ground is also available.	-
29	REGA	O	Internal power supply pin Please connect a capacitor. ***Caution:*** *Regulator output pin for internal circuit should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization.*	

Pin Description – continued

Pin No.	Pin Name(Note 2)	IO	Function	Internal Equivalent Circuit(Note 1)
30	TEST	I	Test pin Please connect to ground.	
31	PDX	I	Power down setting pin High: Active Low: Standby	
32	ERRORX	O	Error flag pin Please connect to pull-up resistor. High: Normal Low: Error detected ***Caution:*** *An error flag occurs when Output Short Protection, DC Voltage Protection, or High Temperature Protection is activated. This flag shows LSI condition during operation.* *Use for purposes other than this product cannot be used.*	
-	EXP-PAD	-	There is no problem when EXP-PAD is left unconnected. However, connecting it to ground is recommended because the radiation performance will be degraded. The connection to any place except for the ground is prohibited.	EXP-PAD for heat radiation

(Note 1) The numerical value of internal equivalent circuit is typical value, not guaranteed value.
(Note 2) On succeeding pages, each pin names means the name of the pin and voltage value which is applied to the pin.
(Note 3) On succeeding pages, OUT1P - OUT1N is OUT1, OUT2P - OUT2N is OUT2.

Block Diagram

(TOP VIEW)

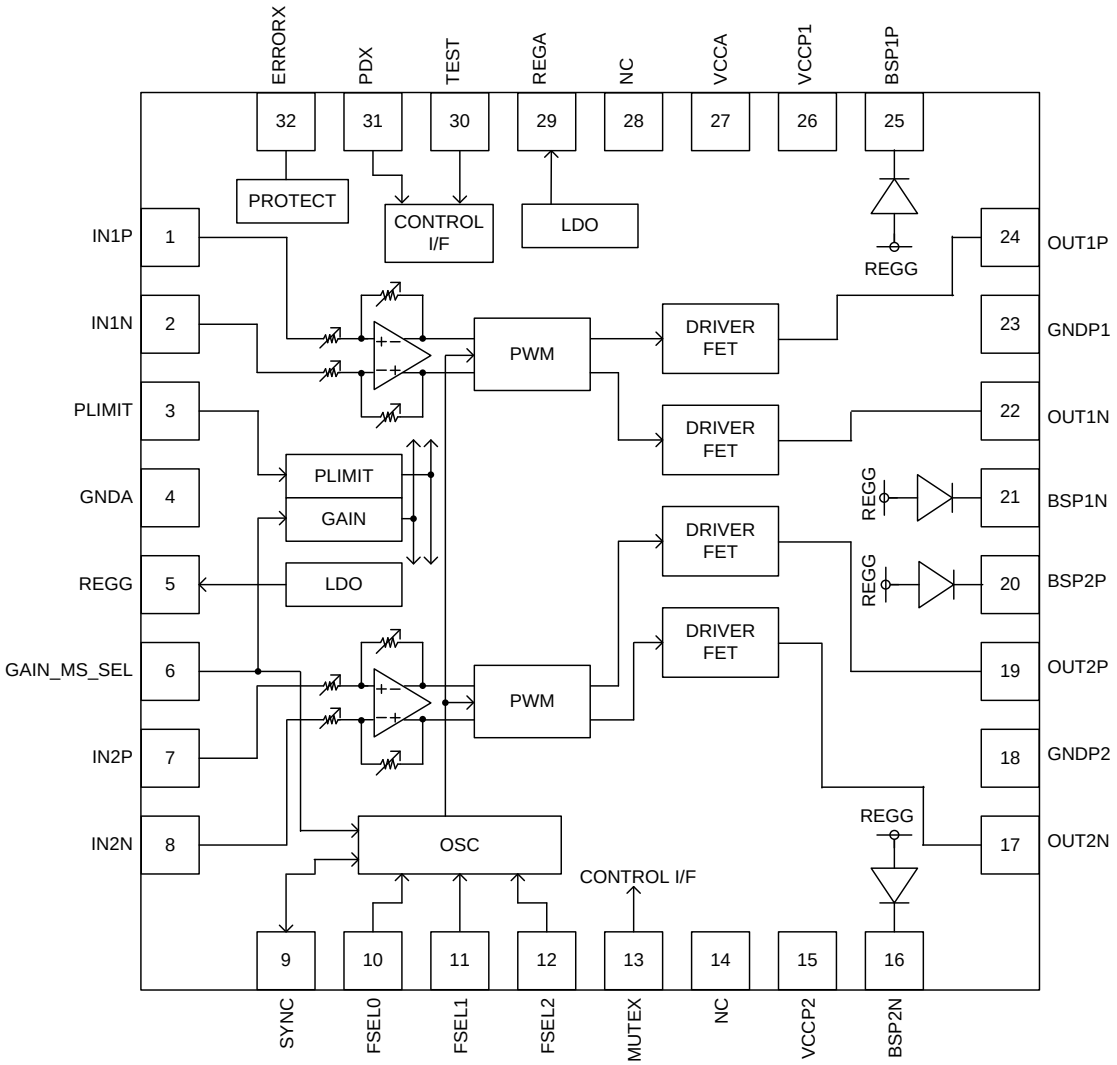


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Target Pins, Conditions
Supply Voltage *(Note 4)*	V_{CCMAX}	-0.3 to +15.5	V	VCCA, VCCP1, VCCP2
Input Voltage1 *(Note 4)*	V_{IN}	-0.3 to +7	V	IN1P, IN1N, IN2P, IN2N, PLIMIT, GAIN_MS_SEL, SYNC *(Note 5)*, FSEL0, FSEL1, FSEL2, PDX, MUTEX
Input Voltage2 *(Note 4)*	V_{ERR}	-0.3 to +7	V	ERRORX
Pin Voltage *(Note 4), (Note 6)*	V_{PIN}	-0.3 to +V_{CCMAX}	V	OUT1P, OUT1N, OUT2P, OUT2N
Storage Temperature Range	Tstg	-55 to +150	°C	-
Maximum Junction Temperature	Tjmax	+150	°C	-

Caution 1: *Operating the LSI over the absolute maximum ratings may damage the LSI. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the LSI is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 4) The voltage that can be applied reference to ground (GNDA, GNDP1, GNDP2).
(Note 5) In case SYNC is specified as input mode.
(Note 6) Please use under this rating including the AC peak waveform (overshoot) for all conditions.
Only undershoot is allowed at condition of ≤ 15.5 V by the VCC reference and ≤ 10 ns (cf. Figure 4)

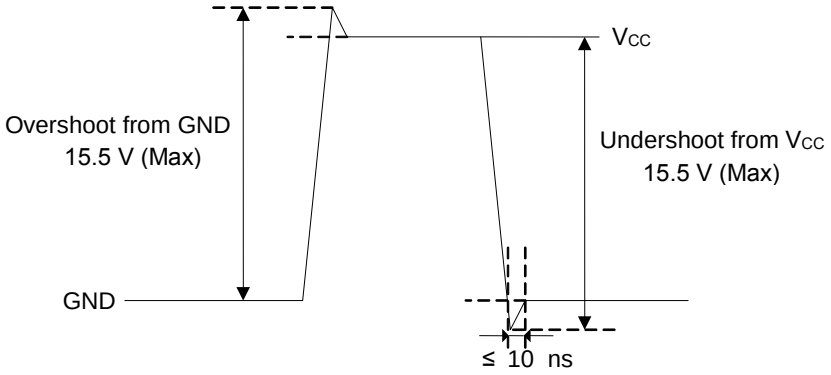


Figure 4. Overshoot and Undershoot

Thermal Resistance(Note 7)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 9)	2s2p(Note 10)	
VQFN032V5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter(Note 8)	Ψ_{JT}	11	5	°C/W

(Note 7) Based on JESD51-2A (Still-Air)
(Note 8) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 9) Using a PCB board based on JESD51-3.
(Note 10) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 11)	
			Pitch	Diameter
4 Layers	TR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 11) This thermal via connects with the copper pattern of all layers.

Use a thermal design that allows for a sufficient margin in consideration of power dissipation under actual operating conditions. This LSI exposes its frame at the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Target Pins, Conditions
Operating Temperature	Topr	-25	+25	+85	°C	-
Supply Voltage	V_{CC}	4.5	-	13	V	VCCA, VCCP1, VCCP2
Load Impedance(Note 12)	R_{L1}	5.4	-	-	Ω	BTL
	R_{L2}	3.2	-	-	Ω	PBTL
High Level Input Voltage	V_{IH}	2.0	-	3.3	V	FSEL0, FSEL1, FSEL2, PDX, MUTEX
Low Level Input Voltage	V_{IL}	0	-	0.8	V	FSEL0, FSEL1, FSEL2, PDX, MUTEX
Low Level Output Voltage	V_{OL}	-	-	0.8	V	ERRORX, I_{OL} = 0.5 mA

(Note 12) Tj < 150 °C

Electrical Characteristics

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, R_L = 8 Ω, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

Parameter	Symbol	Min	Typ	Max	Unit	Target Pins, Conditions
Standby Current	I_{CC1}	-	0.1	25	µA	No load nor filter, PDX = 0 V, MUTEX = 0 V
Mute Current	I_{CC2}	-	10	20	mA	No load nor filter, PDX = 3.3 V, MUTEX = 0 V
Active Current	I_{CC3}	-	16	32	mA	No load or filter, No signal, PDX = 3.3 V, MUTEX = 3.3 V
Regulator Output Voltage	V_{REGG}	4.45	5.55	6.05	V	PDX = 3.3 V, MUTEX = 3.3 V
Input Impedance 1	R_{IN1}	50	-	-	kΩ	MUTEX, PDX, FSEL0, FSEL1, FSEL2, SYNC (Slave mode only)
Input Impedance 2	R_{IN2}	140	200	260	kΩ	PLIMIT
Output Power*(Note 13)*	P_{O1}	-	9	-	W	V_{CC} = 12 V, THD+N = 10 %
Gain 1*(Note 13)*	G_{V1}	19	20	21	dB	P_O = 1 W, GAIN_MS_SEL = 0 V
Gain 2*(Note 13)*	G_{V2}	25	26	27	dB	P_O = 1 W, GAIN_MS_SEL = 2/9 × V_{REGG}
Gain 3*(Note 13)*	G_{V3}	31	32	33	dB	P_O = 1 W, GAIN_MS_SEL = 3/9 × V_{REGG}
Gain 4*(Note 13)*	G_{V4}	35	36	37	dB	P_O = 1 W, GAIN_MS_SEL = 4/9 × V_{REGG}
Total Harmonic Distortion*(Note 13)*	THD	-	0.03	-	%	P_O = 1 W, BW = AES17
Crosstalk*(Note 13)*	CT	60	100	-	dB	P_O = 1 W, 1 kHz BPF
PSRR*(Note 13)*	PSRR	-	55	-	dB	V_{RIPPLE} = 0.2 V_{P-P}, f = 1 kHz
Output Noise Voltage*(Note 13)*	V_{NO}	-	-80	-70	dBV	P_O = 0 W, BW = A-Weight
PWM (Pulse Width Modulation) Frequency	f_{PWM1}	1128	1200	1272	kHz	FSEL2 = 3.3 V, FSEL1 = 3.3 V, FSEL0 = 3.3 V
	f_{PWM2}	940	1000	1060	kHz	FSEL2 = 3.3 V, FSEL1 = 3.3 V, FSEL0 = 0 V
	f_{PWM3}	564	600	636	kHz	FSEL2 = 3.3 V, FSEL1 = 0 V, FSEL0 = 3.3 V
	f_{PWM4}	470	500	530	kHz	FSEL2 = 3.3 V, FSEL1 = 0 V, FSEL0 = 0 V
	f_{PWM5}	376	400	424	kHz	FSEL2 = 0 V, FSEL1 = 3.3 V, FSEL0 = 3.3 V

(Note 13) The typical performance of device is shown in the Limits of these items. It largely depends on the board layout, parts, and power supply.

Typical Performance Curves

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

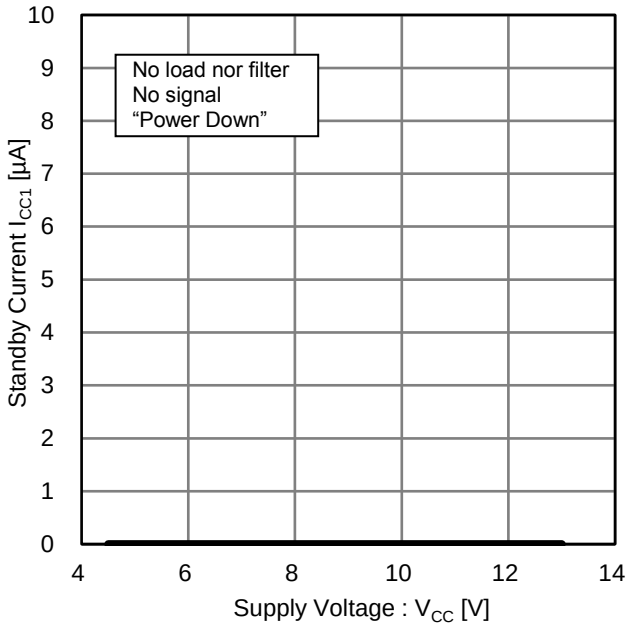


Figure 5. Standby Current vs Supply Voltage (Power Down)

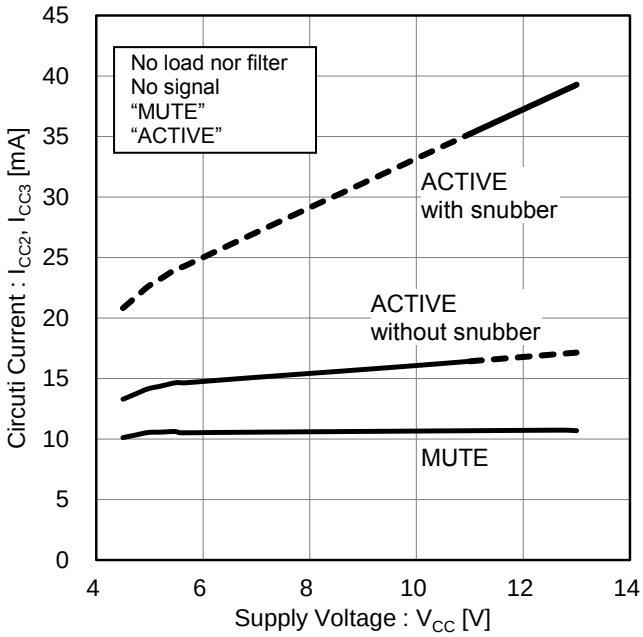


Figure 6. Circuit Current vs Supply Voltage (MUTE, ACTIVE)

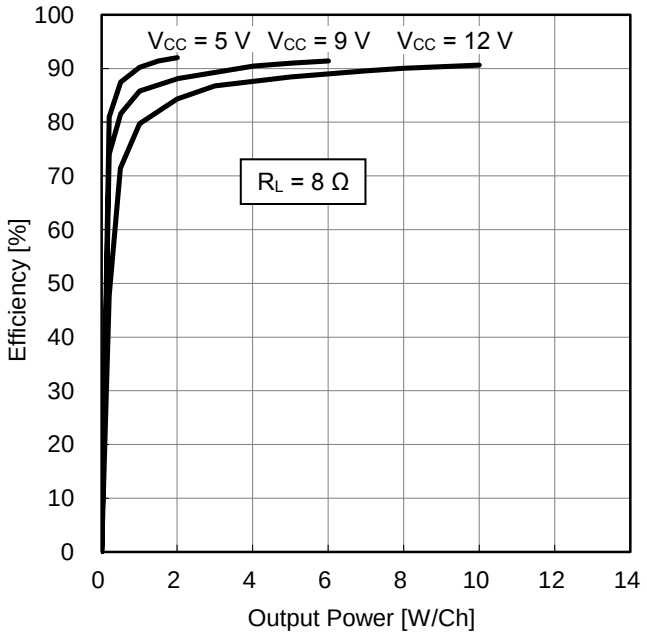


Figure 7. Efficiency vs Output Power (R_L = 8 Ω)

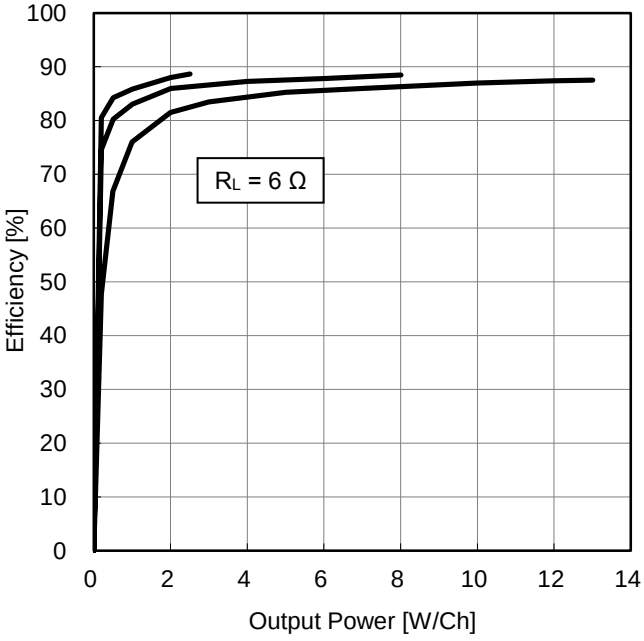


Figure 8. Efficiency vs Output Power (R_L = 6 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

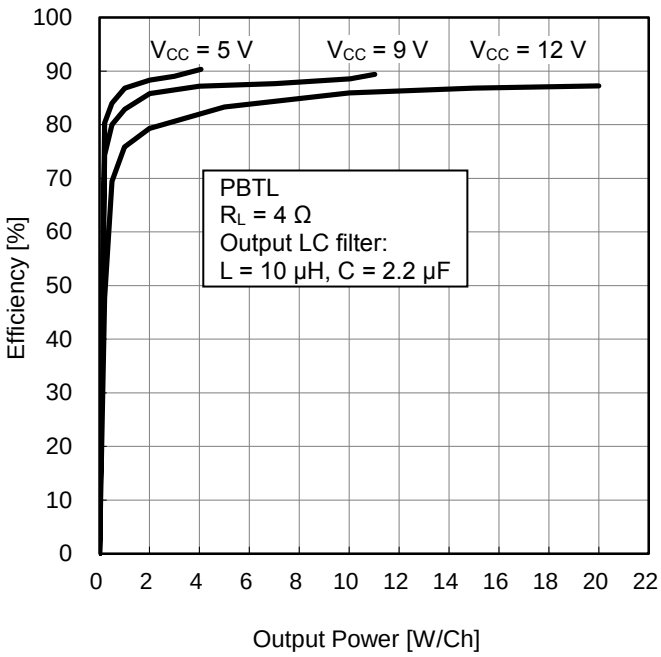


Figure 9. Efficiency vs Output Power (PBTL, R_L = 4 Ω)

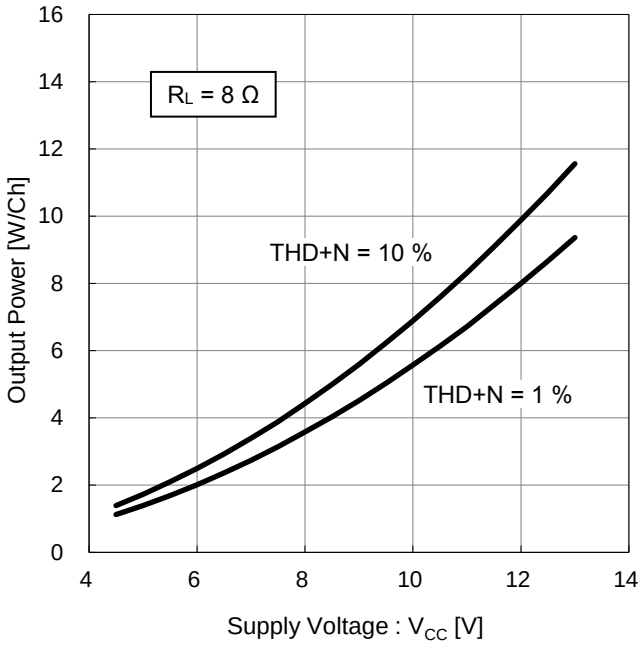


Figure 10. Output Power vs Supply Voltage (R_L = 8 Ω)

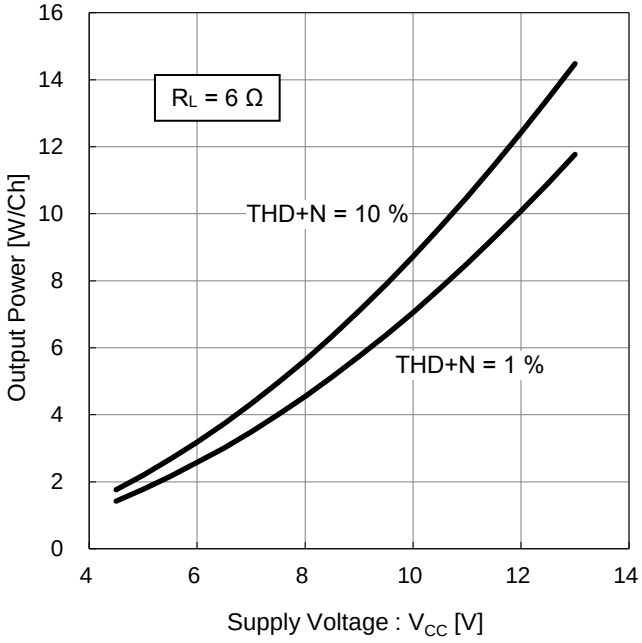


Figure 11. Output Power vs Supply Voltage (R_L = 6 Ω)

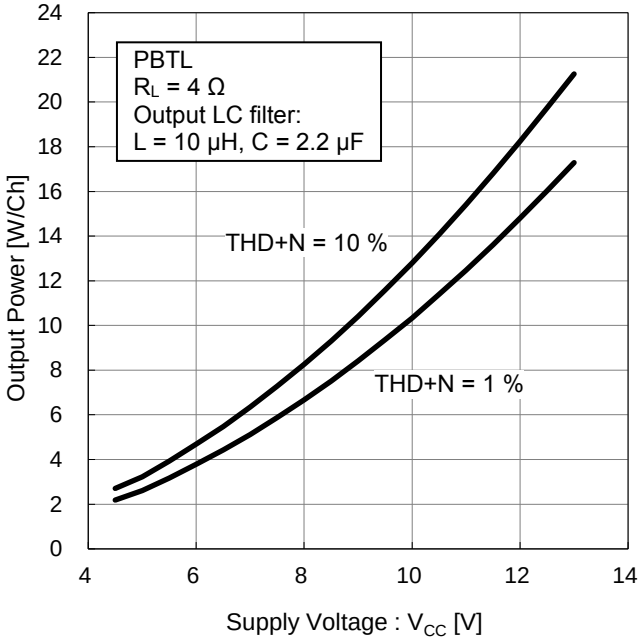


Figure 12. Output Power vs Supply Voltage (PBTL, R_L = 4 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

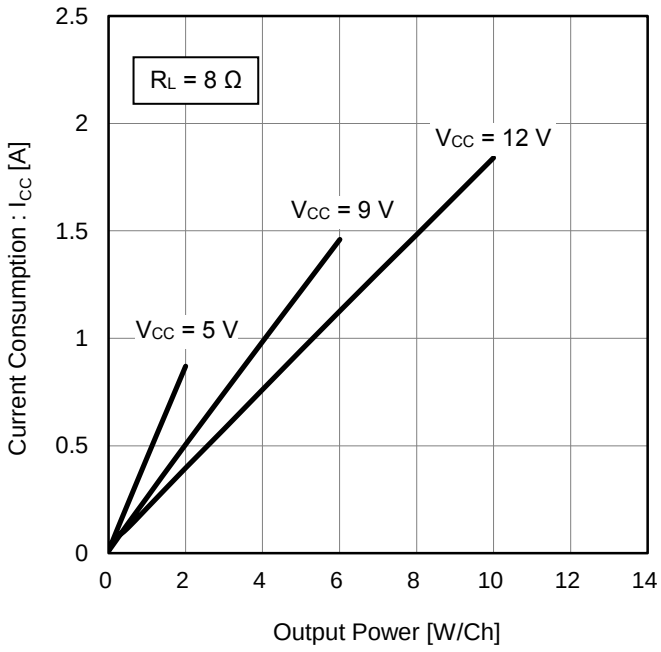


Figure 13. Current Consumption vs Output Power (R_L = 8 Ω)

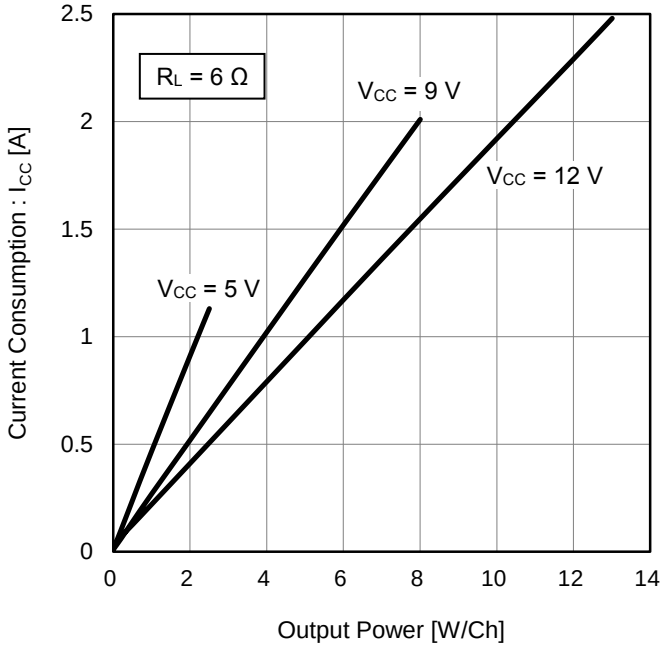


Figure 14. Current Consumption vs Output Power (R_L = 6 Ω)

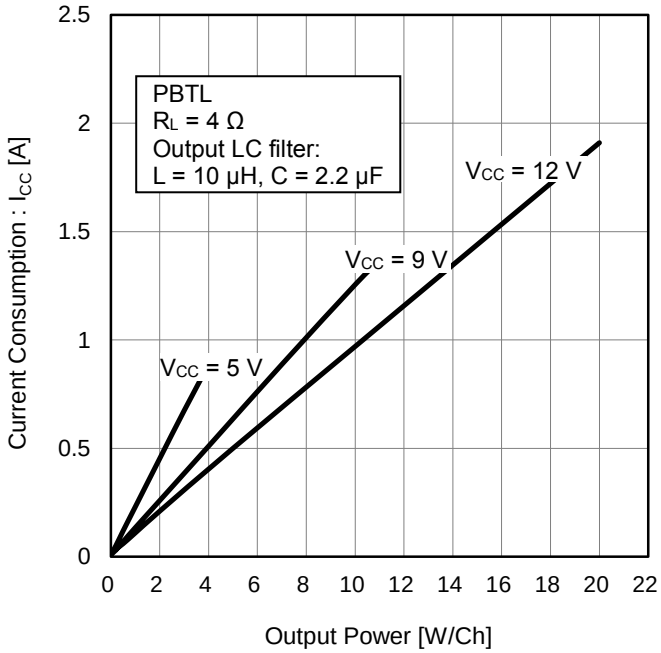


Figure 15. Current Consumption vs Output Power (PBTL, R_L = 4 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

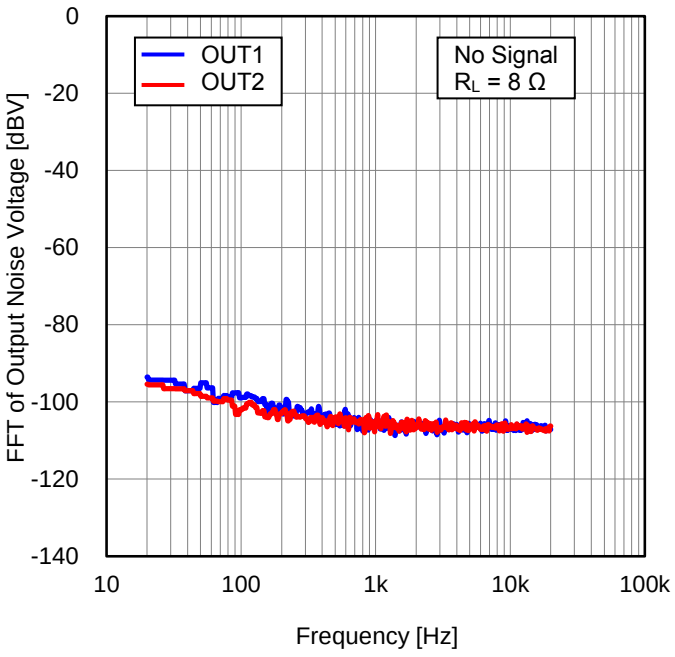


Figure 16. FFT of Output Noise Voltage vs Frequency
(R_L = 8 Ω)

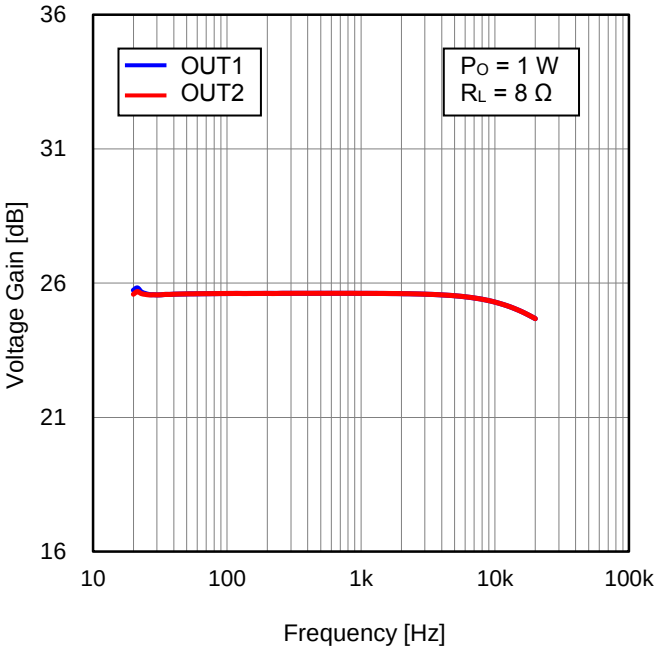


Figure 17. Voltage Gain vs Frequency
(R_L = 8 Ω)

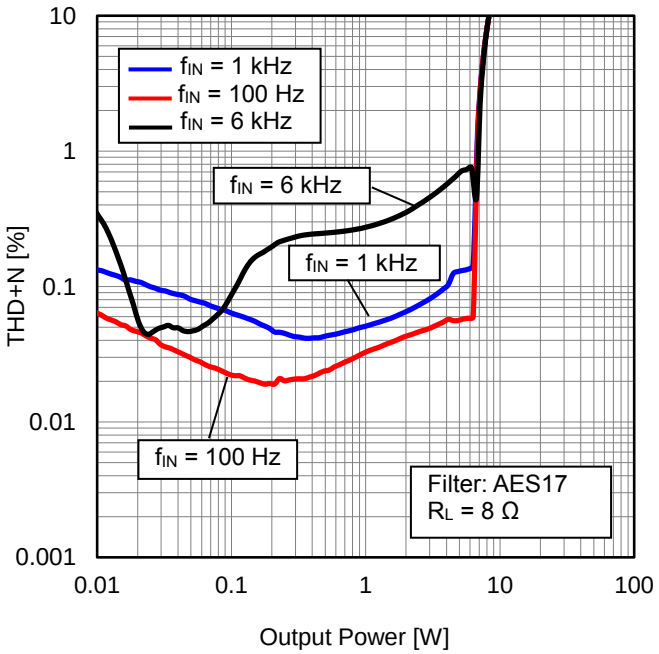


Figure 18. THD+N vs Output Power
(R_L = 8 Ω)

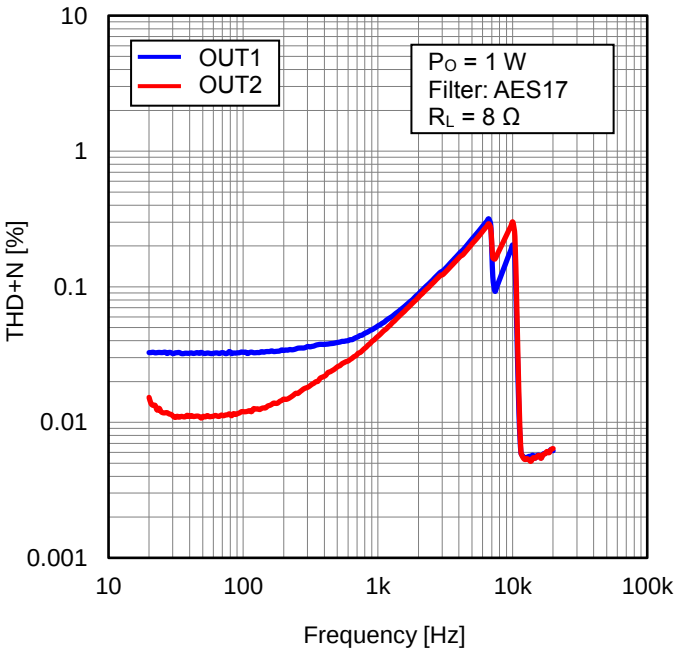


Figure 19. THD+N vs Frequency
(R_L = 8 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

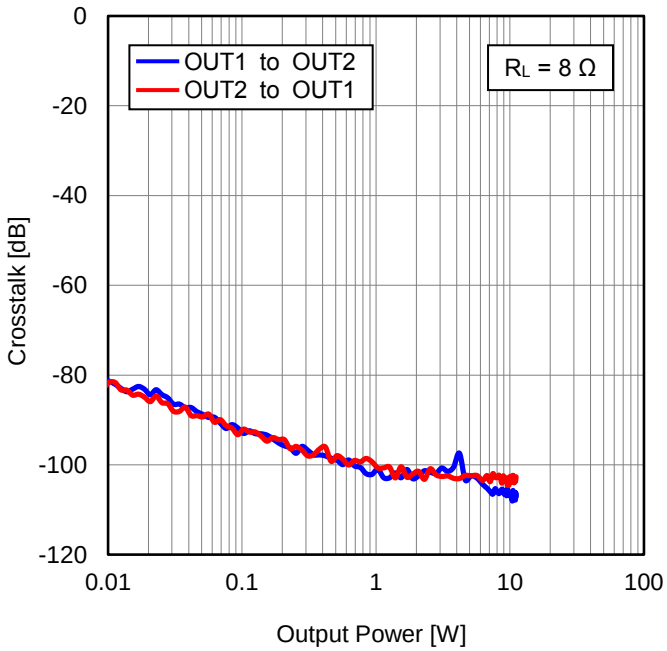


Figure 20. Crosstalk vs Output Power
(R_L = 8 Ω)

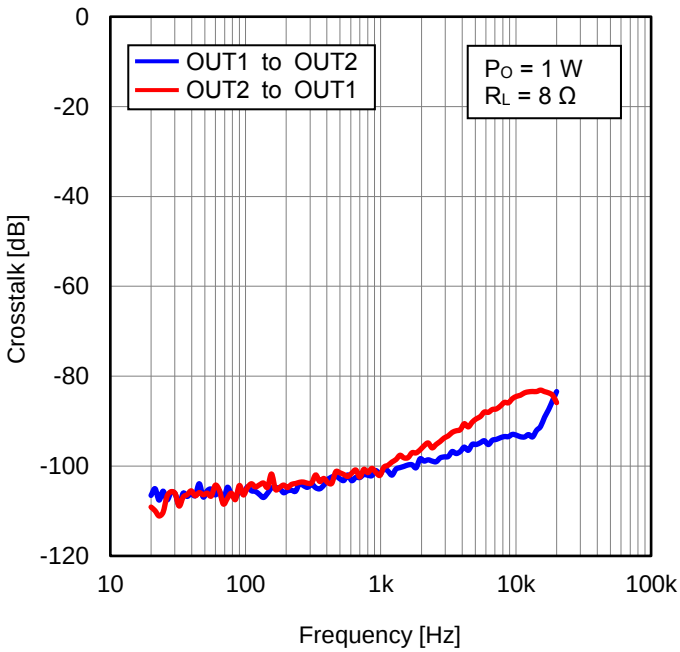


Figure 21. Crosstalk vs Frequency
(R_L = 8 Ω)

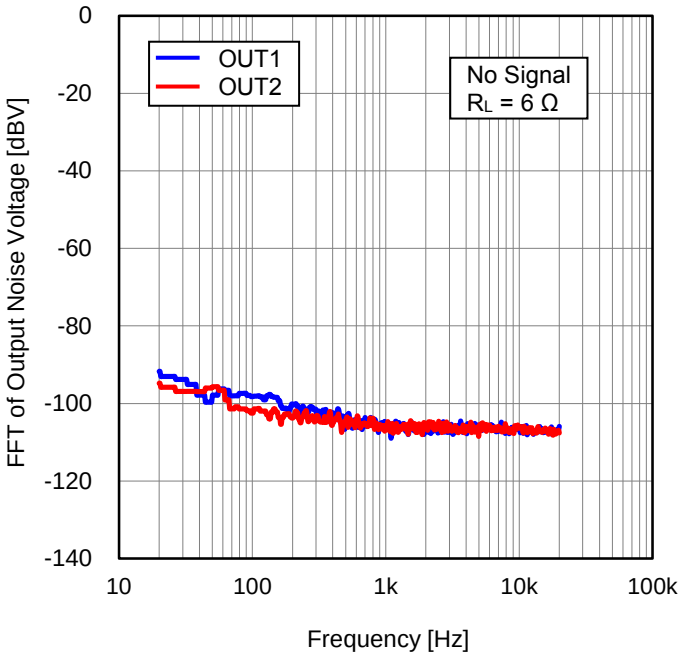


Figure 22. FFT of Output Noise Voltage vs Frequency
(R_L = 6 Ω)

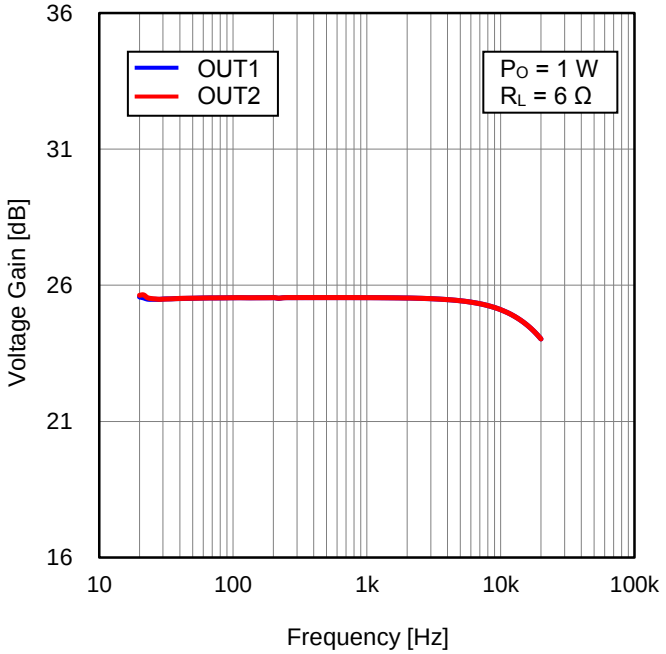


Figure 23. Voltage Gain vs Frequency
(R_L = 6 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

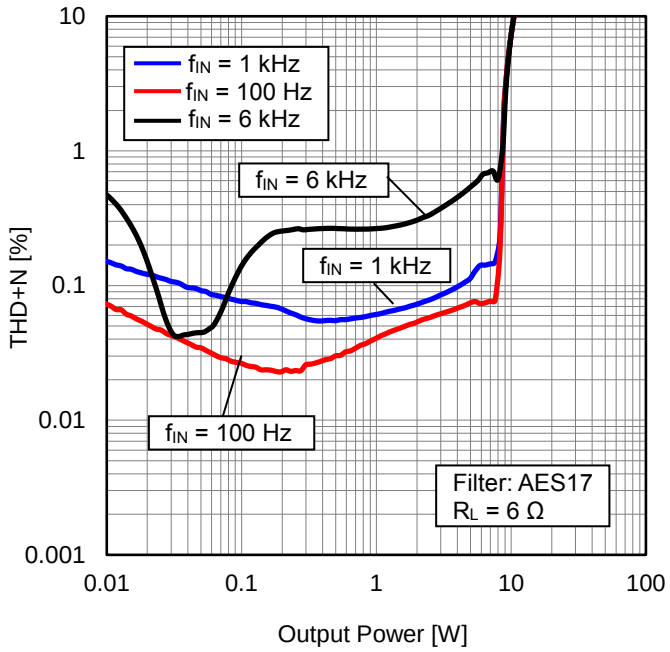


Figure 24. THD+N vs Output Power
(R_L = 6 Ω)

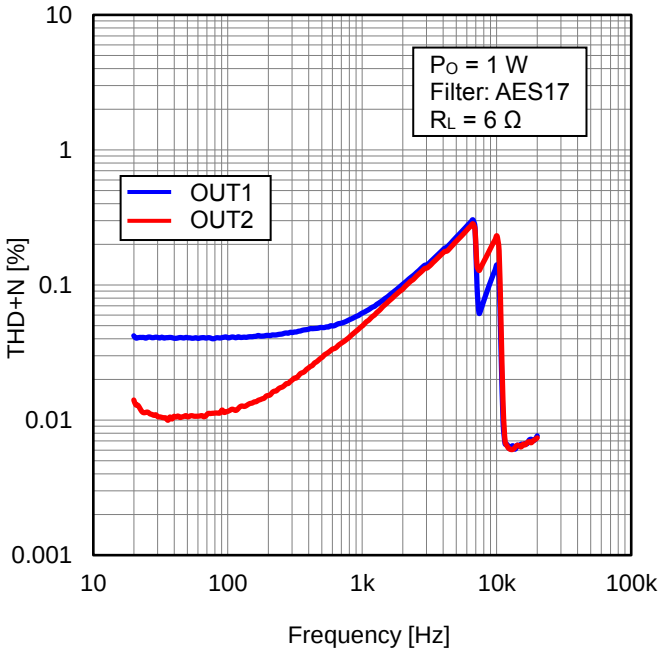


Figure 25. THD+N vs Frequency
(R_L = 6 Ω)

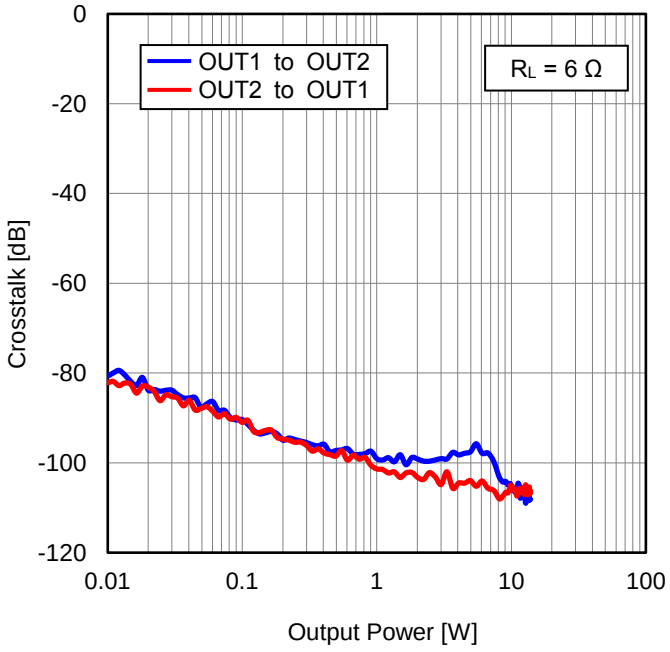


Figure 26. Crosstalk vs Output Power
(R_L = 6 Ω)

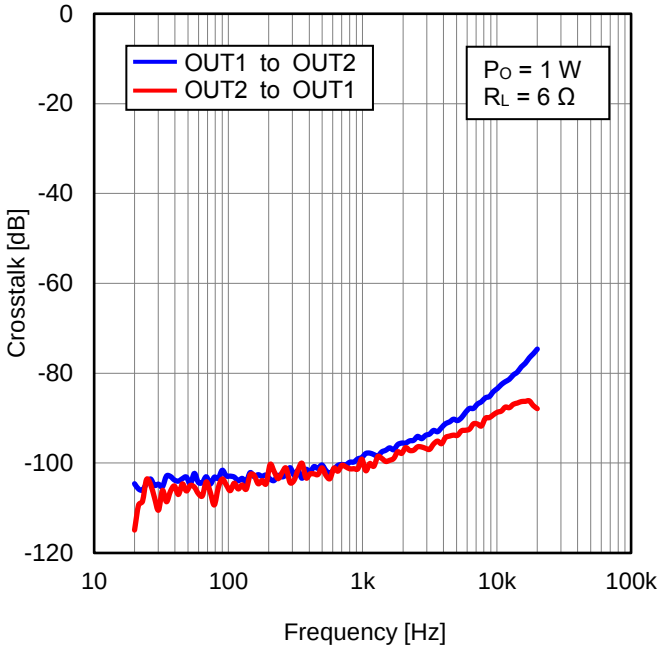


Figure 27. Crosstalk vs Frequency
(R_L = 6 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{PWM} = 600 kHz, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 10 µH, C = 2.2 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

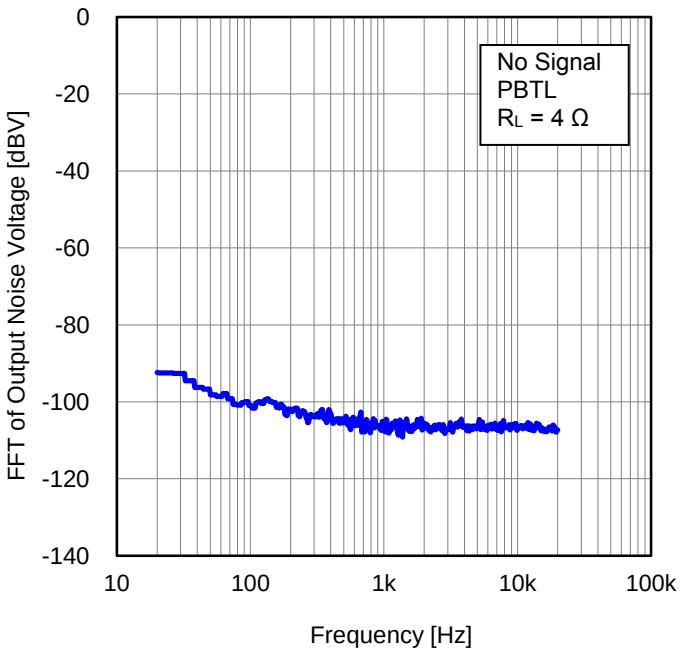


Figure 28. FFT of Output Noise Voltage vs Frequency
(PBTL, R_L = 4 Ω)

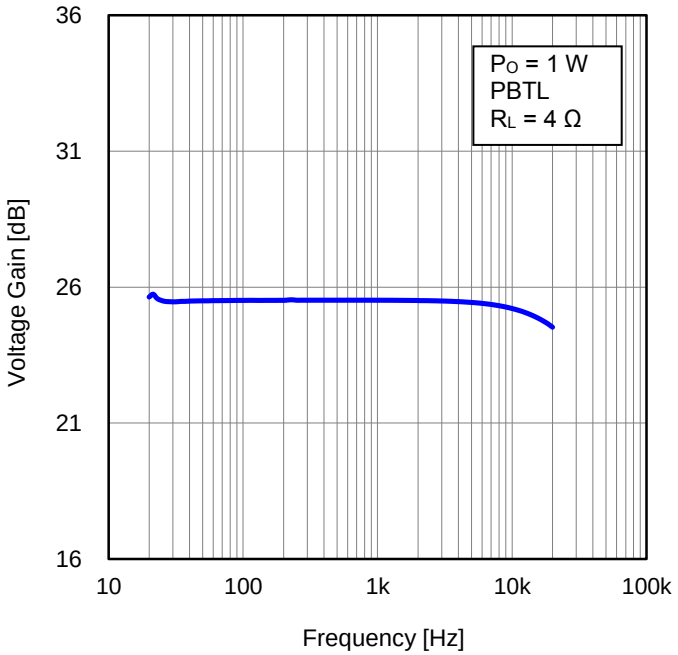


Figure 29. Voltage Gain vs Frequency
(PBTL, R_L = 4 Ω)

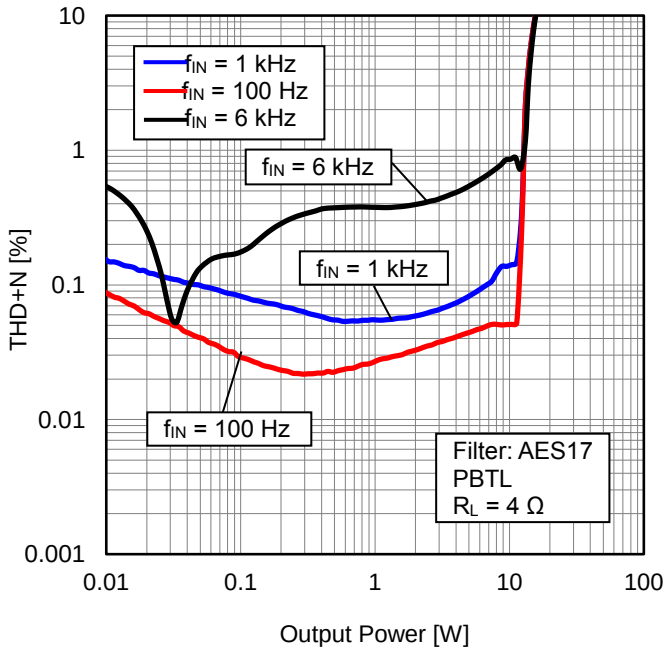


Figure 30. THD+N vs Output Power
(PBTL, R_L = 4 Ω)

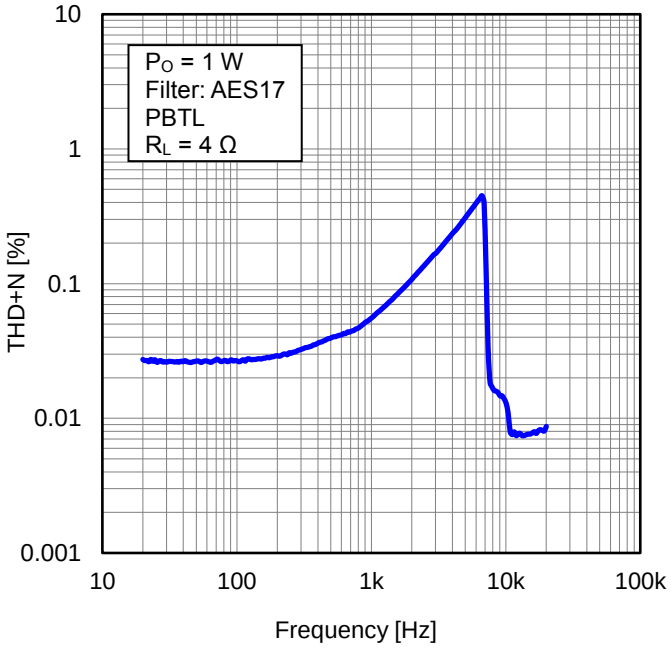


Figure 31. THD+N vs Frequency
(PBTL, R_L = 4 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

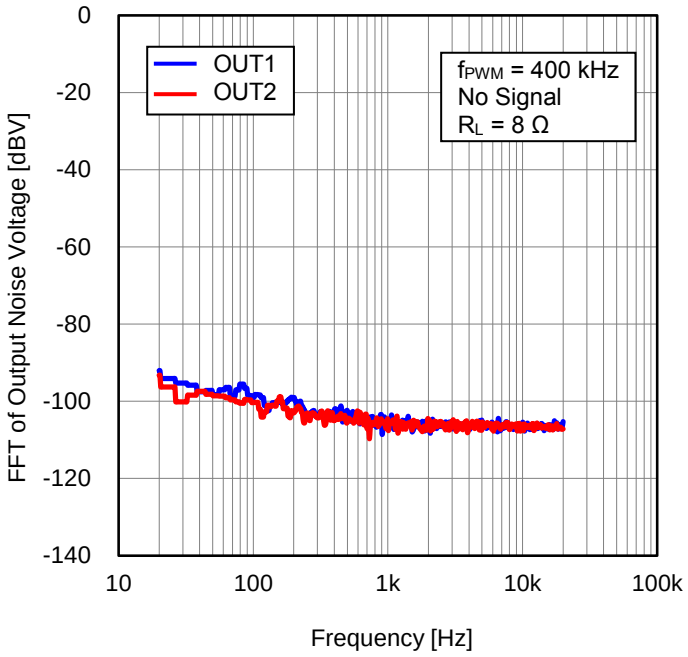


Figure 32. FFT of Output Noise Voltage vs Frequency
(f_{PWM} = 400 kHz, R_L = 8 Ω)

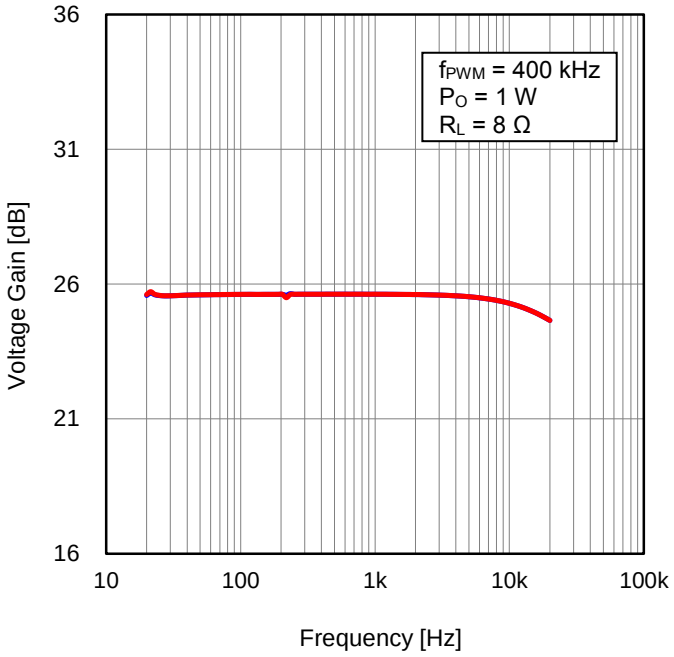


Figure 33. Voltage Gain vs Frequency
(f_{PWM} = 400 kHz, R_L = 8 Ω)

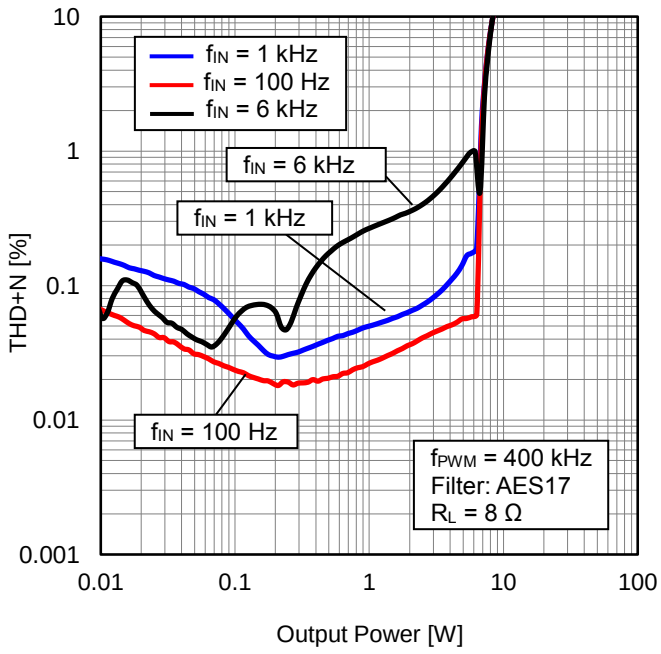


Figure 34. THD+N vs Output Power
(f_{PWM} = 400 kHz, R_L = 8 Ω)

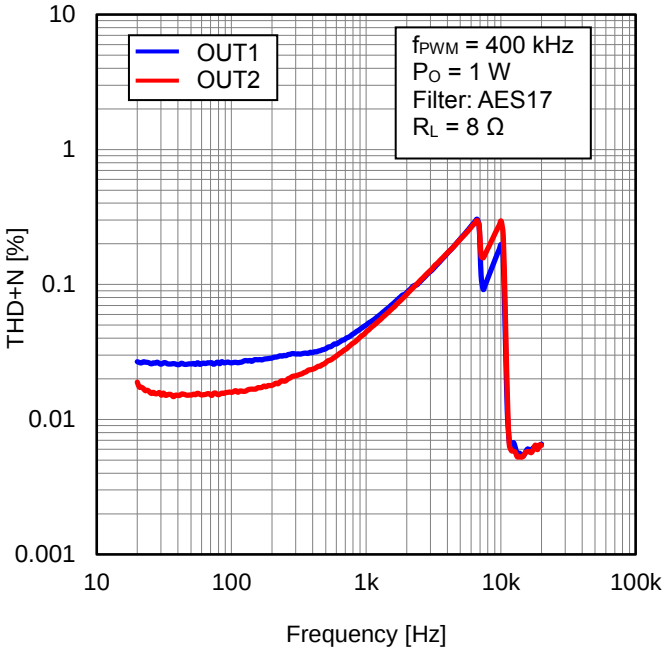


Figure 35. THD+N vs Frequency
(f_{PWM} = 400 kHz, R_L = 8 Ω)

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 11 V, f_{IN} = 1 kHz, PDX = 3.3 V, MUTEX = 3.3 V, PLIMT = 0 V, Gain = 26 dB, Output LC filter: L = 15 µH, C = 1 µF
when V_{CC} > 11 V, snubber circuit is added: C = 680 pF, R = 5.6 Ω)

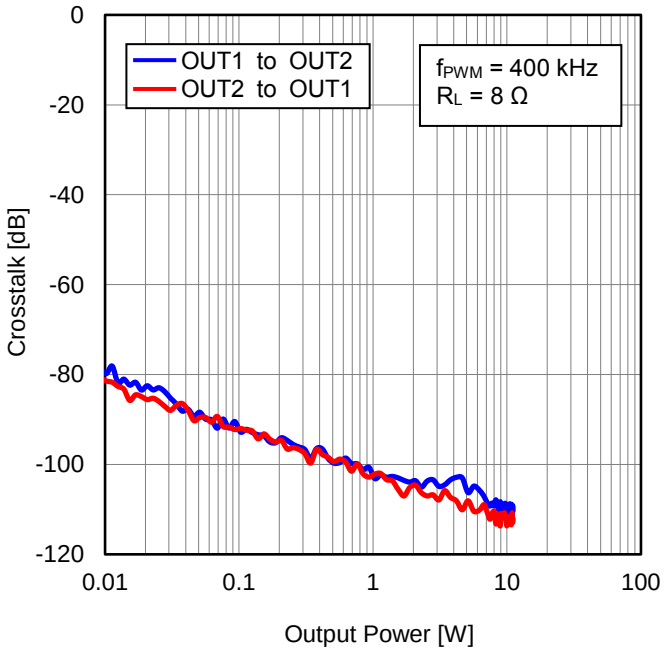


Figure 36. Crosstalk vs Output Power
(f_{PWM} = 400 kHz, R_L = 8 Ω)

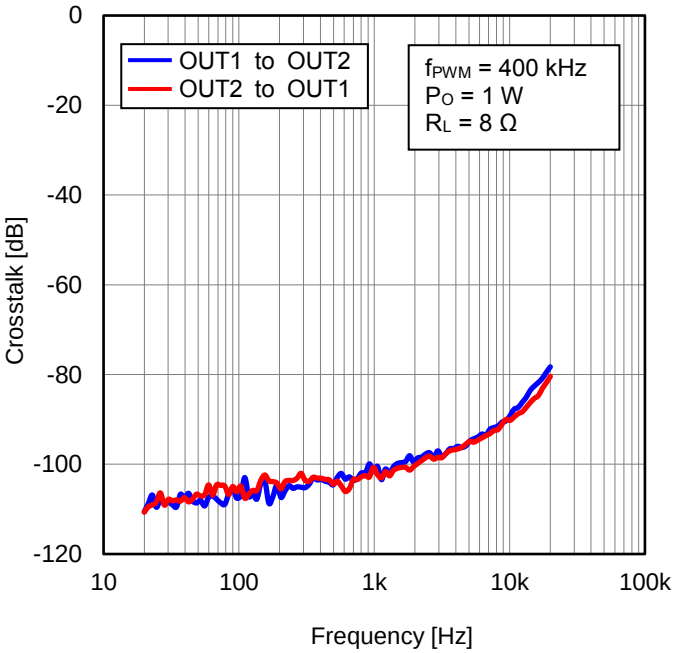


Figure 37. Crosstalk vs Frequency
(f_{PWM} = 400 kHz, R_L = 8 Ω)

Timing Chart

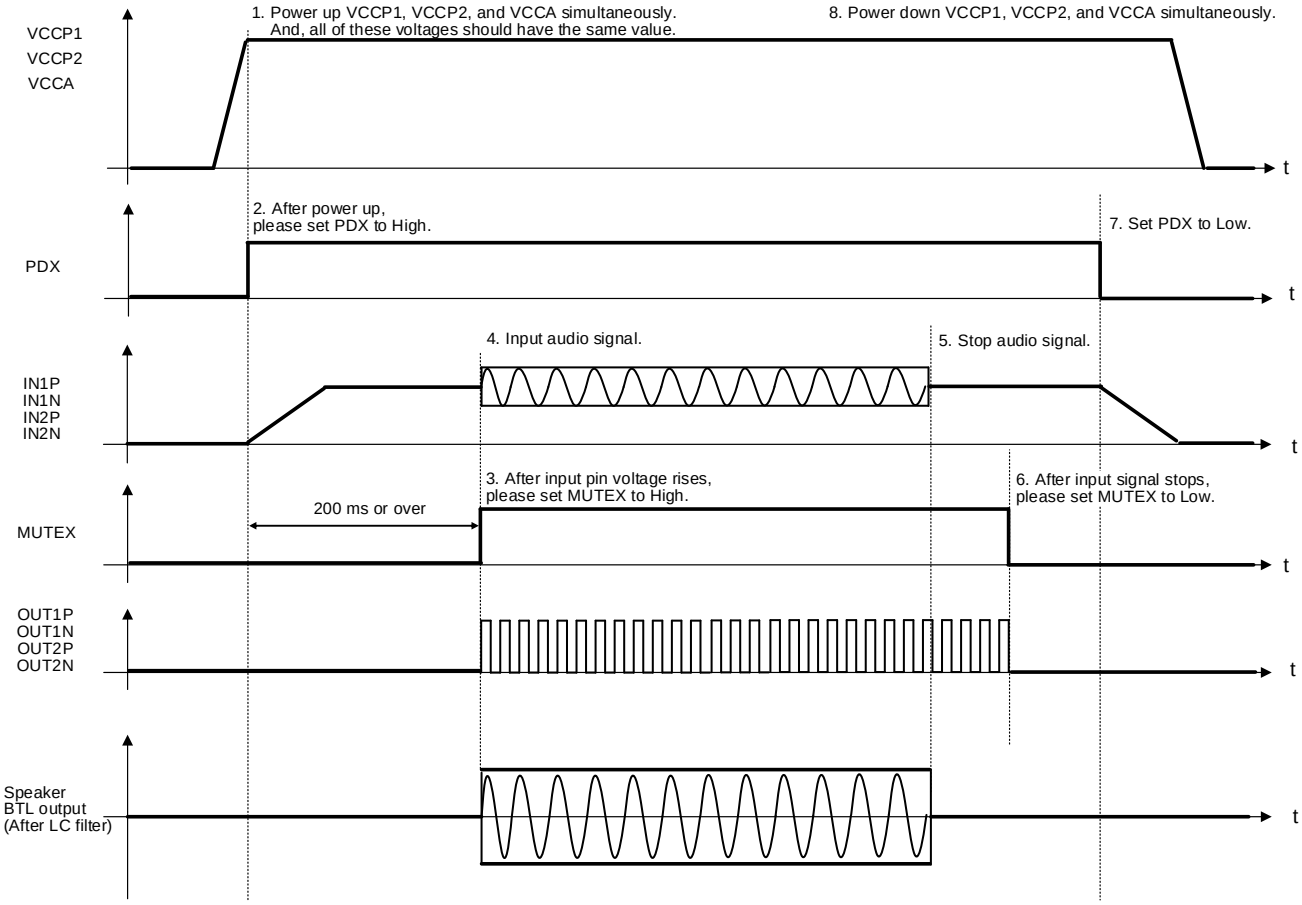


Figure 38. Power Up/Down Sequence

Function Descriptions

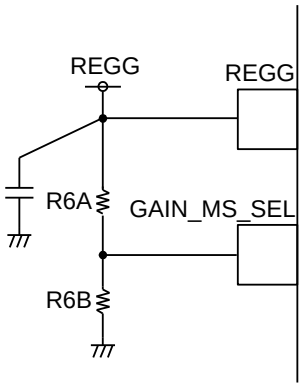
1 The Setting of Power Down and Mute

Pin Setting		Normal		ERROR Detection	
PDX	MUTEX	PWM output OUT1P, 1N, 2P, 2N	ERRORX Output(Note 15)	PWM output OUT1P, 1N, 2P, 2N	ERRORX Output(Note 15)
Low	Low/ High	High-Z_Low(Note 14) (Standby)	High	High-Z_Low(Note 14) (Standby)	High
High	Low	High-Z_Low(Note 14) (MUTE_ON)	High	High-Z_Low(Note 14) (MUTE_ON)	Low
High	High	Active (MUTE_OFF)	High	High-Z_Low(Note 14) (MUTE_ON)	Low

(Note 14) All power transistors are OFF and output pins are pulled down by 40 kΩ (Typ).
(Note 15) ERRORX is pulled up by 10 kΩ resistor.

2 Gain and Master/Slave Setting

Master/slave and gain are set by GAIN_MS_SEL voltage.



R6A(Note 16) (to REGG) [kΩ]	R6B(Note 16) (to ground) [kΩ]	Master/Slave	Gain [dB]	Input Impedance (IN1P,IN1N,IN2P,IN2N) [kΩ]
18	Open	Slave	36	30.0 (Typ)
18	68	Slave	32	45.1 (Typ)
33	68	Slave	26	79.3 (Typ)
51	68	Slave	20	127.9 (Typ)
68	51	Master	36	30.0 (Typ)
68	33	Master	32	45.1 (Typ)
68	18	Master	26	79.3 (Typ)
open	18	Master	20	127.9 (Typ)

(Note 16) Please use 1 % tolerance resistor.

Figure 39. GAIN_MS_SEL Setting

Setting cannot be changed when LSI is active, but it can be set by rebooting (PDX = High to Low to High).

Master/Slave Function

This LSI has master and slave mode, and PWM frequency of two LSIs can be synchronized. In case the LSI is master mode, SYNC becomes signal output pin for synchronization and in case the LSI is slave mode, it becomes signal input pin for synchronization. So, in case PWM frequency of two LSIs need to be synchronized, be sure to connect the SYNC pins each other. Also setting of the FSEL2, FSEL1 and FSEL0 pins of 2 LSIs must be the same.

3 Parallel BTL Function

Parallel BTL mode can be set by connecting IN2P and IN2N to ground.
Please short OUT1P to OUT2P and OUT1N to OUT2N at near the LSI as much as possible.
Do not connect IN1P and IN1N to ground.

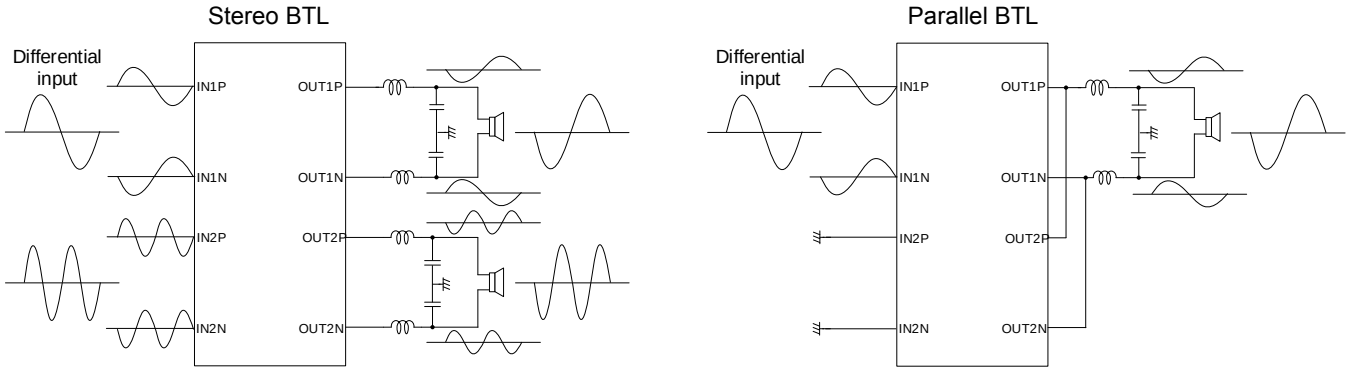


Figure 40. Parallel BTL Mode

Function Descriptions – continued

4 Power Limit Function

It is possible to limit the maximum output voltage for protection of speaker.

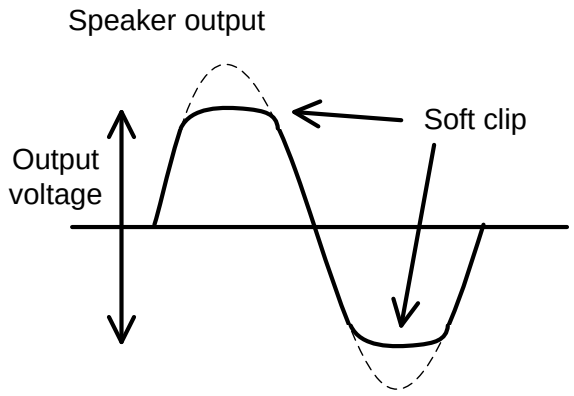


Figure 41. Power Limit Waveform

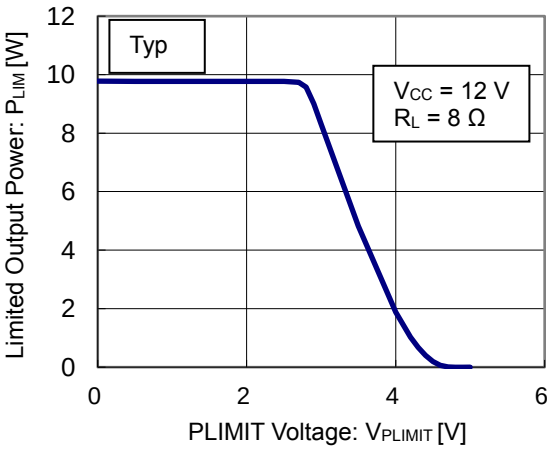


Figure 42. Power Limit

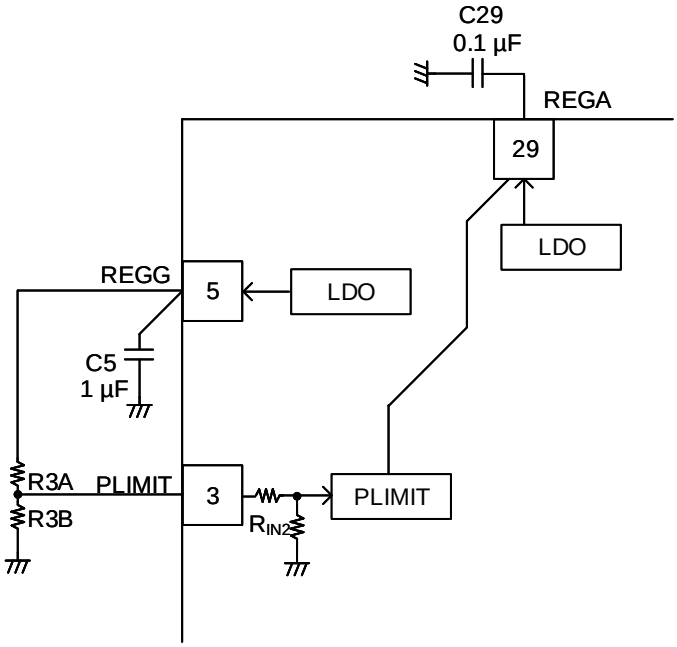


Figure 43. PLIMIT Setting

When the DC voltage is applied to PLIMIT, an output wave is clipped (Figure 41), and output power is limited.
The relation between the voltage of PLIMIT (V_{PLIMIT}) and limited output power P_{LIM} is shown in Figure 42.
It is possible that the voltage V_{PLIMIT} is set by connecting external resistance R3A and R3B (Figure 43).
The examples of setting R3A and R3B is shown in the table below. In case the power limit function is not used, connect PLIMIT to ground.

R3A [kΩ]	R3B [kΩ]	Max output power P_{LIM} [W] (R_L = 8 Ω)		
		Min	Typ	Max
Open	Short to ground	-	(unlimited)	-
12	20	3.4	6.8	13.6
10	20	2.5	5.0	10.0
8.2	20	1.7	3.4	6.8

Function Descriptions – continued

In case the power limit function is used under the setting except the table, P_{LIM} is

$$P_{LIM} = \frac{(V_{REGA} - V_{PLIMIT})^2 \times 39.8}{2R_L} \text{ [W]}$$

$$V_{PLIMIT} = \frac{1}{R_{3A}(\frac{1}{R_{3A}} + \frac{1}{R_{3B}} + \frac{1}{R_{IN2}})} V_{REGG} \text{ [V]}$$

Where:
V_{REGA} is the voltage of REGA, 5.0 V (Typ)
V_{REGG} is the voltage of REGG, 5.55 V (Typ)
R_{IN2} is pull-down resistance of PLIMIT, 200 kΩ (Typ)

Set the R3A and R3B to become the limited power.

5 FSEL2, FSEL1 and FSEL0 Setting (AM Avoidance Function)

The FSEL2, FSEL1 and FSEL0 pins are used for PWM frequency setting. They can change the PWM frequency like below.

FSEL2	FSEL1	FSEL0	PWM Frequency [kHz]
High	High	High	1200 (Typ)
High	High	Low	1000 (Typ)
High	Low	High	600 (Typ)
High	Low	Low	500 (Typ)
Low	High	High	400 (Typ)

Do not set following conditions to become un-recommended frequency:
FSEL2 = Low, FSEL1 = High, FSEL0 = Low
FSEL2 = Low, FSEL1 = Low, FSEL0 = High
FSEL2 = FSEL1 = FSEL0 = Low

6 AM Avoidance Function

PWM frequency is near to AM radio frequency band when this makes interference during AM radio is used, and may negatively affects reception of AM radio wave. This interference can be reduced by adjusting PWM frequency. Below are the recommended settings. For example, when receiving AM radio wave of 1269 kHz in Asia/Europe, PWM frequency must be set to 500 kHz.

AM Frequency [kHz]		Recommended PWM Frequency Setting				
Americas	Asia/ Europe	f_{PWM} = 400 kHz FSEL2 = Low FSEL1 = High FSEL0 = High	f_{PWM} = 500 kHz FSEL2 = High FSEL1 = Low FSEL0 = Low	f_{PWM} = 600 kHz FSEL2 = High FSEL1 = Low FSEL0 = High	f_{PWM} = 1000 kHz FSEL2 = High FSEL1 = High FSEL0 = Low	f_{PWM} = 1200 kHz FSEL2 = High FSEL1 = High FSEL0 = High
	522 to 540	○	-	○	○	○
540 to 917	540 to 914	-	○	-	○	○
917 to 1125	914 to 1122	○	-	○	-	○
1125 to 1375	1122 to 1373	-	○	-	○	-
1375 to 1547	1373 to 1548	○	-	○	○	○
1547 to 1700	1548 to 1701	○	-	○	○	○

Application Examples

1 Application Circuit Example 1 (Stereo BTL, V_{CC} = 4.5 V to 11 V)

Overshoot of PWM output occurs depending on the board layout. Be sure to confirm that the voltage of the output pins are lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added. The example of snubber circuit is shown in the next page.

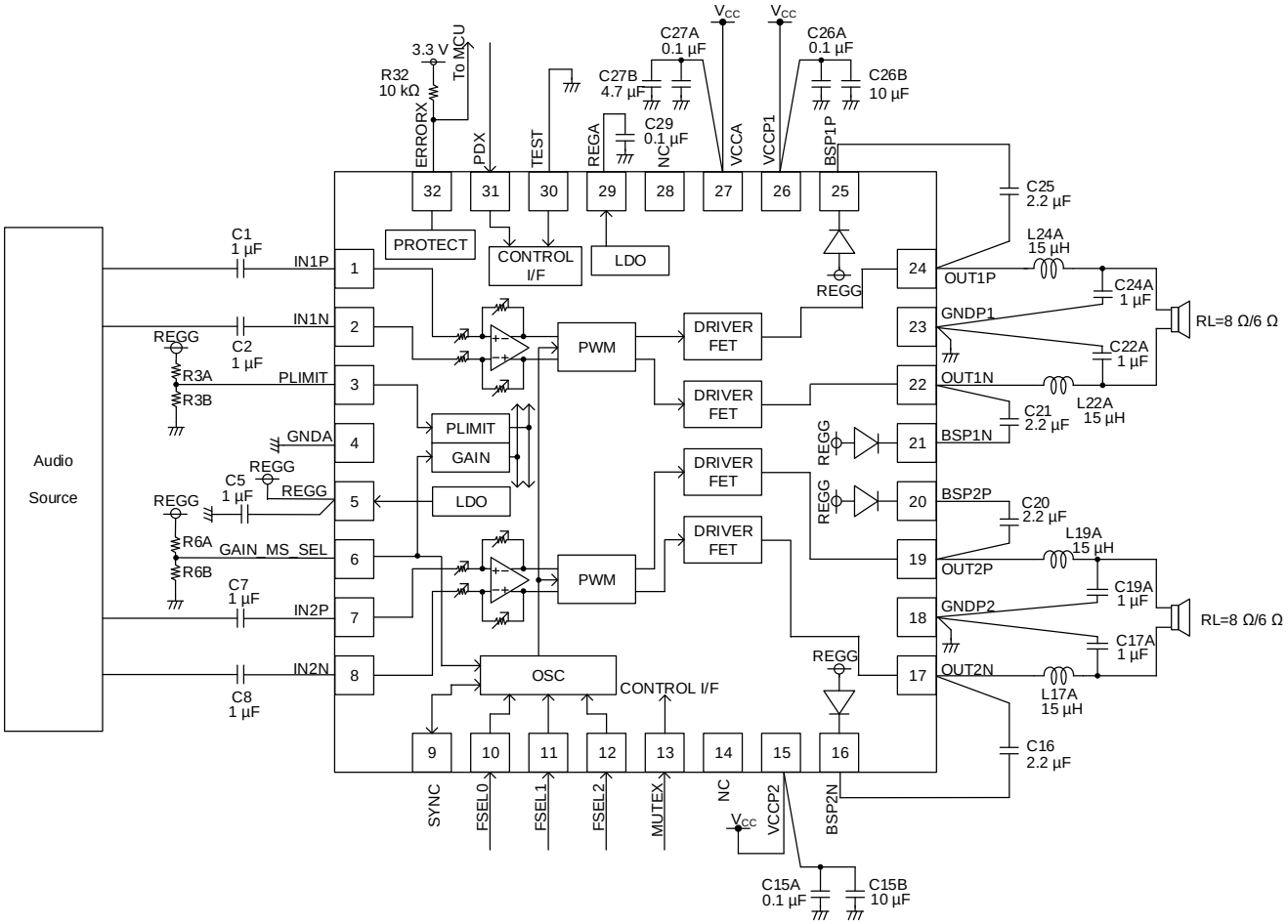


Figure 44. Application Circuit 1

BOM 1 (Stereo BTL, V_{CC} = 4.5 V to 11 V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description 4 Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description 2 Gain and Master/Slave Setting
	1	R6B	
	1	R32	10 kΩ, 1/16 W, J (±5 %)
Capacitor	4	C1, C2, C7, C8	1 µF, 16 V, B (±10 %)
	1	C5*(Note 17)*	1 µF, 16 V, B (±10 %)
	3	C15A, C26A, C27A*(Note 17)*	0.1 µF, 25 V, B (±10 %)
	2	C15B, C26B*(Note 17)*	10 µF, 25 V, B (±10 %)
	4	C16, C20, C21, C25*(Note 17)*	2.2 µF, 16 V, B (±10 %)
	4	C17A, C19A, C22A, C24A	1 µF, 25 V, B (±10 %)
	1	C27B*(Note 17)*	4.7 µF, 25 V, B (±10 %)
	1	C29*(Note 17)*	0.1 µF, 16 V, B (±10 %)
Inductor	4	L17A, L19A, L22A, L24A	15 µH, 2.1 A, ±20 %

(Note 17) Please place it near pin as much as possible. Also, please mount C15 and C26 as close as possible to the V_{CC}/ground pin on the same side as the LSI mounted side. Even if V_{CC}/ground wiring is shorted on the board, either C15 or C26 cannot be removed.

Application Examples – continued

2 Application Circuit Example 2 (Stereo BTL, V_{CC} = 11 V to 13 V)

Please add the snubber circuit at the output pins as shown below when V_{CC} = 11 V to 13 V.

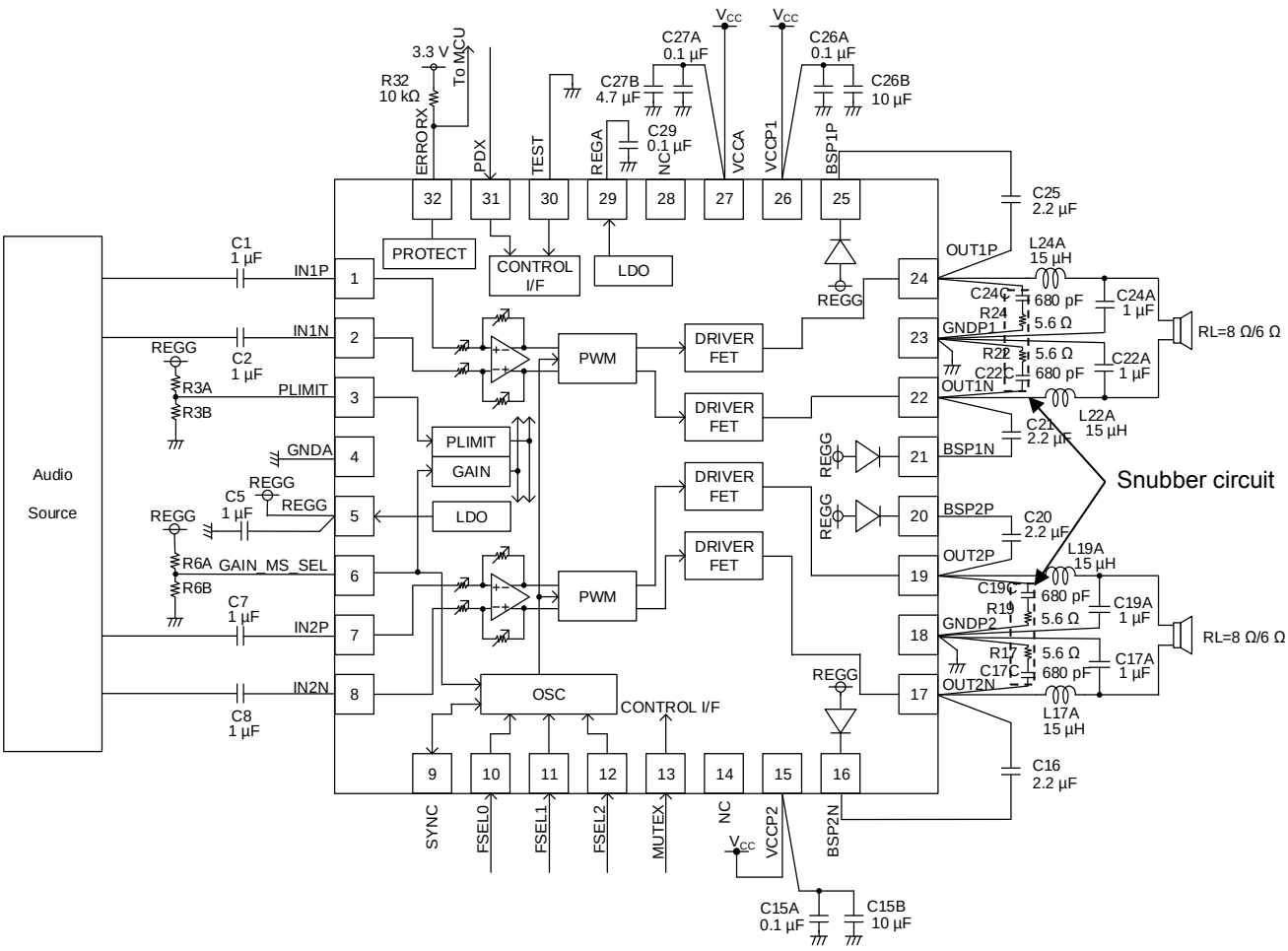


Figure 45. Application Circuit 2

BOM 2 (Stereo BTL, V_{CC} = 11 V to 13 V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description 4 Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description 2 Gain and Master/Slave Setting
	1	R6B	
	1	R32	10 kΩ, 1/16 W, J (±5 %)
	4	R17, R19, R22, R24 *(Note 18)*	5.6 Ω, 1/10 W, J (±5 %)
Capacitor	4	C1, C2, C7, C8	1 µF, 16 V, B (±10 %)
	1	C5 *(Note 18)*	1 µF, 16 V, B (±10 %)
	3	C15A, C26A, C27A *(Note 18)*	0.1 µF, 25 V, B (±10 %)
	2	C15B, C26B *(Note 18)*	10 µF, 25 V, B (±10 %)
	4	C16, C20, C21, C25 *(Note 18)*	2.2 µF, 16 V, B (±10 %)
	4	C17A, C19A, C22A, C24A	1 µF, 25 V, B (±10 %)
	4	C17C, C19C, C22C, C24C *(Note 18)*	680 pF, 25 V, B (±10 %)
	1	C27B *(Note 18)*	4.7 µF, 25 V, B (±10 %)
	1	C29 *(Note 18)*	0.1 µF, 16 V, B (±10 %)
Inductor	4	L17A, L19A, L22A, L24A	15 µH, 2.1 A, ±20 %

(Note 18) Please place it near pin as much as possible. Also, please mount C15 and C26 as close as possible to the V_{CC}/ground pin on the same side as the LSI mounted side. Even if V_{CC}/ground wiring is shorted on the board, either C15 or C26 cannot be removed.

Application Examples – continued

3 Application Circuit Example 3 (Monaural PBTL, V_{CC} = 4.5 V to 11 V)

Overshoot of PWM output occurs depending on the board layout. Be sure to confirm that the voltage of the output pins are lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added. The example of snubber circuit is shown in the next page.

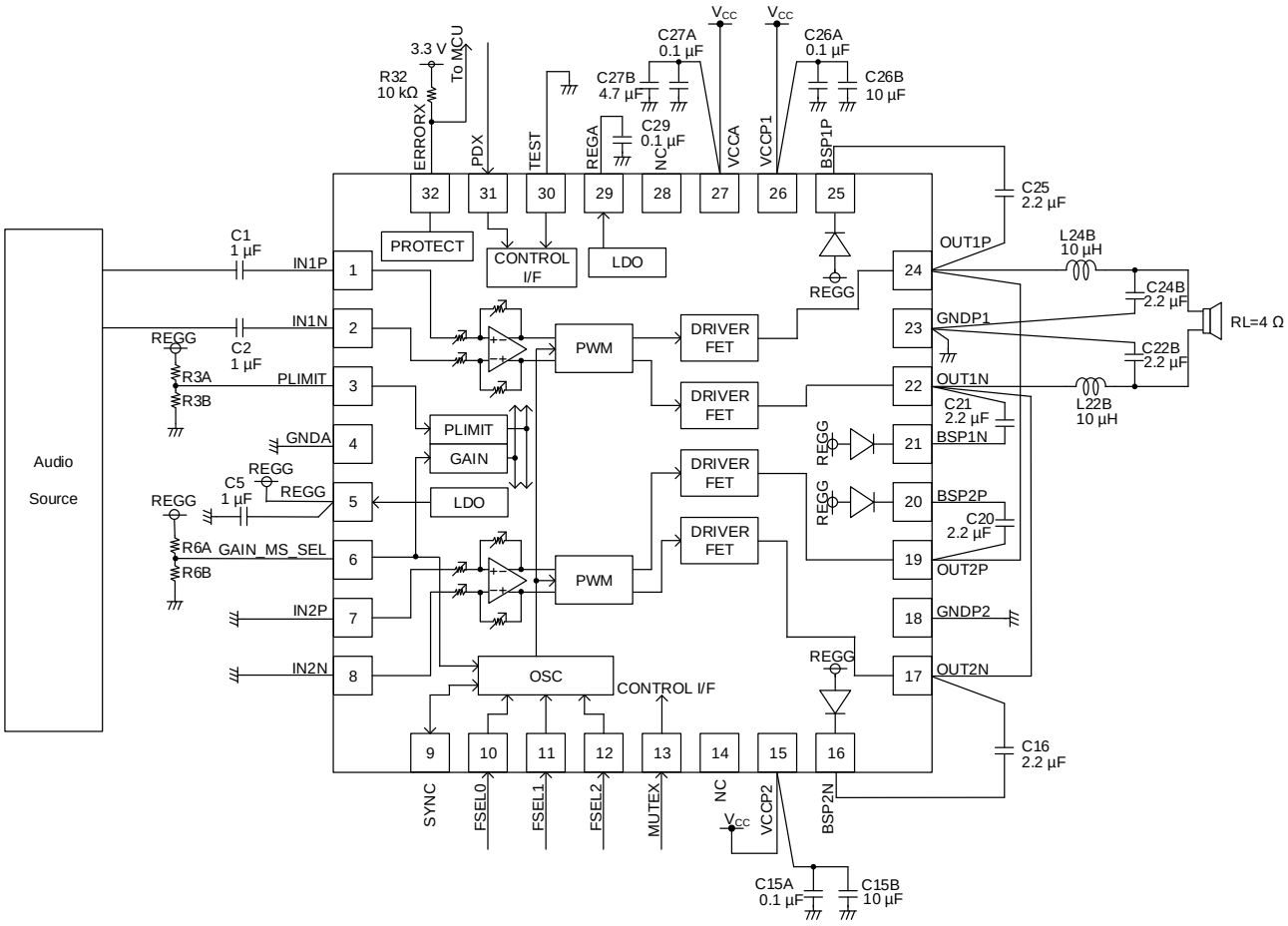


Figure 46. Application Circuit 3

BOM 3 (Monaural PBTL, V_{CC} = 4.5 V to 11 V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description 4 Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description 2 Gain and Master/Slave Setting
	1	R6B	
	1	R32	10 kΩ, 1/16 W, J (±5 %)
Capacitor	2	C1, C2	1 µF, 16 V, B (±10 %)
	1	C5*(Note 19)*	1 µF, 16 V, B (±10 %)
	3	C15A, C26A, C27A*(Note 19)*	0.1 µF, 25 V, B (±10 %)
	2	C15B, C26B*(Note 19)*	10 µF, 25 V, B (±10 %)
	4	C16, C20, C21, C25	2.2 µF, 16 V, B (±10 %)
	2	C22B, C24B*(Note 19)*	2.2 µF, 25 V, B (±10 %)
	1	C27B	4.7 µF, 25 V, B (±10 %)
	1	C29*(Note 19)*	0.1 µF, 16 V, B (±10 %)
Inductor	2	L22B, L24B	10 µH, 2.6 A, ±20 %

(Note 19) Please place it near pin as much as possible. Also, please mount C15 and C26 as close as possible to the V_{CC}/ground pin on the same side as the LSI mounted side. Even if V_{CC}/ground wiring is shorted on the board, either C15 or C26 cannot be removed.

Application Examples – continued

4 Application Circuit Example 4 (Monaural PBTL, V_{CC} = 11 V to 13 V)
Please add the snubber circuit at the output pins as shown below when V_{CC} = 11 V to 13 V.

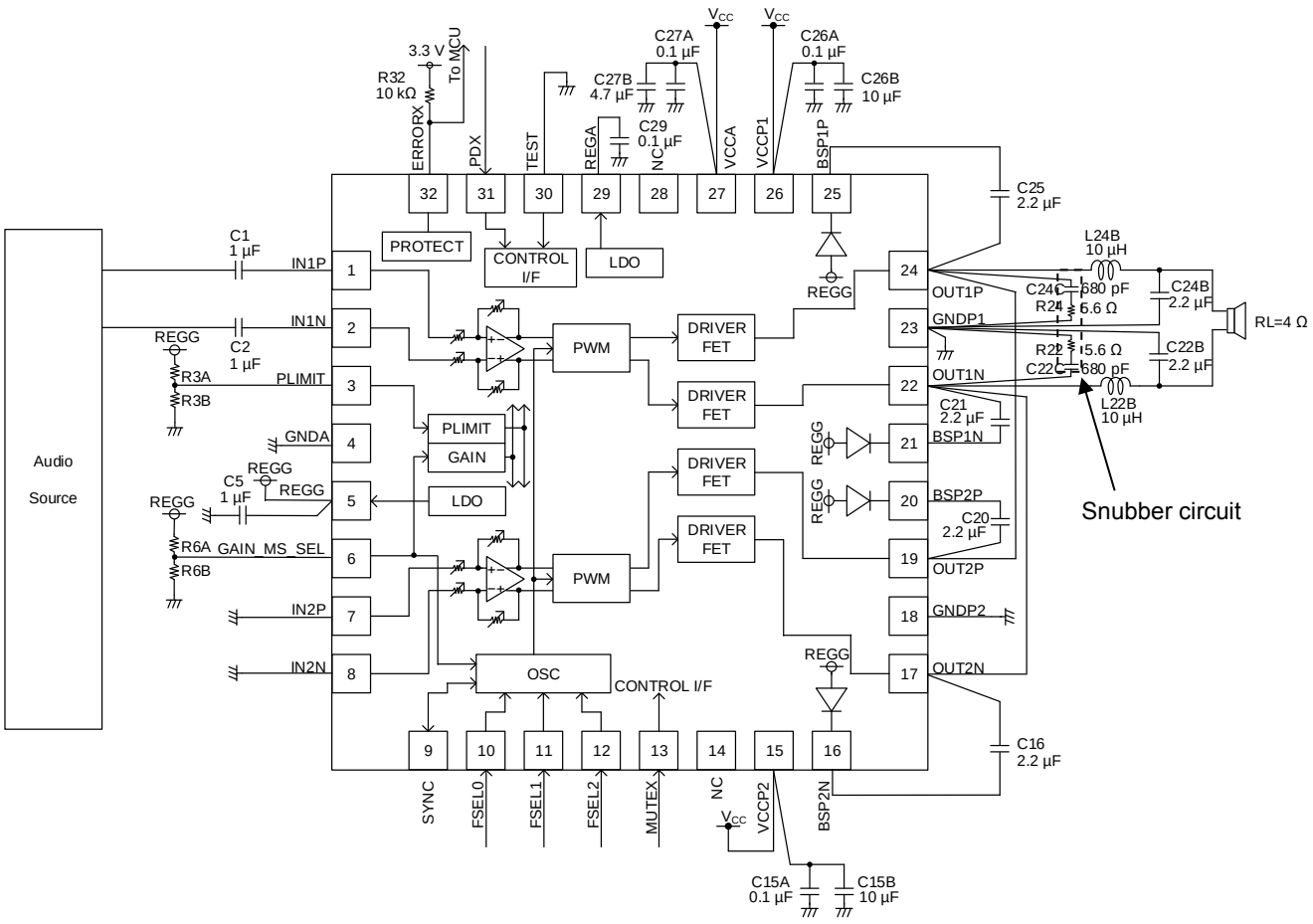


Figure 47. Application Circuit 4

BOM 4 (Monaural PBTL, V_{CC} = 11 V to 13 V)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description 4 Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description 2 Gain and Master/Slave Setting
	1	R6B	
	1	R32	10 kΩ, 1/16 W, J (±5 %)
	2	R22, R24*(Note 20)*	5.6 Ω, 1/10 W, J (±5 %)
Capacitor	2	C1, C2	1 µF, 16 V, B (±10 %)
	1	C5*(Note 20)*	1 µF, 16 V, B (±10 %)
	3	C15A, C26A, C27A*(Note 20)*	0.1 µF, 25 V, B (±10 %)
	2	C15B, C26B*(Note 20)*	10 µF, 25 V, B (±10 %)
	4	C16, C20, C21, C25*(Note 20)*	2.2 µF, 16 V, B (±10 %)
	2	C22B, C24B	2.2 µF, 25 V, B (±10 %)
	2	C22C, C24C*(Note 20)*	680 pF, 25 V, B (±10 %)
	1	C27B*(Note 20)*	4.7 µF, 25 V, B (±10 %)
	1	C29*(Note 20)*	0.1 µF, 16 V, B (±10 %)
Inductor	2	L22B, L24B	10 µH, 2.6 A, ±20 %

(Note 20) Please place it near pin as much as possible. Also, please mount C15 and C26 as close as possible to the V_{CC}/ground pin on the same side as the LSI mounted side. Even if V_{CC}/ground wiring is shorted on the board, either C15 or C26 cannot be removed.

Application Examples – continued

5 Application Example 5 (MASTER/SLAVE mode, V_{CC} = 4.5 V to 11 V)

This GAIN_MS_SEL setting is one example.
So, another Gain setting can be used.

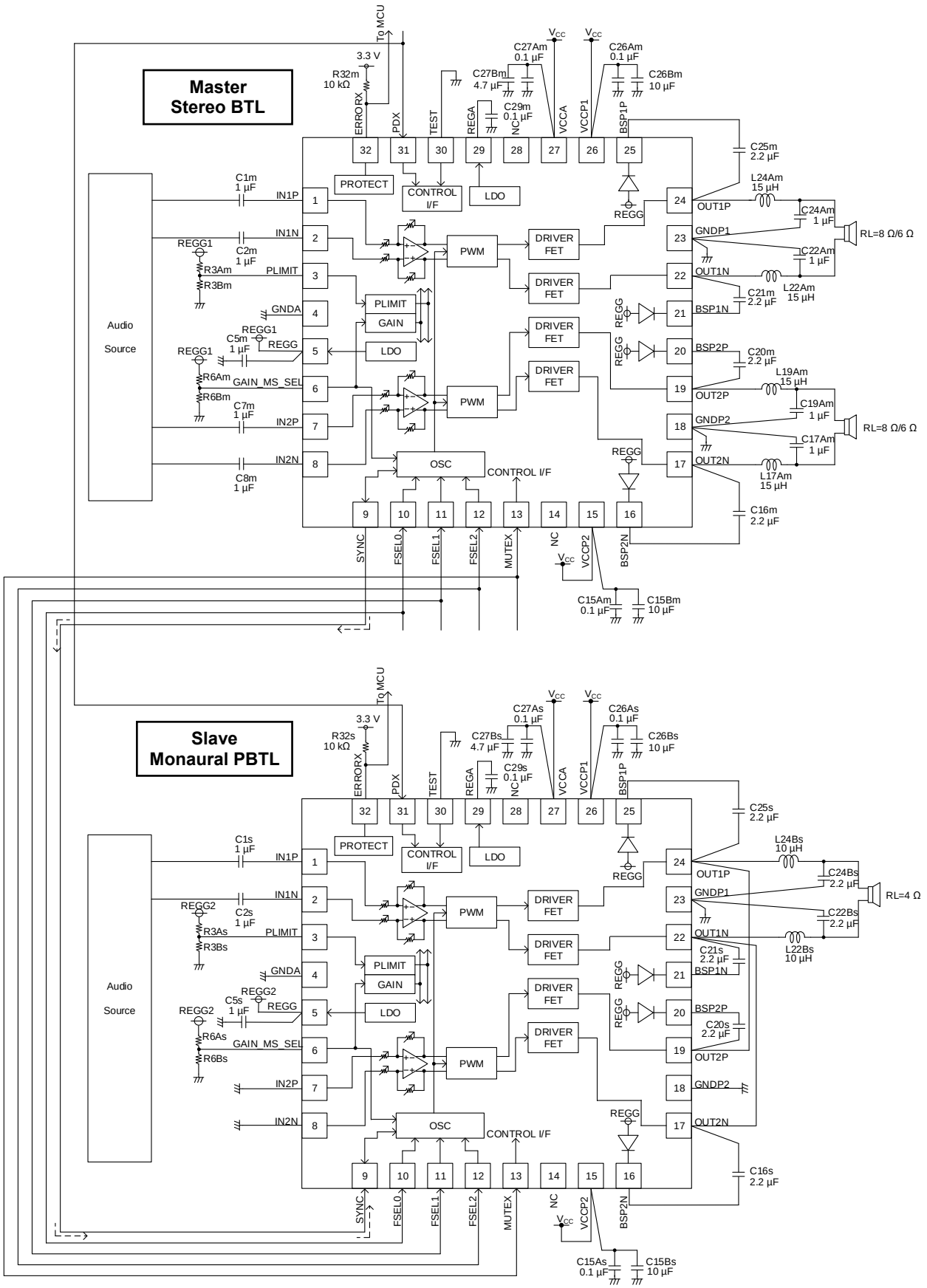


Figure 48. Application Circuit 5

About the Protection Function

Protection Function	Detecting & Releasing Condition		PWM Output OUT1P, 1N, 2P, 2N	ERRORX Output(Note 21)
Output Short Protection	Detecting Condition	Detecting Current = 8 A (Typ)	High-Z_Low (Latch)(Note 22)	Low (Latch)(Note 22)
DC Voltage Protection at Speaker	Detecting Condition	DC voltage is ±3.5 V (Typ) or more for a period of 0.33 s to 0.66 s (Typ).	High-Z_Low (Latch) (Note 22)	Low (Latch)(Note 22)
Overheat Protection	Detecting Condition	Chip temperature is 150 °C (Typ) or more.	High-Z_Low	Low
	Releasing Condition	Chip temperature is 120 °C (Typ) or less.	Active	
Under Voltage Protection	Detecting Condition	Power supply voltage is 4.0 V (Typ) or less.	High-Z_Low	High
	Releasing Condition	Power supply voltage is 4.1 V (Typ) or more.	Active	

(Note 21) ERRORX is pulled up by 10 kΩ resistor.

(Note 22) Once an LSI is latched, the circuit is not released automatically even after an abnormal status is gone.
The following procedures 1. or 2. is available for recovery.
1. After turning MUTEX pin to Low (holding time to Low = 10 ms (Min)), turn back to High again.
2. Restore power supply after dropping to power supply voltage V_{CC} < 3 V (10 ms (Min) holding) which internal power on reset circuit activates.

About the Protection Function – continued

1 Output Short Protection (Short to the Power Supply Protection)

This LSI has PWM output short protection circuit that stops the PWM output when the output speaker is short-circuited to the power supply (V_{CC}) unintentionally.

Detecting Condition - It will detect when MUTEX is set High and the current that flows into the PWM output pin becomes 8 A (Typ) or more for 250 ns (Typ). When the protection function starts, it stops the PWM output and latch output pins to High-Z_Low.

Releasing Method - Latch can be released by the next "1" or "2".
1. After turning the MUTEX pin to Low (holding time to Low = 10 ms (Min)), turn back to High again.
2. Restore power supply after the voltage dropped to internal power on reset circuit activating power supply voltage V_{CC} < 3 V (hold for 10 ms (Min)).

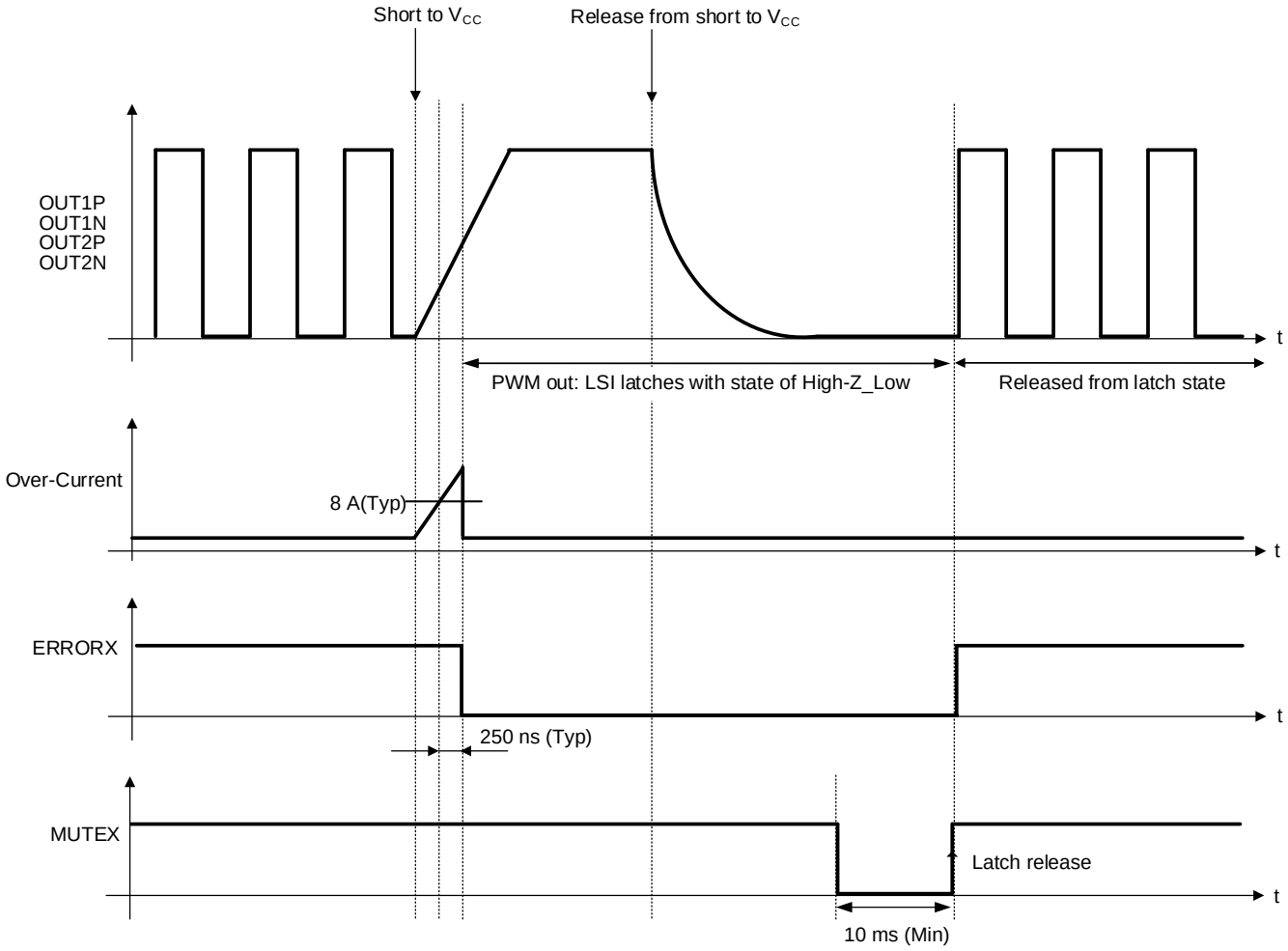


Figure 49. Output Short to the Power Supply Protection Sequence

About the Protection Function – continued

2 Output Short Protection (Short to ground)

This LSI has PWM output short protection circuit that stops the PWM output when the output speaker is short-circuited to ground unintentionally.

Detecting Condition - It will detect when MUTEX is set High and the current that flows into the PWM output pin becomes 8 A (Typ) or more for 250 ns (Typ). When the protection function starts, it stops the PWM output and latch output pins to High-Z_Low.

Releasing Method - Latch can be released by the next "1" or "2".

1. After turning the MUTEX pin to Low (holding time to Low = 10ms (Min)), turn back to High again.
2. Restore power supply after the voltage dropped to internal power on reset circuit activating power supply voltage V_{CC} < 3 V (hold for 10 ms (Min)).

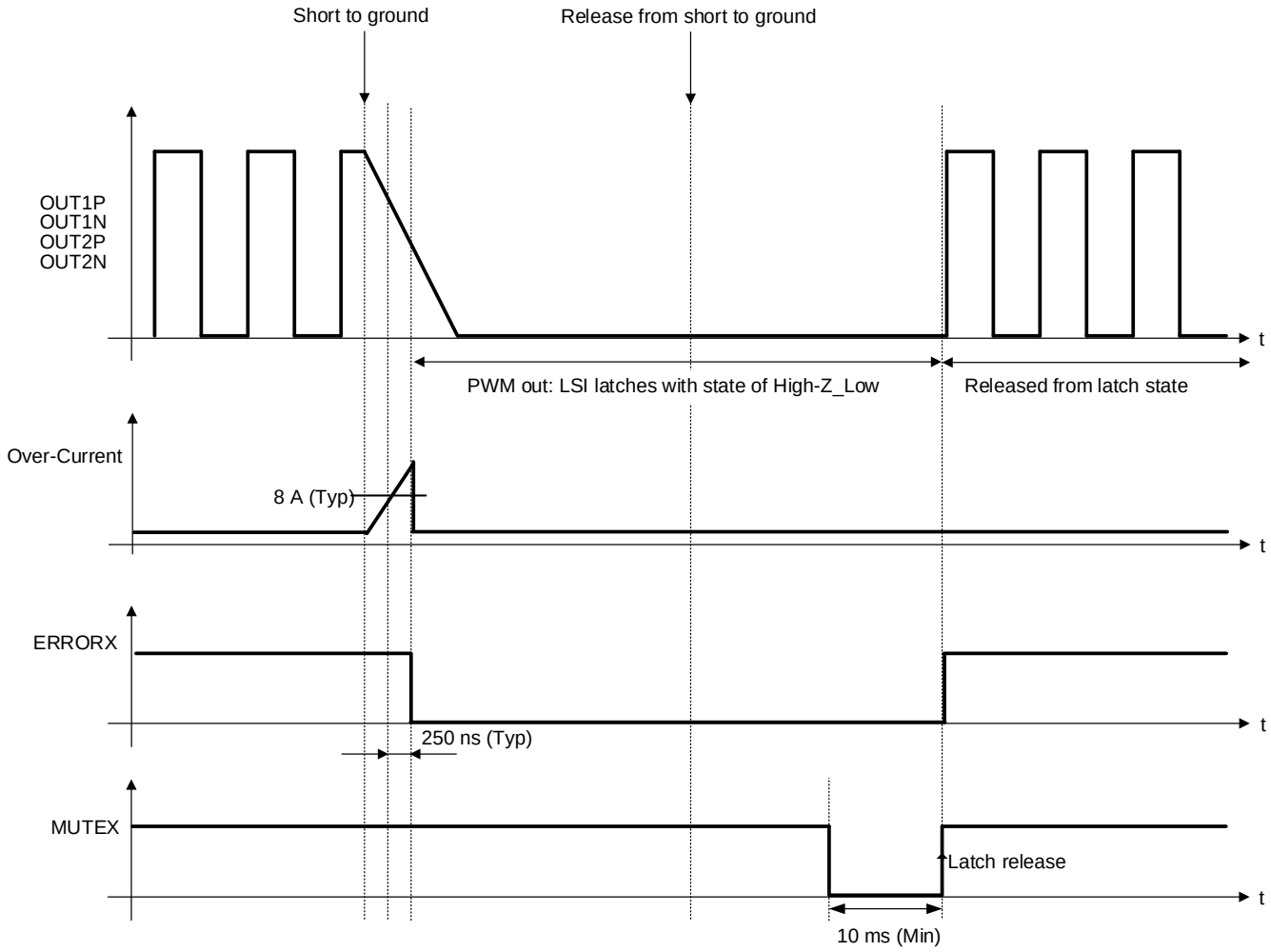


Figure 50. Output Short to GND Protection Sequence

About the Protection Function – continued

3 DC Voltage Protection at speaker

This LSI is integrated with DC voltage protection circuit. When DC voltage is applied to the speaker unintentionally, speaker output will mute, and this protection will prevent the speaker from destruction.

Detecting Condition - In case that the voltage of speaker output is ±3.5 V (Typ) or more in the time interval 0.33 s to 0.66 s (Typ) or more under the condition MUTEX is set to High the protection function starts. When the protection function starts, it stops the PWM output and latch output pins to High-Z_Low.

Releasing Method - Latch can be released by the next "1" or "2".

1. After turning the MUTEX pin to Low (holding time to Low = 10 ms (Min)), turn back to High again.
2. Restore power supply after the voltage dropped to internal power on reset circuit activating power supply voltage V_{CC} < 3 V (hold for 10 ms (Min)).

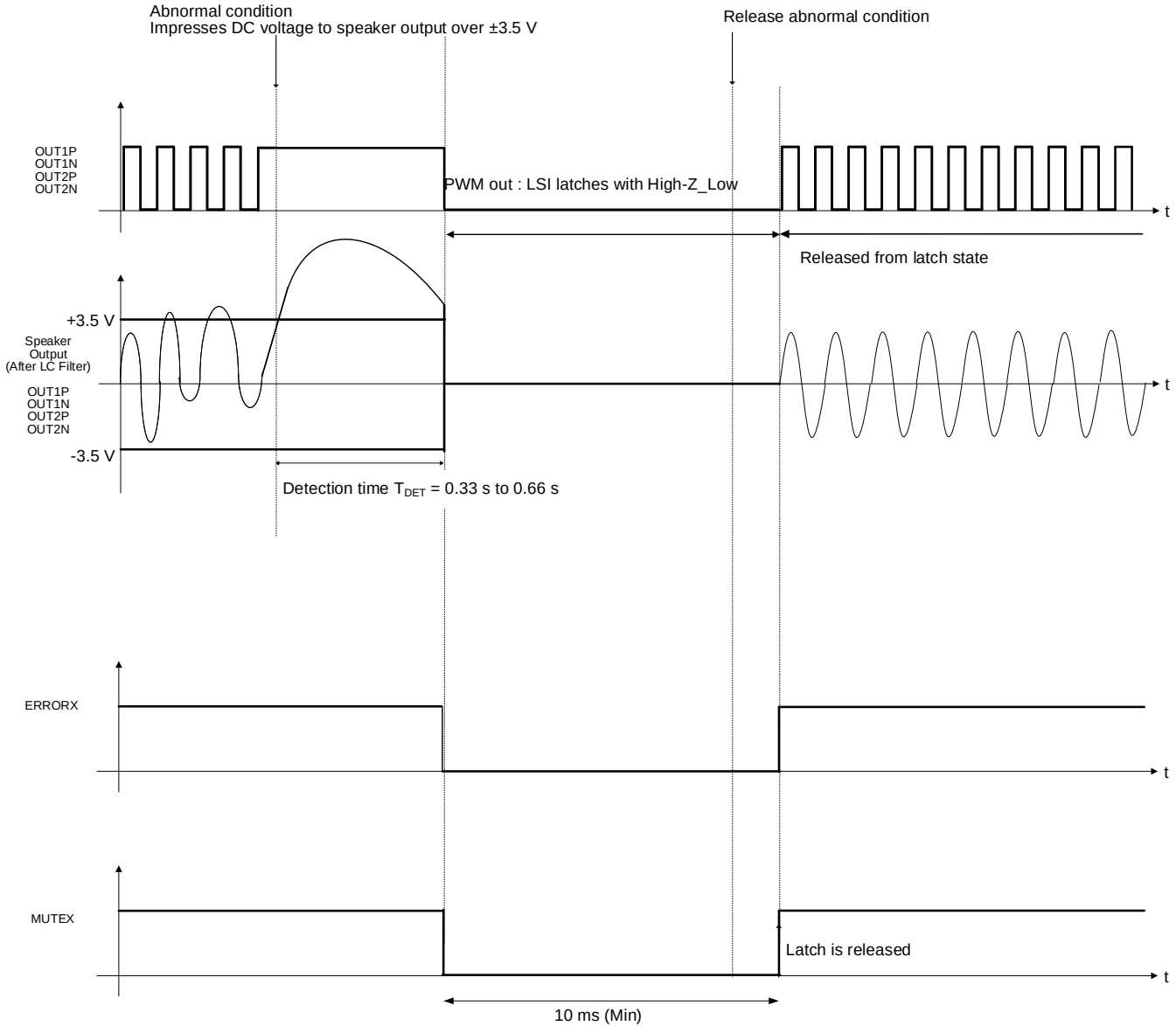


Figure 51. DC Voltage Protection at Speaker Sequence

About the Protection Function – continued

4 Overheat Protection

This LSI has overheat protection circuit that prevents thermal runaway under an abnormal state for the chip temperature exceeded Tjmax = 150 °C (Typ).

Detecting Condition - It will detect when MUTEX is set High and the temperature of the chip becomes 150 °C (Typ) or more. When the protection circuit is activated, the speaker output instantly goes to the state of High-Z_Low.

Releasing Condition - It will release when MUTEX is set High and the temperature of the chip becomes 120 °C (Typ) or less. The speaker output is back to its normal operation immediately when released. (Auto recovery)

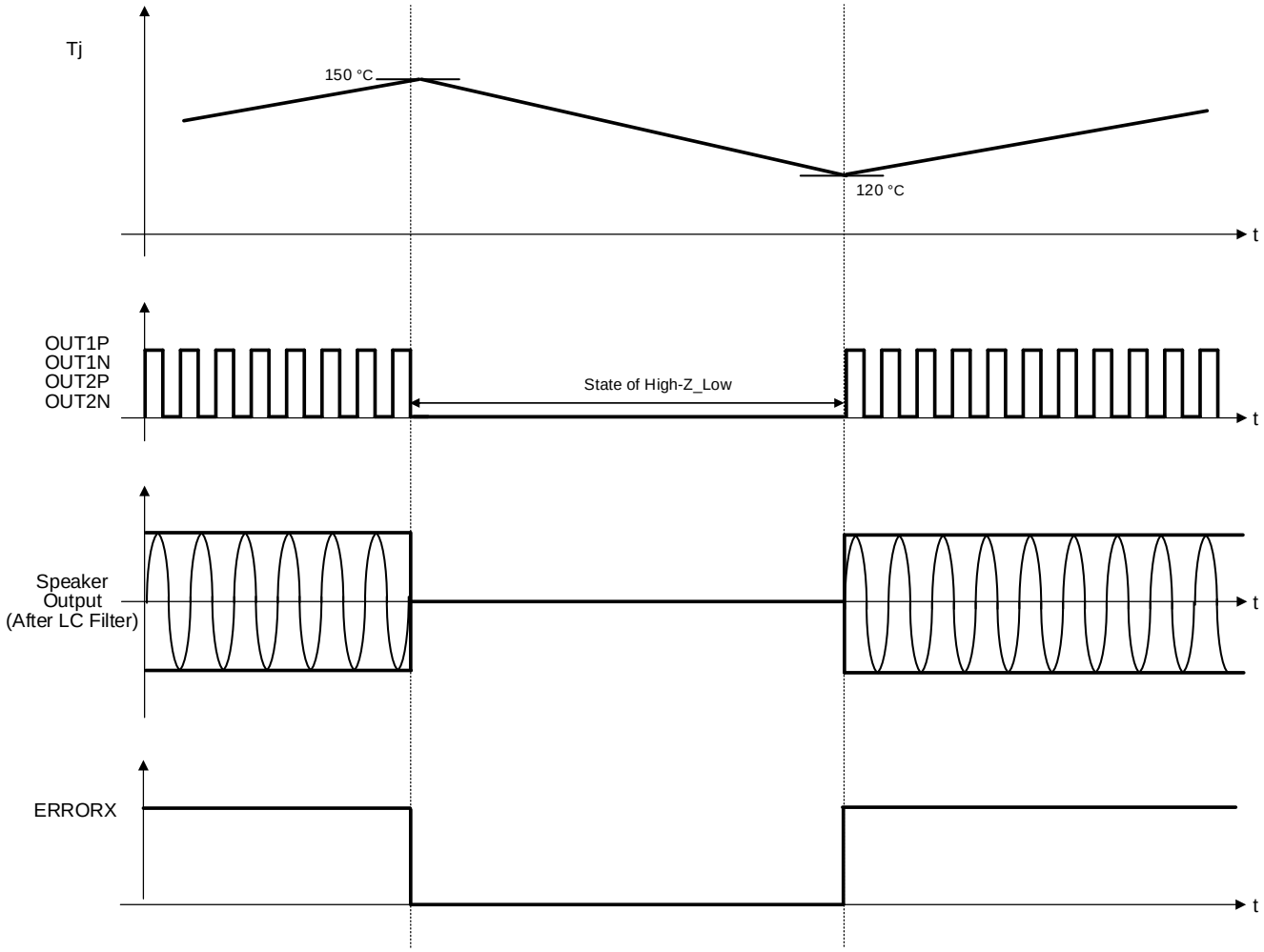


Figure 52. Overheat Protection Sequence

About the Protection Function – continued

5 Under Voltage Protection

This LSI has under voltage protection circuit that mutes the output speaker once extreme drop in the power supply voltage is detected.

Detecting Condition - It will detect when MUTEX is set High and the power supply voltage becomes 4 V or under f(Typ). When under voltage protection circuit is activated, the speaker output instantly goes to the state of High-Z_Low.

Releasing Condition - It will release when MUTEX is set High and the power supply voltage becomes 4.1 V or over (Typ). The speaker output is back to its normal operation immediately when released. (Auto recovery)

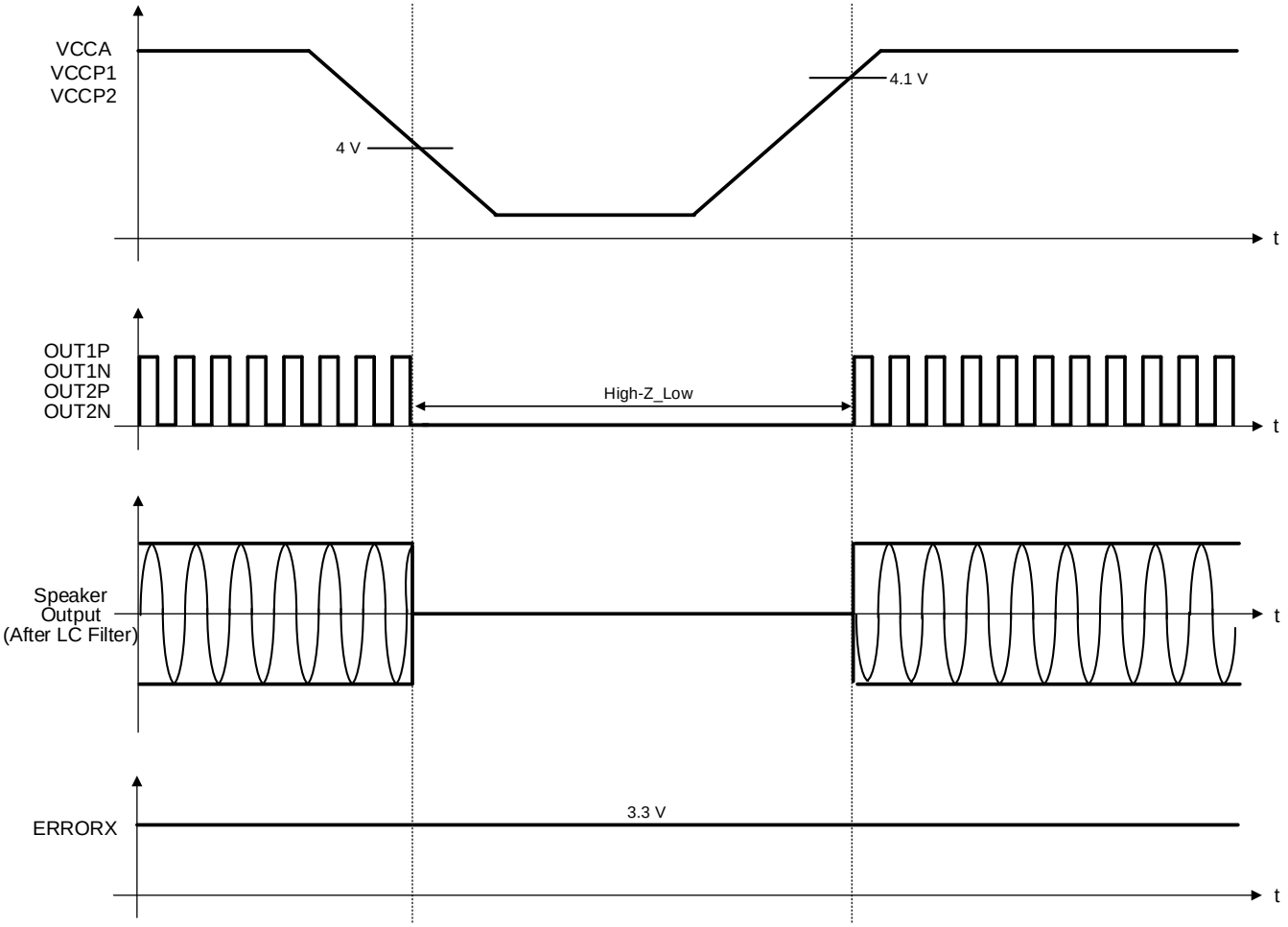


Figure 53. Under Voltage Protection Sequence

Selecting External Components

1 Output LC Filter Circuit

This LSI uses output PWM frequencies any of 400 kHz, 500 kHz, 600 kHz, 1000 kHz or 1200 kHz. Since the current necessary for driving the speaker is supplied through a speaker cable with a long wiring length, the PWM frequency and harmonic components are emitted as EMI noise. Therefore, LC filter is required to eliminate EMI noise.

This section takes an example of an LC type LPF shown below, in which coil L and capacitor C compose a differential filter with an attenuation property of -12 dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_L. This filter reduces unwanted emission this way.

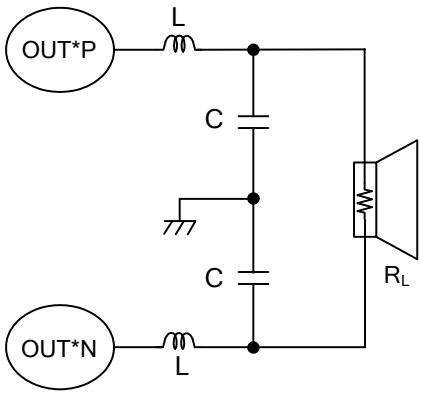


Figure 54. Output LC Filter

The following shows output LC filter constants and cutoff frequencies f_C with typical load impedances.

Stereo BTL

R_L	L	C	f_C
6 Ω, 8 Ω	15 µH	1 µF	41 kHz

Monaural PBTL

R_L	L	C	f_C
4 Ω	10 µH	2.2 µF	34 kHz

Use inductors with low ESR (equivalent series resistance) and with sufficient margin of allowable currents. Power loss will increase if inductors with high ESR are used.
Select a closed magnetic circuit type product in normal cases to prevent emission noise.
Use capacitors with low ESR, and good impedance characteristics at high frequency ranges (100 kHz or higher). Also, select an item with sufficient voltage rating because massive amount of high-frequency current flow is expected.

2 Snubber Circuit Constant

When overshoot/undershoot of PWM Output exceeds absolute maximum rating, or when overshoot/undershoot of PWM output negatively affects EMI noise, snubber circuit is used as shown below. And if V_{CC} > 11 V, the snubber circuit must be added.

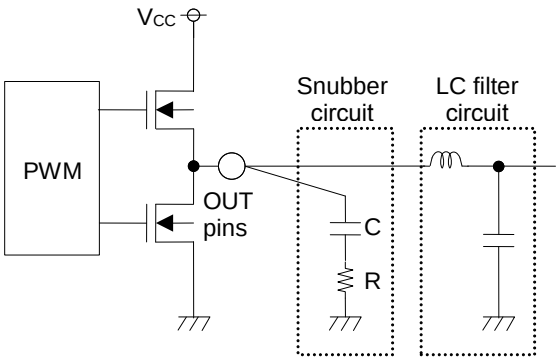


Figure 55. Snubber Circuit

The following table shows ROHM recommended value of "Snubber filter constants" when using ROHM board.

Stereo BTL

R_L	C	R
6 Ω	680 pF, 25 V B (±10 %)	5.6 Ω, 1/10 W J (±5 %)
8 Ω	680 pF, 25 V B (±10 %)	5.6 Ω, 1/10 W J (±5 %)

Monaural PBTL

R_L	C	R
4 Ω	680 pF, 25 V B (±10 %)	5.6 Ω, 1/10 W J (±5 %)

Caution 1: *If the impedance characteristics of the speakers at high-frequency range rise sharply, the LSI might not have stable operation in the resonance frequency range of the LC filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.*

Caution 2: *This LSI has a short protection function. In case that speaker output is shorted to V_{CC} or ground, over current occurs and short protection function starts. Be careful about that back electromotive force of the inductor in LC filter cause output over/undershoot, and the voltage of the output pins may exceed the maximum standard ratings, which leads to LSI destruction.*

Selecting External Components – continued

3 Operating condition with the application component

Parameter	Parts No.	Limit			Unit	Conditions
		Min	Typ	Max		
Tolerance of Capacitor for BSP	C16, C20, C21, C25	1.0*(Note 23)*	2.2	2.95*(Note 24)*	µF	B characteristics, Rated voltage 16 V or more, Ceramic type capacitor recommended

(Note 23) Set the capacitance not to be less than the minimum value in consideration of temperature characteristics and DC-bias properties.
(Note 24) It is the value in consideration of ±10 % tolerance of capacitance and 22 % capacitance change rate. Please use the capacitor within this rating.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the LSI. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the LSI's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the LSI are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the LSI, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the LSI has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the LSI on an application board, connecting a capacitor directly to a low-impedance output pin may subject the LSI to stress. Always discharge capacitors completely after each process or step. The LSI's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the LSI during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the LSI on the PCB. Incorrect mounting may result in damaging the LSI. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an LSI are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the LSI. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the LSI

This monolithic LSI contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When ground > Pin A and ground > Pin B, the P-N junction operates as a parasitic diode.
When ground > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the LSI. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the ground voltage to an input pin (and thus to the P substrate) should be avoided

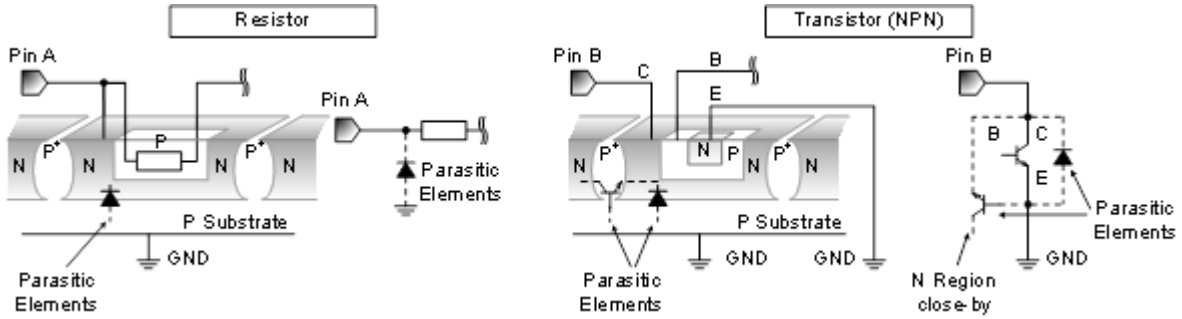


Figure 56. Example of monolithic LSI structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

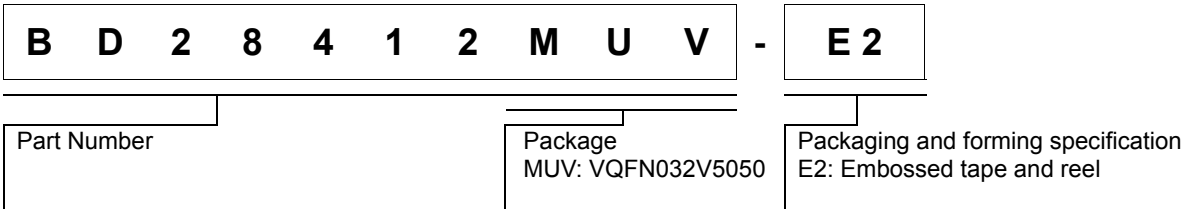
12. Thermal Shutdown Circuit(TSD)

This LSI has a built-in thermal shutdown circuit that prevents heat damage to the LSI. Normal operation should always be within the LSI's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the LSI from heat damage.

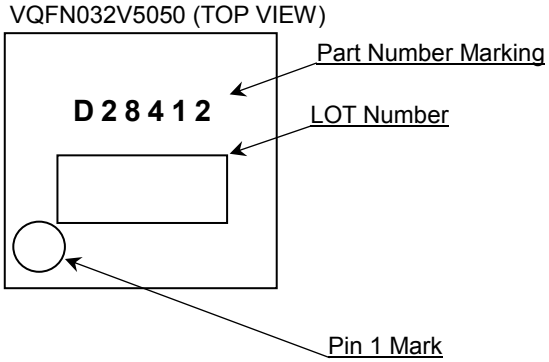
13. Over Current Protection Circuit (OCP)

This LSI incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the LSI should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

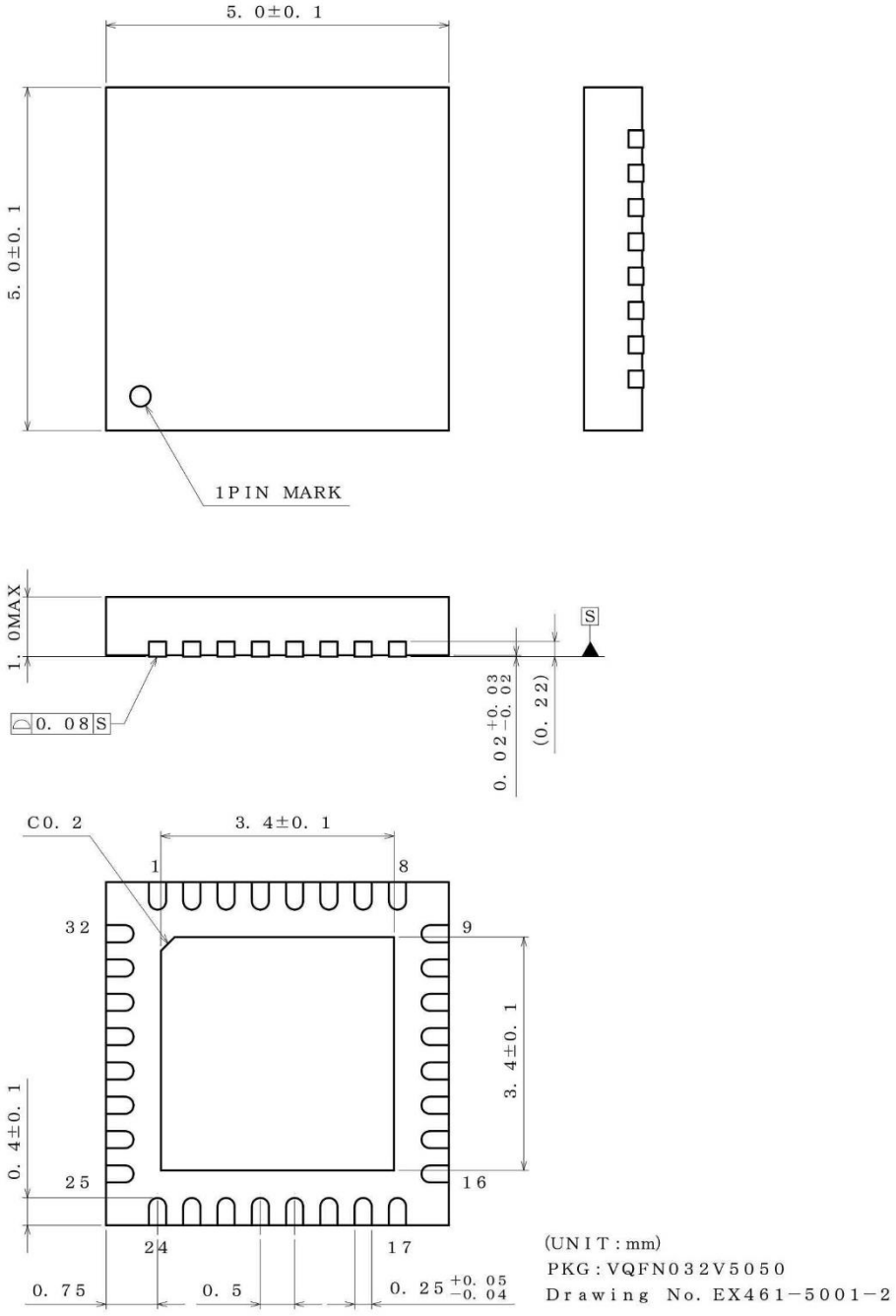


Marking Diagram



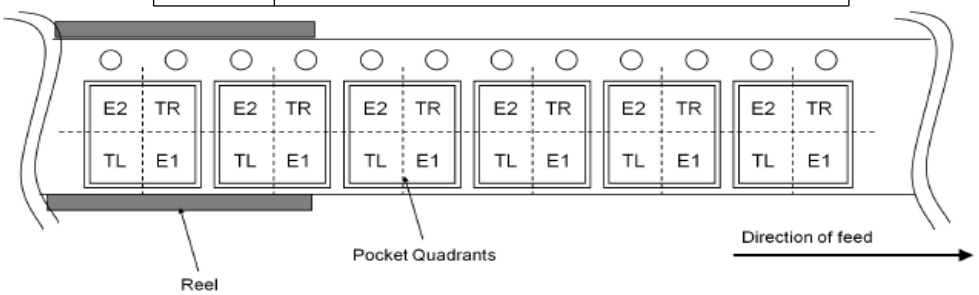
Physical Dimension and Packing Information

Package Name	VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
29.Jan.2016	001	New Release
06.Jun.2016	002	P.3 to P.5 Pin Description P.7 Absolute Maximum Ratings P.7 Thermal Resistance P.8 Thermal Resistance, Copper Pattern P.9 Electrical Characteristics, Input Impedance 1 P.11 to P.18 Typical Performance Curves P.19 Power Up/Down Sequence Figure 38. P.21 Power Limit Function P.23 to P.27 Application Circuit Example P.35 Operating condition with the application component ADD
21.Sep.2016	003	P.28 DC voltage protection P.31 DC voltage protection
15.Feb.2019	004	P.1 Typical Application Circuit Figure 1. P.7 Absolute Maximum Ratings Input Voltage 1 P.10 Typical Performance Curves Figure 5, Figure 6. P.19 Power Up/Down Sequence Figure 38. P.20 (3) Parallel BTL Function P.21 Figure number (41 to 43). P.28 to 31 Japanese font
22.Mar.2019	005	P.5 Add EXP-PAD for heat dissipation to the pin description. P.5 Add Note2 and Note3 to specify the notation in the datasheet. Others Fix the fluctuation of the expression in the datasheet Others Fix paragraph numbering and heading settings of all pages Others Fix all page format to ROHM latest format

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.