

PerFET™ Power Transistor

FEATURES

- Excellent FOM
- AEC-Q101 qualified
- Wettable flank leads for enhanced AOI
- 100% UIS and Rg tested
- 175°C operating junction temperature
- RoHS Compliant
- Halogen-free

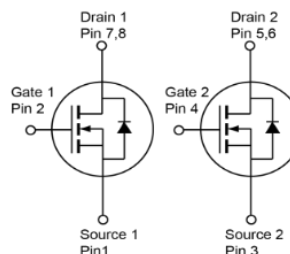
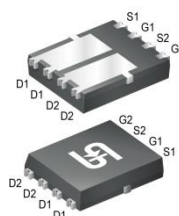
APPLICATIONS

- Automotive applications
- Solenoid and motor drivers
- DC-DC converters

KEY PERFORMANCE PARAMETERS			
PARAMETER		VALUE	UNIT
V_{DS}		100	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	25	mΩ
	$V_{GS} = 7V$	30	
Q_g	$V_{GS} = 10V$	8.4	nC



PDFN56U Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER		SYMBOL	LIMIT
Drain-Source Voltage		V_{DS}	100
Gate-Source Voltage		V_{GS}	± 20
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	31
	$T_C = 100^\circ\text{C}$		22
	$T_A = 25^\circ\text{C}$		7.4
Pulsed Drain Current (Note 1)		I_{DM}	124
Single Pulse Avalanche Current (Note 2)		I_{AS}	7
Single Pulse Avalanche Energy (Note 2)		E_{AS}	7.3
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	54
	$T_C = 125^\circ\text{C}$		18
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175

THERMAL PERFORMANCE			
PARAMETER		SYMBOL	LIMIT
Junction to Case Thermal Resistance		$R_{\theta JC}$	2.8
Junction to Ambient Thermal Resistance (Note 3)		$R_{\theta JA}$	50

Notes:

1. Pulse Width $\leq 100\mu\text{s}$.
2. $L = 0.3\text{mH}$, $V_{GS} = 10V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
3. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 1mA	BV _{DSS}	100	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.4	3	3.6	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 100V	I _{DSS}	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 100V T _J = 125°C		--	--	100	
Drain-Source On-State Resistance (Note 4)	V _{GS} = 10V, I _D = 15.5A	R _{DS(on)}	--	20	25	mΩ
	V _{GS} = 7V, I _D = 15.5A		--	23	30	
Forward Transconductance (Note 4)	V _{DS} = 10V, I _D = 3.9A	g _{fs}	--	14	--	S
Dynamic (Note 5)						
Total Gate Charge	V _{DS} = 50V, I _D = 7.4A, V _{GS} = 7V	Q _g	--	6.2	--	nC
Total Gate Charge	V _{DS} = 50V, I _D = 7.4A, V _{GS} = 10V	Q _g	--	8.4	--	nC
Gate-Source Charge		Q _{gs}	--	2.8	--	
Gate-Drain Charge		Q _{gd}	--	2.3	--	
Input Capacitance	V _{DS} = 60V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	513	--	pF
Output Capacitance		C _{oss}	--	115	--	
Reverse Transfer Capacitance		C _{rss}	--	18	--	
Gate Resistance	f = 1.0MHz	R _g	--	1.1	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V _{DD} = 50V, R _G = 6Ω, I _D = 7.4A, V _{GS} = 10V	t _{d(on)}	--	6.5	--	ns
Turn-On Rise Time		t _r	--	16	--	
Turn-Off Delay Time		t _{d(off)}	--	10	--	
Turn-Off Fall Time		t _f	--	5.9	--	
Source-Drain Diode						
Forward Voltage (Note 4)	I _S = 15.5A, V _{GS} = 0V	V _{SD}	--	--	1.1	V
Reverse Recovery Time	I _S = 7.4A,	t _{rr}	--	40	--	ns
Reverse Recovery Charge	di/dt = 100A/μs	Q _{rr}	--	47	--	nC

Notes:

- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

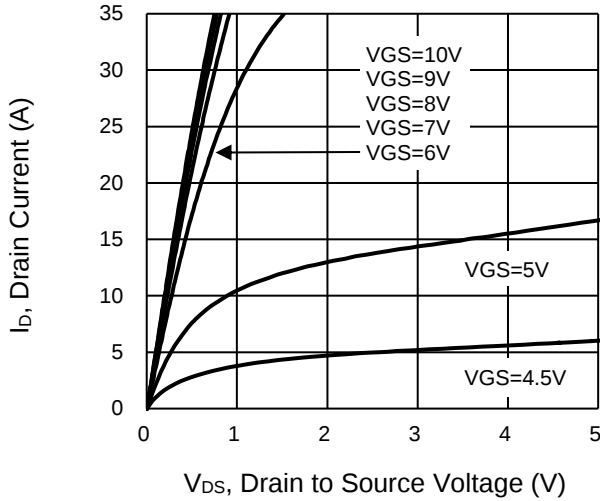
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM250NH10DCR RLG	PDFN56U Dual	2,500pcs / 13" Reel

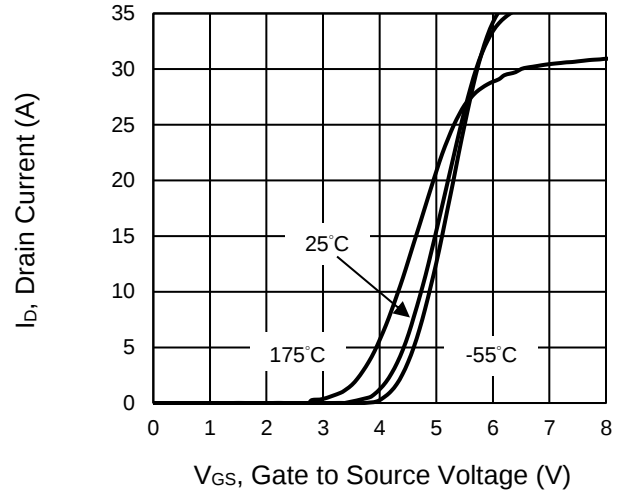
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

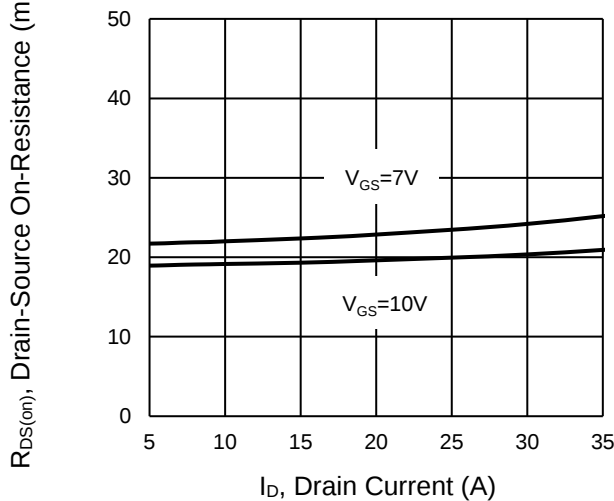
Output Characteristics



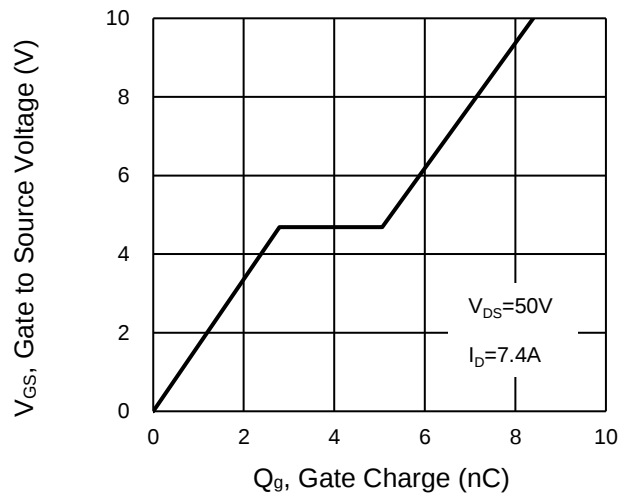
Transfer Characteristics



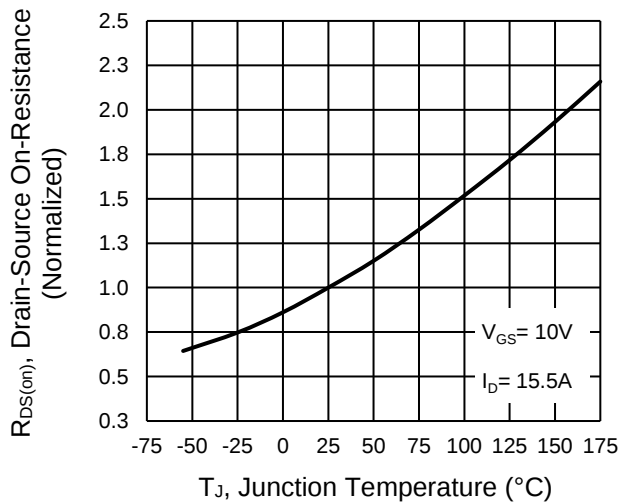
On-Resistance vs. Drain Current



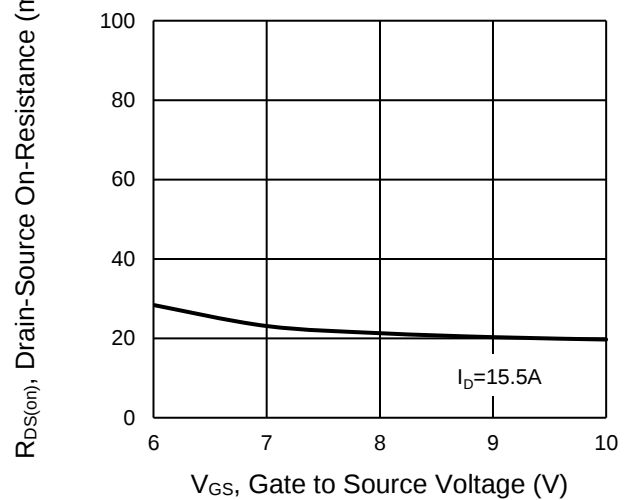
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



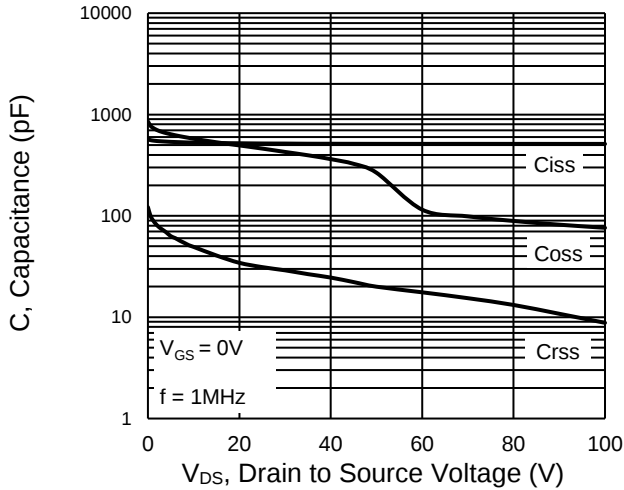
On-Resistance vs. Gate-Source Voltage



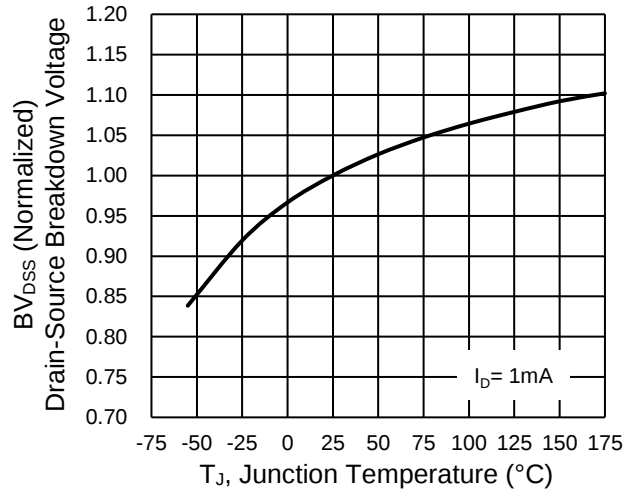
CHARACTERISTICS CURVES

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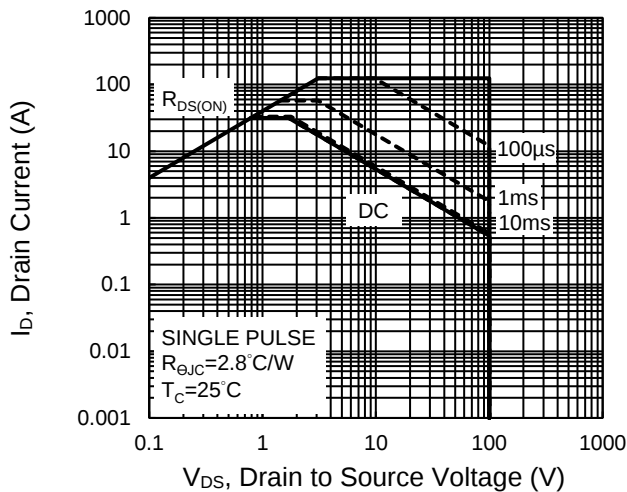
Capacitance vs. Drain-Source Voltage



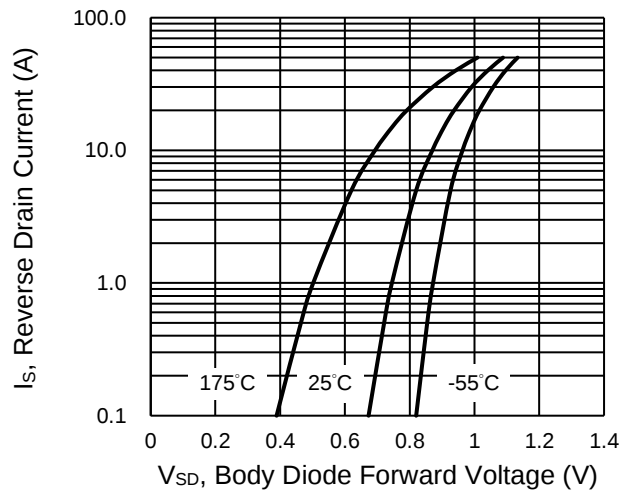
BV_{DSS} vs. Junction Temperature



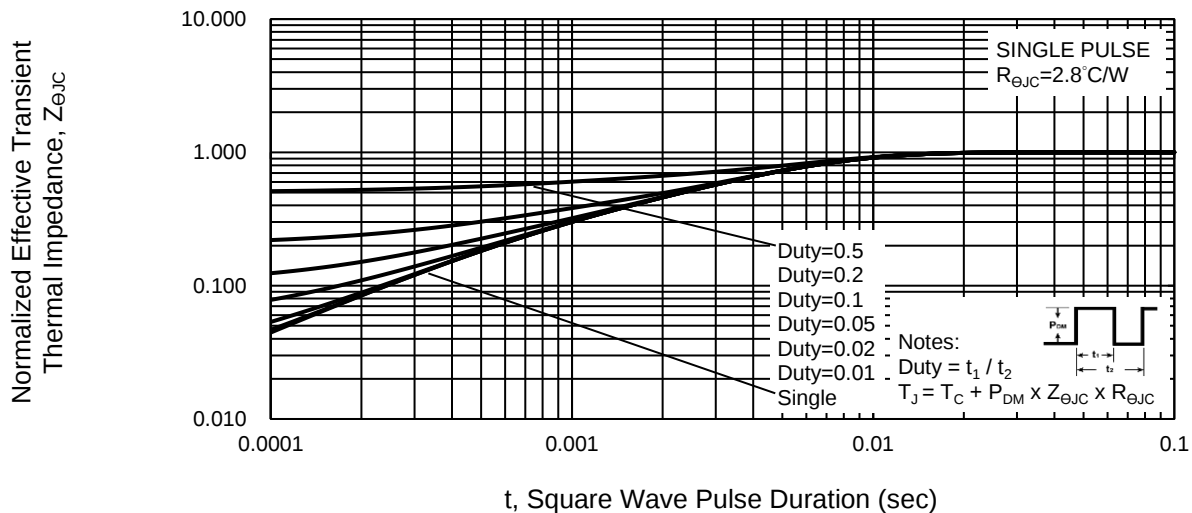
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

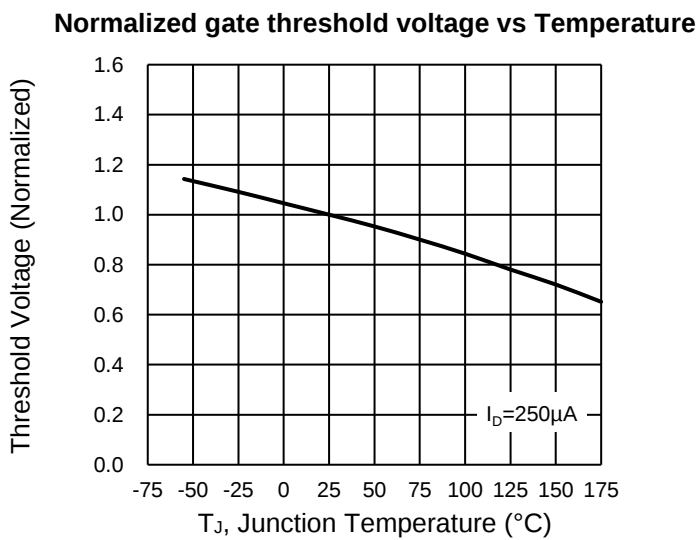
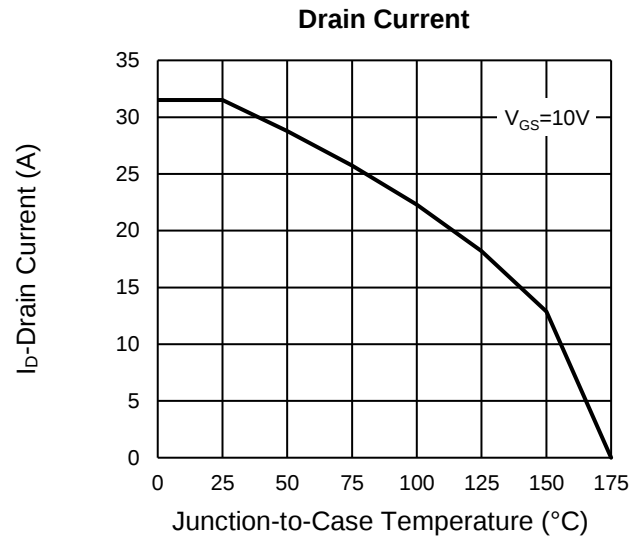
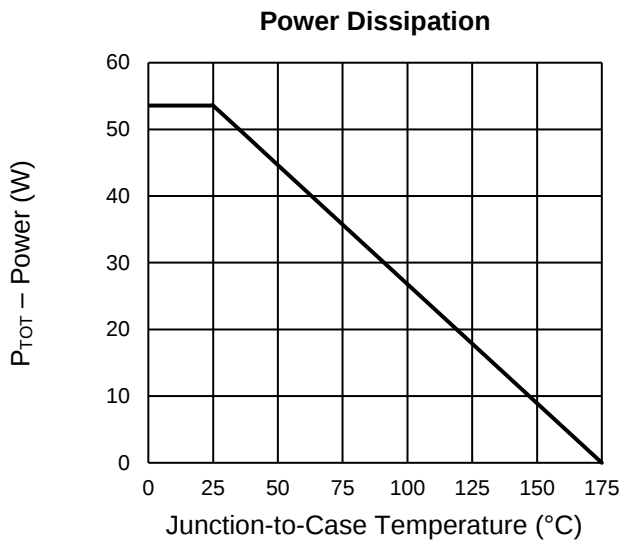


Normalized Thermal Transient Impedance, Junction-to-Case



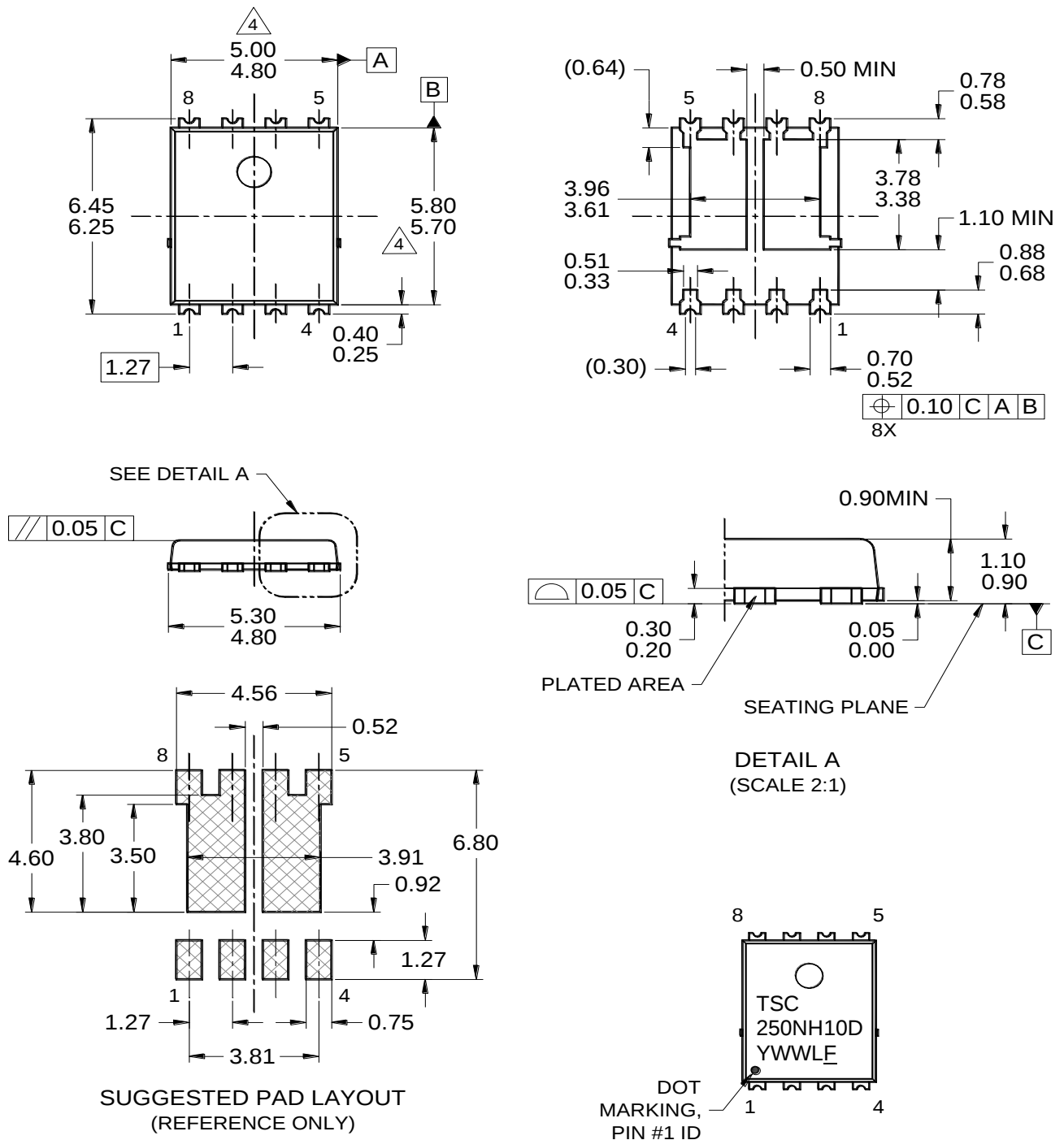
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56U Dual



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111CB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56UD-032 REV B.

MARKING DIAGRAM

250NH10D = Device marking
Y = Year code
WW = Week code (01~52)
L = Lot code (1~9,A~Z)
F = Factory code
- = AEC-Q101 qualified

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