260Pin DDR4 2400 SO-DIMM
4GB~8GB Based on 512Mx8

TS512MSH64V4H #1100
TS1GSH64V4H #1100

Description

DDR4 SO-DIMMs are high-speed and low power memory modules that use 512Mx8bits DDR4 SDRAM in FBGA package and a 4K-bit serial EEPROM on a 260-pin printed circuit board. DDR4 SO-DIMMs are dual In-Line memory modules and are intended for mounting into 260-pin edge connector sockets.

The synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. The large range of operation frequencies and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

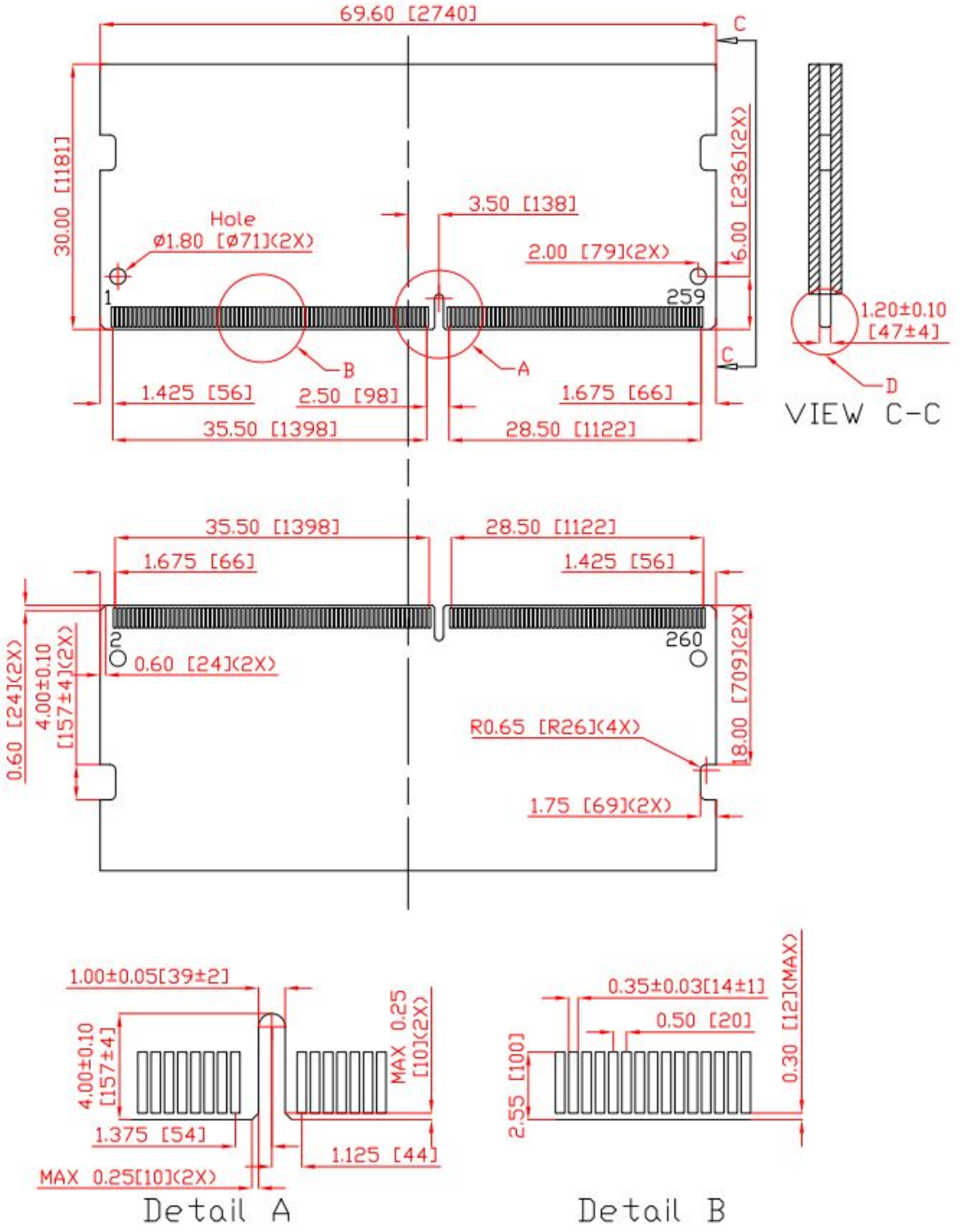
Features

- RoHS compliant
- JEDEC standard 1.2V ± 0.06V power supply
- VDDQ=1.2V ± 0.06V
- Clock Freq: 1200MHZ for 2400Mb/s/Pin.
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 12, 16(DDR4-2400)
- 8 bit pre-fetch
- Burst Length: 8 , 4 with tCCD = 4 which does not allow seamless read or write
- Bi-directional Differential Data-Strobe
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

Pin Identification

Symbol	Function
A0–A14	SDRAM address bus
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n	SDRAM row address strobe
CAS_n	SDRAM column address strobe
WE_n	SDRAM write enable
CS0_n, CS1_n	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
PARITY	SDRAM parity input
VDD	SDRAM I/O and core power supply
12 V	Optional power Supply on socket but not used on UDIMM
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD EEPROM positive power supply
SCL	I^2C serial bus clock for EEPROM
SDA	I^2C serial bus data line for EEPROM
SA0–SA2	I^2C slave address select for EEPROM
ALERT_n	SDRAM ALERT_n
VPP	SDRAM Supply
RESET_n	Set DRAMs to a Known State
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connection

Dimensions (Unit: millimeter)



Note:
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

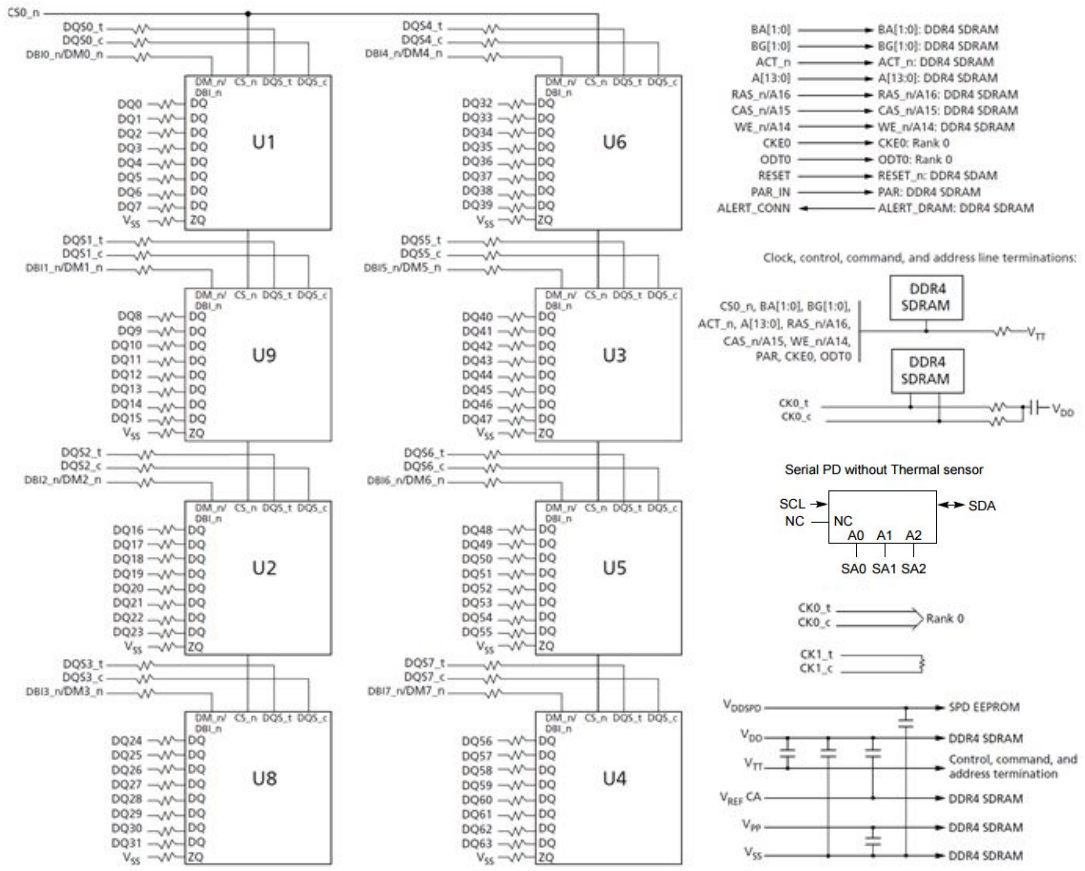
Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VSS	89	VSS	177	DQS4_c	02	VSS	90	VSS	178	DM4_n/ DBI4_n
03	DQ5	91	CB1/NC	179	DQS4_t	04	DQ4	92	CB0/NC	180	VSS
05	VSS	93	VSS	181	VSS	06	VSS	94	VSS	182	DQ39
07	DQ1	95	DQS8_c	183	DQ38	08	DQ0	96	DM8_n/ DBI_n/NC	184	VSS
09	VSS	97	DQS8_t	185	VSS	10	VSS	98	VSS	186	DQ35
11	DQS0_c	99	VSS	187	DQ34	12	DM0_n/ DBI0_n	100	CB6/NC	188	VSS
13	DQS0_t	101	CB2/NC	189	VSS	14	VSS	102	VSS	190	DQ45
15	VSS	103	VSS	191	DQ44	16	DQ6	104	CB7/NC	192	VSS
17	DQ7	105	CB3/NC	193	VSS	18	VSS	106	VSS	194	DQ41
19	VSS	107	VSS	195	DQ40	20	DQ2	108	RESET_n	196	VSS
21	DQ3	109	CKE0	197	VSS	22	VSS	110	CKE1	198	DQS5_c
23	VSS	111	VDD	199	DM5_n/ DBI5_n	24	DQ12	112	VDD	200	DQS5_t
25	DQ13	113	BG1	201	VSS	26	VSS	114	ACT_n	202	VSS
27	VSS	115	BG0	203	DQ46	28	DQ8	116	ALERT_n	204	DQ47
29	DQ9	117	VDD	205	VSS	30	VSS	118	VDD	206	VSS
31	VSS	119	A12	207	DQ42	32	DQS1_c	120	A11	208	DQ43
33	DM1_n/ DBI_n	121	A9	209	VSS	34	DQS1_t	122	A7	210	VSS
35	VSS	123	VDD	211	DQ52	36	VSS	124	VDD	212	DQ53
37	DQ15	125	A8	213	VSS	38	DQ14	126	A5	214	VSS
39	VSS	127	A6	215	DQ49	40	VSS	128	A4	216	DQ48
41	DQ10	129	VDD	217	VSS	42	DQ11	130	VDD	218	VSS
43	VSS	131	A3	219	DQS6_c	44	VSS	132	A2	220	DM6_n/ DBI6_n
45	DQ21	133	A1	221	DQS6_t	46	DQ20	134	NF	222	VSS
47	VSS	135	VDD	223	VSS	48	VSS	136	VDD	224	DQ54
49	DQ17	137	CK0_t	225	DQ55	50	DQ16	138	CK1_t/NF	226	VSS
51	VSS	139	CK0_c	227	VSS	52	VSS	140	CK1_c/NF	228	DQ50
53	DQS2_c	141	VDD	229	DQ51	54	DM2_n/ DBI2_n	142	VDD	230	VSS
55	DQS2_t	143	PARITY	231	VSS	56	VSS	144	A0	232	DQ60
57	VSS	145	BA1	233	DQ61	58	DQ22	146	A10/AP	234	VSS
59	DQ23	147	VDD	235	VSS	60	VSS	148	VDD	236	DQ57
61	VSS	149	CS0_n	237	DQ56	62	DQ18	150	BA0	238	VSS
63	DQ19	151	WE_n/ A14	239	VSS	64	VSS	152	RAS_n/ A16	240	DQS7_c
65	VSS	153	VDD	241	DM7_n/ DBI7_n	66	DQ28	154	VDD	242	DQS7_t
67	DQ29	155	ODT0	243	VSS	68	VSS	156	CAS_n/ A15	244	VSS
69	VSS	157	CS1_n	245	DQ62	70	DQ24	158	A13	246	DQ63
71	DQ25	159	VDD	247	VSS	72	VSS	160	VDD	248	VSS
73	VSS	161	ODT1	249	DQ58	74	DQS3_c	162	C0/ CS2_n/NC	250	DQ59
75	DM3_n/ DBI3_n	163	VDD	251	VSS	76	DQS3_t	164	VREFCA	252	VSS
77	VSS	165	C1, CS3_n, NC	253	SCL	78	VSS	166	SA2	254	SDA
79	DQ30	167	VSS	255	VDDSPD	80	DQ31	168	VSS	256	SA0
81	VSS	169	DQ37	257	VPP	82	VSS	170	DQ36	258	VTT
83	DQ26	171	VSS	259	VPP	84	DQ27	172	VSS	260	SA1
85	VSS	173	DQ33	-	-	86	VSS	174	DQ32	-	-
87	CB5/NC	175	VSS	-	-	88	CB4/NC	176	VSS	-	-

Note:

- NC for Non ECC SO-DIMM.

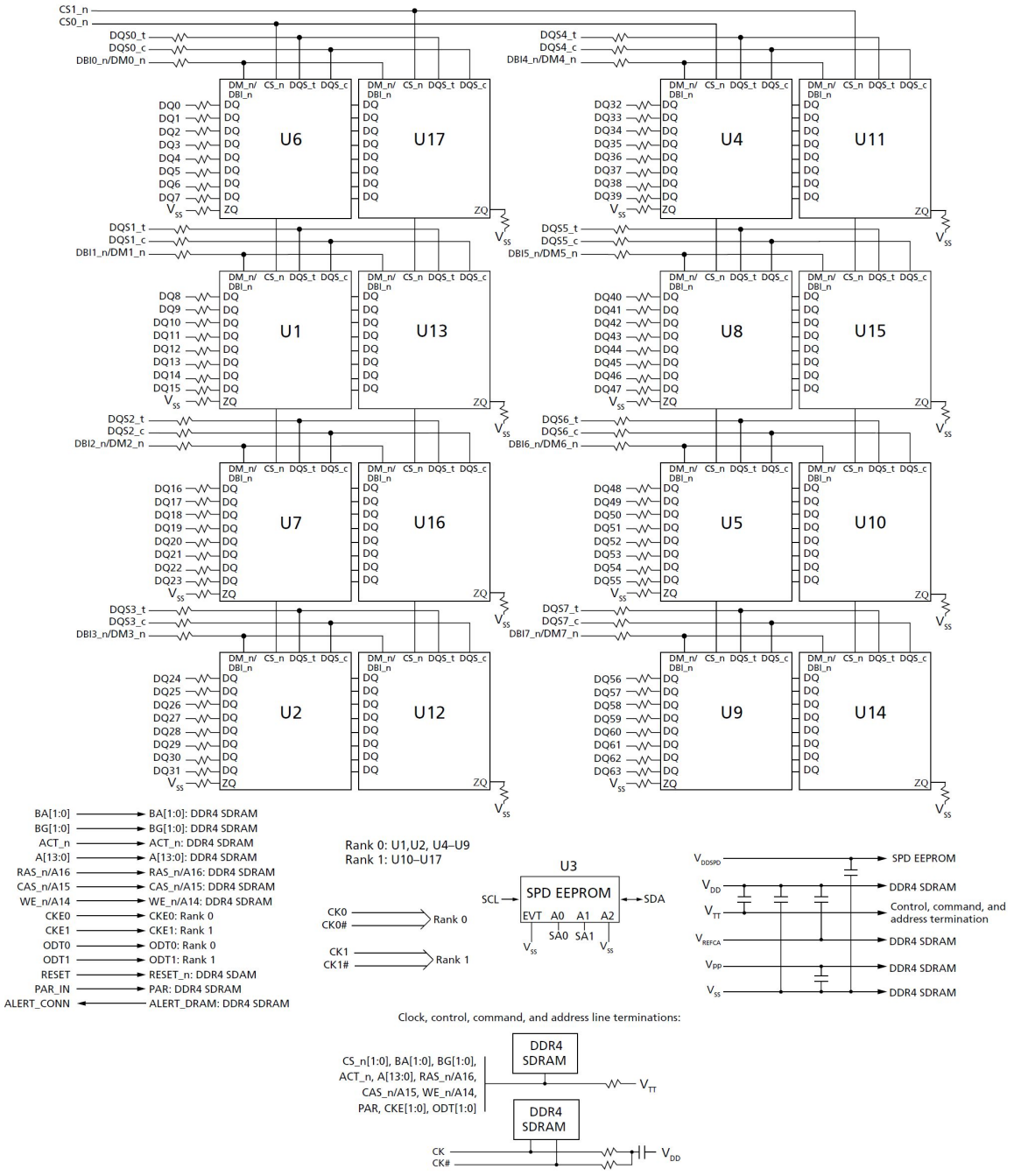
Block Diagram
4GB, 512Mx64 Module(1 Rank x8)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Block Diagram
8GB, 1Gx64 Module(2 Rank x8)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note:
- Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on VDD relative to Vss	VDD	-0.3 ~ 1.5	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.5	V	1
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 3.0	V	3
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.5	V	1
Storage temperature	TSTG	-55~+100	°C	1,2

Note:
- Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the ambient temperature.
- VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2
Supply voltage for Output	VDDQ	1.14	1.2	1.26	V	1, 2
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3

Note:
- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
- DC bandwidth is limited to 20MHz

Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	DDR4-1600/1866/2133/2400		DDR4-2666		Unit	Note
		Min	Max	Min	Max		
I/O Reference Voltage	VREFCA(DC)	0.49*VDDQ	0.51*VDDQ	TBD	TBD	V	1,2
DC Input Logic High	VIH(DC)	VREF+0.075	VDD	TBD	TBD	V	
DC Input Logic Low	VIL(DC)	VSS	VREF-0.075	TBD	TBD	V	
AC Input Logic High	VIH(AC)	VREF+0.1	Note 1	TBD	TBD	V	
AC Input Logic Low	VIL(AC)	Note 1	VREF-0.1	TBD	TBD	V	

Note:
- The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference: approx. ± 12mV)
- For reference: approx. VDD/2 ± 12mV

Differential AC and DC Input Levels

Parameter	Symbol	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	Note
		Min	Max	Min	Max		
differential input high DC	VIHdiff(DC)	+0.150	NOTE 3	TBD	NOTE 3	V	1
differential input low DC	VILdiff(DC)	NOTE 3	-0.150	NOTE 3	TBD	V	1
differential input high AC	VIHdiff(AC)	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
differential input low AC	VILdiff(AC)	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

Note: 1.Used to define a differential signal slew-rate.
2.For CK_t - CK_c use VIH.CA/VIL.CA(AC) of ADD/CMD and VREFCA;
3.These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-ended AC & DC output levels

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666	Unit	Note
DC output high measurement level	VOH(DC)	1.1 x VDDQ	V	
DC output mid measurement level	VOM(DC)	0.8 x VDDQ	V	
DC output low measurement level	VOL(DC)	0.5 x VDDQ	V	
AC output high measurement level	VOH(AC)	(0.7 + 0.15) x VDDQ	V	1
AC output low measurement level	VOL(AC)	(0.7 - 0.15) x VDDQ	V	1

Note: ● The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Differential AC & DC output levels

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666	Unit	Note
AC differential output high measurement level	VOHdiff(AC)	+0.3 x VDDQ	V	1
AC differential output low measurement level	VOLdiff(AC)	-0.3 x VDDQ	V	1

Note: ● The swing of ± 0.3 × VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ at each of the differential outputs.

Temperature Sensor With SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{CC1}	1.7		3.6	V
Supply voltage	V_{CC2}	2.2		3.6	V
Input low voltage: logic 0; all inputs	V_{IL}	-0.5		V_{CC} x 0.3	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{CC} x 0.7		V_{CC} + 0.5	V
Output low voltage: 3mA sink current V_{CC} > 2V	V_{OL}			0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{CC} or V_{SS}	I_{LI}		0.1	2.0	uA
Output leakage current: V_{OUT} = V_{CC} or V_{SS}	I_{LO}		0.1	2.0	uA

IDD Specification parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

4GB, 512Mx64 Module(1 Rank x8)

Parameter	Symbol	DDR4 2400 CL17		Unit
		IDD Max.	IPP Max.	
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	248	32	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	336	24	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	80	24	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	104	24	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	120	24	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	104	24	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	224	24	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	720	24	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	624	24	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1536	144	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	104	32	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1184	72	mA

Note: Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

8GB, 1Gx64 Module(2 Rank x8)

Parameter	Symbol	DDR4 2400 CL17		Unit
		IDD Max.	IPP Max.	
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	368	56	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	456	48	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	160	48	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	208	48	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	240	48	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	208	48	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	448	48	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	840	48	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	744	48	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1656	168	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	208	64	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1304	96	mA

Note: Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	ns
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	TBD	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	TBD	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	ps
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK,5.625 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)		Max(28nCK,30ns)		Max(28nCK,30ns)		Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)		Max(20nCK,23ns)		Max(20nCK,21ns)		Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)		Max(16nCK,17ns)		Max(16nCK,15ns)		Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	ns
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	ns
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	

WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	ns
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	854	-	nCK
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	8	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))										nCK
CS_n to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	nCK
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	-	0.18	tCK(avg)/ 2
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	tCK(avg)/ 2
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-390	180	-330	175	-310	170	ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	-	170	ps
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	nCK
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	nCK
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK
CKE minimum pulse width	tCKE	max (3nCK,5ns)	-	max (3nCK,5ns)	-	max (3nCK,5ns)	-	max (3nCK,5ns)	-	max (3nCK,5ns)	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns

RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	160	-	ns
	4Gb	260	-	260	-	260	-	260	-	260	-	ns
	8Gb	350	-	350	-	350	-	350	-	350	-	ns
	16Gb	550	-	550	-	550	-	550	-	550	-	ns
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	110	-	ns
	4Gb	160	-	160	-	160	-	160	-	160	-	ns
	8Gb	260	-	260	-	260	-	260	-	260	-	ns
	16Gb	350	-	350	-	350	-	350	-	350	-	ns
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	90	-	ns
	4Gb	110	-	110	-	110	-	110	-	110	-	ns
	8Gb	160	-	160	-	160	-	160	-	160	-	ns
	16Gb	260	-	260	-	260	-	260	-	260	-	ns

SERIAL PRESENCE DETECT SPECIFICATION

TS512MSH64V4H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of Bytes Used / Number of Bytes in SPD Device	SPD Byte use: 512Byte SPD Byte total: 512Byte	24
1	SPD Revision	Revision 1.0	10
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	4Gb, 16banks	84
5	SDRAM Addressing	ROW:15, Column:10	19
6	SDRAM Package Type	Monolithic DRAM device	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Options	Reserved	00
9	Other SDRAM Optional Features	PPR not supported	00
10	Secondary SDRAM Package Type	Reserved	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	1Rank, 8bits	01
13	Module Memory Bus Width	Non-ECC, 64bits	03
14	Module Thermal Sensor	Not Support	00
15-16	Reserved	Reserved	00
17	Timebases	MTB 125ps, FTB 1ps	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.833ns	07
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.6ns	0D
20-23	CAS Latencies Supported	10, 11, 12, 13, 14, 15, 16,17,18	F8, 0F, 00, 00
24	Minimum CAS Latency Time (tAAmin)	13.75ns	6E
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.75ns	6E
26	Minimum Row Precharge Delay Time (tRPmin)	13.75ns	6E
27	Upper Nibbles for tRASmin and tRCmin	-	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	32ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	45.75ns	6E
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	260ns	20,08
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	160ns	00,05
34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	110ns	70,03
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	21ns	00,A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	3.3ns	1B
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	4.9ns	28
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5ns	28
41	Upper Nibble for tWRmin	-	00
42	Minimum Write Recovery Time(tWRmin)	15ns	78

43	Upper Nibbles for tWTRmin	-	00
44	Minimum Write to Read Time(tWTR_smin), different bank group	2.5ns	14
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5ns	3C
46~59	Reserved	Reserved	00
60	Connector to SDRAM Bit Mapping	DQ0-3	0C
61	Connector to SDRAM Bit Mapping	DQ4-7	2B
62	Connector to SDRAM Bit Mapping	DQ8-11	2D
63	Connector to SDRAM Bit Mapping	DQ12-15	04
64	Connector to SDRAM Bit Mapping	DQ16-19	16
65	Connector to SDRAM Bit Mapping	DQ20-23	35
66	Connector to SDRAM Bit Mapping	DQ24-27	23
67	Connector to SDRAM Bit Mapping	DQ28-31	0D
68	Connector to SDRAM Bit Mapping	CB0-3	00
69	Connector to SDRAM Bit Mapping	CB4-7	00
70	Connector to SDRAM Bit Mapping	DQ32-25	2C
71	Connector to SDRAM Bit Mapping	DQ36-39	0B
72	Connector to SDRAM Bit Mapping	DQ40-43	03
73	Connector to SDRAM Bit Mapping	DQ44-47	24
74	Connector to SDRAM Bit Mapping	DQ48-51	35
75	Connector to SDRAM Bit Mapping	DQ52-55	0C
76	Connector to SDRAM Bit Mapping	DQ56-59	03
77	Connector to SDRAM Bit Mapping	DQ60-63	2D
78-116	Reserved	Reserved	00
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	0ps	00
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-100ps	9C
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	-75ps	B5
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0ps	00
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	0ps	00
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	0ps	00
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	0ps	00
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-25ps	E7
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	-42ps	D6
126-127	Cyclical Redundancy Code	Cyclical Redundancy Code	71,76
128	Raw Card Extension, Module Nominal Height	29mm<height<=30mm	0F
129	Module Maximum Thickness	Front&Back, 1<thickness<2 mm	11
130	Reference Raw Card Used	Revision 1, Raw card A	20

131	Address Mapping from Edge Connector to DRAM	Standard	00				
132-253	Reserved	Reserved	00				
254-255	Cyclical Redundancy Code (CRC)	Cyclical Redundancy Code	EF,55				
256-319	Reserved	Reserved	00				
320-321	Module Manufacturer ID Code	Transcend	01,4F				
322	Module Manufacturing Location	Taipei	54				
323-324	Module Manufacturing Date	Year, Week	Variable				
325-328	Module Serial Number	Module Serial Number	Variable				
329-348	Module Part Number	TS512MSH64V4H	54	53	35	31	32
			4D	53	48	36	34
			56	34	48	20	20
			20	20	20	20	20
349	Module Revision Code	-	00				
350-351	DRAM Manufacturer ID Code	By Manufacturer	Variable				
352	DRAM Stepping	Stepping information not provided	Variable				
353-367	Manufacturer Specific Data	By Manufacturer	Variable				
368-372	Option Code	#1100	Variable				
373-381	Manufacturer Specific Data	By Manufacturer	Variable				
382-383	Reserved	Reserved	00				
384-511	End User Programmable	By Manufacturer	Variable				

TS1GSH64V4H Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of Bytes Used / Number of Bytes in SPD Device	SPD Byte use: 512Byte SPD Byte total: 512Byte	24
1	SPD Revision	Revision 1.1	11
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	4Gb, 16banks	84
5	SDRAM Addressing	ROW:15, Column:10	19
6	SDRAM Package Type	Monolithic DRAM device	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Options	Reserved	00
9	Other SDRAM Optional Features	PPR not supported	00
10	Secondary SDRAM Package Type	Reserved	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	2Rank, 8bits	09
13	Module Memory Bus Width	Non-ECC, 64bits	03
14	Module Thermal Sensor	Not Support	00
15-16	Reserved	Reserved	00
17	Timebases	MTB 125ps, FTB 1ps	00
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.833ns	07
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.6ns	0D
20-23	CAS Latencies Supported	10, 11, 12, 13, 14, 15, 16,17,18	F8, 0F, 00, 00
24	Minimum CAS Latency Time (tAAmin)	13.5ns	6C
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.5ns	6C
26	Minimum Row Precharge Delay Time (tRPmin)	13.5ns	6C
27	Upper Nibbles for tRASmin and tRCmin	-	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	32ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	45.75ns	6E
30-31	Minimum Refresh Recovery Delay Time (tRFC1min)	260ns	20,08
32-33	Minimum Refresh Recovery Delay Time (tRFC2min)	160ns	00,05
34-35	Minimum Refresh Recovery Delay Time (tRFC4min)	110ns	70,03
36-37	Minimum Four Activate Window Delay Time (tFAWmin)	21ns	00,A8
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	3.3ns	1B
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	4.9ns	28
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	5ns	28
41	Upper Nibble for tWRmin	-	00
42	Minimum Write Recovery Time(tWRmin)	15ns	78

43	Upper Nibbles for tWTRmin	-	00
44	Minimum Write to Read Time(tWTR_smin), different bank group	2.5ns	14
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5ns	3C
46~59	Reserved	Reserved	00
60	Connector to SDRAM Bit Mapping	DQ0-3	2B
61	Connector to SDRAM Bit Mapping	DQ4-7	16
62	Connector to SDRAM Bit Mapping	DQ8-11	2C
63	Connector to SDRAM Bit Mapping	DQ12-15	0B
64	Connector to SDRAM Bit Mapping	DQ16-19	2C
65	Connector to SDRAM Bit Mapping	DQ20-23	16
66	Connector to SDRAM Bit Mapping	DQ24-27	2C
67	Connector to SDRAM Bit Mapping	DQ28-31	0C
68	Connector to SDRAM Bit Mapping	CB0-3	00
69	Connector to SDRAM Bit Mapping	CB4-7	00
70	Connector to SDRAM Bit Mapping	DQ32-25	2C
71	Connector to SDRAM Bit Mapping	DQ36-39	0C
72	Connector to SDRAM Bit Mapping	DQ40-43	15
73	Connector to SDRAM Bit Mapping	DQ44-47	36
74	Connector to SDRAM Bit Mapping	DQ48-51	2B
75	Connector to SDRAM Bit Mapping	DQ52-55	15
76	Connector to SDRAM Bit Mapping	DQ56-59	0B
77	Connector to SDRAM Bit Mapping	DQ60-63	36
78-116	Reserved	Reserved	00
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	0ps	00
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	-100ps	9C
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	-75ps	B5
120	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0ps	00
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	0ps	00
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	0ps	00
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	0ps	00
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	-25ps	E7
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	-42ps	D6
126-127	Cyclical Redundancy Code	Cyclical Redundancy Code	83,52
128	Raw Card Extension, Module Nominal Height	29mm<height<=30mm	0F
129	Module Maximum Thickness	Front&Back, 1<thickness<2 mm	11
130	Reference Raw Card Used	Revision 1, Raw card B	21

131	Address Mapping from Edge Connector to DRAM	Standard	01				
132-253	Reserved	Reserved	00				
254-255	Cyclical Redundancy Code (CRC)	Cyclical Redundancy Code	87,2A				
256-319	Reserved	Reserved	00				
320-321	Module Manufacturer ID Code	Transcend	01,4F				
322	Module Manufacturing Location	Taipei	54				
323-324	Module Manufacturing Date	Year, Week	Variable				
325-328	Module Serial Number	Module Serial Number	Variable				
329-348	Module Part Number	TS1GSH64V4H	54	53	31	47	53
			48	36	34	56	34
			48	20	20	20	20
			20	20	20	20	20
349	Module Revision Code	-	00				
350-351	DRAM Manufacturer ID Code	By Manufacturer	Variable				
352	DRAM Stepping	Stepping information not provided	Variable				
353-367	Manufacturer Specific Data	By Manufacturer	Variable				
368-372	Option Code	#1100	Variable				
373-381	Manufacturer Specific Data	By Manufacturer	Variable				
382-383	Reserved	Reserved	00				
384-511	End User Programmable	By Manufacturer	Variable				