REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22												
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RAJESH PITHADIA

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
17-01-10

REVISION LEVEL

MICROCIRCUIT, DIGITAL-LINEAR, REDUNDANT, ATTACHMENT UNIT INTERFACE TRANSCEIVER, MONOLITHIC SILICON

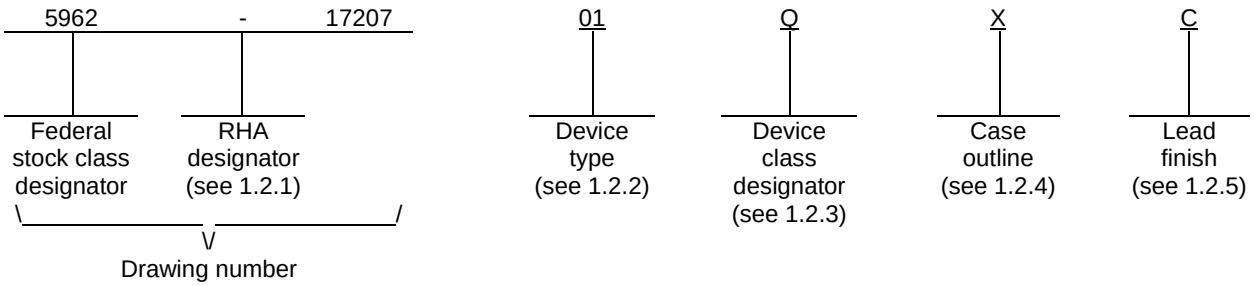
SIZE	CAGE CODE	
A	**67268**	**5962-17207**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLK3118	Quad, redundant, 10 gigabits per second attachment unit interface transceiver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	400	Ceramic Land Grid Array (LGA)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage range: 2/

V_{DD}, V_{DDA}	-0.3 V to +1.5 V
V_{DDQ}	-0.3 V to +2.5 V
V_{DDB}	-0.3 V to +3 V
V_{DDT}	-0.3 V to +2 V
Input voltage range (V_{IN}), LVCMOS	-0.5 V to +3 V
Input voltage range (V_{IN}), HSTL class 1	-0.5 V to +2 V
Maximum power dissipation (P_D)	2.4 W 3/
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	8.6°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	17.7°C/W

1.4 Recommended operating conditions.

Core supply voltage (V_{DD})	+1.14 V to +1.26 V
Bias supply voltage (V_{DDB}), LVCMOS Input/Output	+2.37 V to +2.63 V
Bias supply voltage (V_{DDT}),	+1.14 V to +1.26 V
Input/output supply voltage (V_{DDQ}), HSTL class 1	+1.4 V to +1.6 V
Analog supply voltage (V_{DDA})	+1.14 V to +1.26 V
Core supply current (I_{DD})	770 mA 3/
Input/output supply current (I_{DDQ})	415 mA 3/
Bias supply current (I_{DDB})	35 mA 3/
Analog supply current (I_{DDA})	240 mA 3/
Input reference voltage (V_{REF}), HSTL class 1	+0.71 V to 0.79 V 4/
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values, except differential input/output bus voltages, are with respect to network ground terminal.
3/ Operating frequency of 156.25 MHz.
4/ The value of V_{REF} may be selected to provide optimum noise margin in the system. The value of V_{REF} is expected to be 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}. Peak-to-peak ac noise on V_{REF} may not exceed ±2% V_{REF} (dc).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference clock (REFCLKP/N) 1/							
Differential input voltage	V_{IO}		1, 2, 3	01	250	2000	mVP-P
Input capacitance	C_{IN}	See 4.4.1c	4	01		3	pF
Differential input impedance	R_{IN}		1	01	80	120	Ω
Frequency		Minimum data rate	9,10,11	01	125 – 0.01%	125 + 0.01%	MHz
		Maximum data rate			156.25 – 0.01%	156.25 – 0.01%	
Accuracy			1, 2, 3	01	-200	200	ppm
Duty cycle			1, 2, 3	01	40	60	%
LVCMOS							
High level output voltage	V_{OH}	I_{OH} = -100 µA, driver enabled	1, 2, 3	01	V_{DDO} – 0.2		V
Low level output voltage	V_{OL}	I_{OH} = -100 µA, driver enabled	1, 2, 3	01		0.2	V
High level input voltage	V_{IH}		1, 2, 3	01	0.7 x V_{DDO}		V
Low level input voltage	V_{IL}		1, 2, 3	01	0	0.3 x V_{DDO}	V
High level/low level input current	I_{IH},I_{IL}		1, 2, 3	01		±1	µA
Low impedance input current	I_{IZ}	Driver only, driver disabled	1, 2, 3	01		±20	µA
Input capacitance	C_{IN}	See 4.4.1c	4	01		5	pF
Voltage at PAD	V_{PAD}		1	01		V_{DDO}	V
High speed transceiver logic (HSTL) signals							
High level output voltage, DC	V_{OH}		1, 2, 3	01	V_{DDO} – 0.4	V_{DDO}	V
Low level output voltage, DC	V_{OL}		1, 2, 3	01		0.4	V
High level output voltage, AC	V_{OH}		1, 2, 3	01	V_{DDO} – 0.5	V_{DDO}	V
Low level output voltage, AC	V_{OL}		1, 2, 3	01		0.5	V
High level input voltage, DC	V_{IH}	DC input, logic high	1, 2, 3	01	V_{REF} + 0.1	V_{DDO} + 0.3	V
Low level input voltage, DC	V_{IL}	DC input, logic low	1, 2, 3	01	-0.3	V_{REF} - 0.1	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High speed transceiver logic (HSTL) signals – continued.							
High level input voltage, AC	V_{IH}	AC input, logic high	1, 2, 3	01	V_{REF} + 0.2		V
Low level input voltage, AC	V_{IL}	AC input, logic low	1, 2, 3	01		V_{REF} - 0.2	V
High level output current, DC	I_{OH}	V_{DDQ} = 1.5 V	1, 2, 3	01	-8		mA
Low level output current, DC	I_{OL}	V_{DDQ} = 1.5 V	1, 2, 3	01	8		mA
Input capacitance	C_{IN}	See 4.4.1c	4	01		4	pF
Setup time, TXD[31:0], TXC[3:0] setup prior to TCLK transition high or low	t_{su}	Timing relative to V_{REF}	9, 10, 11	01	-368	-39	ps
		See figure 3	9, 10, 11		480		
Hold time, TXD[31:0], TXC[3:0] hold after TCLK transition high or low	t_h	Timing relative to V_{REF}	9, 10, 11	01	-442	-130	ps
		See figure 3	9, 10, 11		480		
Setup time, RXD[31:0], RXC[3:0] setup prior to RCLK transition high or low	t_{su}	See figure 4	9, 10, 11	01	960		ps
Hold time, RXD[31:0], RXC[3:0] hold after RCLK transition high or low	t_h	See figure 4	9, 10, 11	01	960		ps
Duty cycle, Receive Data Clock and Transmit Data Clock	DC		9, 10, 11	01	45	55	%
Management data I/O (MDIO)							
Management data clock period (MDC)	t_{period}	See figure 5	9, 10, 11	01	400		ns
MDIO setup to ↑ MDC	t_{su}	See figure 5	9, 10, 11	01	10		ns
MDIO hold to ↑ MDC	t_h	See figure 5	9, 10, 11	01	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial transmitter/receiver							
TX output differential peak-to-peak voltage swing	$V_{OD(PP)}$	Maximum pre-emphasis enabled. Emphasized bit. See figure 6	1, 2, 3	01	730	970	mV_{P-P}
TX output differential peak-to-peak voltage swing	$V_{OD(PD)}$	Pre-emphasis enabled. de-emphasized bit. See figure 6	1, 2, 3	01	440	600	mV_{P-P}
		Maximum pre-emphasis disabled	1, 2, 3		840	1100	
RX input leakage current	I_{IKG}		1, 2, 3	01	-10	10	µA
Input capacitance	C_{IN}	See 4.4.1c	4			2	pF
Differential output signal rise, fall time (20% to 80%)	t_r, t_f	R_L = 50 Ω, CL = 5 pF See figure 6	9, 10, 11	01	80	160	ps
Total delay from RX input to RD output	t_d	See figure 7	9, 10, 11	01		700	bit times
Total delay from TD input to TX output	t_d	See figure 8	9, 10, 11	01		600	bit times

1/ This clock should be crystal referenced to meet the requirements of Table I.

Case X

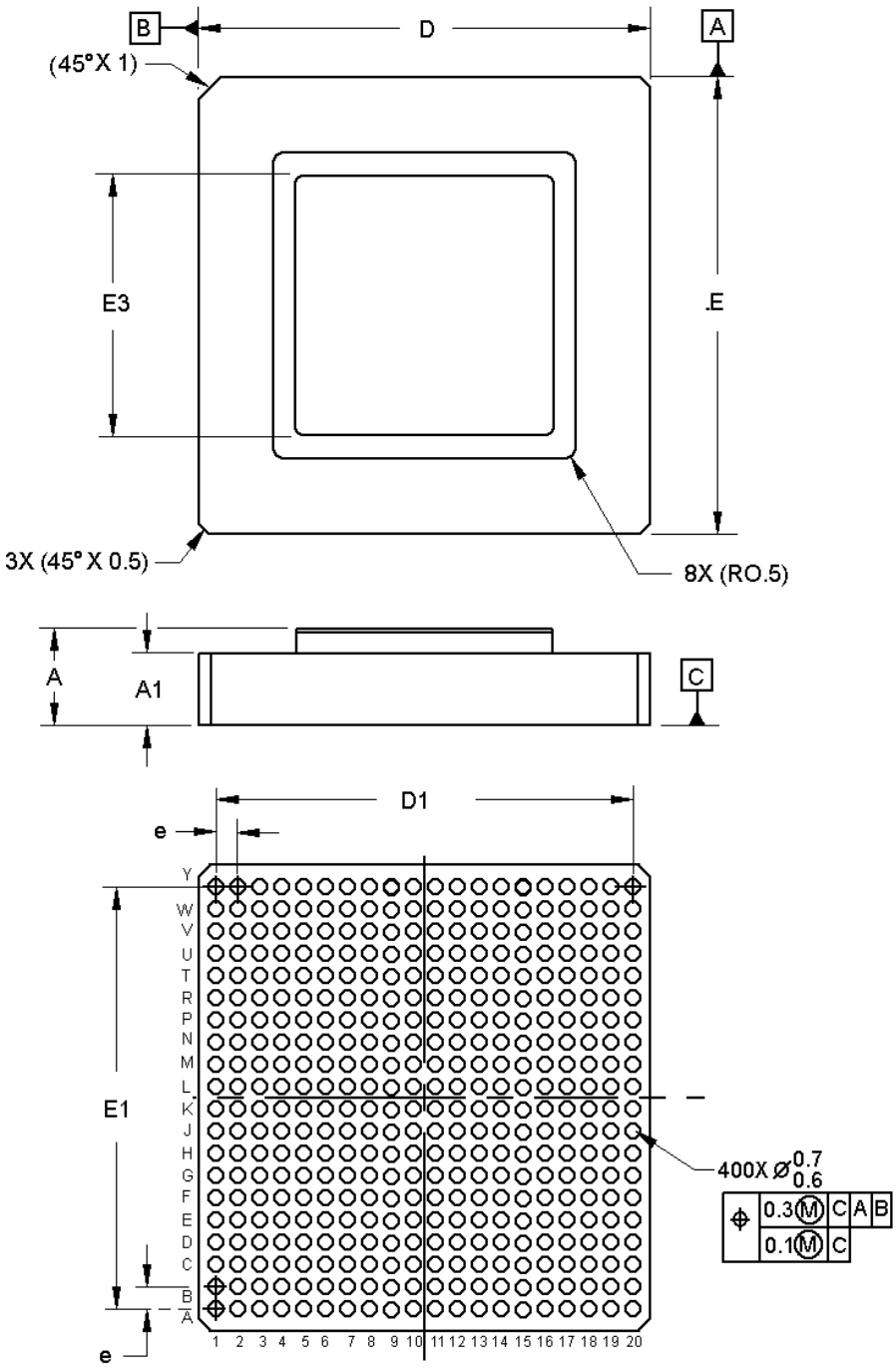


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-17207
		REVISION LEVEL	SHEET 8

DSCC FORM 2234
APR 97

Case X –continued.

Symbol	Millimeters	
	Min	Max
A	----	5.07
A1	2.97	3.63
D/E	20.74	21.06
D1/E1	19.00 BSC	
E3	11.85	12.15
e	1.000 BSC	

FIGURE 1. Case outline – continued.

Device Type	01	Device Types	01	Device Types	01
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
VDD	A1	VDDIO	C1	VDD	E1
VDDIO	A2	TXC1	C2	NUI	E2
VTT	A3	GND-GP1	C3	GND-GPI	E3
VDD	A4	TXD24	C4	VPP	E4
GND-GP1	A5	VREF	C5	VDD	E5
TXD20	A6	TXD26	C6	GND	E6
TXD22	A7	TXD27	C7	GND	E7
TXD30	A8	TXD29	C8	GND	E8
GND	A9	TXC3	C9	GND	E9
GND	A10	GND	C10	VDDIO	E10
NC-GPO	A11	RXD31	C11	GND	E11
VDDIO	A12	RXD26	C12	VDDIO	E12
VDD	A13	RXD22	C13	VDD	E13
GND	A14	RXD23	C14	GND	E14
VDDIO	A15	RXC2	C15	GND	E15
VDDIO	A16	VTP-PD1	C16	GND	E16
VDD	A17	RXD24	C17	VDDIO	E17
NC-GPO	A18	RXD14	C18	VDDQ	E18
VDDIO	A19	RXD16	C19	RXD17	E19
VDD	A20	GND	C20	RCLK	E20
VTT	B1	VDDIO	D1	VTT	F1
TXD13	B2	VDD	D2	TCLK	F2
TXD14	B3	TXC2	D3	VDDIO	F3
TXD15	B4	QGND	D4	VTT	F4
TXD16	B5	TXD25	D5	VDDIO	F5
TXD21	B6	VDDIO	D6	GND	F6
TXD23	B7	A_B	D7	GND	F7
TXD28	B8	GND-GPI	D8	GND	F8
TXD31	B9	RSTN	D9	GND	F9
GND	B10	GND	D10	GND	F10
RXC3	B11	RXD30	D11	GND	F11
RXD25	B12	RXD27	D12	VDDIO	F12
RXD21	B13	RXD28	D13	GND	F13
VDDIO	B14	NC-GPO	D14	GND	F14
GND	B15	GND	D15	VDDIO	F15
VTP-PU1	B16	VDD	D16	GND	F16
RXD20	B17	RXD29	D17	VDDIO	F17
GND	B18	RXD18	D18	RXD12	F18
RXD13	B19	RXD19	D19	VDDIO	F19
VDDIO	B20	VDD	D20	RXD11	F20

FIGURE 2. Terminal connections.

Device Type	01	Device Types	01	Device Types	01
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
TXD12	G1	TXD7	J1	TXD5	L1
TXD11	G2	TXD8	J2	TXD3	L2
TXD19	G3	VDDIO	J3	QGND	L3
VDDIO	G4	VDDQ	J4	TXD4	L4
VDD	G5	VTT	J5	VTT	L5
GND	G6	GND	J6	GND	L6
GND	G7	GND	J7	GND	L7
GND	G8	GND	J8	GND	L8
GND	G9	GND	J9	GND	L9
GND	G10	GND	J10	GND	L10
GND	G11	GND	J11	GND	L11
GND	G12	GND	J12	GND	L12
GND	G13	GND	J13	GND	L13
GND	G14	GND	J14	VDDIO	L14
VDD	G15	VDD	J15	VDD	L15
VDDQ	G16	GND	J16	VTT	L16
GND	G17	RXC1	J17	RXD3	L17
VDDQ	G18	VTP_PD2	J18	VDDIO	L18
RXD10	G19	GND	J19	GND	L19
RXD9	G20	RXD4	J20	RXD0	L20
TXD10	H1	TXD6	K1	GND-GPI	M1
TXD9	H2	VREF	K2	TXD2	M2
TXD17	H3	GND-GPI	K3	TXD1	M3
TXD18	H4	TXC0	K4	TXD0	M4
VDD	H5	VDD	K5	VDDQ	M5
GND	H6	GND	K6	GND	M6
GND	H7	GND	K7	GNDA	M7
GND	H8	GND	K8	GNDA	M8
GND	H9	GND	K9	GNDA	M9
GND	H10	GND	K10	GNDA	M10
GND	H11	GND	K11	GNDA	M11
GND	H12	GND	K12	GNDA	M12
GND	H13	GND	K13	GNDA	M13
GND	H14	GND	K14	GNDA	M14
GND	H15	VDDQ	K15	GND	M15
VDDQ	H16	RXD5	K16	VTT	M16
VTP_PU2	H17	RXD7	K17	VREF	M17
RXD15	H18	RXC0	K18	GND-GPI	M18
RXD8	H19	RXD2	K19	NC-GPO	M19
RXD6	H20	RXD1	K20	GND-GPI	M20

FIGURE 2. Terminal connections – Continued.

Device Type	01	Device Types	01	Device Types	01
Case Outline	X	Case Outline	X	Case Outline	X
Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number
RETIME	N1	NC-GPO	R1	DVAD2	U1
NC-GPO	N2	NC-GPO	R2	MDIO	U2
GND-GPI	N3	NC-GPO	R3	GNDA	U3
NC-GPO	N4	NUI3	R4	RDP10	U4
VDD	N5	VDDQ	R5	GNDA	U5
GND	N6	VDDA	R6	RDP30	U6
GNDA	N7	NC-GPO	R7	GNDA	U7
GNDA	N8	VDDA	R8	TDP20	U8
GNDA	N9	REFCLKP	R9	GNDA	U9
GNDA	N10	REFCLKN	R10	TDP00	U10
GNDA	N11	NC-GPO	R11	GNDA	U11
GNDA	N12	GNDA	R12	RDP11	U12
GNDA	N13	VDDA	R13	GNDA	U13
GNDA	N14	VDDA	R14	RDP31	U14
VDD	N15	VDDIO	R15	GNDA	U15
GND	N16	VDDA	R16	TDP21	U16
GND-GPI	N17	VDDIO	R17	GNDA	U17
GND	N18	NC-GPO	R18	TDP01	U18
IDLE	N19	NUI1	R19	TMS	U19
NC-GPO	N20	NC-GPO	R20	TRSTN	U20
NC-GPO	P1	DVAD4	T1	DVAD1	V1
NC-GPO	P2	MDC	T2	NC-GPO	V2
GND-GPI	P3	DVAD3	T3	VDDA	V3
NC-GPO	P4	VDD	T4	RDN10	V4
VDDQ	P5	NUI2	T5	VDDT	V5
GND	P6	GNDA	T6	RDN30	V6
GNDA	P7	NC-GPO	T7	VDDA	V7
GNDA	P8	GNDA	T8	TDN20	V8
VDDA	P9	VDD	T9	VDDA	V9
VDDA	P10	NUI4	T10	TDN00	V10
VDDA	P11	NC-GPO	T11	VDDT	V11
GNDA	P12	GNDA	T12	RDN11	V12
VDDA	P13	GNDA	T13	VDDA	V13
GNDA	P14	GNDA	T14	RDN31	V14
VDD	P15	GNDA	T15	VDDA	V15
VTT	P16	IREFTX	T16	TDN21	V16
VREF	P17	VREFTX	T17	VDDT	V17
NC-GPO	P18	NC-GPO	T18	TDN01	V18
GND-GPI	P19	VDDA	T19	TDO	V19
NC-GPO	P20	NC-GPO	T20	VDDIO	V20

FIGURE 2. Terminal connections – Continued.

Device Type	01
Case Outline	X
Terminal Symbol	Terminal Number
DVAD0	W1
VIATST	W2
RDP00	W3
GNDA	W4
RDP20	W5
GNDA	W6
TDP30	W7
GNDA	W8
TDP10	W9
GNDA	W10
RDP01	W11
GNDA	W12
RDP21	W13
GNDA	W14
TDP31	W15
GNDA	W16
TDP11	W17
GNDA	W18
TDI	W19
VDD	W20
VDDIO	Y1
VDDT	Y2
RDN00	Y3
VDDA	Y4
RDN20	Y5
VDDA	Y6
TDN30	Y7
VDDT	Y8
TDN10	Y9
VDDA	Y10
RDN01	Y11
VDDA	Y12
RDN21	Y13
VDDT	Y14
TDN31	Y15
VDDA	Y16
TDN11	Y17
VDDA	Y18
VDDIO	Y19
TCLK	Y20

FIGURE 2. Terminal connections – Continued.

Clock pins	
Terminal symbol	Description
REFCLKP/ REFCLKN	Differential Reference Input Clock: This differential pair accepts DPECL compatible signals. AC coupling is required. An on-chip 100 Ω termination resistor is placed differentially between the pins. No external biasing is required. This clock is 156.25 MHz ± 200 ppm.
TCLK	Transmit Data Clock**:** This is the input 156.25 MHz ±200 ppm 10 Gigabit Media Independent Interface (XGMII) transmit data path clock input. It is used to sample TXD (31:0), and TXC (3:0).
RCLK	Receive Data Clock: This is the output 156.25-MHz ±200 ppm 10 Gigabit Media Independent Interface (XGMII) receive data path clock output. This clock is centered in the middle of the DDR RXD (31:0) and RXC (3:0) data output pins.
Serial side data pins	
Terminal symbol	Description
TDP30/TDN30 TDP20/TDN20 TDP10/TDN10 TDP00/TDN00	Transmit Differential Pairs, 10 gigabit per second Attachment Unit Interface (XAUI) Lane A: High speed serial outputs. Minimum bit time 320 ps.
TDP31/TDN31 TDP21/TDN21 TDP11/TDN11 TDP01/TDN01	Transmit Differential Pairs, 10 gigabit per second Attachment Unit Interface (XAUI) Lane B: High speed serial outputs. Minimum bit time 320 ps.
RDP30/RDN30 RDP20/RDN20 RDP10/RDN10 RDP00/RDN00	Receive Differential Pairs, 10 gigabit per second Attachment Unit Interface (XAUI) Lane A: High speed serial inputs with on-chip 100 Ω differential termination. Each input pair is terminated differentially across an on-chip 100 Ω resistor.
RDP31/RDN31 RDP21/RDN21 RDP11/RDN11 RDP01/RDN01	Receive Differential Pairs, 10 gigabit per second Attachment Unit Interface (XAUI) Lane B: High speed serial inputs with on-chip 100 Ω differential termination. Each input pair is terminated differentially across an on-chip 100 Ω resistor.
Parallel data pins	
Terminal symbol	Description
TXD(31:0)	Transmit Data: Parallel data on this bus is clocked on the rising and falling edge of TCLK.
TXC(3:0)	Transmit Data Control: 10 Gigabit Media Independent Interface (XGMII) inputs. This bus is clocked on both edges of TCLK.
RXD(31:0)	Receive Data: Parallel data on this bus is valid on the rising and falling edge of RCLK. These pins have internal series termination to provide direct connection to a 50 Ω transmission line.
RXC(3:0)	Receive Data Control: 10 Gigabit Media Independent Interface (XGMII) control outputs. This data is valid on both the rising and falling edge of RCLK. These pins have internal series termination to provide direct connection to a 50 Ω transmission line.

FIGURE 2. Terminal connections – Continued.

Joint Test Action Group (JTAG) test port interface pins	
Terminal symbol	Description
TDI	JTAG Input Data: TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	JTAG Output Data: TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When JTAG port is not in use, TDO is in a high impedance state.
TMS	JTAG Mode Select: TMS is used to control the state of the internal test port controller.
TCK	JTAG Clock: TCK is used to clock state information and test data into and out of the device during the operation of the test port.
TRST_N	JTAG Test Reset: TRST_N is used to reset the JTAG logic into system operational mode.
Management data interface pins	
Terminal symbol	Description
MDIO	Management Data I/O: MDIO is the bi-directional serial data path for the transfer of management data to and from the protocol device.
MDC	Management Data Clock: MDC is the clock reference for the transfer of management data to and from the protocol device.
DVAD(4:0)	Management PHY Address Device Address: DVAD (4:1) is the externally set physical address given to this device used to distinguish one device from another. DVAD (0) is actually used to determine whether the device responds as a DTE (=1) or PHY (=0) XGXS device (4.xxx or 5.xxx on register accesses). These are typically pulled up or pulled down in the asystem application.
Miscellaneous pins	
Terminal symbol	Description
A_B	XAUI Lane Select: In RETIME mode, A/B selects which data is reflected on the XGMII outputs. In Redundant Transceiver Modes, A/B selects whether XAUI A or XAUI B data is reflected on the XGMII output interface, if so enabled. A_B = 1 → A side selected A_B = 0 → B side selected
RETIME	Re-Timer Mode Enable: When RETIME is high, serial inputs from XAUI Channels A RX are synchronized and output on XAUI Channels B TX, and vice-versa.
IDLE	IDLE: When RETIME is low, and IDLE is high, IDLE codes (valid AKR sequences) will be sent out to the non-selected serial interface instead of bridged XGMII transmit traffic packet data. When RETIME is low and IDLE is low, both XAUI A and XAUI B transmit data will reflect the actual XGMII TX packet data. When RETIME is high, this pin should be considered a don't care input.
RSTN	Chip Reset: When asserted low, this signal reinitializes the entire device. Must be asserted for at least 10 µs after device power up.

FIGURE 2. Terminal connections – Continued.

Voltage supply and reference pins	
Terminal symbol	Description
GND	Digital ground.
GNDA	Analog ground.
VDD	1.2 V supply (core digital voltage)
VPP	Efuse Controller Voltage (1.2 V): Must be tied to 1.2 V in the system application.
VDDA	1.2 V analog supply voltage.
VDDIO	2.5 V LVCMOS input/output supply voltage.
VREF	Input threshold for HSTL inputs (0.75 V)
VTT	End termination voltage for HSTL inputs (0.75 V)
VDDQ	HSTL input/output supply voltage (1.5 V)
VDDT	1.2 V termination supply (used on Serializer/DeSerializer (SERDES) macro).
QGND	Quiet ground. For HSTL inputs.
VIATEST	Via Test. Grounded in the system application.
GPI [11:0]	General Purpose Input. Must be grounded in the system application.
GPO [11:0]	General Purpose Output. Must be no connect in the system application.
NUI	No connect in the system application.
NUI4	Direct connection to 2.5 V board power plane.
VREFTX	VREF for SERDES TX. Connect to 1.2 V.
NUI3	No connect in the system application.
NUI4	No connect in the system application.
IREFTX	0 Ω connection to 2.5 V power plane.
NUI1	No connect in the system application.
VTP_PU1	External 50 Ω pull-up to VDDQ (1% tolerance).
VTP_PD1	External 50 Ω pull-down to VSS (1% tolerance).
VTP_PU2	External 50 Ω pull-up to VDDQ (1% tolerance).
VTP_PD2	External 50 Ω pull-down to VSS (1% tolerance).

FIGURE 2. Terminal connections – Continued.

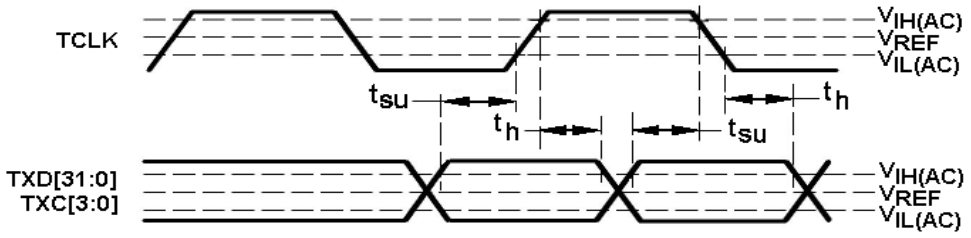


FIGURE 3. HSTL data input timing waveform.

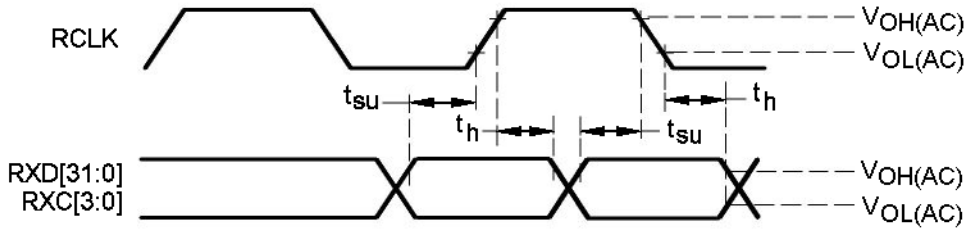


FIGURE 4. HSTL output timing waveform.

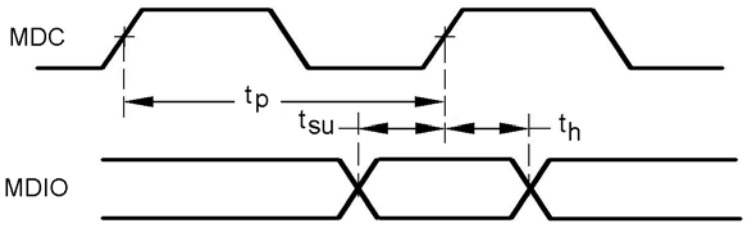


FIGURE 5. MDIO read/write timing waveform.

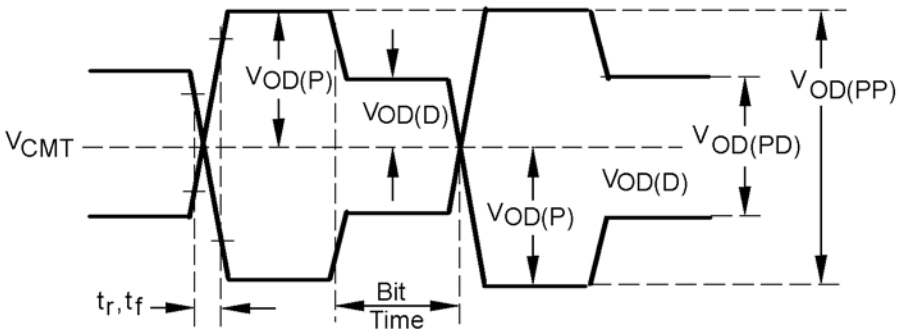


FIGURE 6. Transmit output waveform parameter definition.

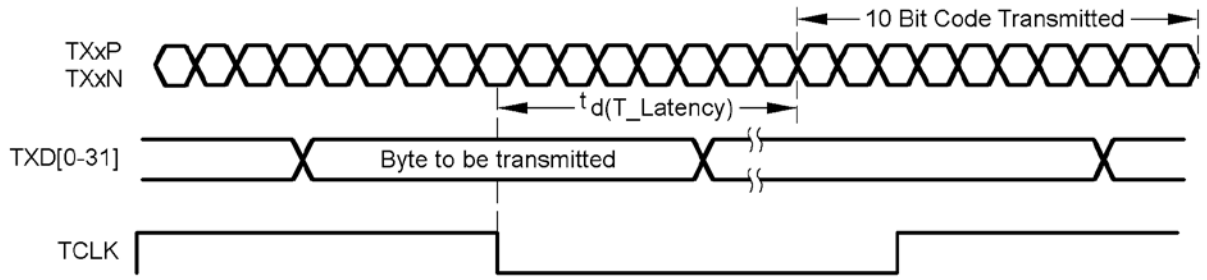


FIGURE 7. Transmission latency timing waveform.

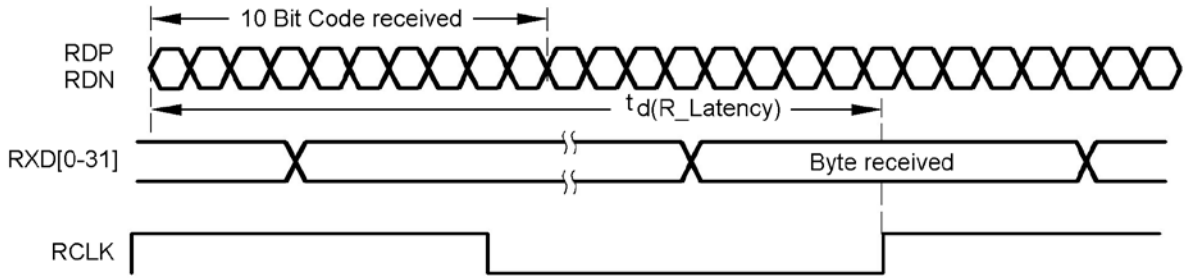


FIGURE 8. Receiver latency timing waveform.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,9	1,9
Final electrical parameters (see 4.2)	1,2,3,4, 1/ 9,10,11	1,2,3,4, 1/ 9,10,11
Group A test requirements (see 4.4)	1,2,3,4, 9,10,11	1,2,3,4, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,4, 9,10,11	1,2,3,4, 9,10,11
Group D end-point electrical parameters (see 4.4)	1,9	1,9
Group E end-point electrical parameters (see 4.4)	----	----

1/ PDA applies to subgroup 1.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-01-10

Approved sources of supply for SMD 5962-17207 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-1720701QXC	01295	TLK3118MZMA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.