

Features

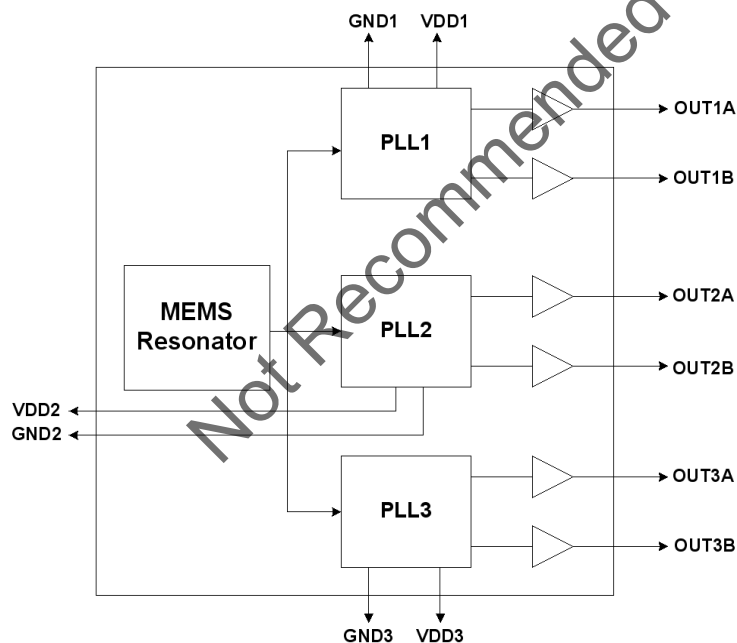
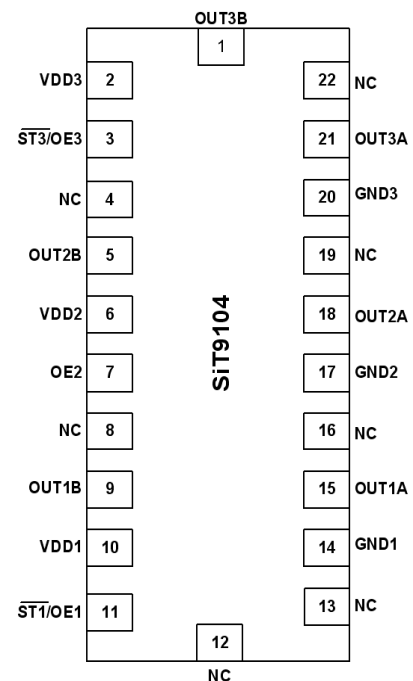
- Extremely low RMS period jitter
 - 5 ps (typical)
- Wide frequency range
 - 1 MHz to 220 MHz
- Up to six single-ended CMOS outputs
- Low frequency tolerance
 - ± 25 PPM or ± 50 PPM
- Operating voltage
 - 1.8, 2.5 or 3.3 V
 - Other voltages up to 3.63 V (contact SiTime)
- Operating temperature range:
 - Industrial, -40 to 85°C
 - Extended Commercial, -20 to 70°C
- Small footprint
 - 22-pin, 7.0 x 5.0 x 0.90 mm QFN package
- All packages are Pb-free and ROHs compliant
- Ultra-reliable start up and greater immunity from interference

Benefits

- Replacing up to six crystal oscillators
- No crystal or load capacitors required
- Eliminates crystal qualification time
- 50% + board saving space
- More cost effective than quartz oscillators, quartz crystals and clock ICs.
- Completely quartz-free

Applications

- Consumer Electronics Applications
- Automotive Applications
- Industrial Applications
- HDTV, STB, DVD-R, Printer, MFP
- Gigabit Ethernet
- 10 Gigabit Ethernet
- Fibre Channel
- Ethernet
- SATA / SAS
- USB 2.0
- PCI-Express

Block Diagram**Pinout**

Pin Description

Pin No.	Name	Pin Description
4, 8, 12, 13, 16, 19, 22	NC	Do not connect pins, leave them floating
1	OUT3B	Same as OUT3A at VDD3 level (1.8V or 2.5V or 3.3V) or No Connect
2	VDD3	Power supply for OUT3A and OUT3B. Connect to 1.8V or 2.5V or 3.3V
3	ST3/OE3	Standby or Output Enable pin for OUT3A and OUT3B.
5	OUT2B	Same as OUT2A at VDD2 level (1.8V or 2.5V or 3.3V) or No Connect
6	VDD2	Power supply for OUT2A and OUT2B. Connect to 1.8V or 2.5V to 3.3V - VDD2 must be on all times for proper operation
7	OE2	Output Enable pin for OUT2A and OUT2B
9	OUT1B	Same as OUT1A at VDD1 level (1.8V or 2.5V or 3.3V) or No Connect
10	VDD1	Power supply for OUT1A and OUT2A. Connect to 1.8V or 2.5V or 3.3V
11	ST1/OE1	Standby or Output Enable pin for OUT1A and OUT1B
14	GND1	VDD1 power supply ground. Connect to Ground
15	OUT1A	1 to 220 MHz programmable clock output at VDD1 level (1.8V or 2.5V or 3.3V) or No Connect
17	GND2	VDD2 power supply ground. Connect to Ground
18	OUT2A	1 to 220 MHz programmable clock output at VDD2 level (1.8V or 2.5V or 3.3V) or No Connect
20	GND3	VDD3 power supply ground. Connect to Ground
21	OUT3A	1 to 220 MHz programmable clock output at VDD3 level (1.8V or 2.5V or 3.3V)

Pins 3,7,11

Pin #s 3,7,11 Functionality
OE (3,7,11)
H or Open; specified frequency output
L: output is high impedance
ST (3,11)
H or Open; specified frequency output
L: output is low level (weak pull down) oscillation stops

Description

The SiT9104 is a multiple factory programmable clock generator with embedded MEMS resonator. The device uses SiTime propriety MEMS technology, MEMS First, to enable a single chip solution with multiple outputs for consumer and communications applications.

The SiT9104 has three PLLs that can be programmed to generate any frequency outputs from 1 to 220 MHz.

Each PLL is connected to two output buffers that can generate up to three unrelated frequencies.

Programming Description

The SiT9104 is a factory programmable device. All the parameters in table 1 given as "Enter Data" can be programmed into the SiT9104. Both outputs generated off of the same PLL are required to have same frequency i.e. OUT1A and OUT1B should be at the same frequency since they are generated from PLL1.

Table 1.

	PLL1				PLL2				PLL3			
Pin Name	OUT1A 1-220MHz or NC	OUT1B 1-220MHz or NC	ST1/OE1	VDD1 1.8/2.5/3.3V	OUT2A 1-220MHz or NC	OUT2B 1-220MHz or NC	OE2	VDD2 1.8/2.5/3.3V	OUT3A 1-220MHz or NC	OUT3B 1-220MHz or NC	ST3/OE3	VDD3 1.8/2.5/3.3V
Pin No.	15	9	11	10	18	5	7	6	21	1	3	2
Program Value	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"	"Enter Data"

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Absolute Maximum Table

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	+4.00	V
Theta JA (with copper plane on VDD and GND)	–	27.5	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins)	–	47	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125 °C, Process, VDD (0 to 3.6V)	–	1,000+	years
Human Body Model (JESD22-A114)	2000	–	–
Charged Device Model (JESD22-C101)	750	–	–
Machine Model (JESD22-A115)	200	–	–

Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Supply Voltages, VDD ^[1]	2.97	3.3	3.63	V
	2.25	2.5	2.75	V
	1.7	1.8	1.9	V
Extended Commercial Operating Temperature	-20	-	70	°C
Industrial Operating Temperature	-40	-	85	°C
Maximum Load Capacitance	-	-	15	pF

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	MIL-STD-883F, Method 1010-65-150°C (1000 cycle)
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1

Note:

1. The 2.5V and 3.3V devices can operate from 2.75V to 2.97V as well, however, the data sheet parameters cannot be guaranteed. Please contact factory for more information.

DC Electrical Specifications

VDD = 3.3V ±10%, -40 to 85°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Output Voltage High	IOH = -9 mA	90	-	-	%Vdd
Output Voltage Low	IOL = 9 mA	-	-	10	%Vdd
Input Voltage High	Pins 3,7,11	70	-	-	%Vdd
Input Voltage Low	Pins 3,7,11	-	-	30	%Vdd
Operating Current	OUT2[A] = 30 MHz, OUT2B = NC VDD1=VDD3= 0V, 15 pF load	-	-	26	mA
Operating Current	OUT2[A] = 125MHz, OUT2B = NC VDD1=VDD3= 0V, 15 pF load	-	-	31	mA
Standby Current	Outputs are weakly pulled down, ST[1,3] = GND	-	30	50	μA
Power Up Time	Time from minimum power supply voltage	-	-	10	ms

VDD = 2.5V ±10%, -40 to 85°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Output Voltage High	IOH = -7 mA	90	-	-	%Vdd
Output Voltage Low	IOL = 7mA	-	-	10	%Vdd
Input Voltage High	Pins 3,7,11	70	-	-	%Vdd
Input Voltage Low	Pins 3,7,11	-	-	30	%Vdd
Operating Current	OUT2[A] = 30 MHz, OUT2B = NC VDD1=VDD3= 0V, 15 pF load	-	-	26	mA
Operating Current	OUT2[A] = 125MHz, OUT2B = NC VDD1=VDD3= 0V, 15 pF load	-	-	31	mA
Standby Current	Outputs are weakly pulled down, ST[1,3] = GND	-	30	50	μA
Power Up Time	Time from minimum power supply voltage	-	-	10	ms

VDD = 1.8V ±5%, -40 to 85°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Output Voltage High	IOH = -5 mA	90	-	-	%Vdd
Output Voltage Low	IOL = -5 mA	-	-	10	%Vdd
Input Voltage High	Pins 3,7,11	70	-	-	%Vdd
Input Voltage Low	Pins 3,7,11	-	-	30	%Vdd
Operating Current	OUT2[A] = 30 MHz, OUT2B = NC VDD1=VDD3= 0V, 15 pF load	-	-	26	mA
Operating Current	OUT2[A] = 125MHz, OUT2B = NC VDD1=VDD3= 0V, 15 pF load	-	-	31	mA
Standby Current	Outputs are weakly pulled down, ST[1,3] = GND	-	30	50	μA
Power Up Time	Time from minimum power supply voltage	-	-	10	ms

AC Electrical Specifications

VDD = 3.3V ±10%, -40 to 85°C

Parameter	Condition		Min.	Typ.	Max.	Unit
Clock Output Frequency	All the outputs		1	–	220	MHz
Frequency Stability	Inclusive of initial tolerance, operating temp., rated power supply voltage change, load change	-20 to 70°C -40 to 85°C	-25	–	+25	PPM
			-50	–	+50	PPM
Aging	First year @ 25°C		–	–	1	PPM
Clock Output Duty Cycle	Output frequency= 1 to 125 MHz		45	–	55	%
	Output frequency= 125 to 200 MHz		40	–	60	%
Clock Output Rise Time	15 pF Load, 20% to 80% VDD		–	1	1.5	ns
Clock Output Fall Time	15 pF Load, 80% to 20% VDD		–	1	1.5	ns
RMS Period Jitter	OUT1A,OUT2A, OUT3A = 75 MHz		–	2.6	5	ps
	OUT1A,OUT2A, OUT3A = 125 MHz		–	2.4	3.6	ps
RMS Phase Jitter (Random)	OUT1A = 75 MHz (900 kHz to 7.5 MHz)		–	0.81	–	ps
	OUT1A = 106.25 MHz (637 kHz to 10 MHz)		–	1.64	–	ps
	OUT1A = 125 MHz (1.875 MHz to 20 MHz)		–	0.38	–	ps

VDD = 2.5V ±10%, -40 to 85°C

Parameter	Condition		Min.	Typ.	Max.	Unit
Clock Output Frequency	All the outputs		1	–	220	MHz
Frequency Stability	Inclusive of initial tolerance, operating temp., rated power supply voltage change, load change	-20 to 70°C -40 to 85°C	-25	–	+25	PPM
			-50	–	+50	PPM
Aging	First year @ 25°C		–	–	1	PPM
Clock Output Duty Cycle	Output frequency= 1 to 125 MHz		45	–	55	%
	Output frequency= 125 to 200 MHz		40	–	60	%
Clock Output Rise Time	15 pF Load, 20% to 80% VDD		–	1	1.5	ns
Clock Output Fall Time	15 pF Load, 80% to 20% VDD		–	1	1.5	ns
RMS Period Jitter	OUT1A, OUT2A, OUT3A = 75 MHz		–	3	6	ps
	OUT1A, OUT2A, OUT3A = 125 MHz		–	2.8	5	ps
RMS Phase Jitter (Random)	OUT1A = 75 MHz (900 kHz to 7.5 MHz)		–	0.87	–	ps
	OUT1A = 106.25 MHz (637 kHz to 10 MHz)		–	1.7	–	ps
	OUT1A = 125 MHz (1.875 MHz to 20 MHz)		–	0.41	–	ps

VDD = 1.8V ±5%, -40 to 85°C

Parameter	Condition		Min.	Typ.	Max.	Unit
Clock Output Frequency	All the outputs		1	–	220	MHz
Frequency Stability	Inclusive of initial tolerance, operating temp., rated power supply voltage change, load change	-20 to 70°C -40 to 85°C	-25	–	+25	PPM
			-50	–	+50	PPM
Aging	First year @ 25°C		–	–	1	PPM
Clock Output Duty Cycle	Output frequency= 1 MHz to 125MHz		45	–	55	%
	Output frequency= 125 MHz to 220 MHz		40	–	60	%
Clock Output Rise Time	15 pF Load, 20% to 80% VDD		–	1	1.5	ns

VDD = 1.8V $\pm$ 5%, -40 to 85°C (continued)

Parameter	Condition	Min.	Typ.	Max.	Unit
Clock Output Fall Time	15 pF Load, 80% to 20% VDD	–	1	1.5	ns
RMS Period Jitter	OUT1A, OUT2A, OUT3A = 75 MHz	–	7.3	14	ps
	OUT1A, OUT2A, OUT3A = 125 MHz	–	7.1	14	ps
RMS Phase Jitter (Random)	OUT1A = 75 MHz (900 kHz to 7.5 MHz)	–	0.85	–	ps
	OUT1A = 106.25 MHz (637 kHz to 10 MHz)	–	1.72	–	ps
	OUT1A = 125 MHz (1.875 MHz to 20 MHz)	–	1.06	–	ps

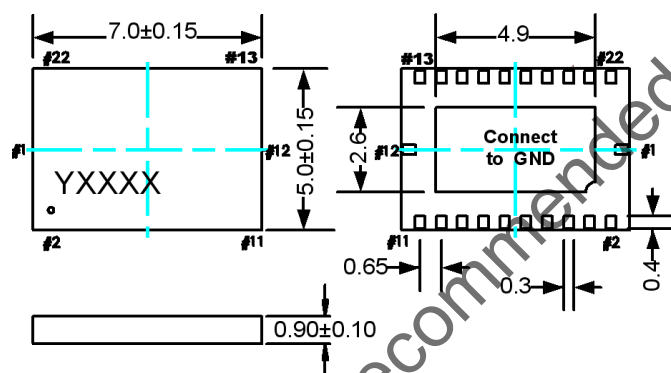
Ordering Information^[2]

Part Number	Package Description	Frequency Stability	Product Flow
SiT9104AC-2xxx	22-pin QFN	$\pm$ 25ppm	-20°C to 70°C
SiT9104AI-2xxx	22-pin QFN	$\pm$ 25ppm	-40°C to 85°C
SiT9104AC-3xxx	22-pin QFN	$\pm$ 50ppm	-20°C to 70°C
SiT9104AI-3xxx	22-pin QFN	$\pm$ 50ppm	-40°C to 85°C

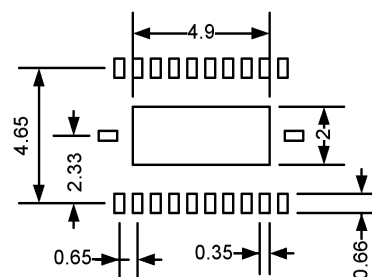
Package Information^[3]

Dimension (mm)

7.0 x 5.0 x 0.90mm



Land Pattern (recommended) (mm)^[4]



Notes:

- "xxx" denotes the assigned product dash number.
- "Y" denotes manufacturing origin and "XXXX" denotes manufacturing lot number. The value of "Y" depend on the assembly location of the device.
- A capacitor of value 0.1μF between VDD and GND is recommended.

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