Dear customer

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Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

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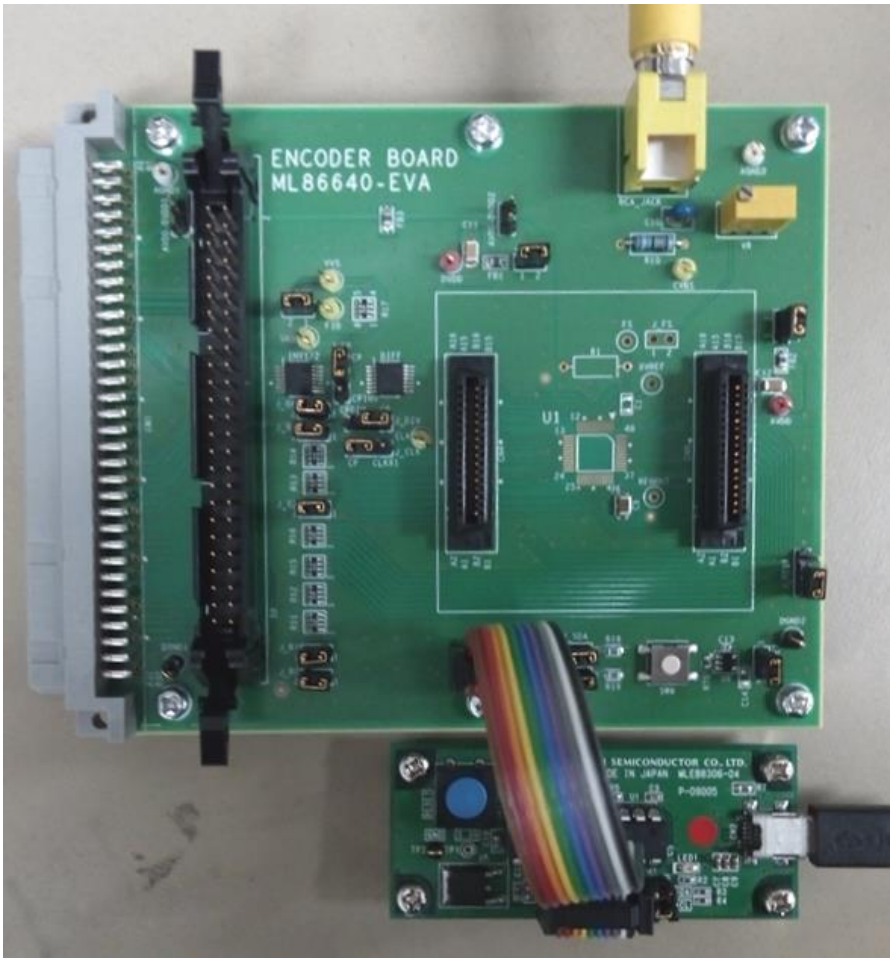
ML86640 Evaluation Board User's Manual

NTSC/PAL Video Encoder with P/I conversion function

■ General Description

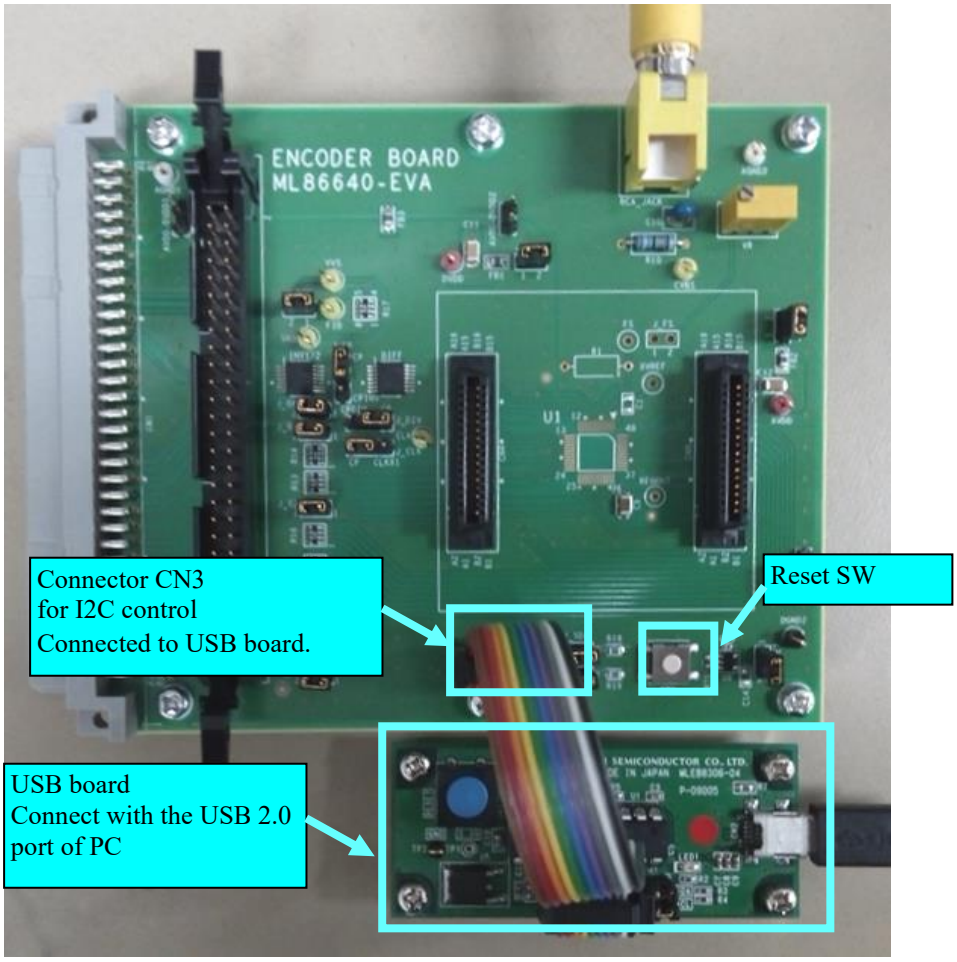
This User's Manual describes the evaluation board of the digital video encoder ML86640 corresponding to the NTSC/PAL signal and equipped with P/I conversion .

■ Evaluation Board Constitution



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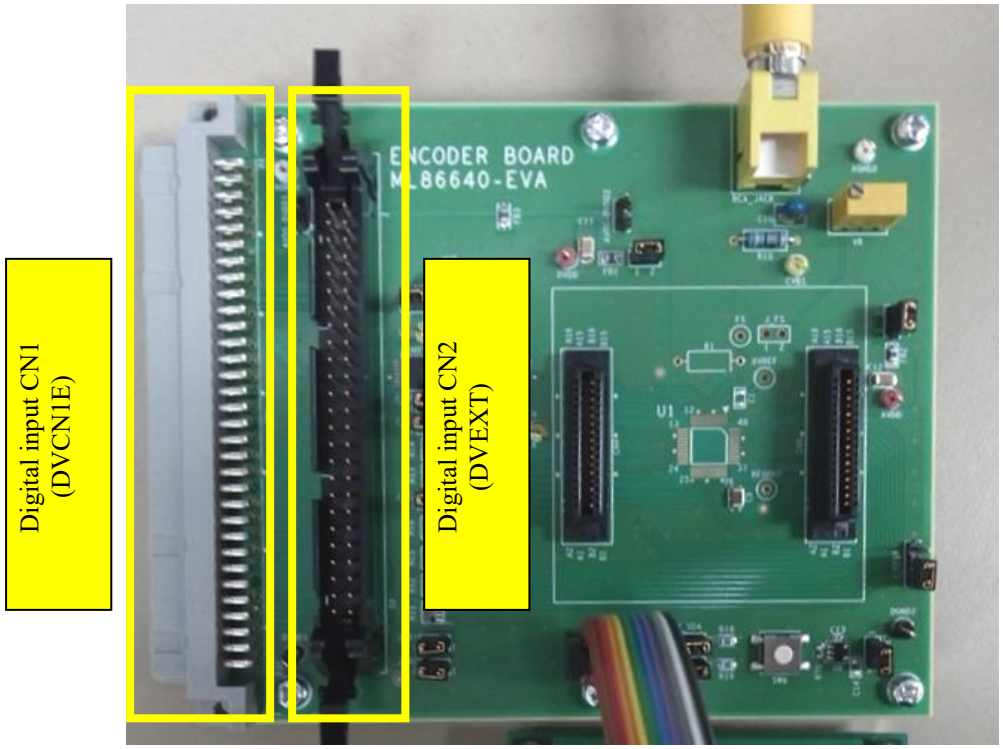
■ RESET and I2C control



CN3 Pin assignment FFC-10BMEP1 (HTK)	
PIN	NAME
1	VCC5(+5V)
2	VCC5(+5V)
3	DGND
4	DGND
5	-
6	-
7	-
8	RESET
9	SCL
10	SDA

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■ Input



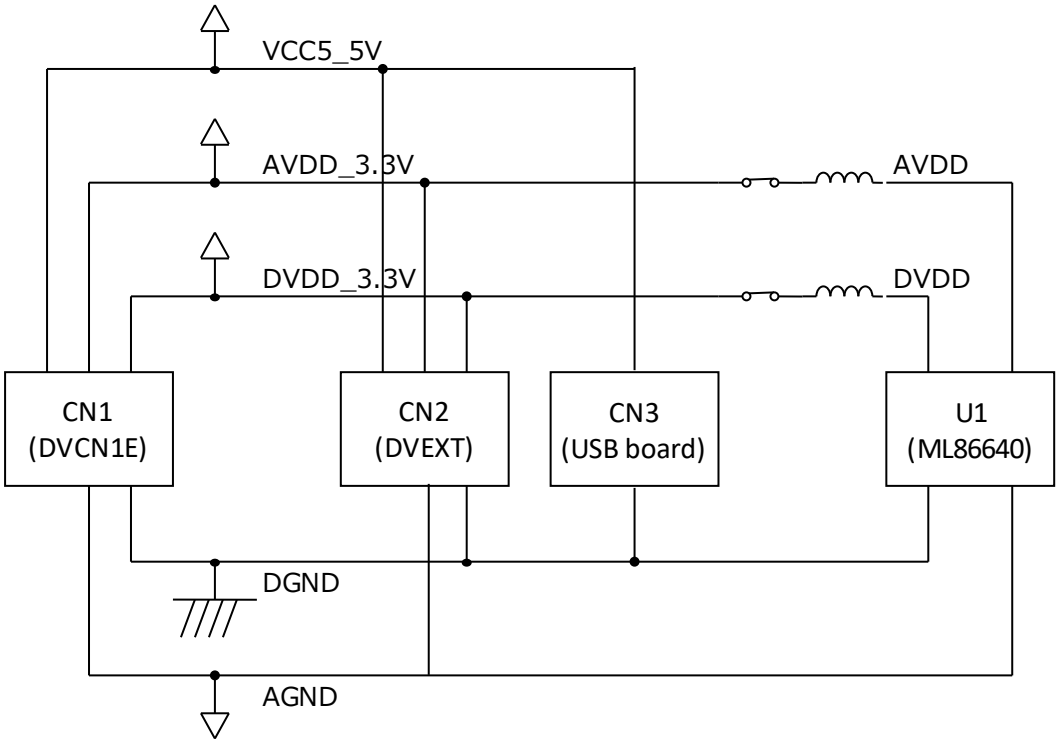
CN1 Pin assignment PCN10C-64S-254DS (HRS)			
NAME	PIN	PIN	NAME
VCC5_5V	A1	B1	VCC5_5V
-	A2	B2	-
AVDD_3.3V	A3	B3	AVDD_3.3V
AGND	A4	B4	AGND
AGND	A5	B5	AGND
-	A6	B6	-
-	A7	B7	-
DVDD_3.3V	A8	B8	DVDD_3.3V
SCL	A9	B9	SDA
DGND	A10	B10	DGND
CLKX1	A11	B11	CLK
DGND	A12	B12	DGND
RESET	A13	B13	DGND
DGND	A14	B14	DGND
DGND	A15	B15	-
-	A16	B16	FIELD
HSYNC_L	A17	B17	VSYNC_L
-	A18	B18	-
G7	A19	B19	G6
G5	A20	B20	G4
G3	A21	B21	G2
G1	A22	B22	G0
DGND	A23	B23	DGND
B0	A24	B24	B1
B2	A25	B25	B3
B4	A26	B26	B5
B6	A27	B27	B7
R0	A28	B28	R1
R2	A29	B29	R3
R4	A30	B30	R5
R6	A31	B31	R7
DVDD_3.3V	A32	B32	DVDD_3.3V

CN2 Pin assignment HIF3BA-50PA-254DSA (HRS)			
PIN	NAME	PIN	NAME
1	-	26	G3
2	-	27	G2
3	VCC5_5V	28	G1
4	VCC5_5V	29	G0
5	DVDD_3.3V	30	DGND
6	DVDD_3.3V	31	B7
7	RESET	32	B6
8	-	33	B5
9	SDA	34	B4
10	DGND	35	DGND
11	SCL	36	B3
12	DGND	37	B2
13	-	38	B1
14	-	39	B0
15	VSYNC_L	40	DGND
16	FIELD	41	R7
17	HSYNC_L	42	R6
18	DGND	43	R5
19	CLK	44	R4
20	DGND	45	DGND
21	G7	46	R3
22	G6	47	R2
23	G5	48	R1
24	G4	49	R0
25	DGND	50	DGND

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This board is powered from either CN1 or CN2. For example, there are six DVDD_3.3V pins: CN1-A8, CN1-A32, CN1-B8, CN1-B32, CN2-5, and CN2-6.

Because they are all tied together on the board, at least one of them must be provided from external power supply, and the rest can be left unconnected. Same goes for VCC5_5V, AVDD_3.3V, AGND, and DGND.



Note that VCC5_5V is not for ML86640 but for USB board via CN3. If the USB board is powered by USB bus, VCC5_5V shall be left unconnected.

For detail, see schematic.

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■ Register setting

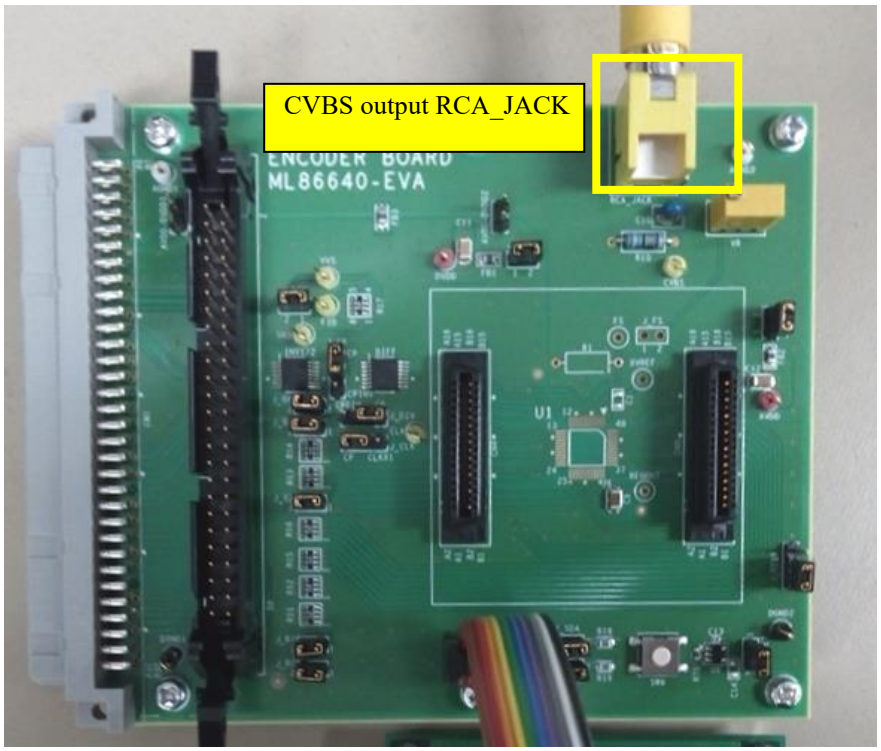
The default setting of input signal is the NTSC RGB 24bit progressive signal.
Change the following register to change an input signal.
Installation of USB driver and VAStudio2 is necessary for the change of the internal register.
Refer to each manual for the installation of USB driver and VAStudio2.

Register of the input video format

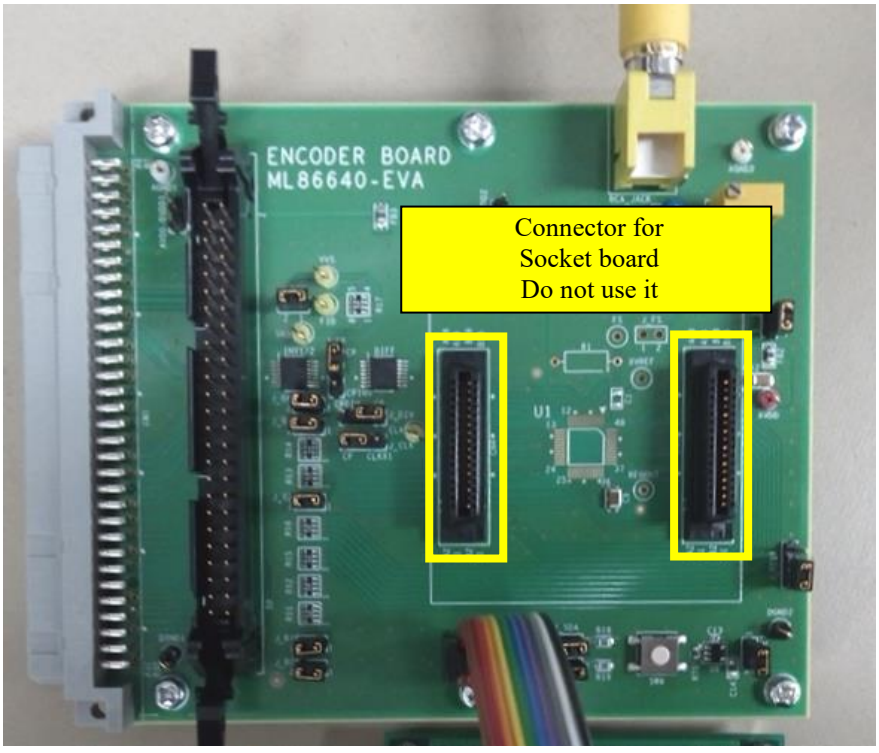
					#00h[4]	#00h[3]	#00h[2]	#01h[2]	#01h[1]	#01h[0]
Scan form	Data type	Bit width	Chroma sampling rate	Input CLK frequency [MHz]	DDRMOD	MLTDAT	IMODSEL2	I444SEL	IRGBSEL	IPRGSEL
Interrace	ITU-R BT.BT.656-4	8bit	4:2:2	27MHz	0	0	1	0	0	0
	YCbCr 4:2:2 8bit + H,V	8bit	4:2:2	27MHz	0	1	1	0	0	0
	ITU-R BT.BT.656-4 (DDR)	8bit	4:2:2	13.5MHz	1	0	1	0	0	0
	YCbCr 4:2:2 8bit + H,V (DDR)	8bit	4:2:2	13.5MHz	1	1	1	0	0	0
	YCbCr 4:2:2 16bit + H,V	16bit	4:2:2	13.5MHz	0	0	0	0	0	0
	YCbCr 4:4:4 24bit + H,V	24bit	4:4:4	13.5MHz	0	0	0	1	0	0
	RGB 4:4:4 24bit + H,V	24bit	4:4:4	13.5MHz	0	0	0	1	1	0
Progressive	ITU-R BT.BT.656-4	8bit	4:2:2	54MHz	0	0	1	0	0	1
	YCbCr 4:2:2 8bit + H,V	8bit	4:2:2	54MHz	0	1	1	0	0	1
	ITU-R BT.BT.656-4 (DDR)	8bit	4:2:2	27MHz	1	0	1	0	0	1
	YCbCr 4:2:2 8bit + H,V (DDR)	8bit	4:2:2	27MHz	1	1	1	0	0	1
	YCbCr 4:2:2 16bit + H,V	16bit	4:2:2	27MHz	0	0	0	0	0	1
	YCbCr 4:4:4 24bit + H,V	24bit	4:4:4	27MHz	0	0	0	1	0	1
	RGB 4:4:4 24bit + H,V	24bit	4:4:4	27MHz	0	0	0	1	1	1

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■ Output



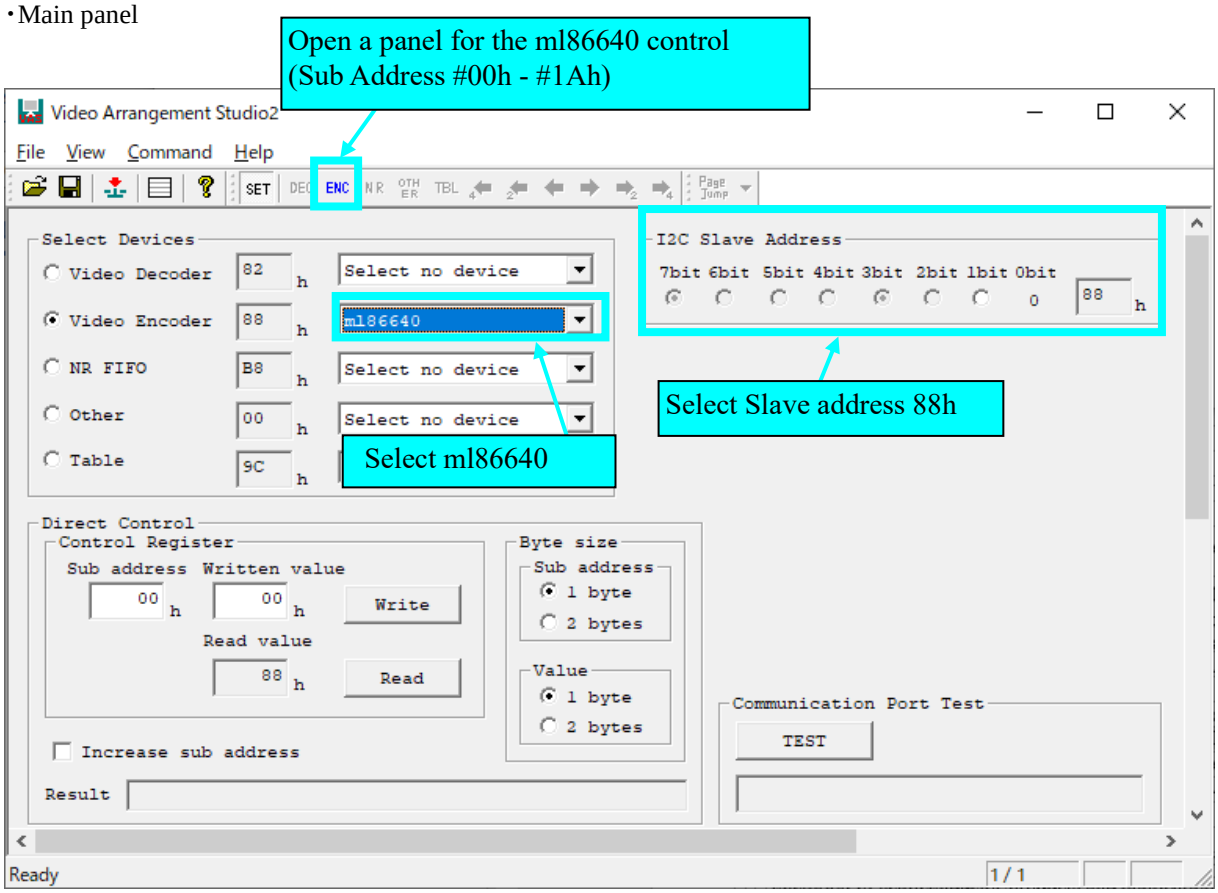
■ Others



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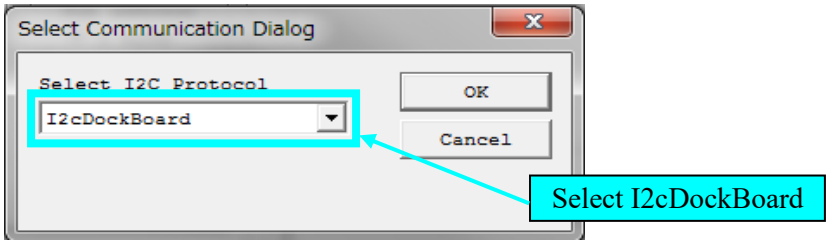
■ Video Arrangement Studio2

・Main panel

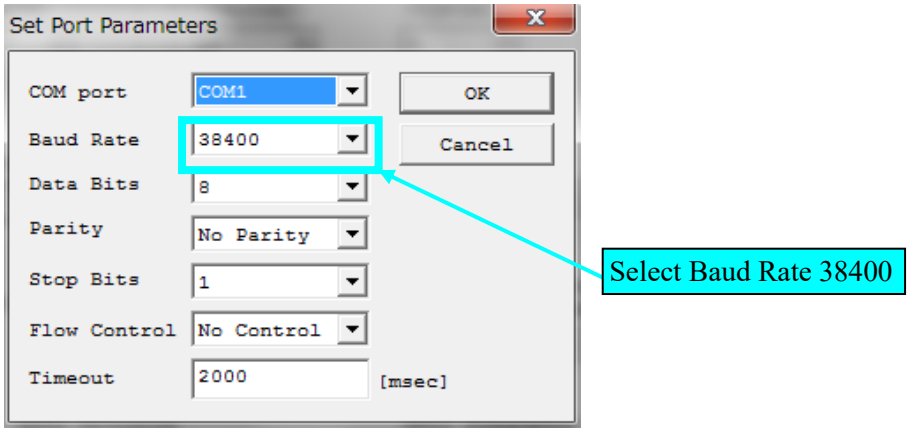


・Communication protocol setting

File → Select Port



File → Set Port Parameters



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Revision history

Document No.	Issue date	Pages		Description
		Previous Edition	New Edition	
FEBL86640-01	2017.01.05	-	8	First edition issued
FEBL86640-02	2017.07.27	8	8	CVBS output RCA_JACK
FEBL86640-03	2018.03.30	8	8	P3: Note it about a method to supply power
FEBL86640-04	2023.12.12	8	9	P3: Added VCC5_5V to CN1 and CN2
FEBL86640-05	2024.03.13	9	9	P9: Updated “Notice”

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